

Individual Subsystem - Final Check Files

Schematic Editor

File Edit View Place Inspect Tools Preferences Help

Violations (0) Ignored Tests (5)

Show: All Errors Warnings Exclusions

Delete Marker Delete All Markers Run ERC Close

Electrical Rules Checker

Root (p)

Selection Filter

All items Symbols Wires Graphics Text Pins Labels Images Other items

C:\Users\rgrag\OneDrive - Arizona State University\College\SEM 514\Individual subsystem\Individual-sub... Z 1.35 X -1200 Y 3000 dx -1200 dy 3000 dist 3231 grid 50 mils Select Item(s)

PCB Editor

File Edit View Place Route Inspect Tools Preferences Help

Track: use netclass width Via: use netclass sizes F.Cu (PgUp) 100.000 mils (2.5400 mm) Zoom 1.50

Design Rules Checker

Refill all zones before performing DRC Test for parity between PCB and schematic Report all errors for each track

Violations (0) Unconnected Items (0) Schematic Parity (not run) Ignored Tests (6)

Show: All Errors Warnings Exclusions

Delete Marker Delete All Markers Run DRC Close

Appearance

- E.Cu
- Adhesive
- Adhesive
- Paste
- Paste
- Silkscreen
- Silkscreen
- Mask
- Mask
- Drawings
- User Comments
- User Ecol1
- User Ecol2
- EdgeCuts
- Margin
- Countertop
- Countertop
- F.Fab
- User 1
- User 2
- User 3

Layer Display Options

Presets (Ctrl+Tab):

Viewports (Shift+Tab):

Selection Filter

- All items
- Footprints
- Tracks
- Pads
- Zones
- Graphics
- Rule Areas
- Dimensions
- Locked items
- Net
- Yaxis
- Xaxis
- Other Items