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C.Y.S.: BSCpE-3A

**#6-TITLE:** EX-OR gate

**LOGIC GATE SYMBOL:**



**7486**

**TRUTH TABLE:**

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

**VHDL CODE:**

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity xor2 is
  Port (
    X: in STD_LOGIC;
    Y: in STD_LOGIC;
    Z: out STD_LOGIC
  );
end xor2;

--Dataflow model

architecture behav1 of xor2 is
begin

  Z<= x xor y;  --Signal Assignment Statement

end behav1;
```

-- Behavioral model

```
architecture behav2 of xor2 is  
begin
```

```
    process (x, y)  
    begin
```

```
        If (x/=y) then    -- Compare with truth table  
            Z <= '1';  
        else  
            Z <= '0';  
        end if;
```

```
    end process;
```

```
end behav2;
```

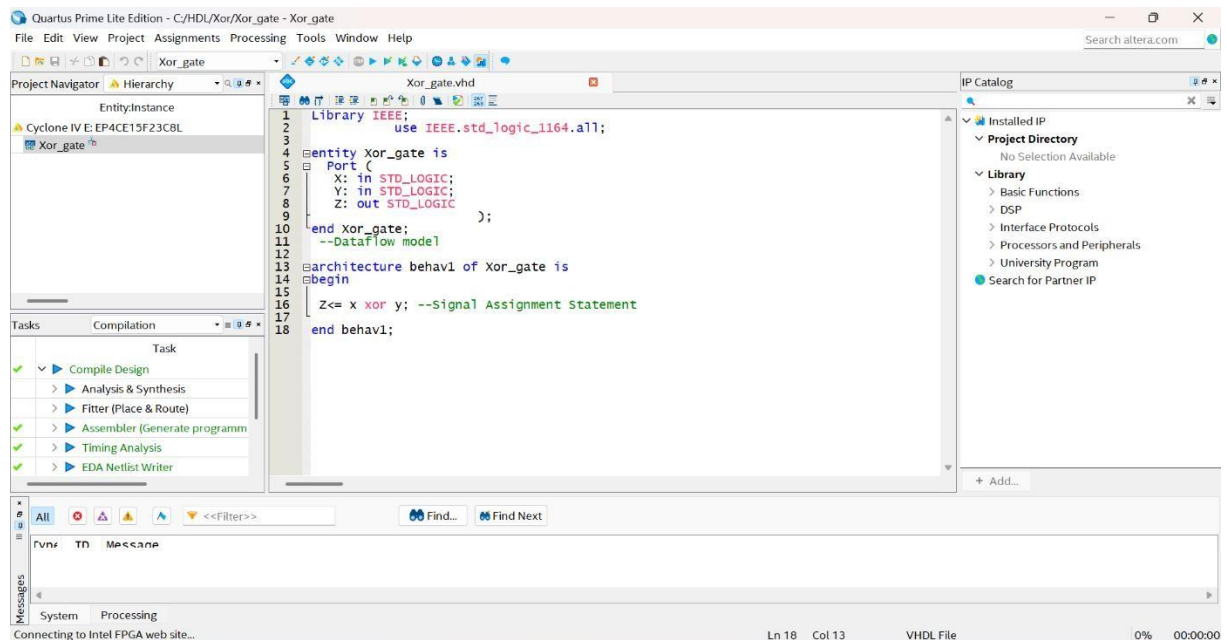
OUTPUT WAVEFORM:



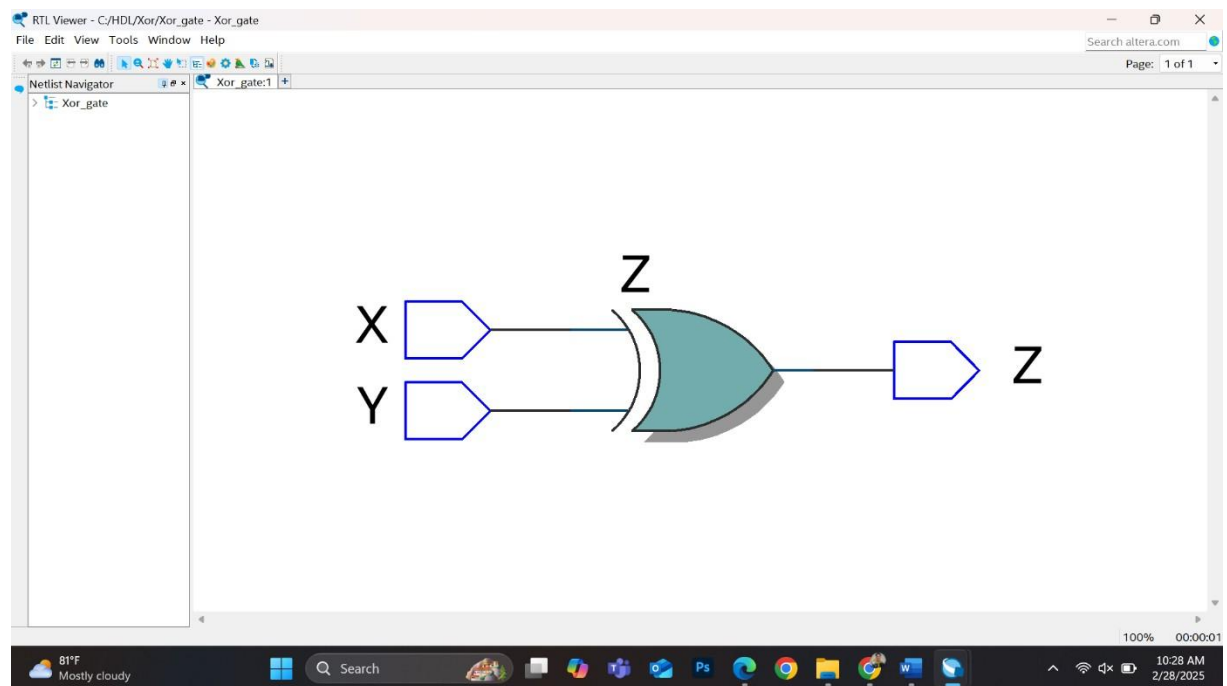
## Experiment results:

## DATA FLOW EXPERIMENTS:

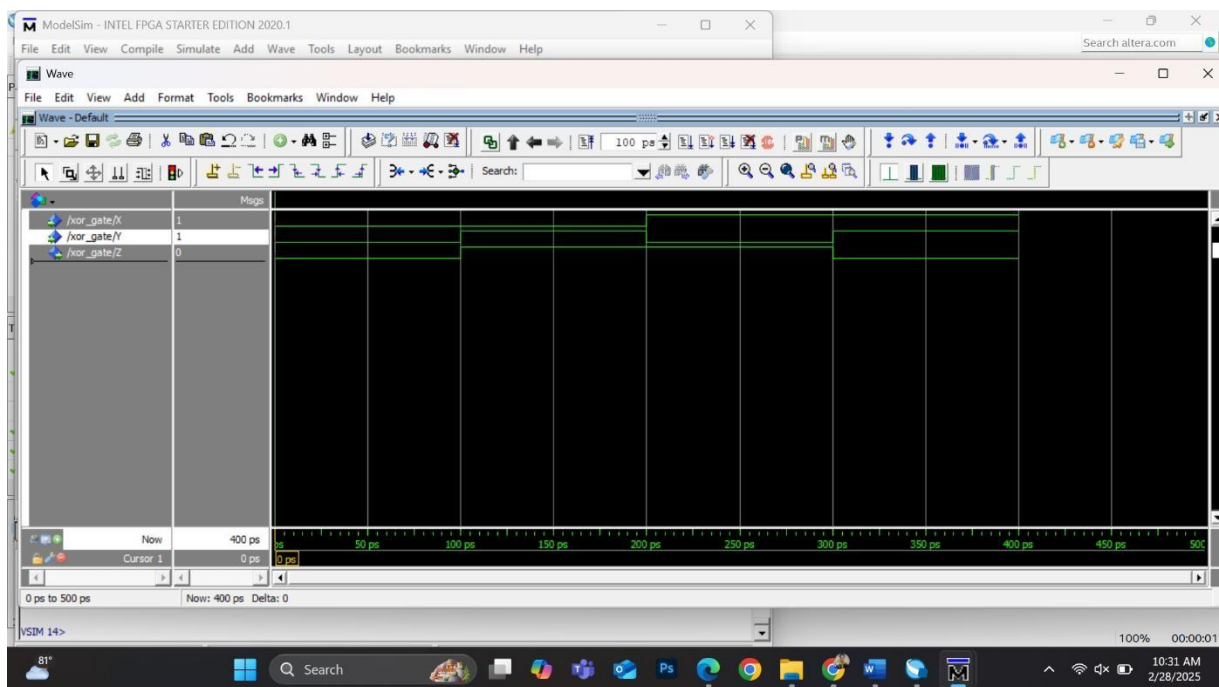
## CODE:



## LOGIC GATE:



## WAVE FORM:



## BEHAVIORAL EXPERIMENTS:

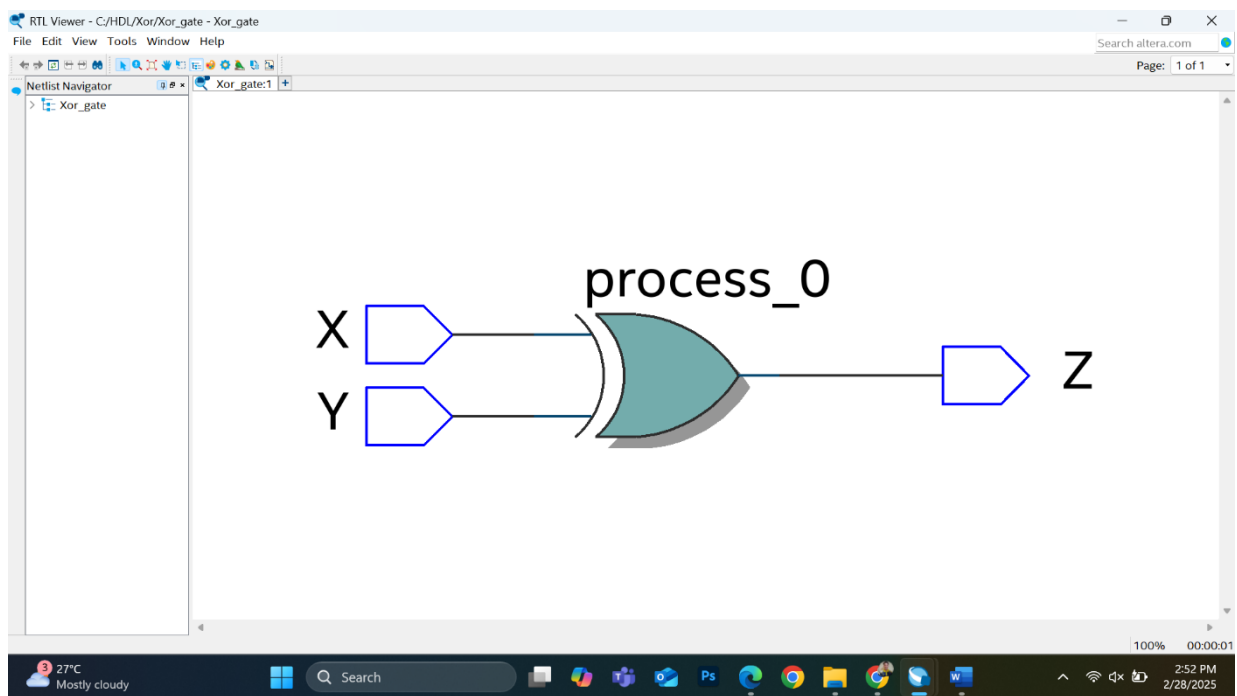
## CODE:

```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity Xor_gate is
5  Port (
6  X: in STD_LOGIC;
7  Y: in STD_LOGIC;
8  Z: out STD_LOGIC
9  );
10 end Xor_gate;
11
12 architecture behav2 of Xor_gate is
13 begin
14 process (X, Y)
15 begin
16   if (X=Y) then -- Compare with truth table
17     Z <= '1';
18   else
19     Z <= '0';
20   end if;
21 end process;
22 end behav2;
```

The screenshot also shows the Project Navigator, Tasks pane, and Messages pane. The Messages pane displays the following messages:

```
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
```

## LOGIC GATE:



## WAVE FORM:

