Name: Richard Raymond J. Canda

C.Y.S.: BSCpE-3A

#2-TITLE: OR gate

LOGIC GATE SYMBOL:

7432

TRUTH TABLE:

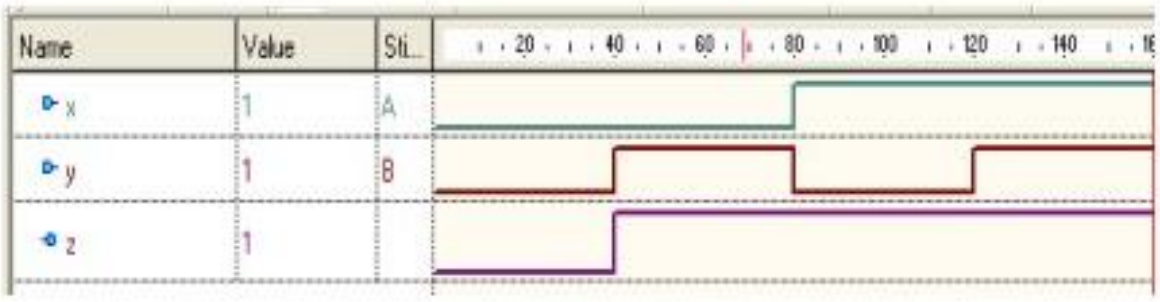
x	y	z
0	0	0
0	1	1
1	0	1
1	1	1

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity OR2 is
        port(
                x : in STD_LOGIC;
                y : in STD_LOGIC;
                z : out STD_LOGIC
            );
end OR2;

--Dataflow model
architecture behav1 of OR2 is
 begin

   Z <= x or y;          --Signal Assignment Statement

end behav1;
```

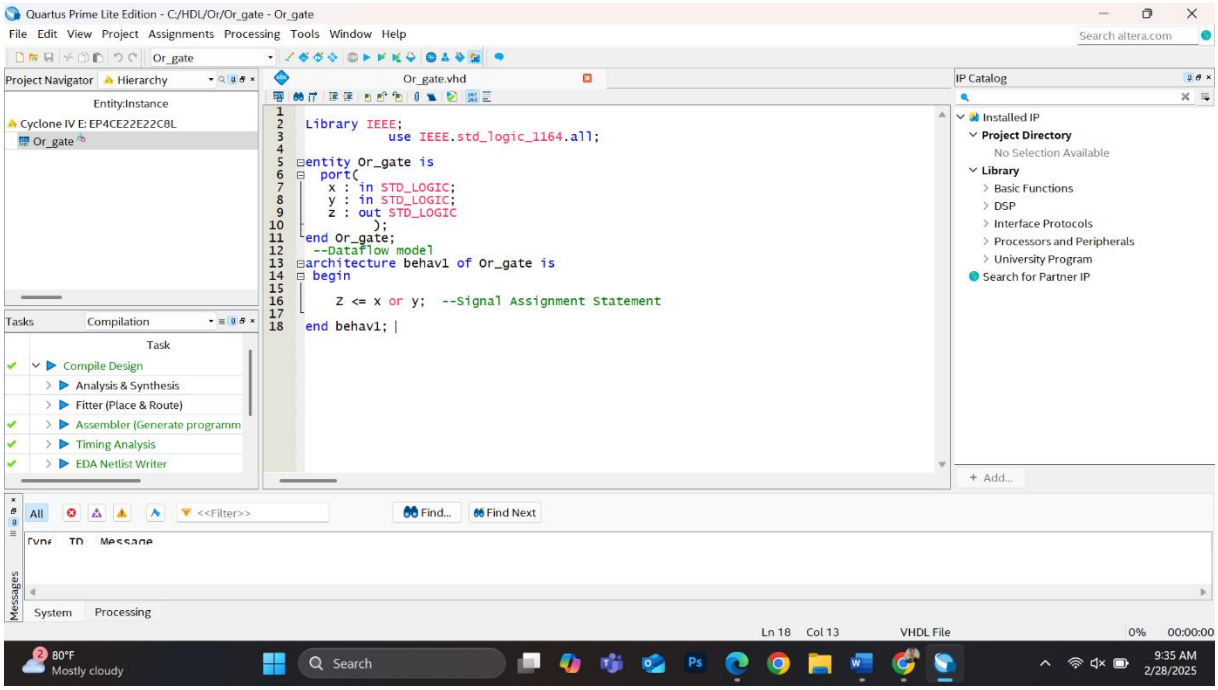
```
-- Behavioral model

        architecture behav2 of OR2 is
         begin

            process (x, y)
              begin

                  if (x='0' and y='0') then  -- Compare with truth table
                    Z <= '0';
                  else
                    Z<= '1';
                  end if;

              end process;

        end behav2;
```

OUTPUT WAVEFORM:

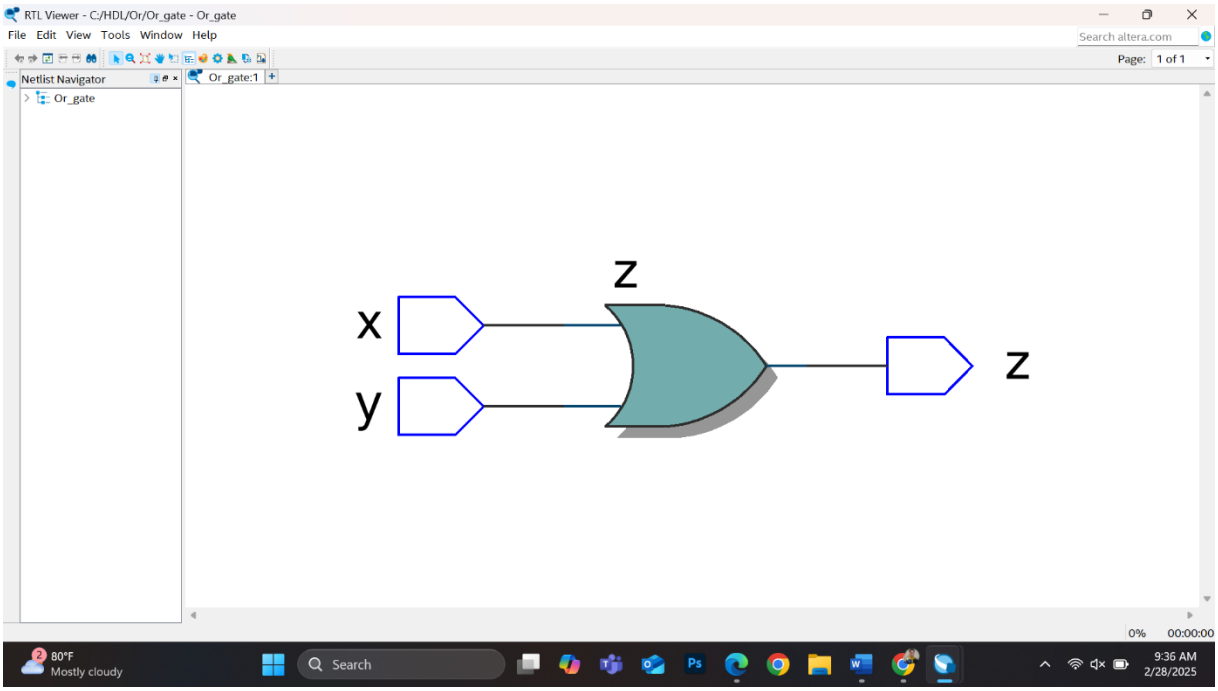


Experiment results:

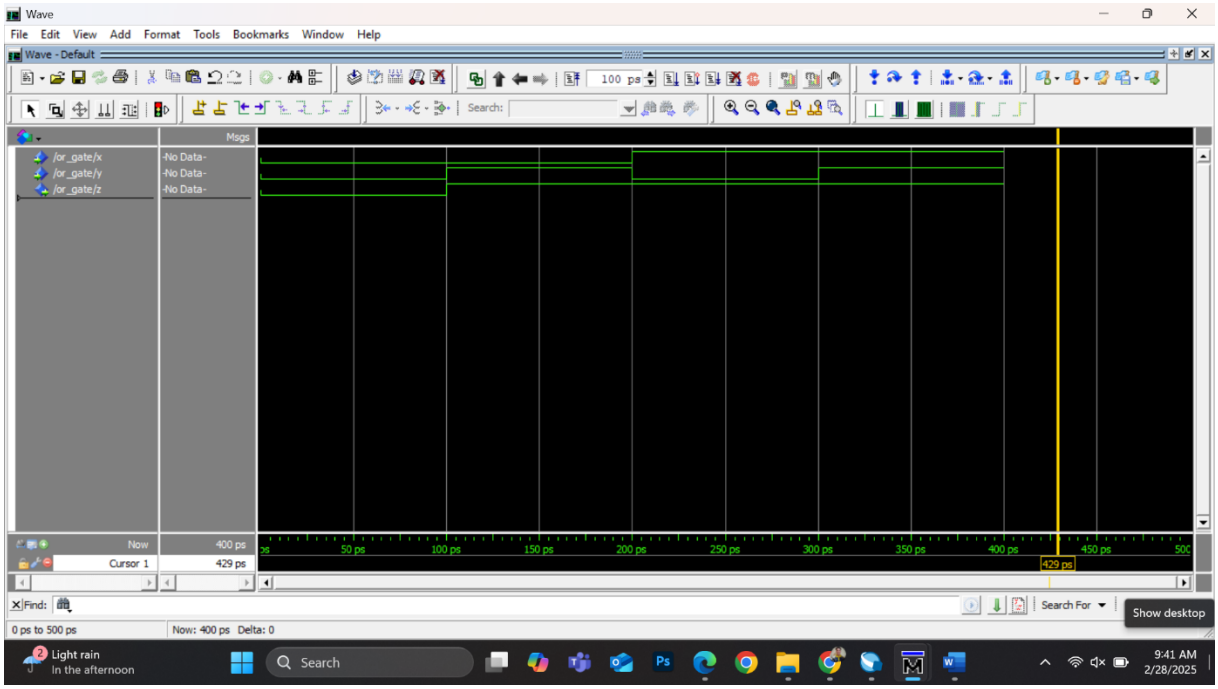
CODE



LOGIC GATE



WAVE


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Msgs
/or_gate/x
/or_gate/y
/or_gate/z
-No Data-
-No Data-
-No Data-
Now
400 ps
Cursor 1
429 ps
50 ps
100 ps
150 ps
200 ps
250 ps
300 ps
350 ps
400 ps
450 ps
429 ps
Find:
Search For
Show desktop
0 ps to 500 ps
Now: 400 ps Delta: 0
Light rain
In the afternoon
Search
9:41 AM
2/28/2025