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C.Y.S.: BSCpE-3A

#4-TITLE: NAND gate

LOGIC GATE SYMBOL:

7400

TRUTH TABLE:

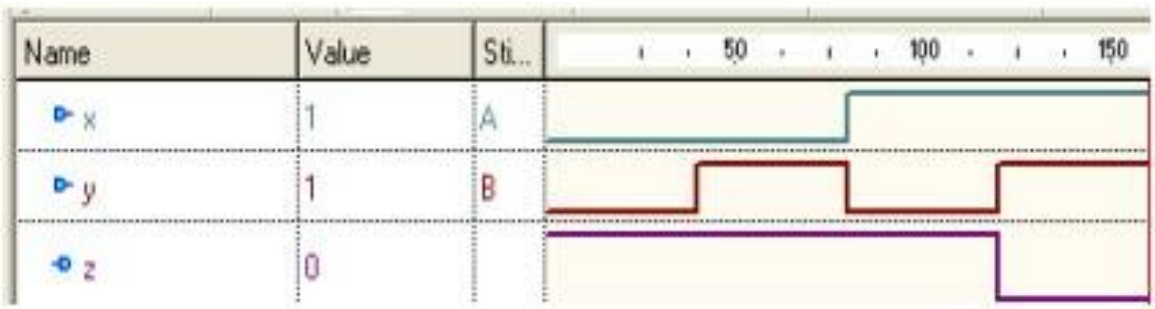
x	y	z
0	0	1
0	1	1
1	0	1
1	1	0

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity nand2 is
        port(
                x : in STD_LOGIC;
                y : in STD_LOGIC;
                z : out STD_LOGIC
            );
end nand2;
```

```
--Dataflow model

        architecture behav1 of nand2 is
        begin

                z<= x nand y;          --Signal Assignment Statement

        end behav1;


-- Behavioral model

        architecture behav2 of nand2 is
        begin

         Process (x, y)
          Begin

            If (x='1' and y='1') then  -- Compare with truth table
                Z <= '0';
            else
                Z <= '1';
            end if;

         end process;

       end behav2;
```

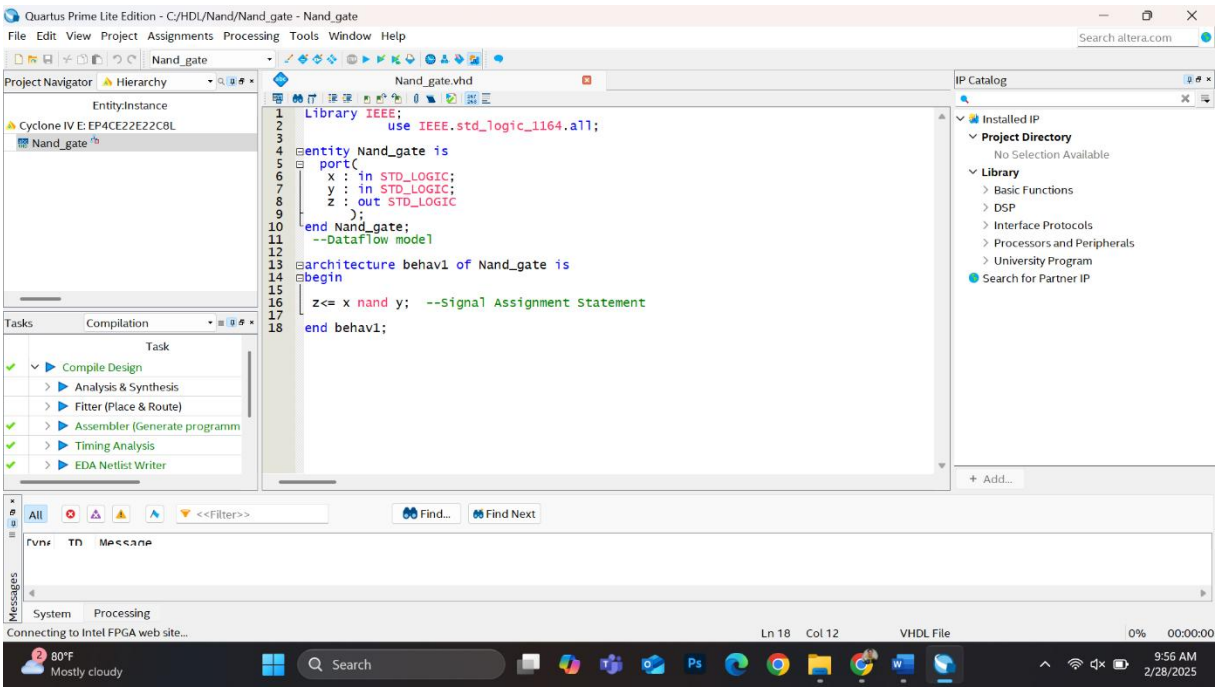
OUTPUT WAVEFORM:



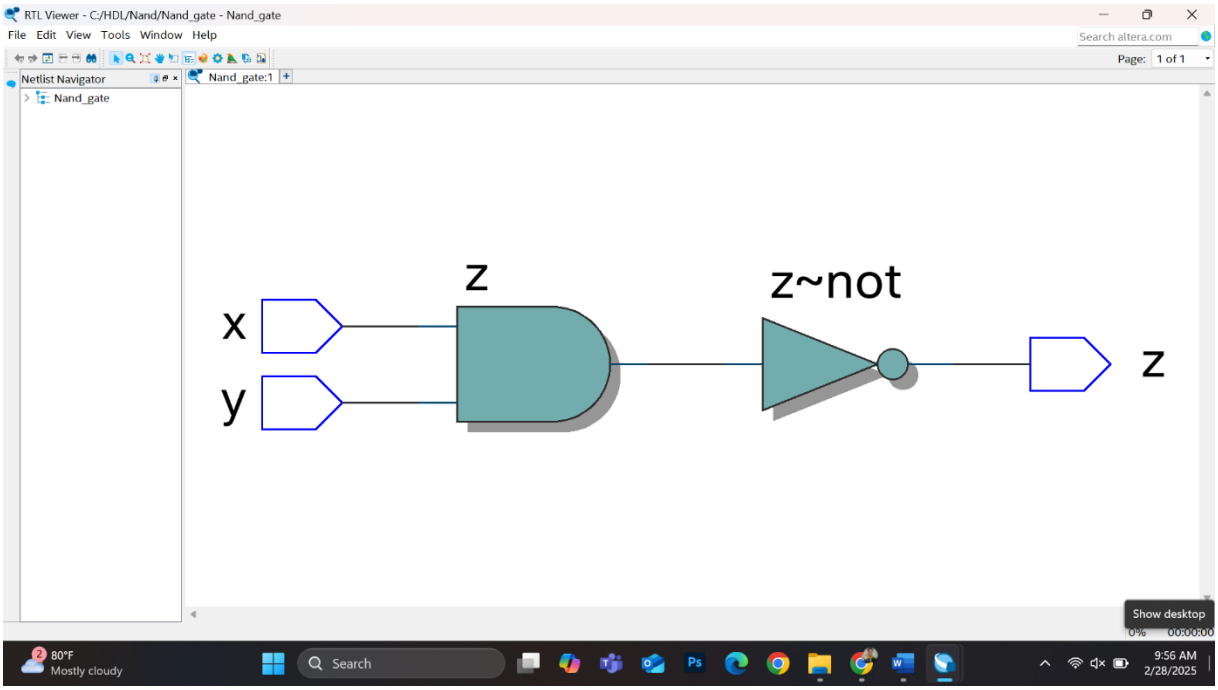
Experiment results:

DATA FLOW MODEL EXPERIMENT:

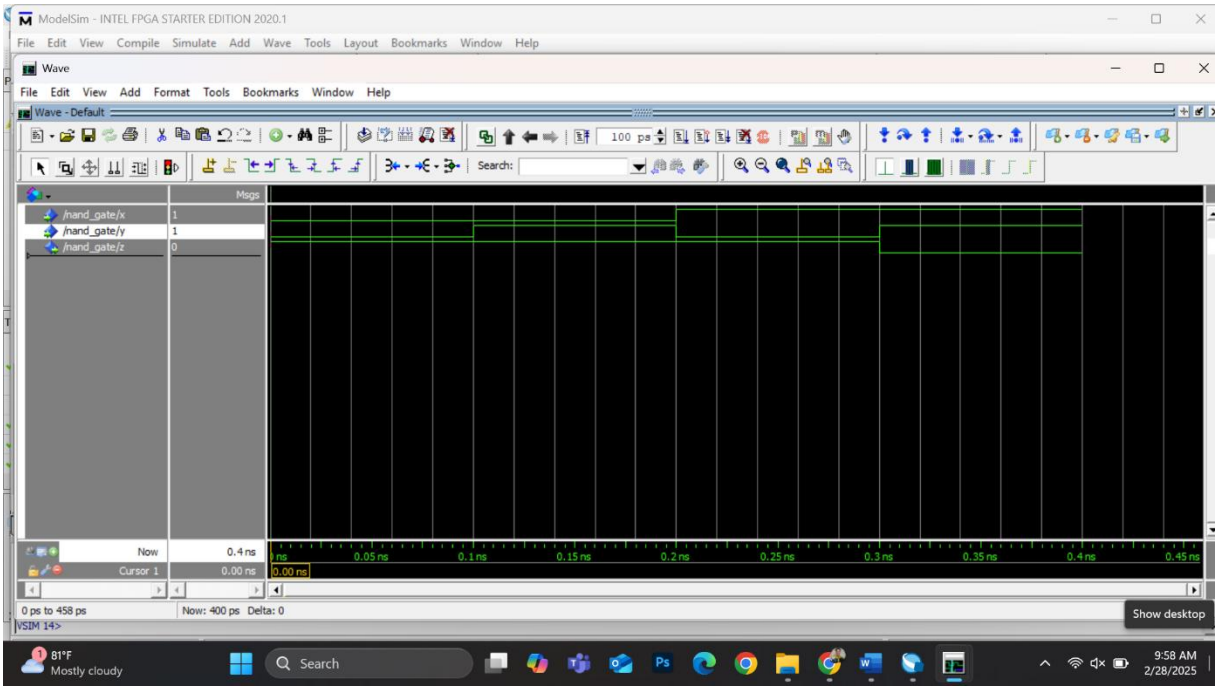
CODE:



LOGIC GATE:

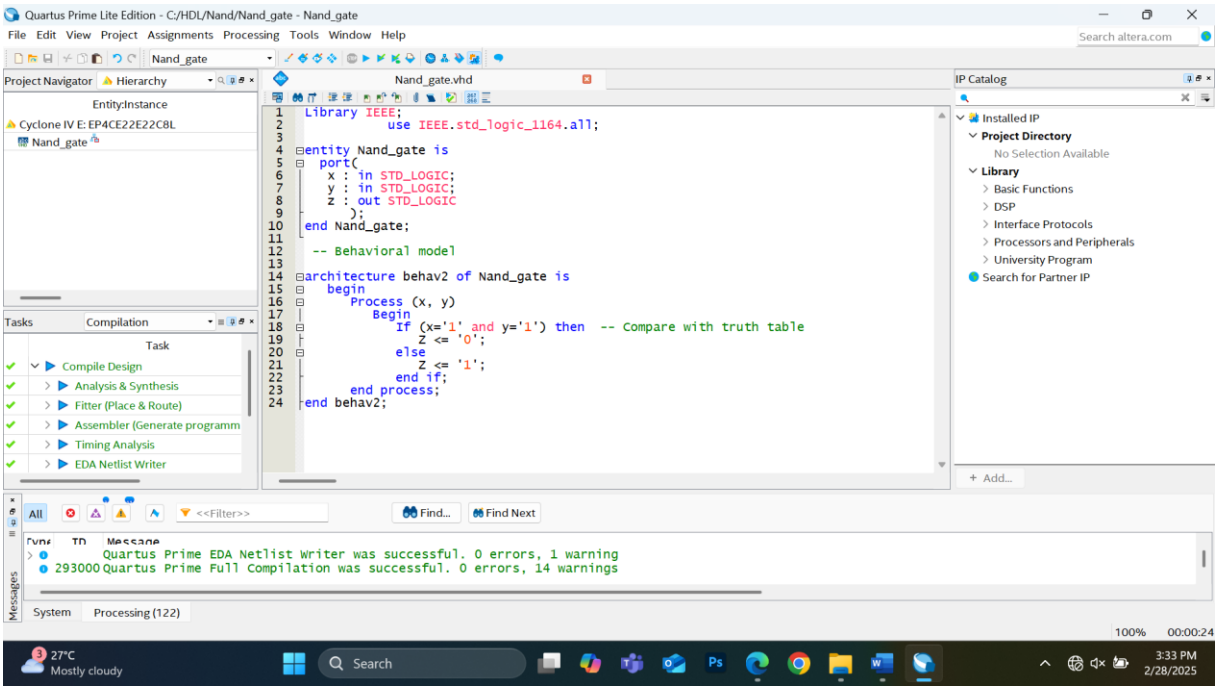


WAVEFORM:

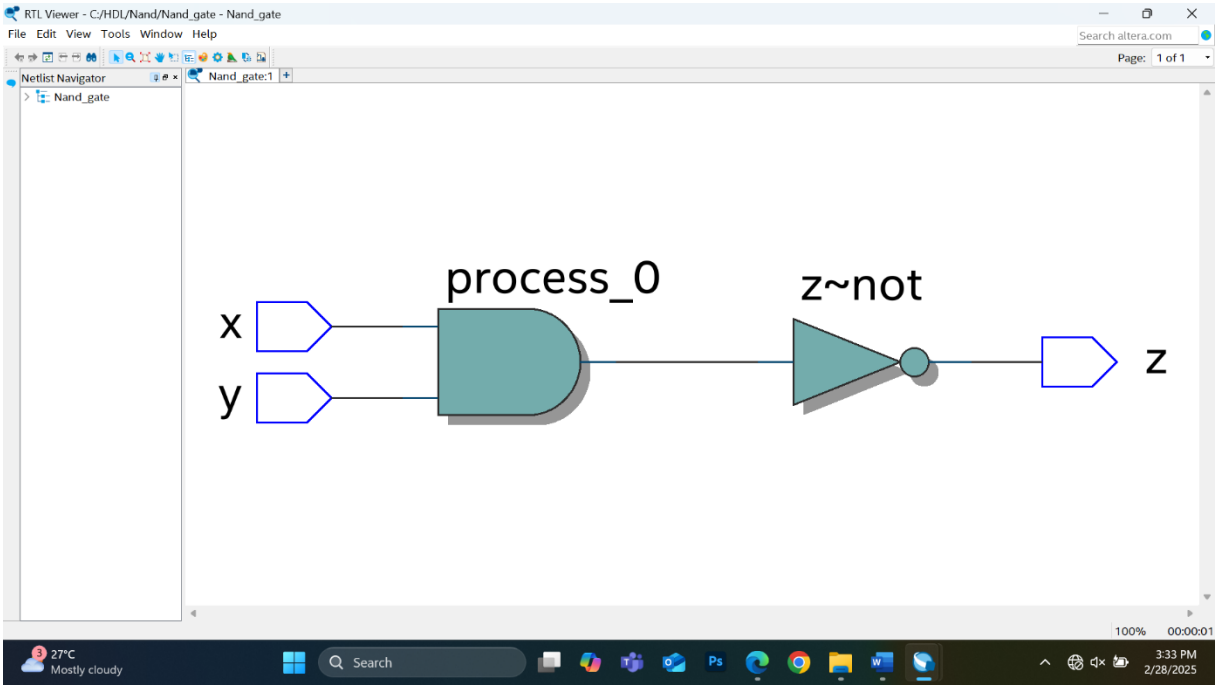


BEHAVIORAL MODEL EXPERIMENT:

CODE:



LOGIC GATE:



WAVEFORM: