Name: Richard Raymond J. Canda

C.Y.S.: BSCpE – 3A

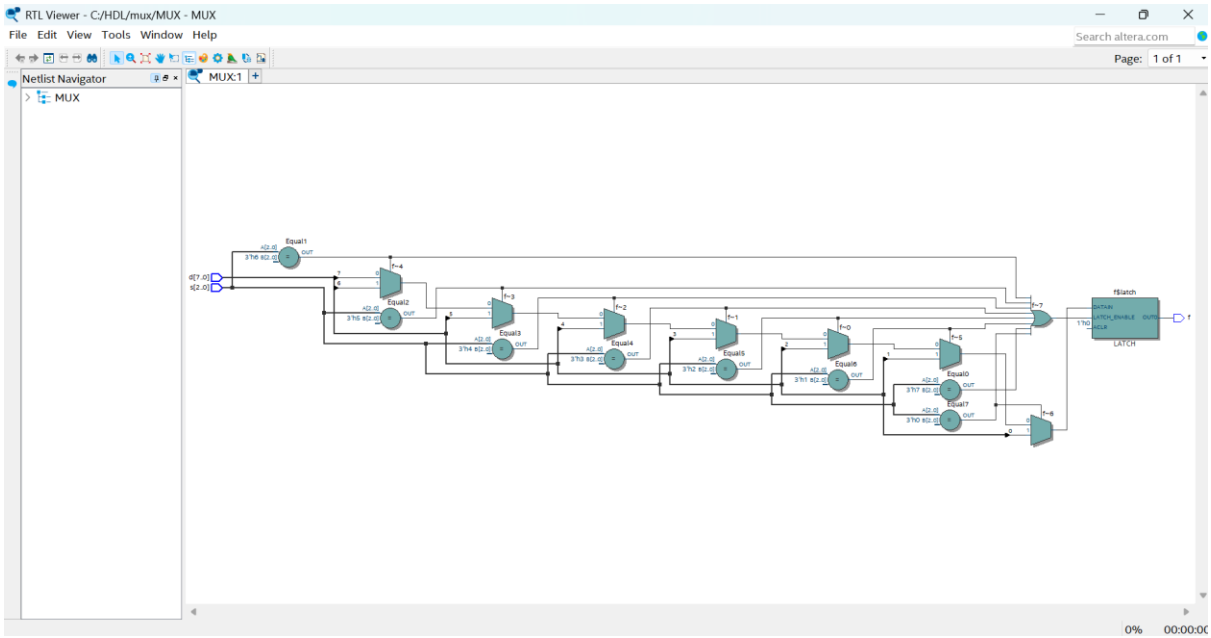
The **CODE:**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity MUX is
   Port ( d : in  STD_LOGIC_VECTOR (7 downto 0);
          s : in  STD_LOGIC_VECTOR (2 downto 0);
          f : out  STD_LOGIC);
end MUX-;
architecture Behavioral of MUX is
begin
f<= d(0) when s="000" else
d(1) when s="001" else
d(2) when s="010" else
d(3) when s="011" else
d(4) when s="100" else
d(5) when s="101" else
d(6) when s="110" else
d(7) when s="111";
end Behavioral;
```

mux.tdf | MUX.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5  entity MUX is
6      Port ( d : in  STD_LOGIC_VECTOR (7 downto 0);
7             s : in  STD_LOGIC_VECTOR (2 downto 0);
8             f : out  STD_LOGIC);
9  end MUX;
10 architecture Behavioral of MUX is
11 begin
12 f<= d(0) when s="000" else
13 d(1) when s="001" else
14 d(2) when s="010" else
15 d(3) when s="011" else
16 d(4) when s="100" else
17 d(5) when s="101" else
18 d(6) when s="110" else
19 d(7) when s="111";
20 end Behavioral;
```

THE **LOGIC GATE**:



THE **WORKBENCH:**