Name: Richard Raymond J. Canda

C.Y.S.: BSCpE-3A

1.LOGIC GATES

AIM: Write a VHDL code for all the logic gates.

#1-TITLE: AND gate

LOGIC GATE SYMBOL:

7408N

TRUTH TABLE:

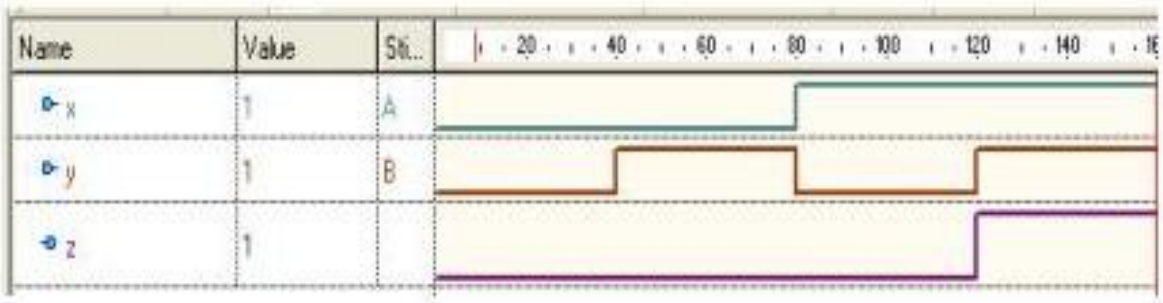
x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity AND2 is
        port(
                x : in STD_LOGIC;
                y : in STD_LOGIC;
                z : out STD_LOGIC
            );
end AND2;
```

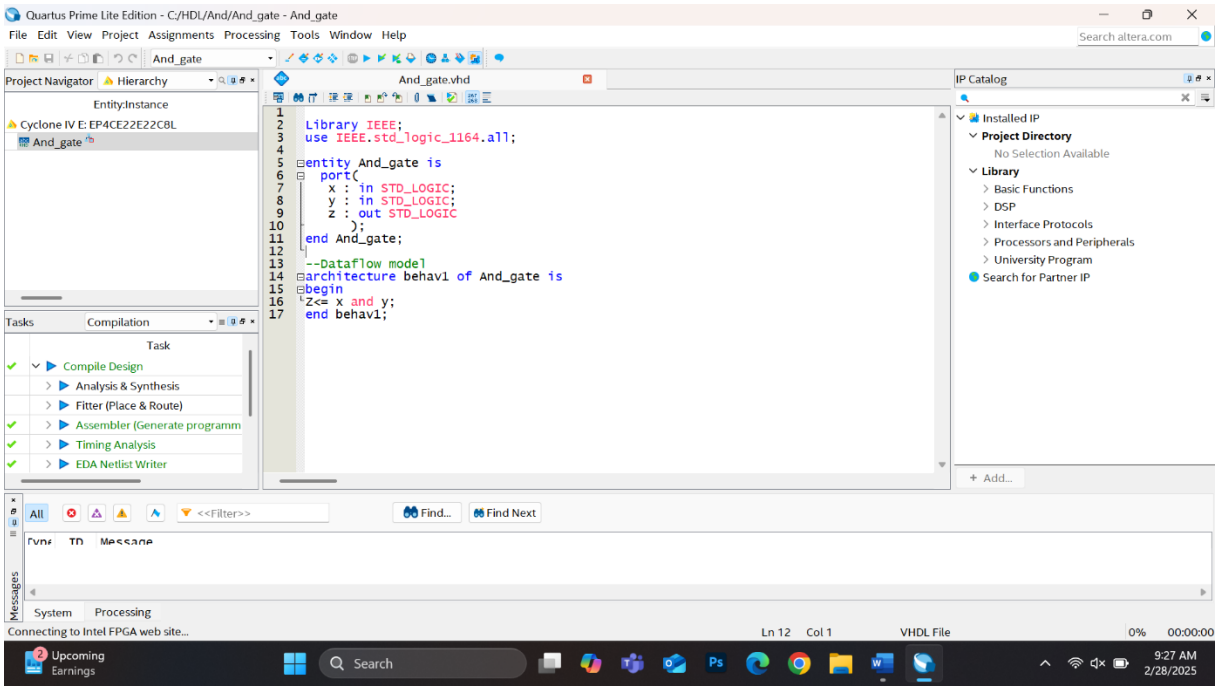
```
--Dataflow model

architecture behav1 of AND2 is
begin

   Z<= x and y;          --Signal Assignment Statement

end behav1;

-- Behavioral model

architecture behav2 of AND2 is
begin

   process (x, y)
    begin

        if (x='1' and y='1') then    -- Compare with truth table
         Z <= '1';
        else
         Z <= '0';
        end if;

   end process;

end behav2;
```

OUT PUT WAVE FORM:

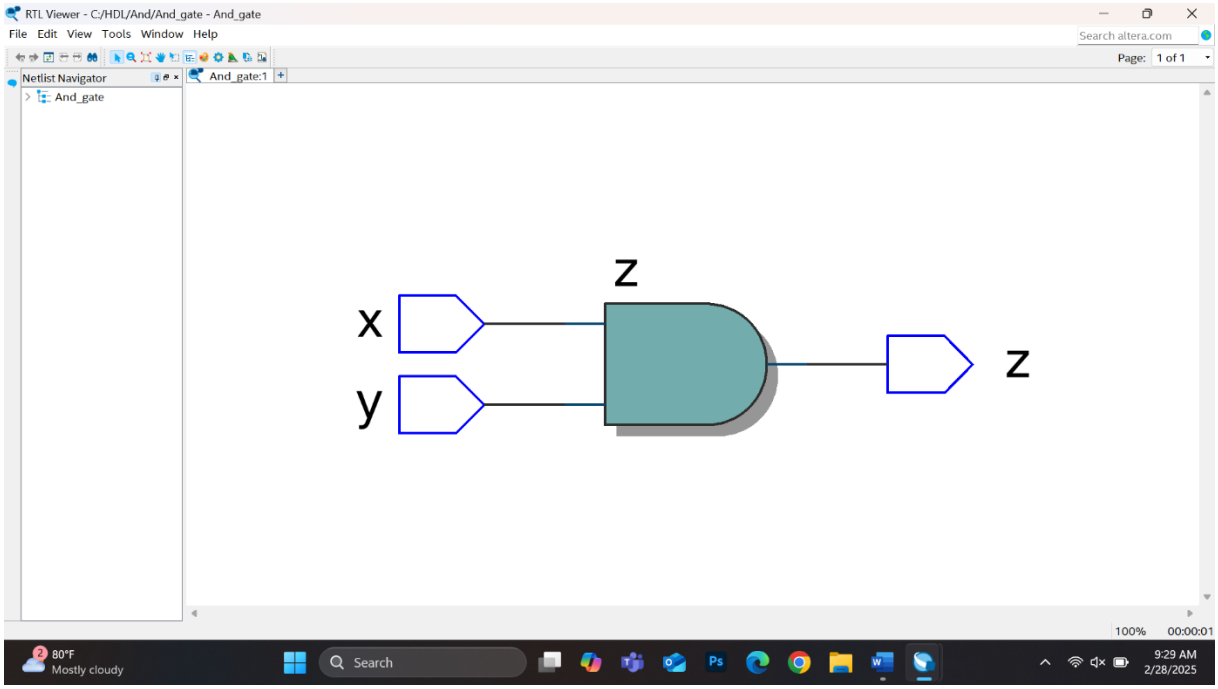


Experiment results:

CODE



LOGIC GATES



WAVE in TEST BENCH