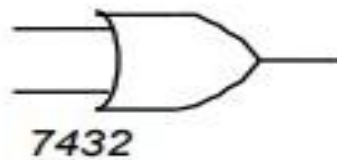


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C.Y.S.: BSCpE-3A

#2-TITLE: OR gate

LOGIC GATE SYMBOL:



TRUTH TABLE:

| x | y | z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity OR2 is
  port(
    x : in STD_LOGIC;
    y : in STD_LOGIC;
    z : out STD_LOGIC
  );
end OR2;

--Dataflow model
architecture behav1 of OR2 is
begin

  Z <= x or y;      --Signal Assignment Statement

end behav1;
```

→ Behavioral model

```
architecture behav2 of OR2 is  
begin
```

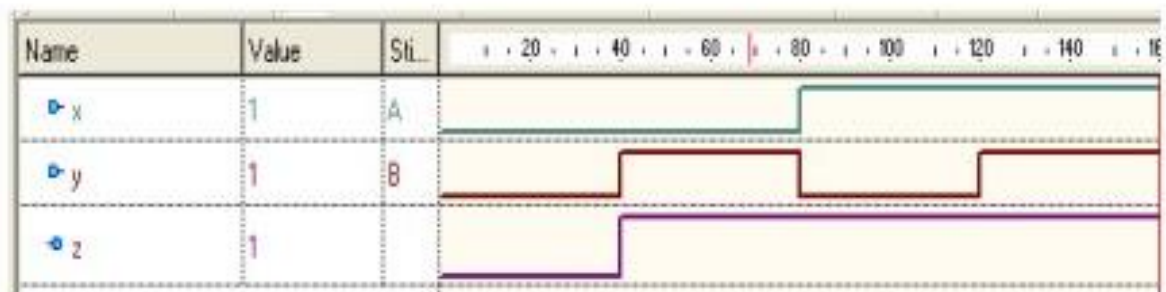
```
    process (x, y)  
    begin
```

```
        if (x='0' and y='0') then -- Compare with truth table  
            Z <= '0';  
        else  
            Z <= '1';  
        end if;
```

```
    end process;
```

```
end behav2;
```

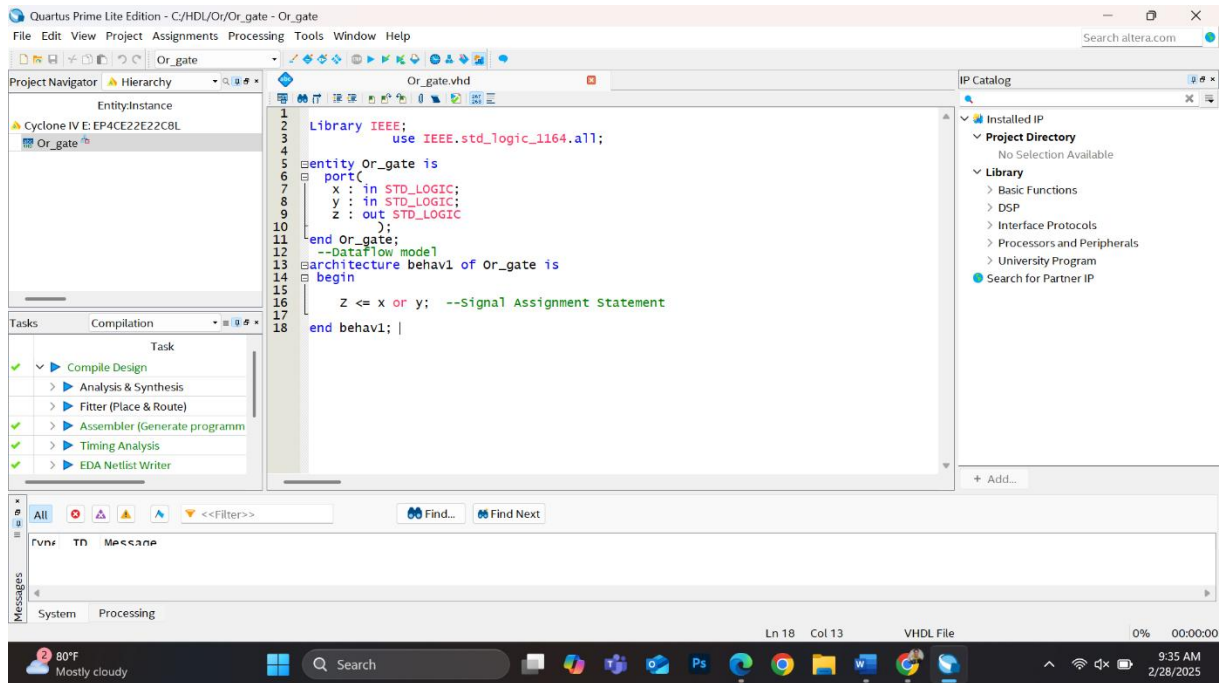
OUTPUT WAVEFORM:



Experiment results:

DATA FLOW MODEL EXPERIMENTS:

CODE:

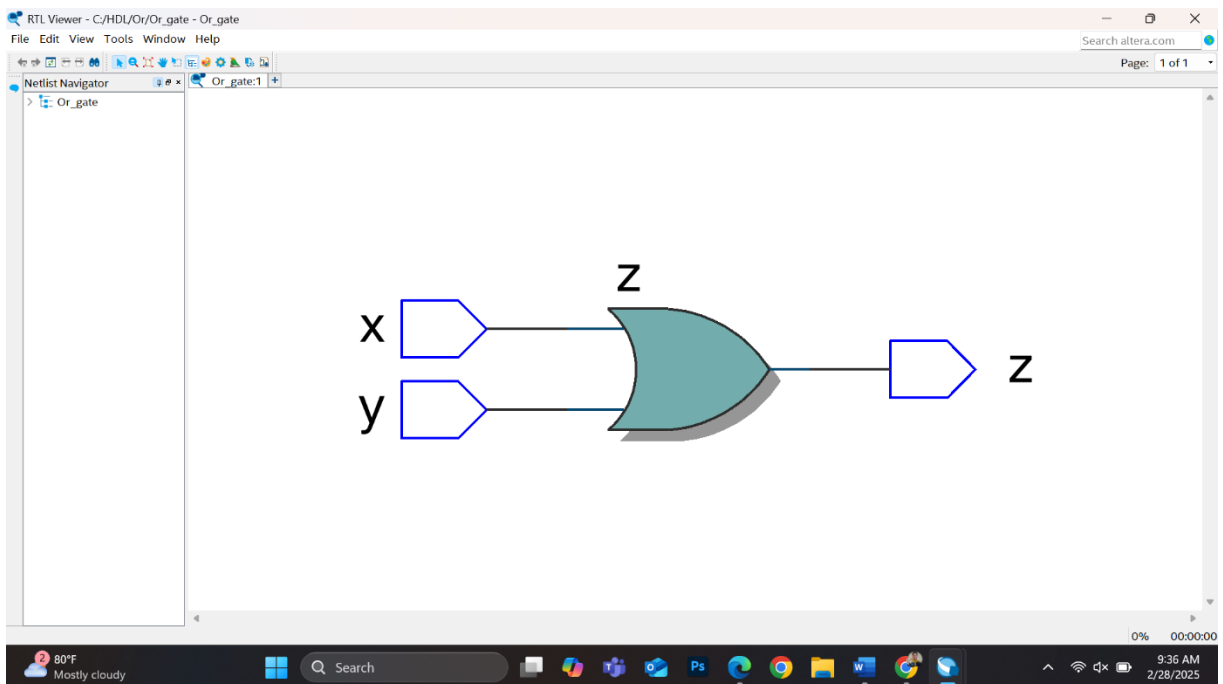


The screenshot shows the Quartus Prime Lite Edition interface. The main window displays the VHDL code for an OR gate named 'Or_gate'. The code is as follows:

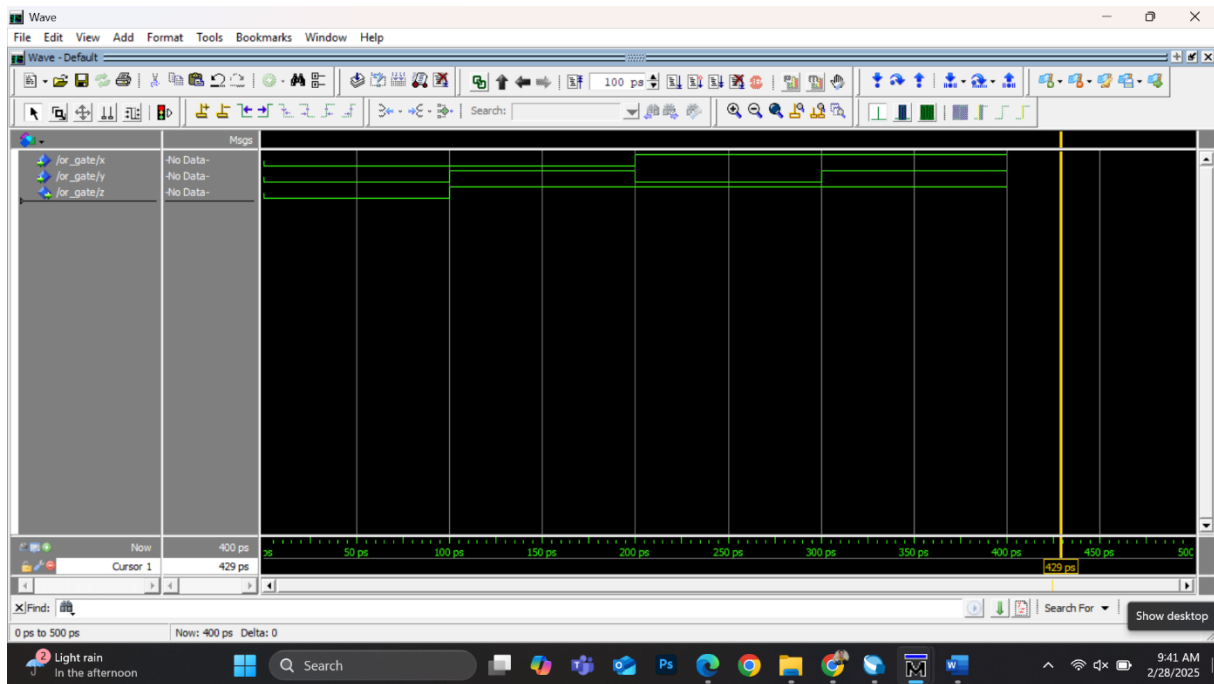
```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4
5  entity Or_gate is
6  port(
7    x : in STD_LOGIC;
8    y : in STD_LOGIC;
9    z : out STD_LOGIC
10 );
11 end Or_gate;
12 --Dataflow model
13 architecture behav1 of Or_gate is
14 begin
15     z <= x or y; --Signal Assignment Statement
16 end behav1;
```

The interface also shows the Project Navigator on the left, the Tasks window, and the IP Catalog on the right. The status bar at the bottom indicates the file is 'Or_gate.vhd' and the current position is 'Ln 18, Col 13'.

LOGIC GATE:



WAVEFORM:



BEHAVIORAL MODEL EXPERIMENTS:

CODE:

```
Quartus Prime Lite Edition - C:/HDL/Or/Or_gate - Or_gate
File Edit View Project Assignments Processing Tools Window Help
Search altera.com

Project Navigator | Hierarchy | Or_gate.vhd | IP Catalog

EntityInstance
Cyclone IV E: EP4CE22E22CBL
Or_gate

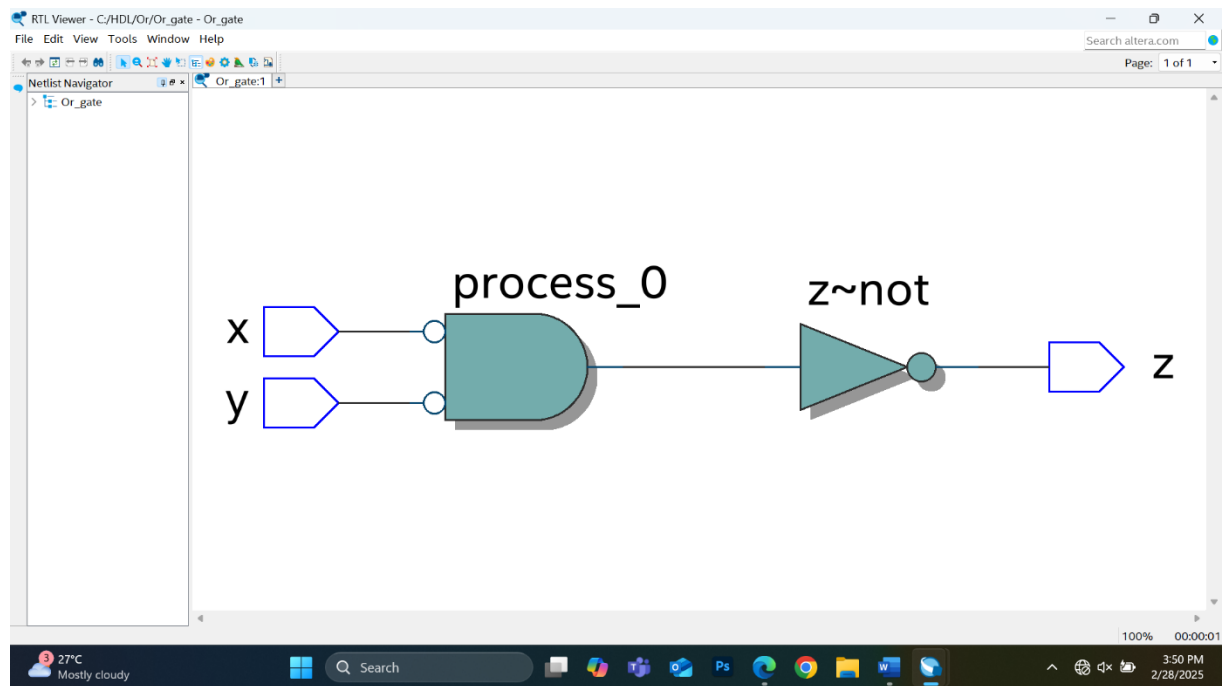
Tasks | Compilation | Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate program)
Timing Analysis
EDA Netlist Writer

1
2 Library IEEE;
3   use IEEE.std_logic_1164.all;
4
5 entity Or_gate is
6   port(
7     x : in STD_LOGIC;
8     y : in STD_LOGIC;
9     z : out STD_LOGIC
10  );
11 end Or_gate;
12
13 -- Behavioral model
14
15 architecture behav2 of Or_gate is
16   begin
17     process (x, y)
18     begin
19       if (x='0' and y='0') then -- Compare with truth table
20         z <= '0';
21       else
22         z <= '1';
23       end if;
24     end process;
25   end behav2;
26
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP

+ Add...

Messages
System Processing (122)
100% 00:00:26
27°C Mostly cloudy
Search
3:50 PM 2/28/2025
```

LOGIC GATE:



WAVEFORM:

