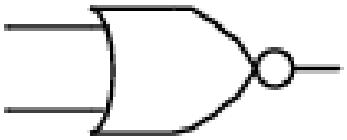
Name: Richard Raymond J. Canda

C.Y.S.: BSCpE-3A

#5- TITLE: NOR gate

LOGIC GATE SYMBOL:



7402

TRUTH TABLE:

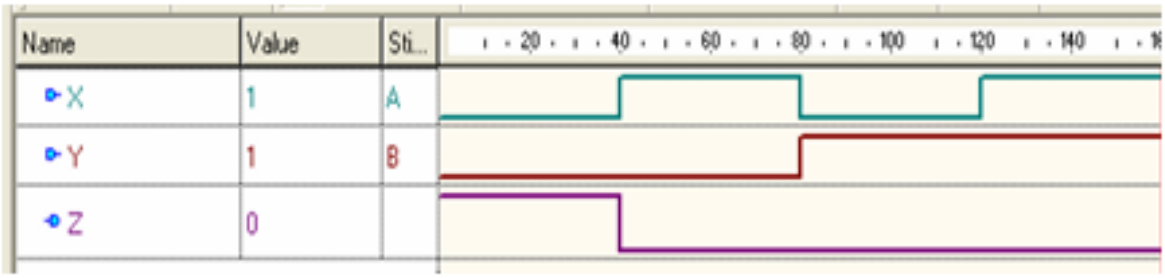
x	y	z
0	0	1
0	1	0
1	0	0
1	1	0

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity nor2 is
        Port (
                X: in STD_LOGIC;
                Y: in STD_LOGIC;
                Z: out STD_LOGIC
            );
end nor2;
```

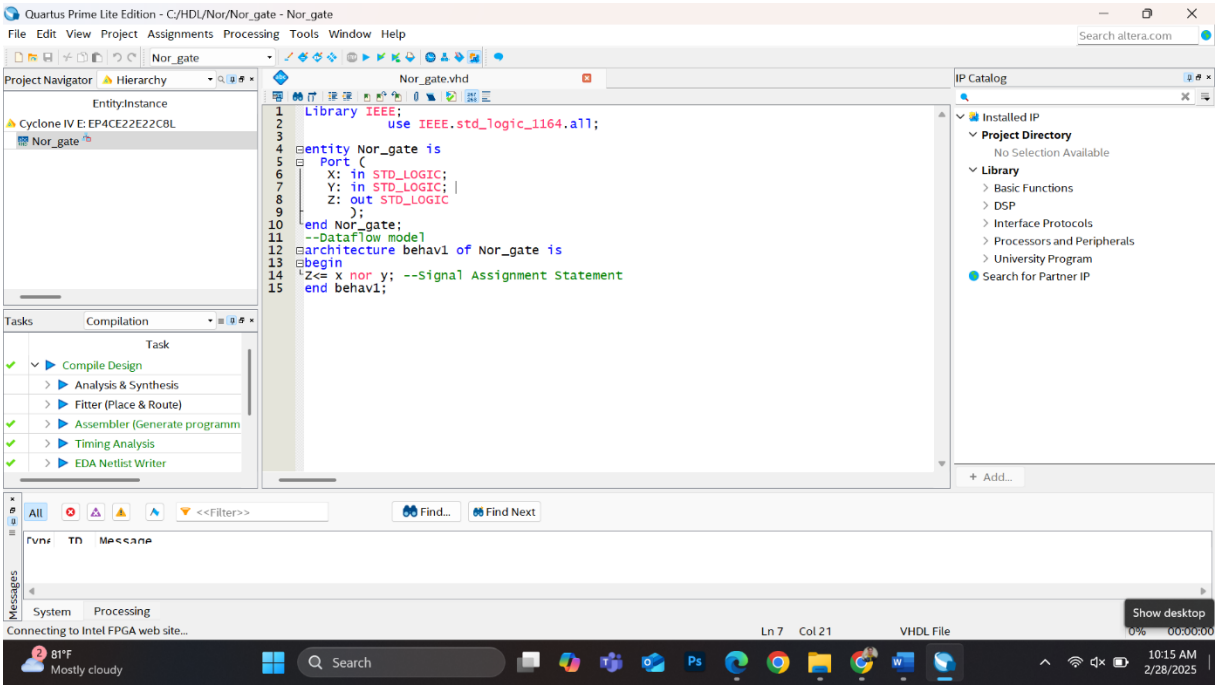
```
--Dataflow model

        architecture behav1 of nor2 is
        begin

                Z<= x nor y;    --Signal Assignment Statement

        end behav1;

-- Behavioral model

architecture behav2 of nor2 is
begin

          process (x, y)
           begin

             If (x='0' and y='0') then   -- Compare with truth table
               Z <= '1';
             else
               Z <= '0';
             end if;

           end process;

         end behav2;
```

OUTPUT WAVEFORM:

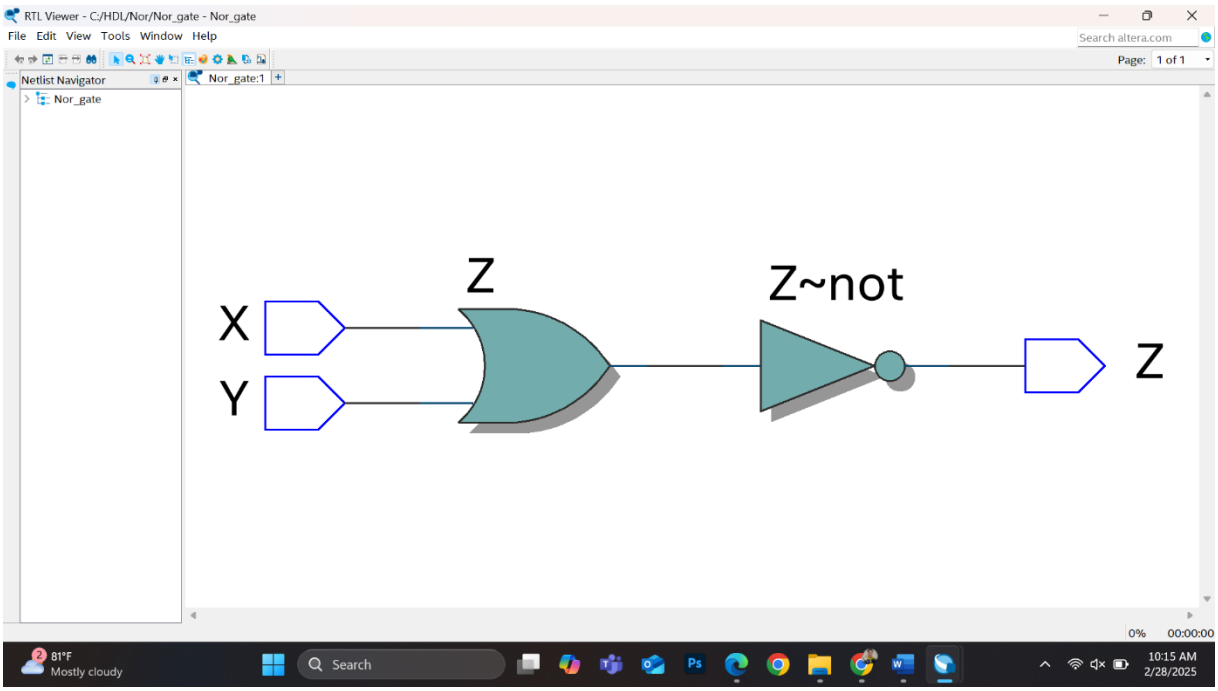


Experiment results:

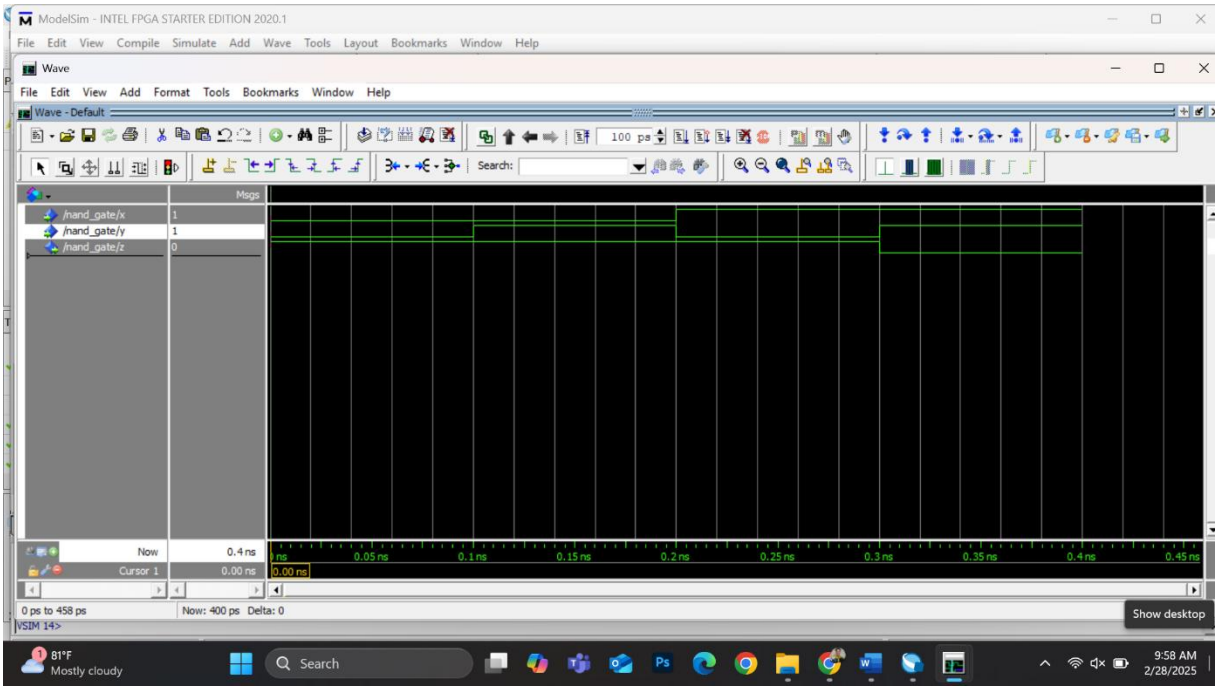
CODE



LOGIC GATE



WAVE


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/nand_gate/x
/nand_gate/y
/nand_gate/z
1
1
0
Now
0.4 ns
Cursor 1
0.00 ns
0.05 ns
0.1 ns
0.15 ns
0.2 ns
0.25 ns
0.3 ns
0.35 ns
0.4 ns
0.45 ns
0 ps to 458 ps
Now: 400 ps Delta: 0
VSIM 14>
Show desktop
81°F
Mostly cloudy
Search
9:58 AM
2/28/2025