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C.Y.S.: BSCpE-3A

#2-TITLE: OR gate

LOGIC GATE SYMBOL:

7432

TRUTH TABLE:

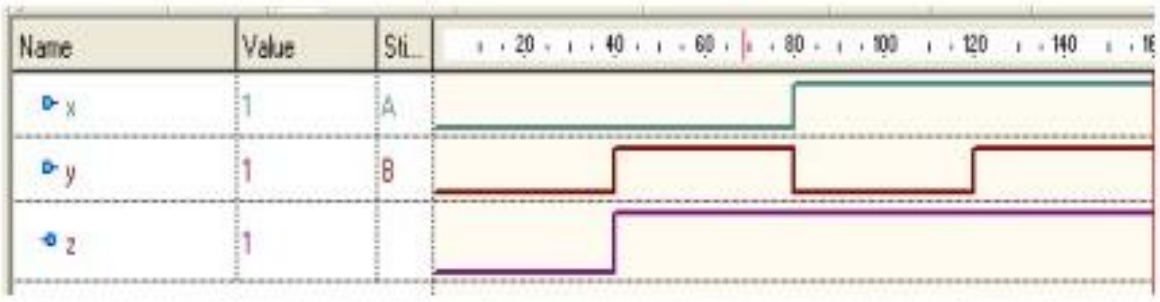
x	y	z
0	0	0
0	1	1
1	0	1
1	1	1

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity OR2 is
        port(
                x : in STD_LOGIC;
                y : in STD_LOGIC;
                z : out STD_LOGIC
            );
end OR2;

--Dataflow model
architecture behav1 of OR2 is
 begin

   Z <= x or y;          --Signal Assignment Statement

end behav1;
```

```
-- Behavioral model

        architecture behav2 of OR2 is
         begin

            process (x, y)
              begin

                  if (x='0' and y='0') then  -- Compare with truth table
                    Z <= '0';
                  else
                    Z<= '1';
                  end if;

              end process;

        end behav2;
```

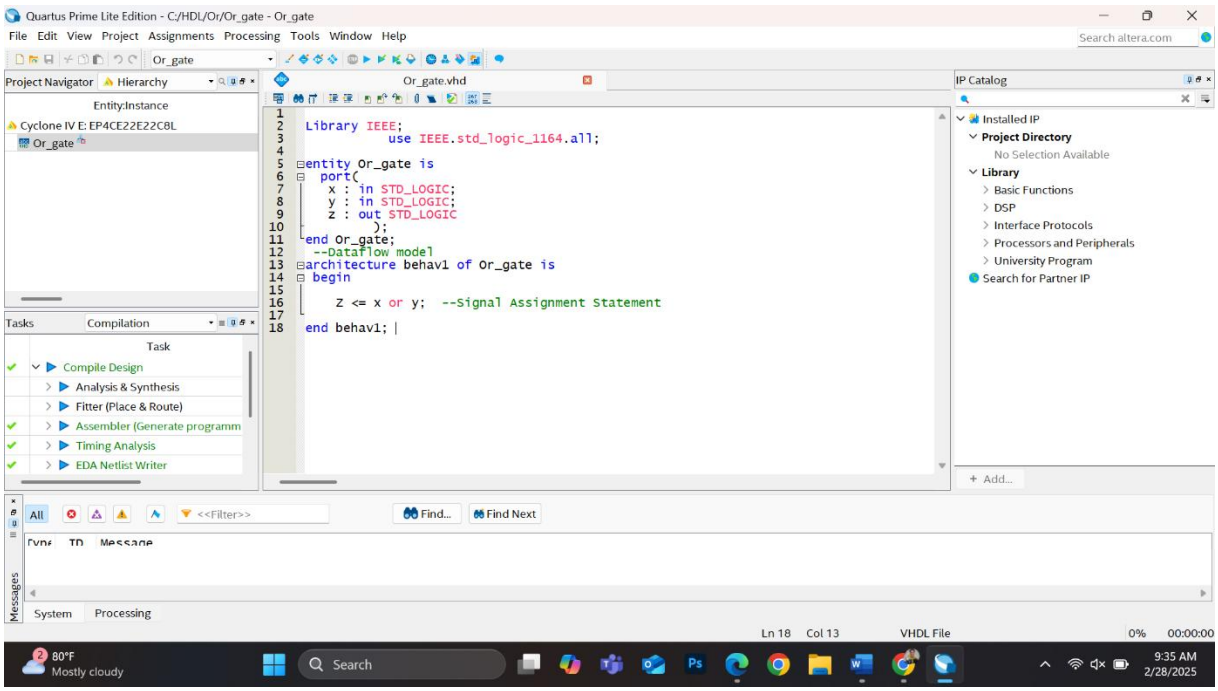
OUTPUT WAVEFORM:



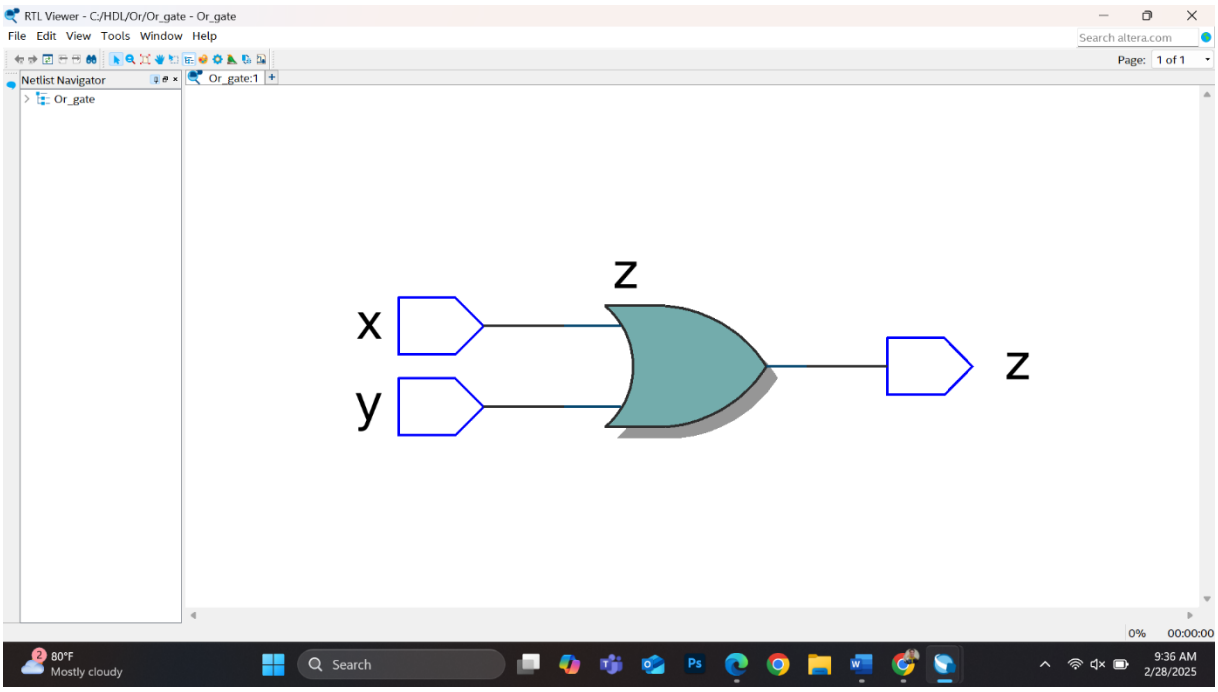
Experiment results:

DATA FLOW MODEL EXPERIMENTS:

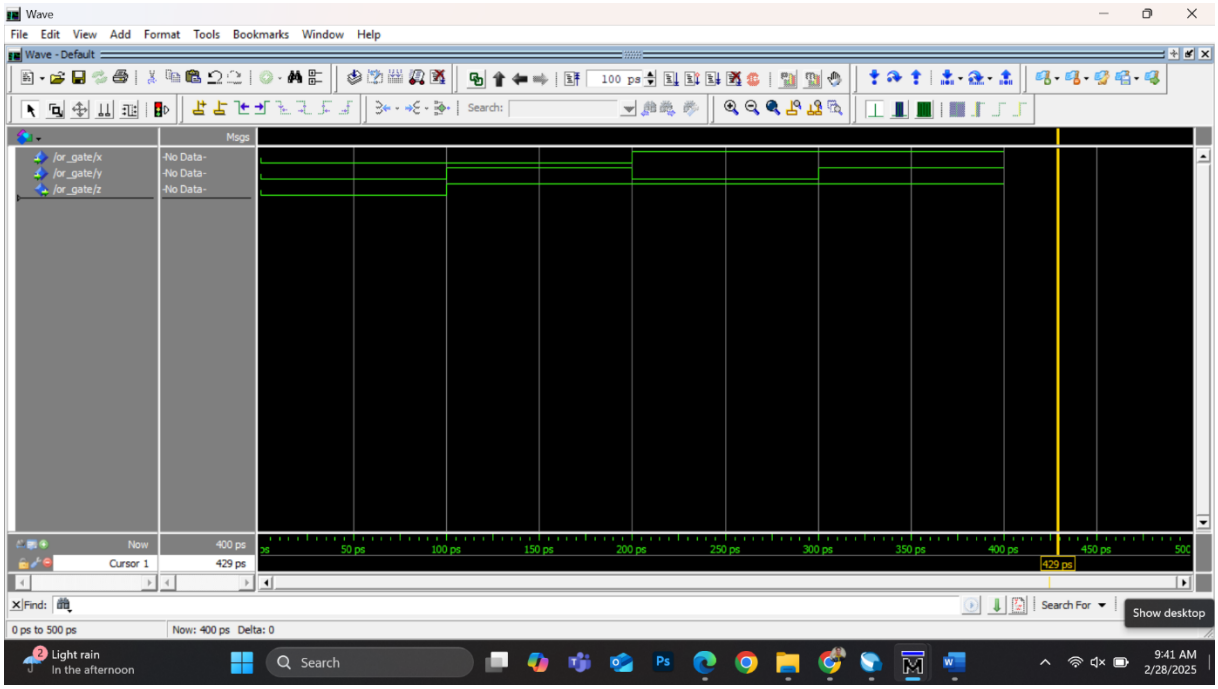
CODE:



LOGIC GATE:

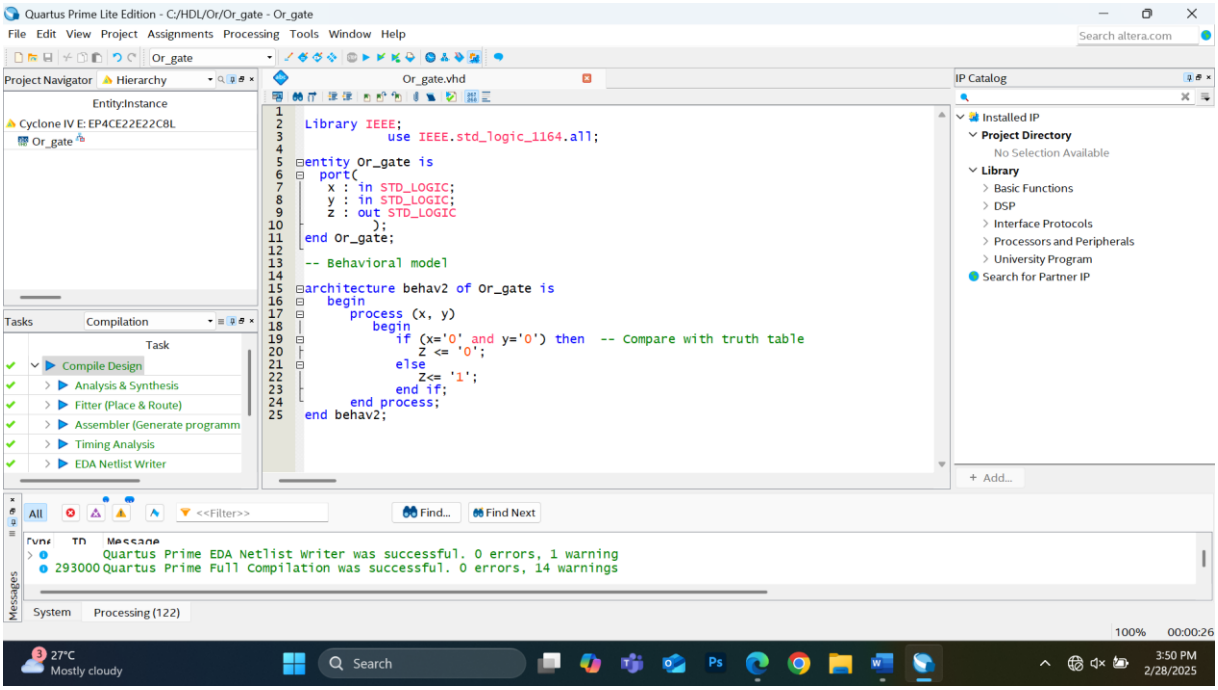


WAVEFORM:

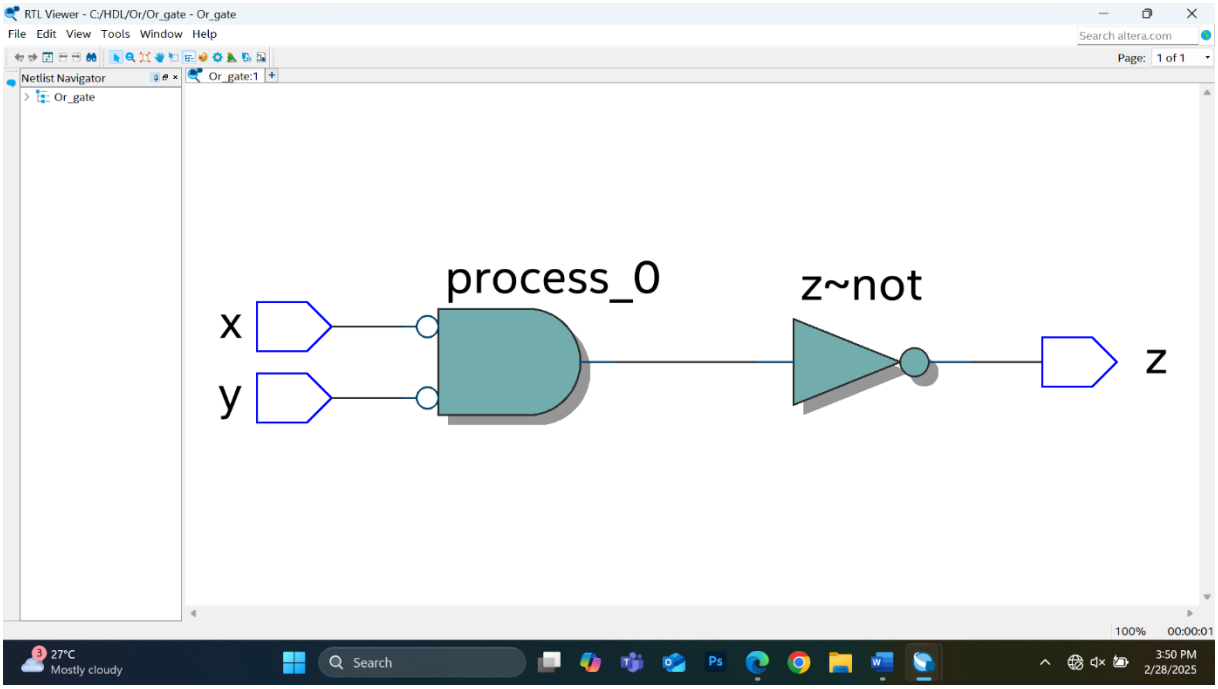


BEHAVIORAL MODEL EXPERIMENTS:

CODE:



LOGIC GATE:



WAVEFORM: