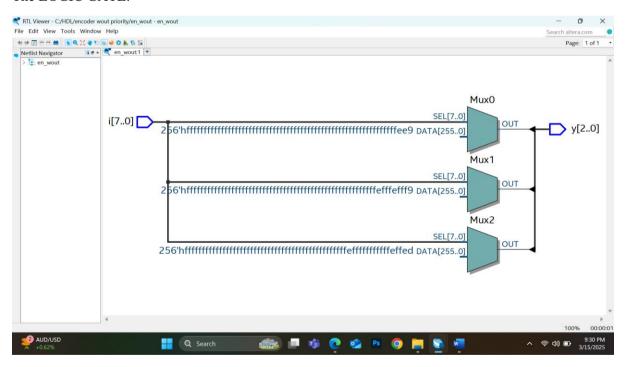
```
Name: Richard Raymond J. Canda
C.Y.S.: BSCpE - 3A
The CODE:
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity en_wout is
  Port (i: in STD_LOGIC_VECTOR (7 downto 0);
      y: out STD_LOGIC_VECTOR (2 downto 0));
end en_wout;
architecture Behavioral of en_wout is
begin
with i select
y<="000" when "00000001",
"001" when "00000010",
"010" when "00000100",
"011" when "00001000",
"100" when "00010000",
"101" when "00100000",
"110" when "01000000",
```

"111" when others;

end Behavioral;

```
en wout.vhd
library IEEE;
      use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
 2
 3
 4
      use IEEE.STD_LOGIC_UNSIGNED.ALL;
 5
    ⊟entity en_wout is
 6
           Port ( i : in STD_LOGIC_VECTOR (7 downto 0);
    7
                    y : out STD_LOGIC_VECTOR (2 downto 0));
 8
     Lend en_wout;
 9
    □architecture Behavioral of en_wout is
10
    ⊟beain
11
      with i select
     y<="000" when "00000001",
"001" when "00000010",
"010" when "00000100",
12
13
14
      "011" when "00001000".
15
     "100" when "00001000",
"101" when "00100000",
"110" when "01000000",
16
17
18
     "111" when others;
19
20
      end Behavioral;
```

The LOGIC GATE:



The **WAVEFORM**:

