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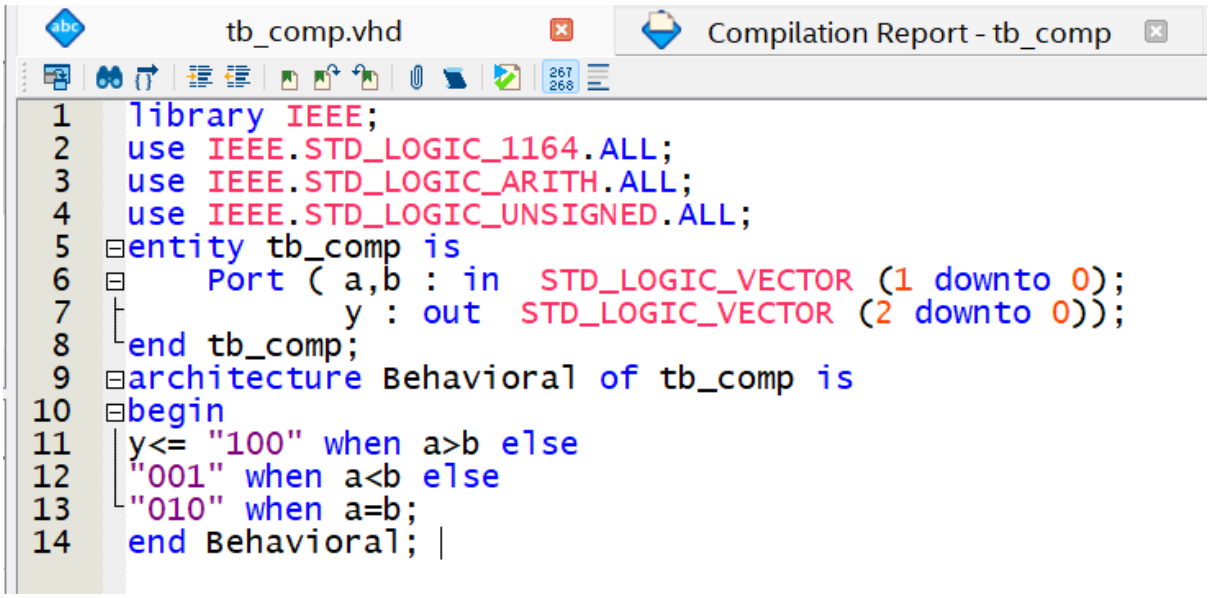
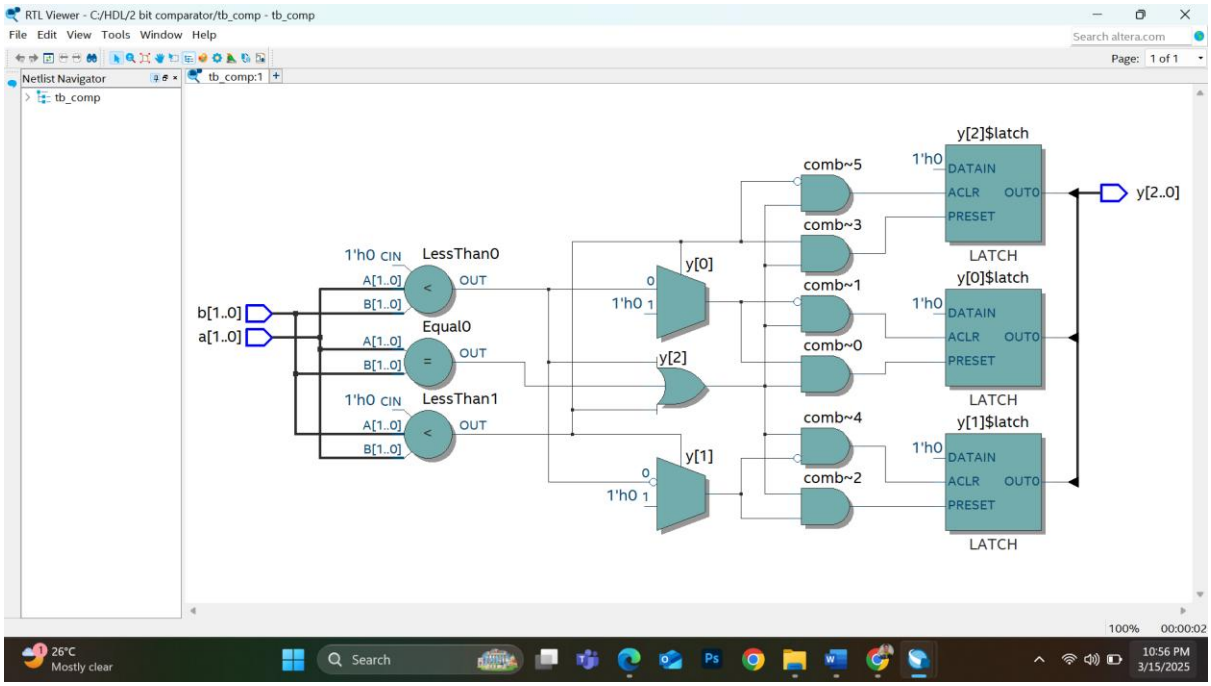
C.Y.S.: BSCpE – 3A

The CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity tb_comp is
    Port ( a,b : in  STD_LOGIC_VECTOR (1 downto 0);
           y : out  STD_LOGIC_VECTOR (2 downto 0));
end tb_comp;
architecture Behavioral of tb_comp is
begin
y<= "100" when a>b else
"001" when a<b else
"010" when a=b;
end Behavioral;
```



The LOGIC GATE:



The WAVEFORM: