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C.Y.S.: BSCpE-3A

#7-TITLE: EX-NOR gate

LOGIC GATE SYMBOL:

74135

TRUTH TABLE:

x	y	z
0	0	1
0	1	0
1	0	0
1	1	1

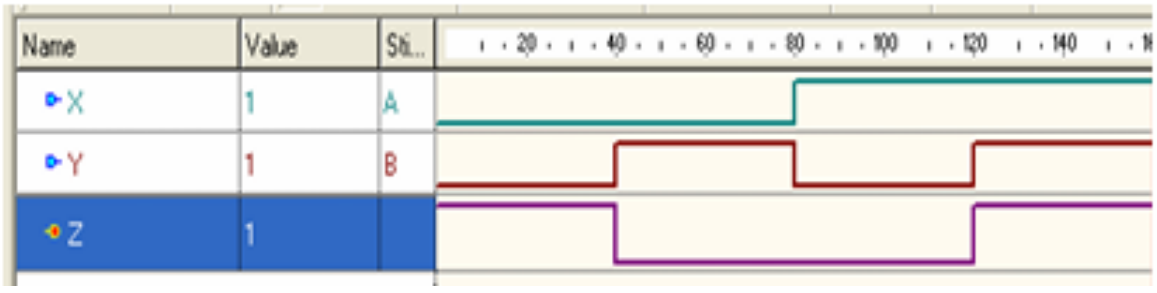
VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity xnor2 is
        Port (
                X: in STD_LOGIC;
                Y: in STD_LOGIC;
                Z: out STD_LOGIC
            );
end xnor2;
```

```
--Dataflow model

        architecture behav1 of xnor2 is
        begin

                Z<= x xnor y;  --Signal Assignment Statement

        end behav1;
```

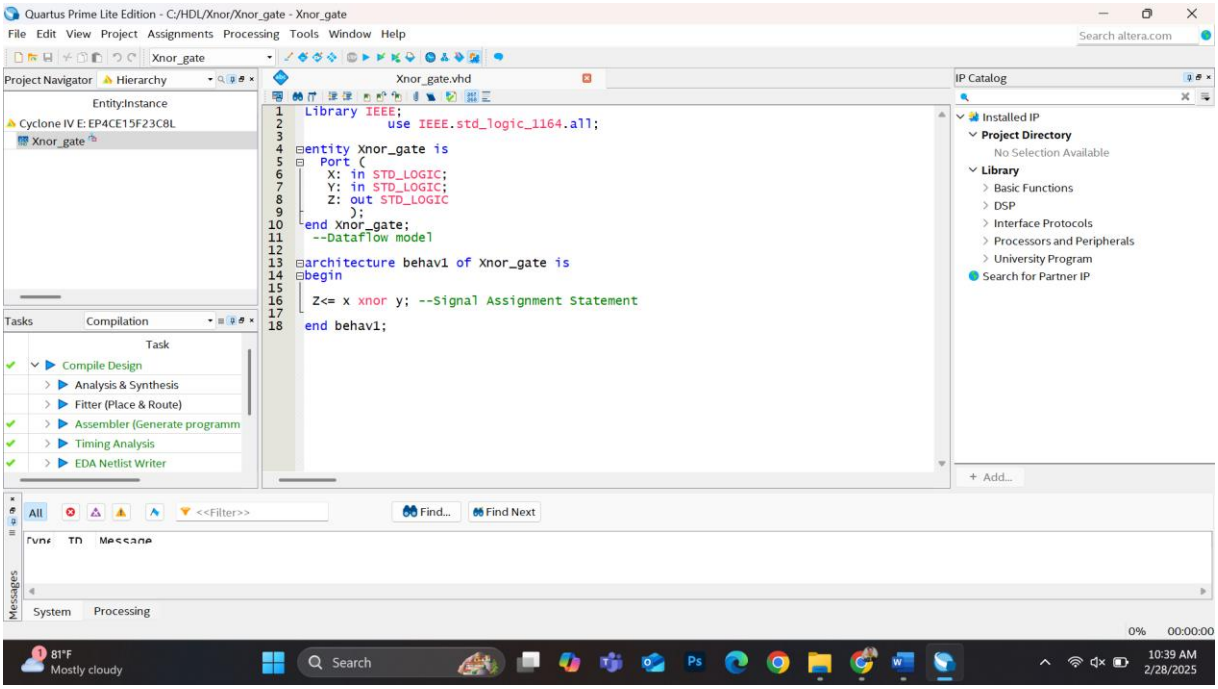
```
-- Behavioral model

        architecture behav2 of xnor2 is
        begin

          process (x, y)
           begin

            If (x=y) then      -- Compare with truth table
               Z <= '1';
             else
               Z<= '0';
            end if;

          end process;

        end behav2;
```

OUTPUT WAVEFORM:

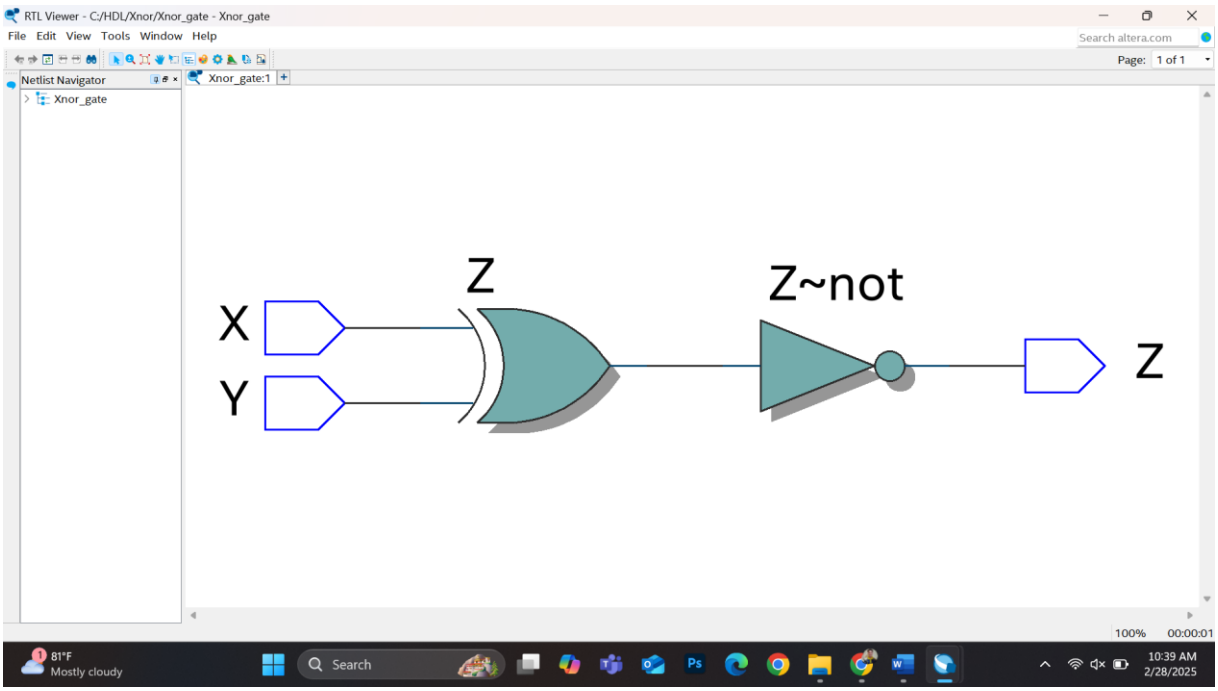


Experiment results:

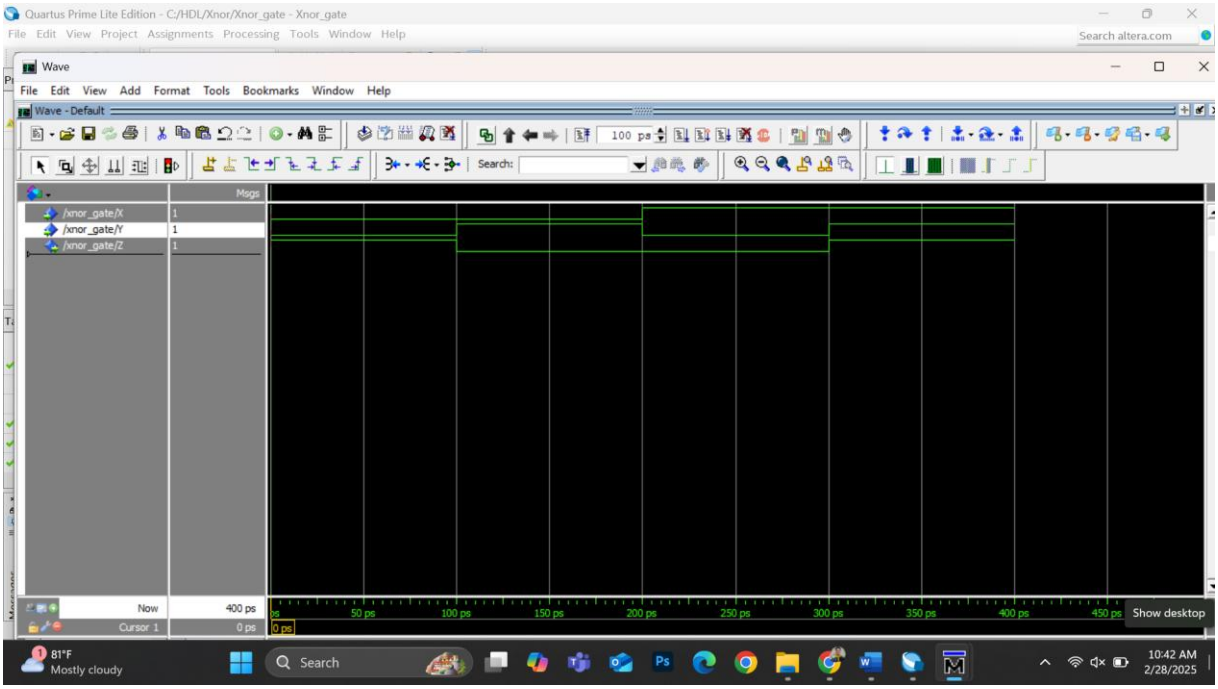
CODE



LOGIC GATE



WAVE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