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C.Y.S.: BSCpE-3A

#6-TITLE: EX-OR gate

LOGIC GATE SYMBOL:



7486

TRUTH TABLE:

| x | y | z |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity xor2 is
  Port (
    X: in STD_LOGIC;
    Y: in STD_LOGIC;
    Z: out STD_LOGIC
  );
end xor2;

--Dataflow model

architecture behav1 of xor2 is
begin

  Z<= x xor y;  --Signal Assignment Statement

end behav1;
```

-- Behavioral model

```
architecture behav2 of xor2 is  
begin
```

```
    process (x, y)  
    begin
```

```
        If (x/=y) then    -- Compare with truth table  
            Z <= '1';  
        else  
            Z <= '0';  
        end if;
```

```
    end process;
```

```
end behav2;
```

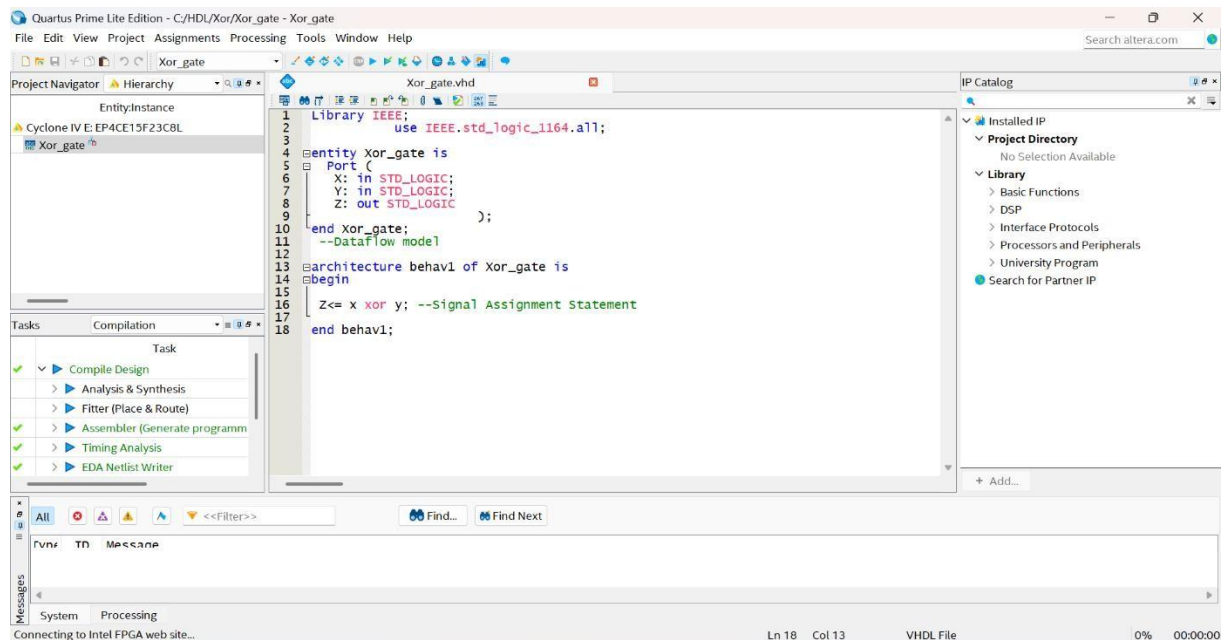
OUTPUT WAVEFORM:



Experiment results:

DATA FLOW MODEL EXPERIMENTS:

CODE:

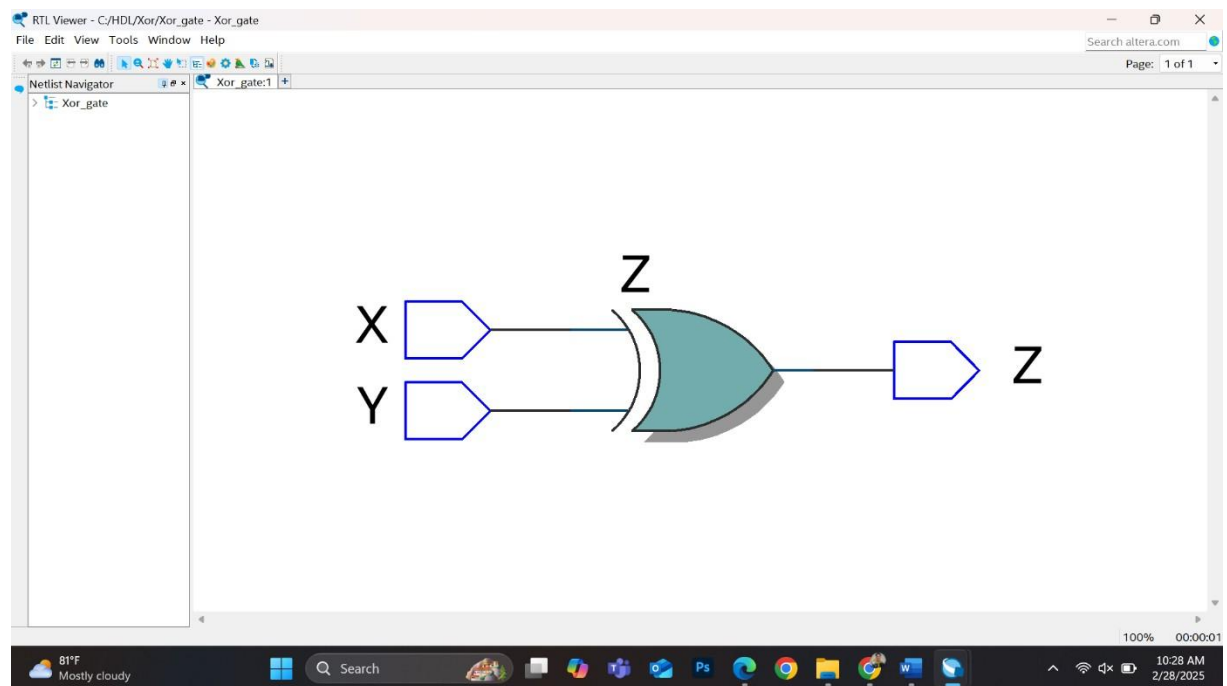


The screenshot shows the Quartus Prime Lite Edition interface. The main window displays the VHDL code for an XOR gate named 'Xor_gate'. The code is as follows:

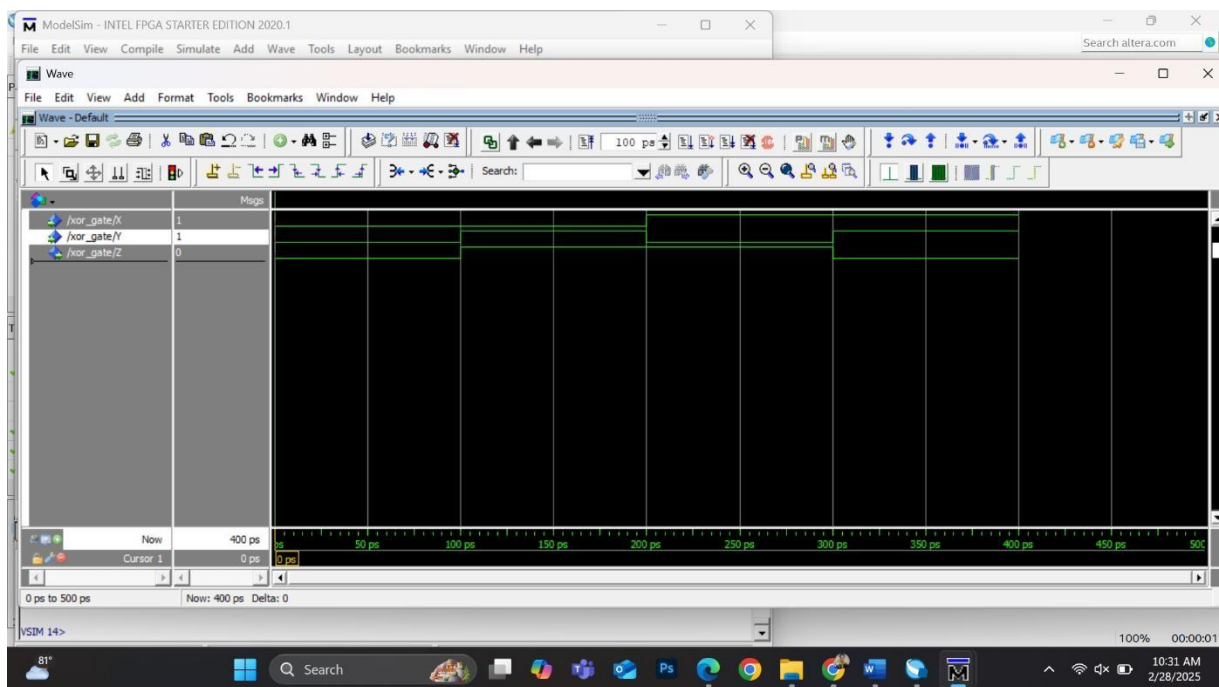
```
1  Library IEEE;  
2  use IEEE.std_logic_1164.all;  
3  
4  entity Xor_gate is  
5  Port (  
6    X: in STD_LOGIC;  
7    Y: in STD_LOGIC;  
8    Z: out STD_LOGIC  
9  );  
10 end Xor_gate;  
11 --Dataflow model  
12  
13 architecture behav1 of Xor_gate is  
14 begin  
15     Z <= x xor y; --Signal Assignment Statement  
16  
17 end behav1;  
18
```

The left pane shows the Project Navigator with the 'Xor_gate' entity selected. The right pane shows the IP Catalog. The bottom status bar indicates the file is 'Xor_gate.vhd' and the current position is 'Ln 18 Col 13'.

LOGIC GATE:



WAVE FORM:



BEHAVIORAL MODEL EXPERIMENTS:

CODE:

```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity Xor_gate is
5  port (
6    X: in std_logic;
7    Y: in std_logic;
8    Z: out std_logic
9  );
10 end Xor_gate;
11
12 architecture behav2 of Xor_gate is
13 begin
14   process (X, Y)
15   begin
16     if (X=Y) then -- Compare with truth table
17       Z <= '1';
18     else
19       Z <= '0';
20     end if;
21   end process;
22 end behav2;
```

The screenshot also shows the Project Navigator, Tasks window, and Messages window. The Messages window displays the following output:

```
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
```

RTL Viewer - C:/HDL/Xor/Xor_gate - Xor_gate

File Edit View Tools Window Help

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Netlist Navigator

Xor_gate:1

Xor_gate

process_0

X

Y

Z

100% 00:00:01

27°C Mostly cloudy

Search

2:52 PM 2/28/2025