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C.Y.S.: BSCpE-3A

## 1.LOGIC GATES

**AIM:** Write a VHDL code for all the logic gates.

**#1-TITLE:** AND gate

**LOGIC GATE SYMBOL:**



**TRUTH TABLE:**

x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

**VHDL CODE:**

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity AND2 is
    port(
        x : in STD_LOGIC;
        y : in STD_LOGIC;
        z : out STD_LOGIC
    );
end AND2;
```

*--Dataflow model*

```
architecture behav1 of AND2 is  
begin
```

```
    Z <= x and y;    --Signal Assignment Statement
```

```
end behav1;
```

*-- Behavioral model*

```
architecture behav2 of AND2 is  
begin
```

```
    process (x, y)  
    begin
```

```
        if (x='1' and y='1') then -- Compare with truth table
```

```
            Z <= '1';
```

```
        else
```

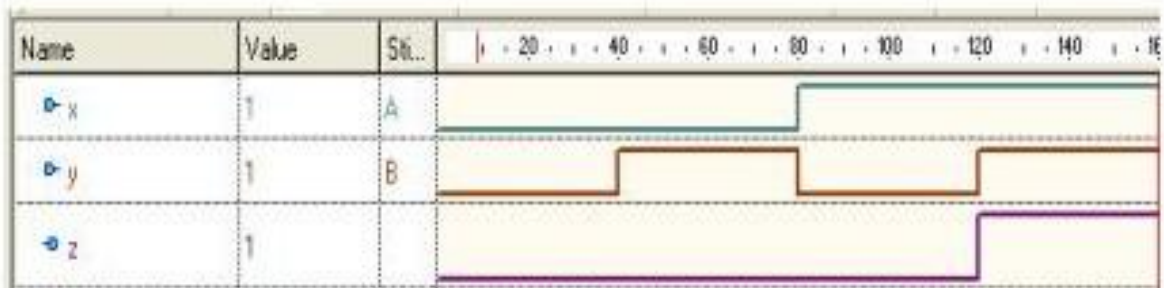
```
            Z <= '0';
```

```
        end if;
```

```
    end process;
```

```
end behav2;
```

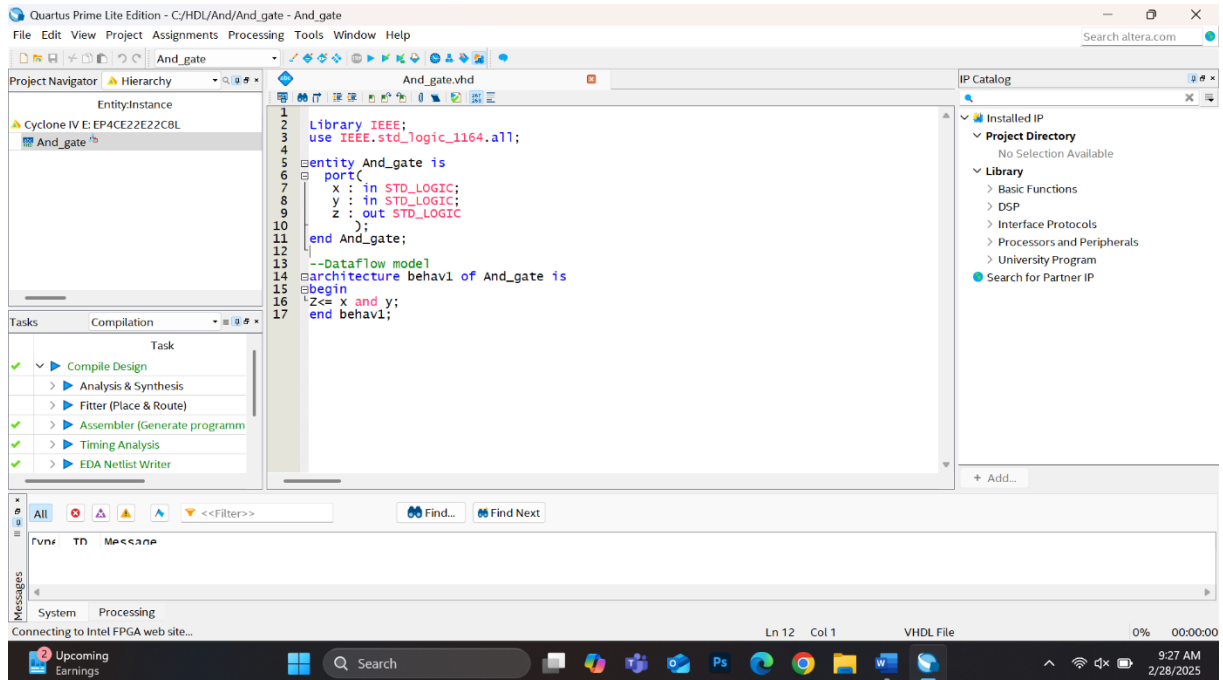
**OUT PUT WAVE FORM:**



## Experiment results:

## DATA FLOW MODEL EXPERIMENTS:

## CODE:

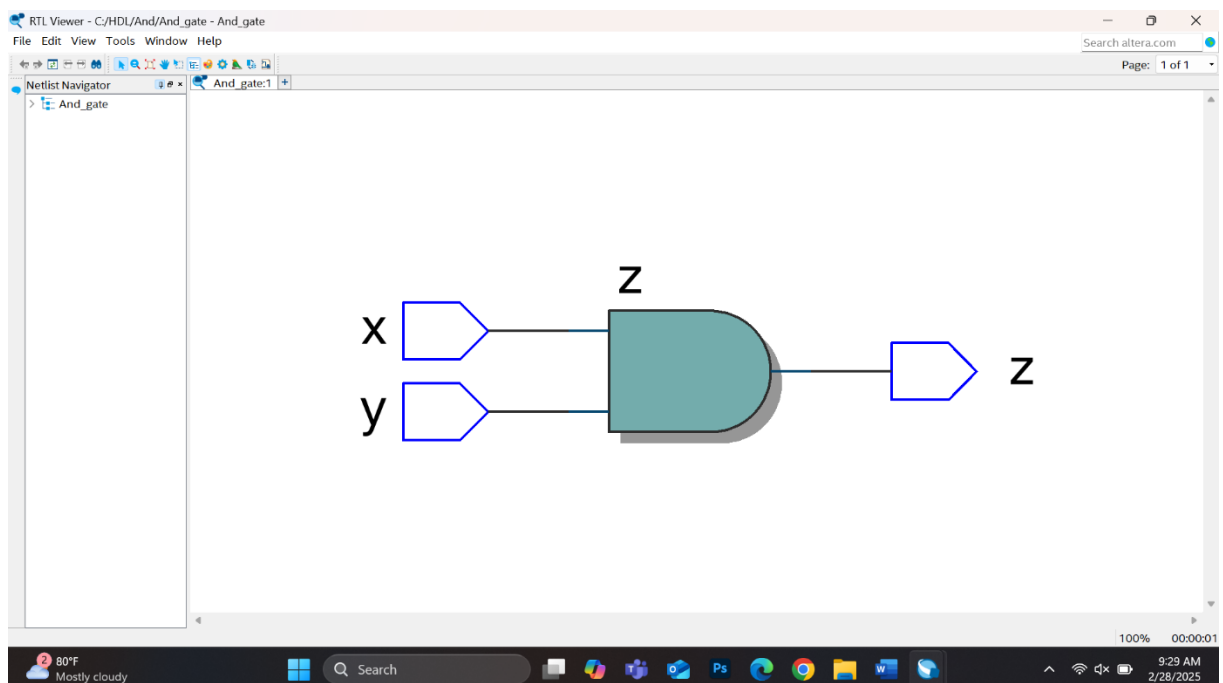


The screenshot shows the Quartus Prime Lite Edition interface. The main window displays the VHDL code for an AND gate. The code is as follows:

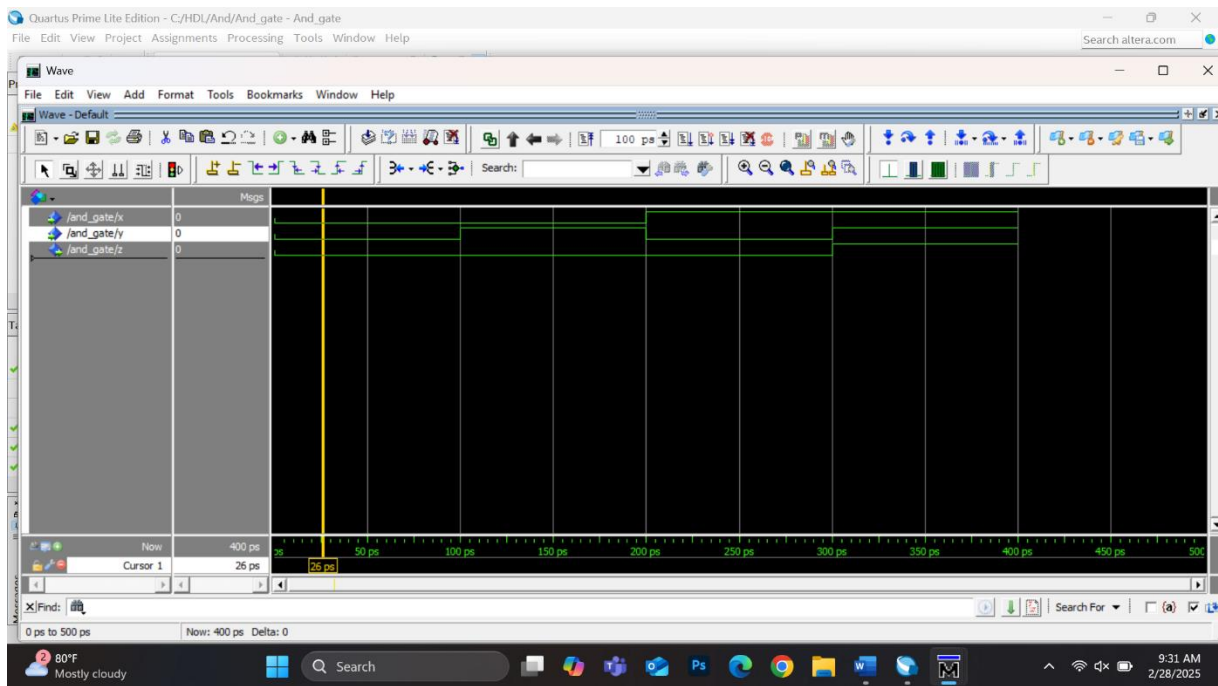
```
1  Library IEEE;  
2  use IEEE.std_logic_1164.all;  
3  
4  
5  entity And_gate is  
6  port(  
7      x : in STD_LOGIC;  
8      y : in STD_LOGIC;  
9      z : out STD_LOGIC  
10     );  
11 end And_gate;  
12  
13 --Dataflow model  
14 architecture behavi of And_gate is  
15 begin  
16     z<= x and y;  
17 end behavi;
```

The left pane shows the Project Navigator with the hierarchy: Cyclone IV E: EP4CE22E22CBL > And\_gate. The bottom pane shows the Tasks window with a list of tasks: Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate program), Timing Analysis, and EDA Netlist Writer. The status bar at the bottom indicates the file is And\_gate.vhd, line 12, column 1, and the device is Cyclone IV E: EP4CE22E22CBL.

## LOGIC GATES:



## WAVEFORM:



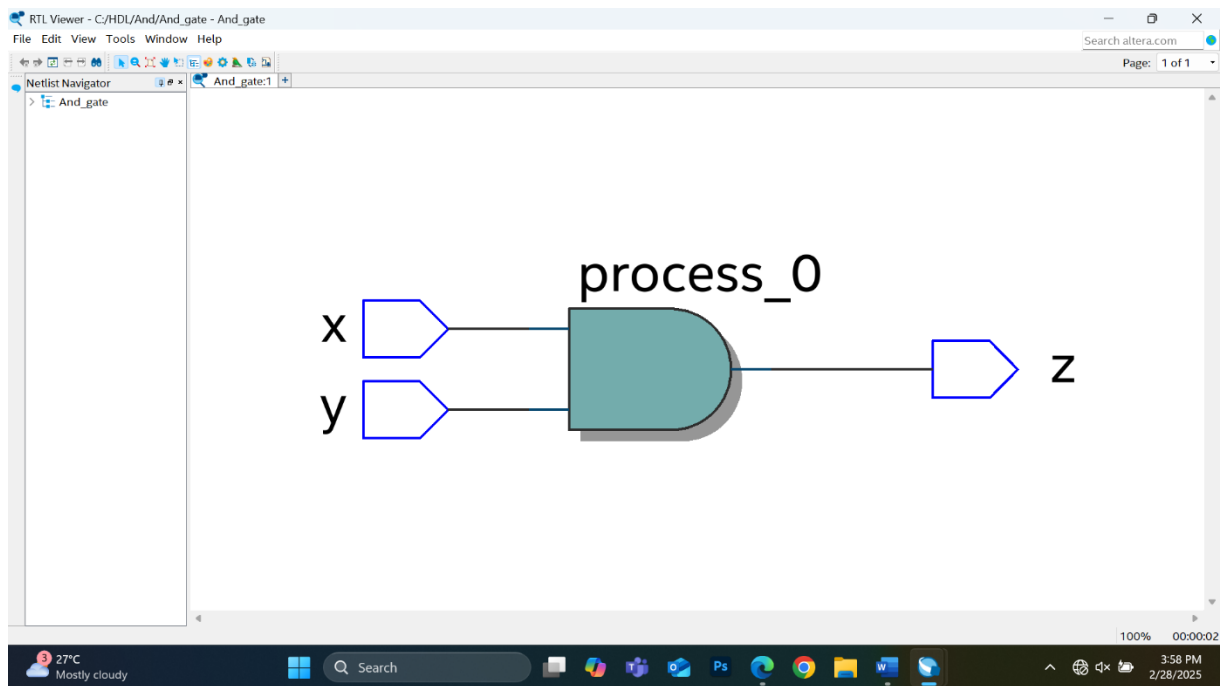
## BEHAVIORAL MODEL EXPERIMENTS:

## CODE:

```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4
5  entity And_gate is
6  port(
7    x : in STD_LOGIC;
8    y : in STD_LOGIC;
9    z : out STD_LOGIC
10 );
11 end And_gate;
12
13 architecture behav2 of And_gate is
14 begin
15   process (x, y)
16   begin
17     if (x='1' and y='1') then -- Compare with truth table
18       z <= '1';
19     else
20       z <= '0';
21     end if;
22   end process;
23 end behav2;
```

The screenshot shows the Quartus Prime Lite Edition interface with the behavioral model code for 'And\_gate.vhd' displayed in the main editor. The code defines an entity 'And\_gate' with three inputs (x, y, z) and one output (z). The architecture 'behav2' implements a logic function where z is 1 if (x=1 and y=1) and 0 otherwise. The code is commented with '-- Compare with truth table'. The left pane shows the Project Navigator with the hierarchy of the project, including the entity 'And\_gate'. The bottom status bar shows the current time as 26 ps and the delta time as 0 ps.

## LOGIC GATE:



## WAVEFORM:

