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C.Y.S.: BSCpE-3A

#6-TITLE: EX-OR gate

LOGIC GATE SYMBOL:

7486

TRUTH TABLE:

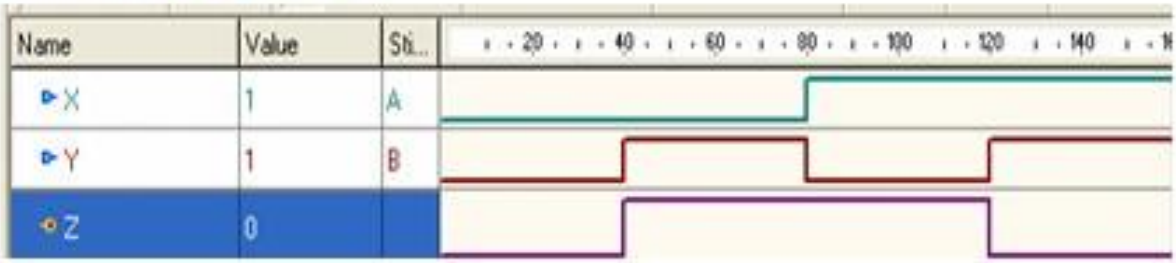
x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity xor2 is
        Port (
                X: in STD_LOGIC;
                Y: in STD_LOGIC;
                Z: out STD_LOGIC
              );
end xor2;

--Dataflow model

architecture behav1 of xor2 is
begin

        Z<= x xor y;    --Signal Assignment Statement

end behav1;
```

```
-- Behavioral model

        architecture behav2 of xor2 is
        begin

          process (x, y)
           begin

             If (x/=y) then      -- Compare with truth table
                Z <= '1';
             else
                Z<= '0';
             end if;

           end process;

        end behav2;
```

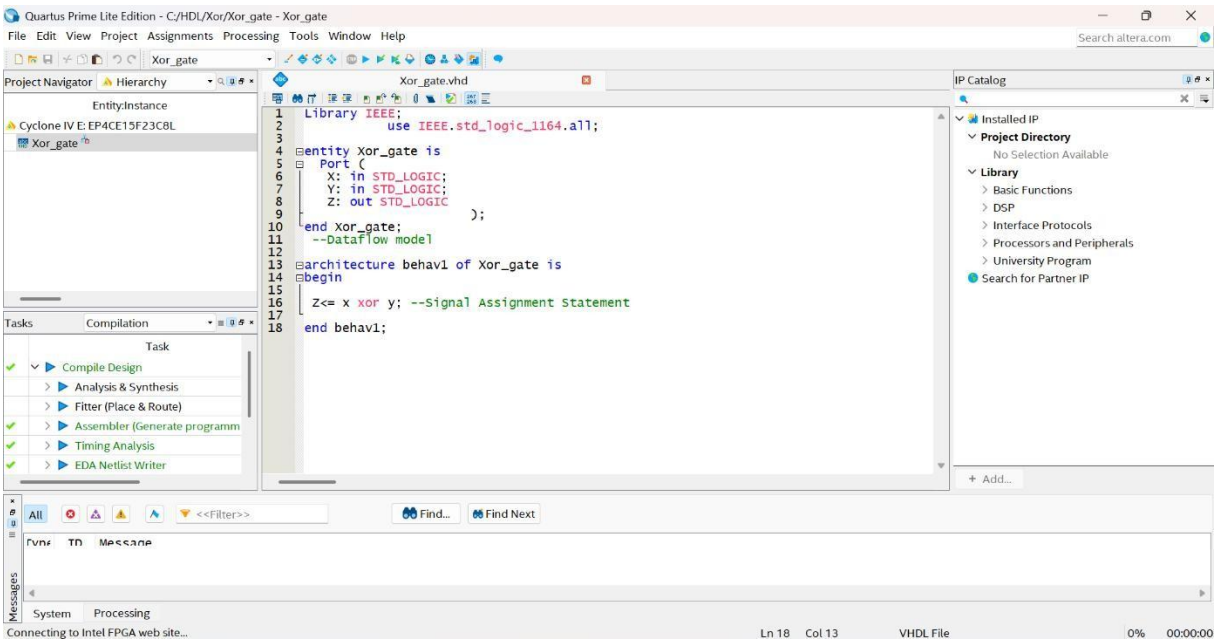
OUTPUT WAVEFORM:



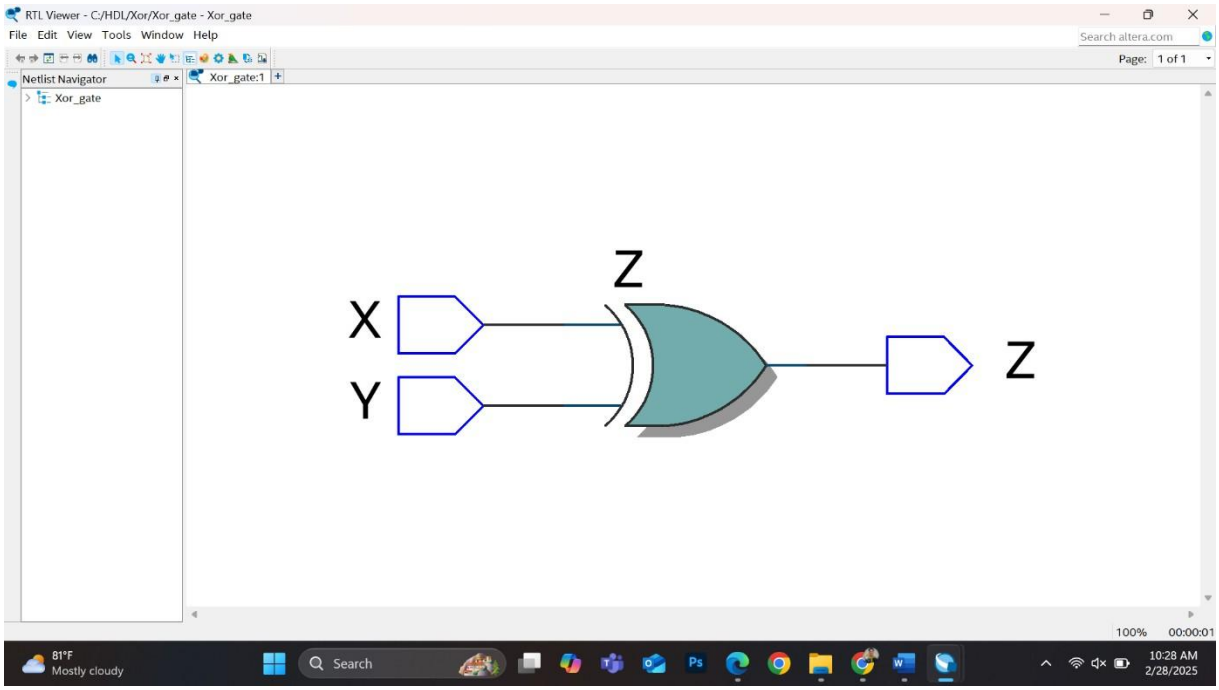
Experiment results:

DATA FLOW EXPERIMENTS:

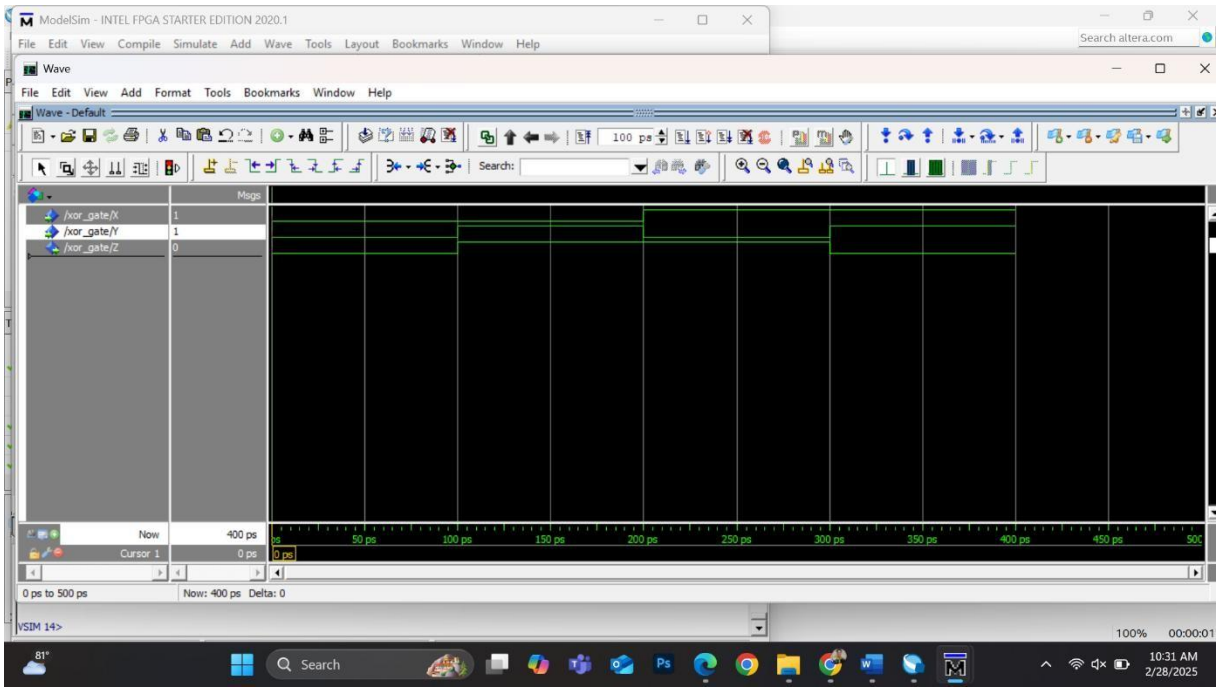
CODE:



LOGIC GATE:

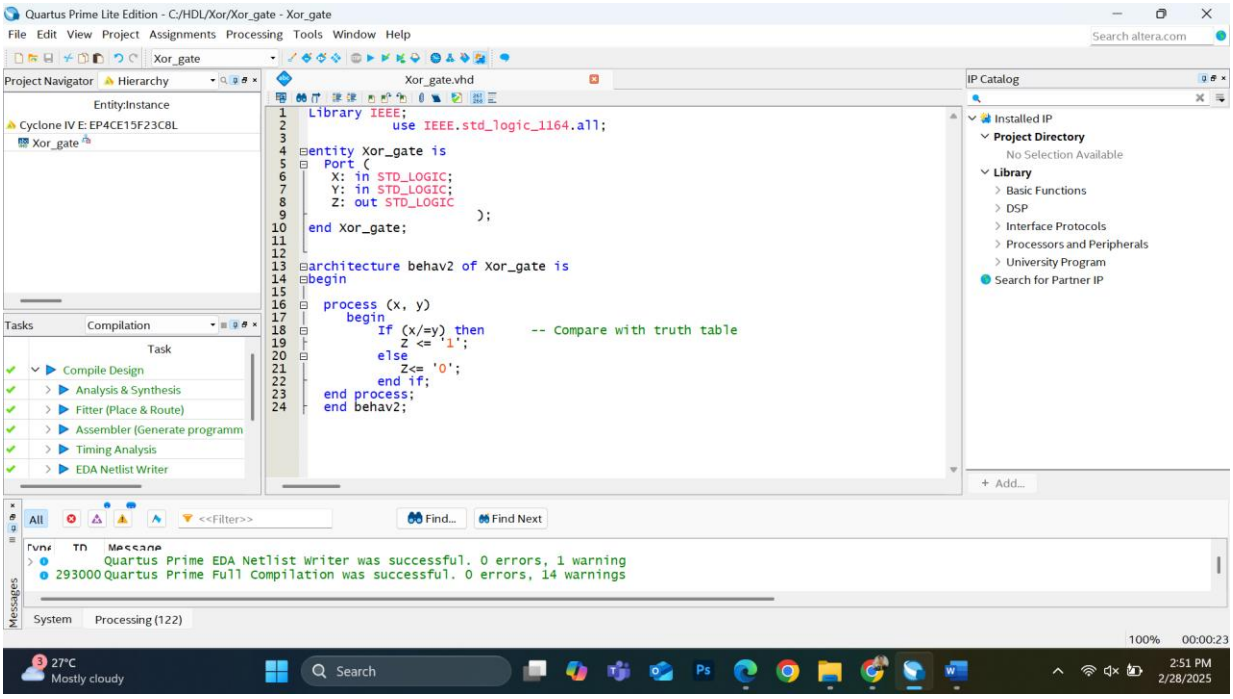


WAVE FORM:

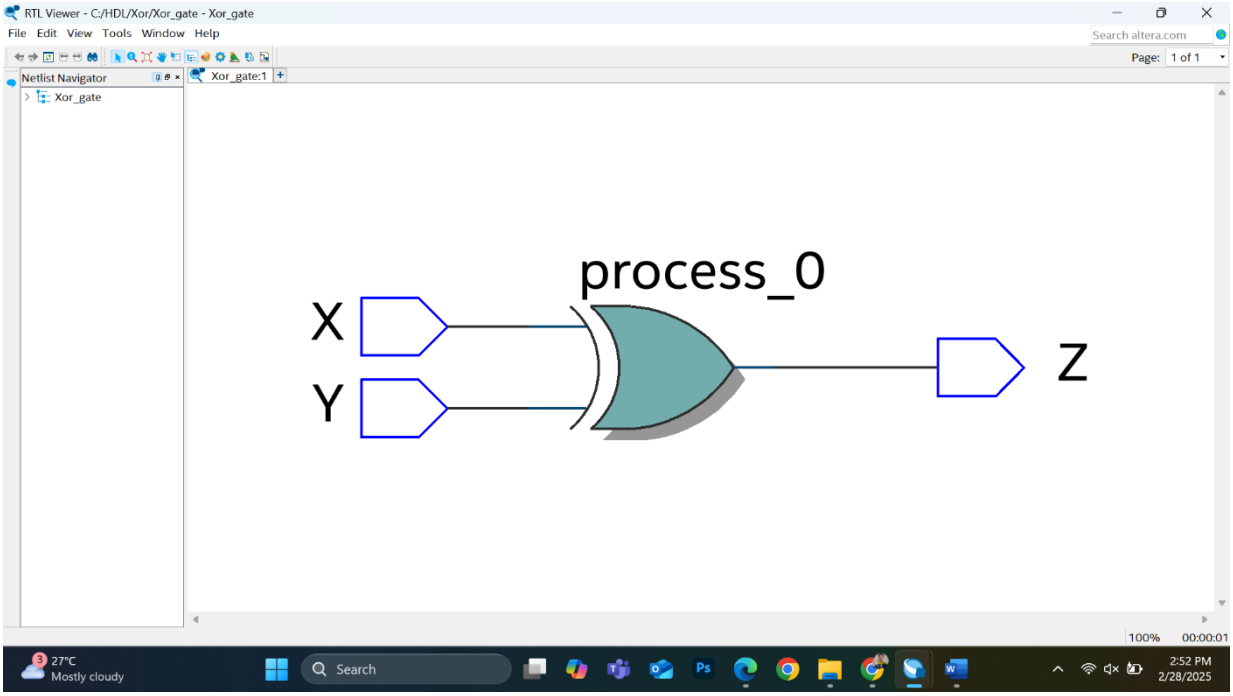


DATA FLOW EXPERIMENTS:

CODE:



LOGIC GATE:



WAVE FORM: