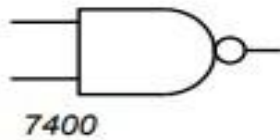


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**#4-TITLE:** NAND gate

**LOGIC GATE SYMBOL:**



**TRUTH TABLE:**

x	y	z
0	0	1
0	1	1
1	0	1
1	1	0

---

**VHDL CODE:**

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity nand2 is
  port(
    x : in STD_LOGIC;
    y : in STD_LOGIC;
    z : out STD_LOGIC
  );
end nand2;
```

–Dataflow model

```
architecture behav1 of nand2 is  
begin
```

```
    z <= x nand y;           –Signal Assignment Statement
```

```
end behav1;
```

– Behavioral model

```
architecture behav2 of nand2 is  
begin
```

```
    Process (x, y)  
    Begin
```

```
        If (x='1' and y='1') then – Compare with truth table
```

```
            Z <= '0';
```

```
        else
```

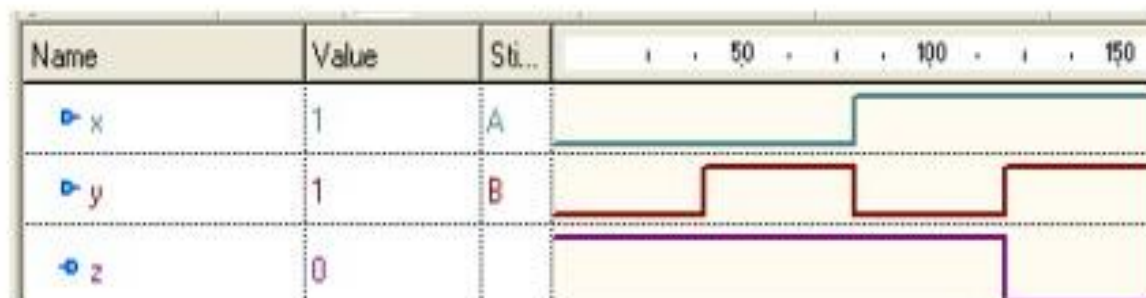
```
            Z <= '1';
```

```
        end if;
```

```
    end process;
```

```
end behav2;
```

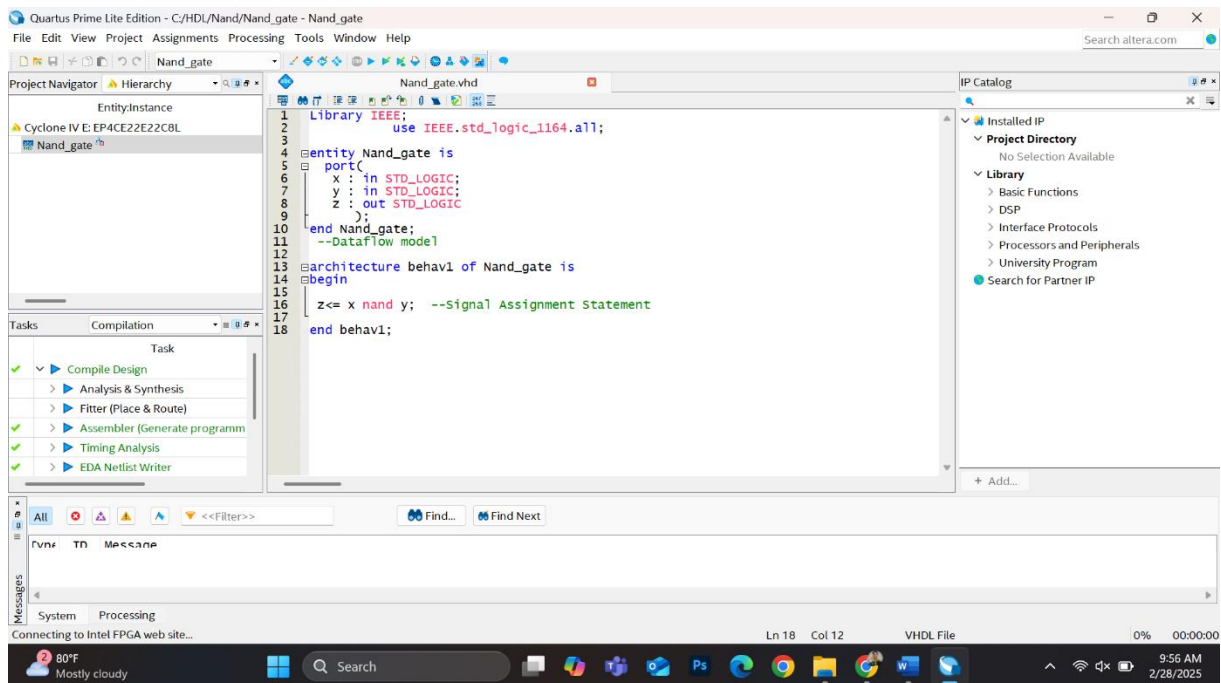
**OUTPUT WAVEFORM:**



## Experiment results:

## DATA FLOW MODEL EXPERIMENT:

### CODE:

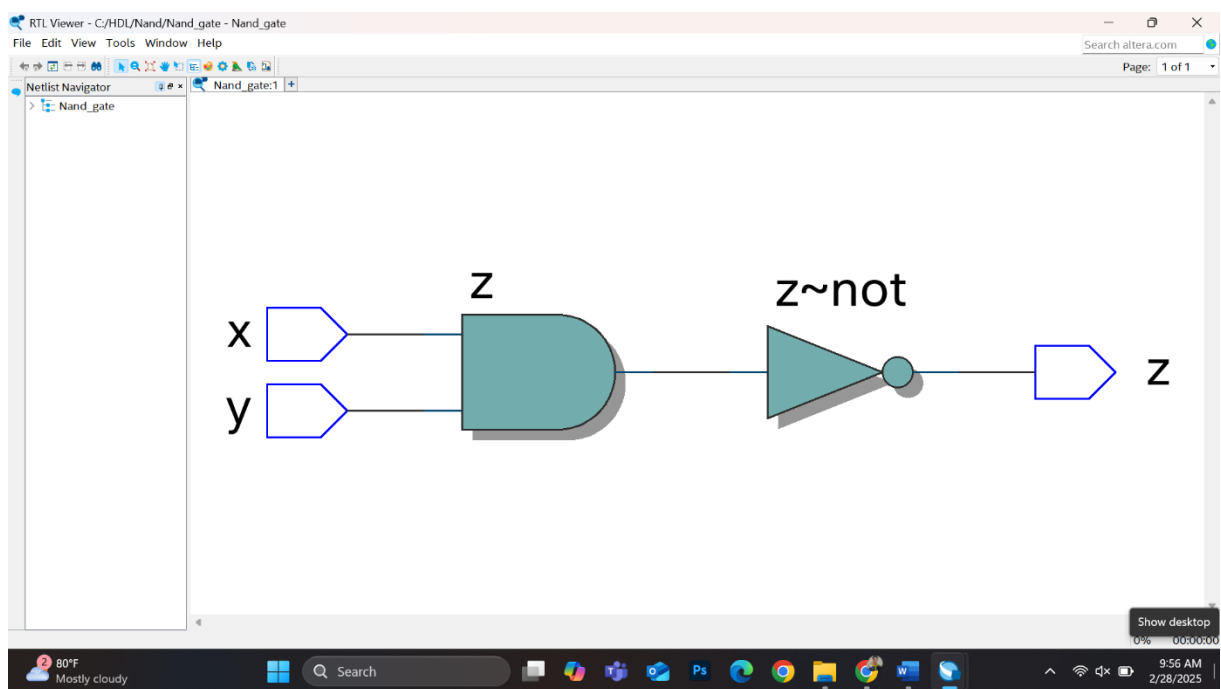


The screenshot shows the Quartus Prime Lite Edition interface. The main window displays the VHDL code for a NAND gate. The code is as follows:

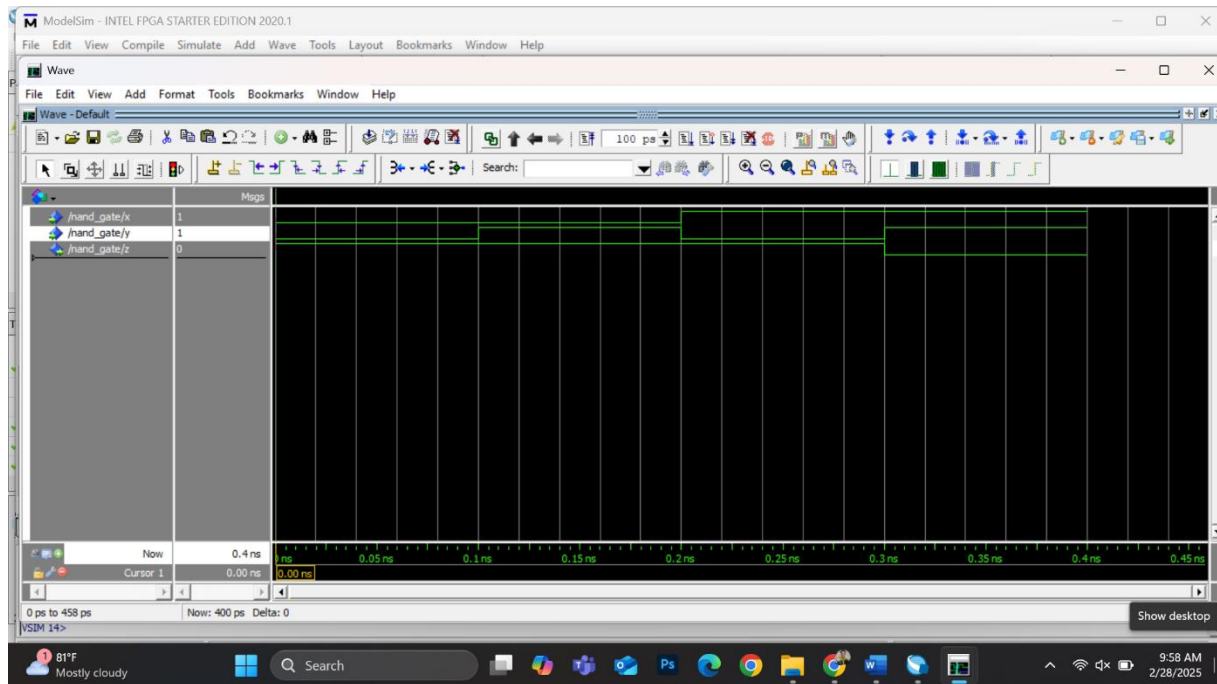
```
1 Library IEEE;
2 use IEEE.std_logic_1164.all;
3
4 entity Nand_gate is
5 port(
6   x : in STD_LOGIC;
7   y : in STD_LOGIC;
8   z : out STD_LOGIC
9 );
10 end Nand_gate;
11 --Dataflow model
12
13 architecture behav1 of Nand_gate is
14 begin
15   z <= x nand y; --Signal Assignment Statement
16 end behav1;
```

The interface also shows the Project Navigator on the left, the IP Catalog on the right, and the Messages window at the bottom. The status bar at the bottom indicates the file is Nand\_gate.vhd, line 18, column 12.

### LOGIC GATE:



## WAVEFORM:



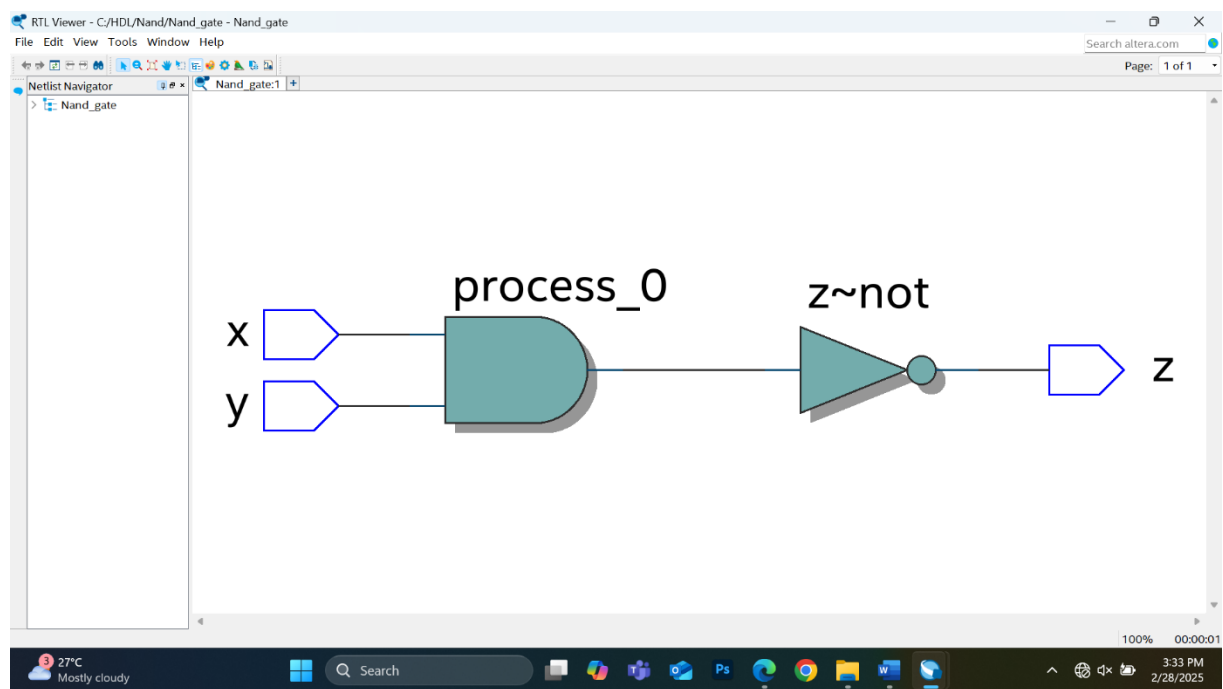
## BEHAVIORAL MODEL EXPERIMENT:

## CODE:

```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity Nand_gate is
5  port(
6    x : in STD_LOGIC;
7    y : in STD_LOGIC;
8    z : out STD_LOGIC
9  );
10 end Nand_gate;
11
12 -- Behavioral model
13
14 architecture behav2 of Nand_gate is
15 begin
16   process (x, y)
17   begin
18     if (x='1' and y='1') then -- Compare with truth table
19       z <= '0';
20     else
21       z <= '1';
22     end if;
23   end process;
24 end behav2;
```

The screenshot shows the Quartus Prime Lite Edition interface. The main window displays the VHDL code for a Nand\_gate. The code is a behavioral model that implements a NAND gate using a process block. The process block takes two inputs, x and y, and produces an output z. The output z is set to '0' if both x and y are '1', and '1' otherwise. The code is saved as `Nand_gate.vhd`. The Project Navigator on the left shows the hierarchy of the project, including the `Nand_gate` entity. The Messages window at the bottom shows the compilation results, indicating that the compilation was successful with 0 errors and 14 warnings.

## LOGIC GATE:



## WAVEFORM:

