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C.Y.S.: BSCpE – 3A

The **CODE:**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity demux is
   Port (
      D : in STD_LOGIC;        -- Data input
      S : in STD_LOGIC_VECTOR(2 downto 0); -- Select input (3 bits for 8 outputs)
      Y : out STD_LOGIC_VECTOR(7 downto 0)  -- 8-bit output
   );
end demux;

architecture Behavioral of demux is
begin
   process(D, S)
   begin
      -- Default all outputs to '0'
      Y <= "00000000";

      -- Based on the select input, assign the data (D) to one of the 8 outputs
      case S is
         when "000" => Y(0) <= D;
         when "001" => Y(1) <= D;
         when "010" => Y(2) <= D;
         when "011" => Y(3) <= D;
         when "100" => Y(4) <= D;
         when "101" => Y(5) <= D;
         when "110" => Y(6) <= D;
```

```
        when "111" => Y(7) <= D;
        when others => Y <= "00000000"; -- If select input is invalid
    end case;
  end process;
end Behavioral;
```

demux.vhd | Compilation Report - demux

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity demux is
5      Port (
6          D : in STD_LOGIC;          -- Data input
7          S : in STD_LOGIC_VECTOR(2 downto 0); -- Select input (3 bits for 8 outputs)
8          Y : out STD_LOGIC_VECTOR(7 downto 0)  -- 8-bit output
9      );
10 end demux;
11
12 architecture Behavioral of demux is
13 begin
14     process(D, S)
15     begin
16         -- Default all outputs to '0'
17         Y <= "00000000";
18
19         -- Based on the select input, assign the data (D) to one of the 8 outputs
20         case S is
21             when "000" => Y(0) <= D;
22             when "001" => Y(1) <= D;
23             when "010" => Y(2) <= D;
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25             when "100" => Y(4) <= D;
26             when "101" => Y(5) <= D;
27             when "110" => Y(6) <= D;
28             when "111" => Y(7) <= D;
29             when others => Y <= "00000000"; -- If select input is invalid
```
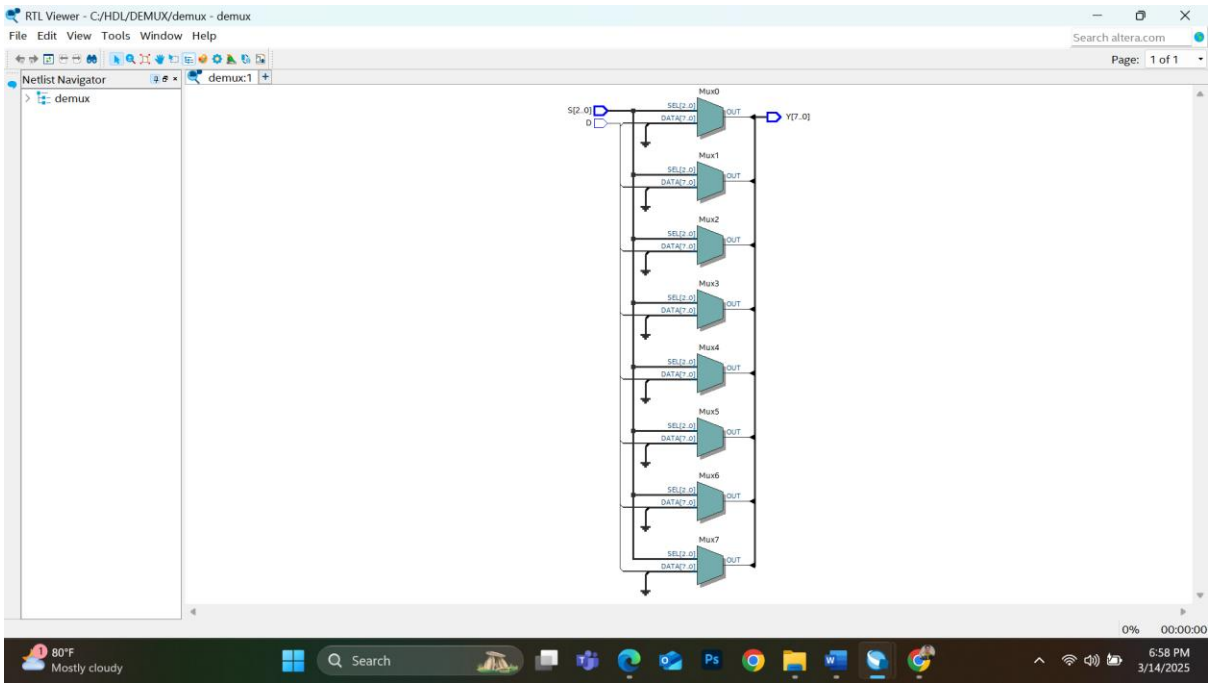

The **LOGIC GATE:**



The **WORKBENCH:**