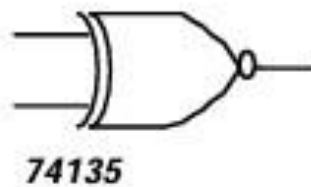


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C.Y.S.: BSCpE-3A

#7-TITLE: EX-NOR gate

LOGIC GATE SYMBOL:



TRUTH TABLE:

x	y	z
0	0	1
0	1	0
1	0	0
1	1	1

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity xnor2 is
  Port (
    X: in STD_LOGIC;
    Y: in STD_LOGIC;
    Z: out STD_LOGIC
  );
end xnor2;
```

--Dataflow model

```
architecture behav1 of xnor2 is  
begin
```

```
    Z<= x xnor y; --Signal Assignment Statement
```

```
end behav1;
```

-- Behavioral model

```
architecture behav2 of xnor2 is  
begin
```

```
    process (x, y)  
    begin
```

```
        If (x=y) then      -- Compare with truth table
```

```
            Z <= '1';
```

```
        else
```

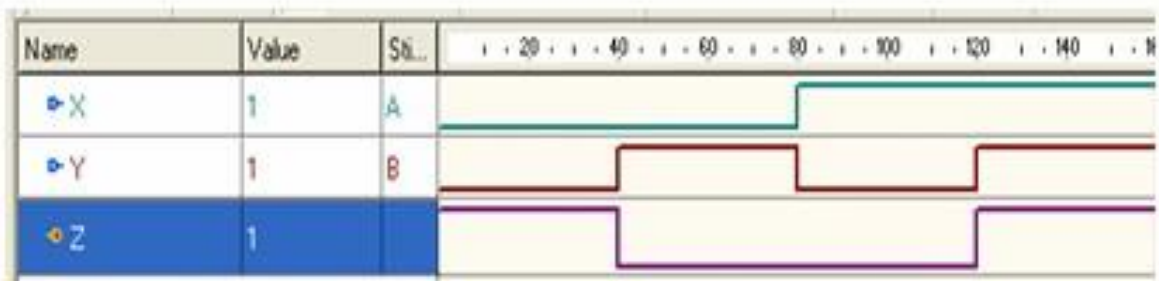
```
            Z<= '0';
```

```
        end if;
```

```
    end process;
```

```
end behav2;
```

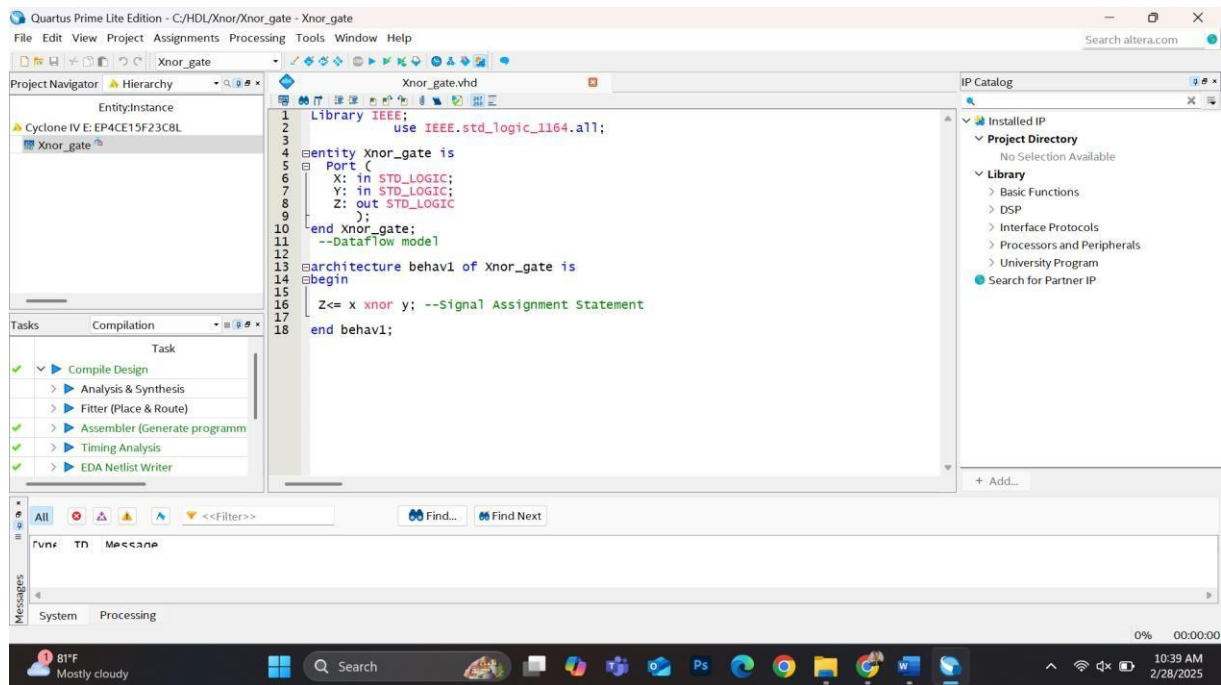
OUTPUT WAVEFORM:



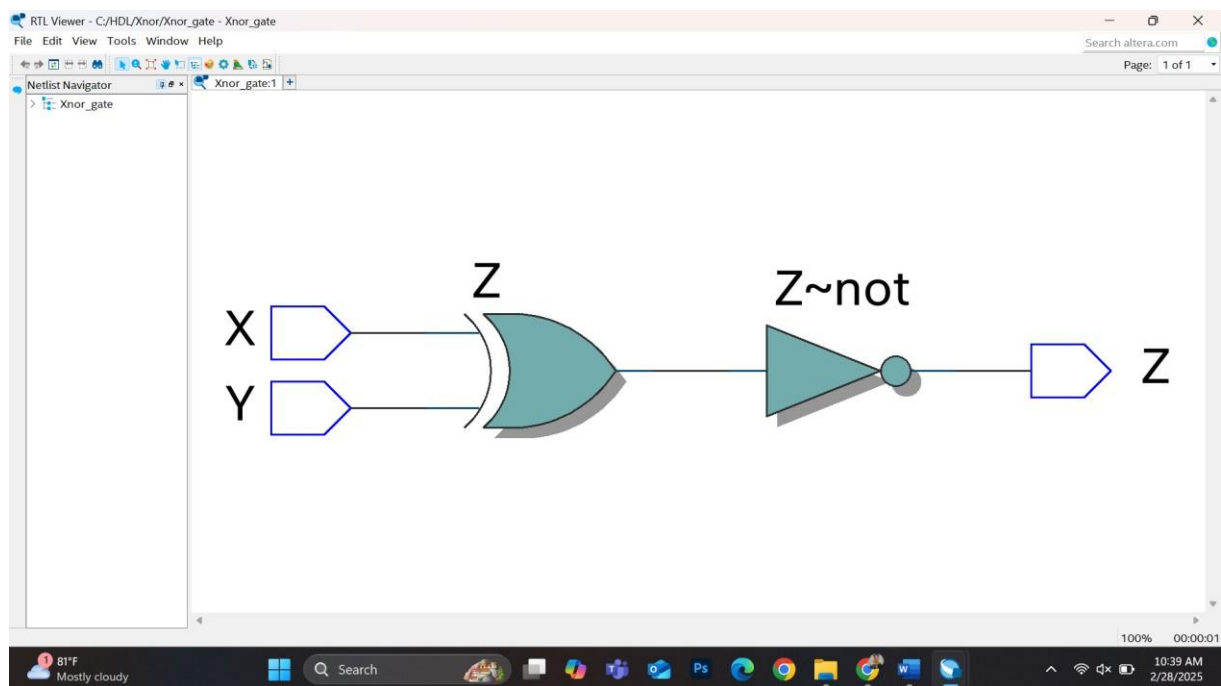
Experiment results:

DATA FLOW MODEL EXPERIMENTS:

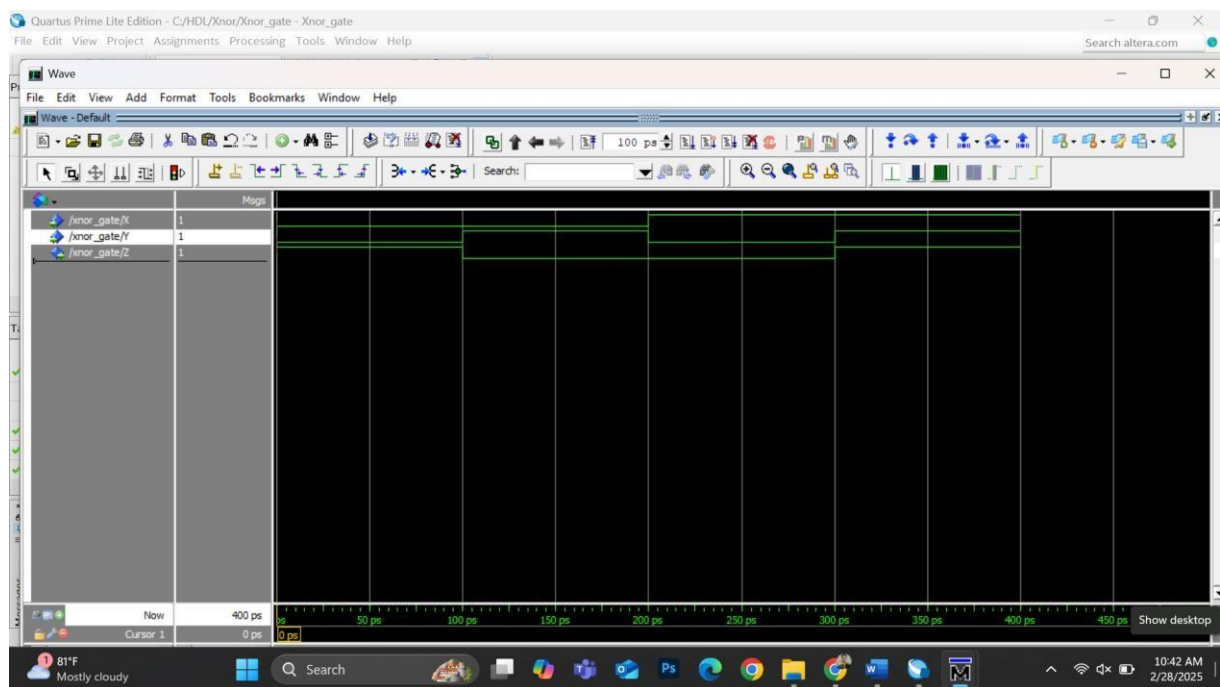
CODE



LOGIC GATE:



WAVE FORM:



BEHAVIORAL MODEL EXPERIMENTS:

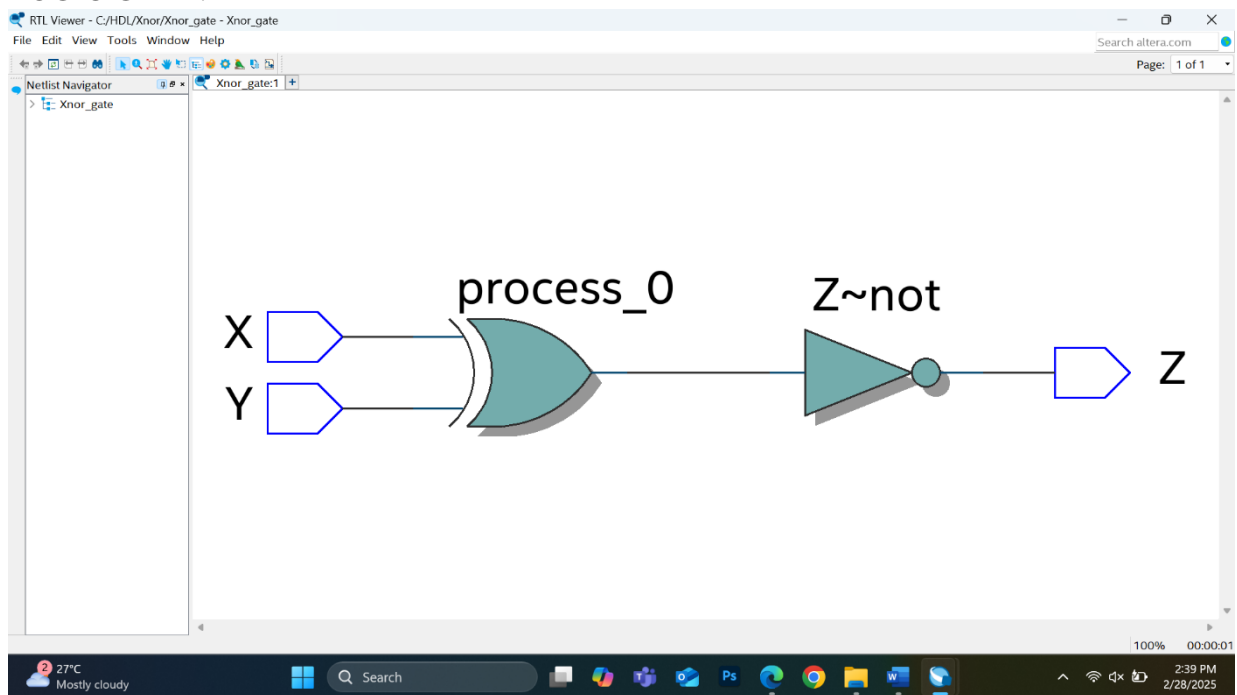
CODE:

```
Quartus Prime Lite Edition - C:/HDL/Xnor/Xnor_gate - Xnor_gate
File Edit View Project Assignments Processing Tools Window Help
Search altera.com

Xnor_gate.vhd
1  Library IEEE;
2      use IEEE.std_logic_1164.all;
3
4  entity Xnor_gate is
5      Port (
6          X: in STD_LOGIC;
7          Y: in STD_LOGIC;
8          Z: out STD_LOGIC
9      );
10 end Xnor_gate;
11
12 architecture behav2 of Xnor_gate is
13 begin
14     process (X, Y)
15     begin
16         if (X=Y) then
17             Z <= '1';
18         else
19             Z <= '0';
20         end if;
21     end process;
22 end behav2;
```

The screenshot shows the Quartus Prime Lite Edition interface with the Xnor_gate.vhd file open. The code is displayed in the main editor window. The code defines an entity Xnor_gate with three ports: X (input), Y (input), and Z (output). The architecture behav2 implements the Xnor logic using a process block. The process block has two inputs, X and Y, and one output, Z. The process block contains an if statement that checks if X is equal to Y. If X is equal to Y, Z is set to '1'. Otherwise, Z is set to '0'. The process block is named behav2. The bottom status bar shows the current line as Ln 15, Col 7, and the file type as VHDL File. The bottom status bar also shows the current time as 2:36 PM on 2/28/2025.

LOGIC GATE:



WAVE FORM:

