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1.LOGIC GATES

AIM: Write a VHDL code for all the logic gates.

#1-TITLE: AND gate

LOGIC GATE SYMBOL:



TRUTH TABLE:

x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity AND2 is
    port(
        x : in STD_LOGIC;
        y : in STD_LOGIC;
        z : out STD_LOGIC
    );
end AND2;
```

--Dataflow model

```
architecture behav1 of AND2 is  
begin
```

```
    Z<= x and y;    --Signal Assignment Statement
```

```
end behav1;
```

-- Behavioral model

```
architecture behav2 of AND2 is  
begin
```

```
    process (x, y)  
    begin
```

```
        if (x='1' and y='1') then -- Compare with truth table
```

```
            Z <= '1';
```

```
        else
```

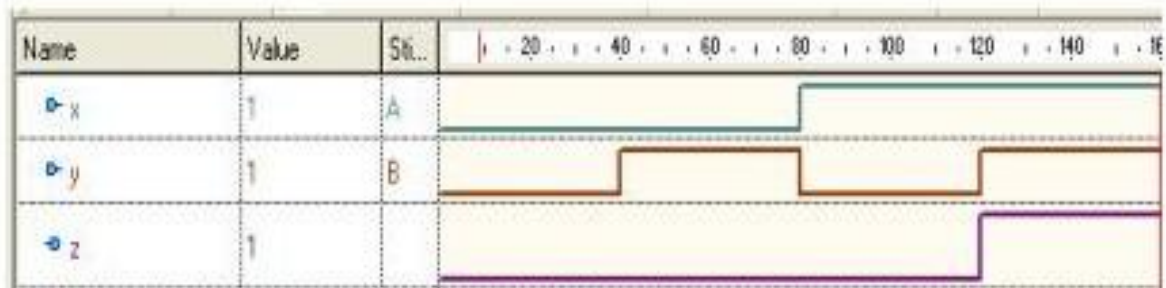
```
            Z <= '0';
```

```
        end if;
```

```
    end process;
```

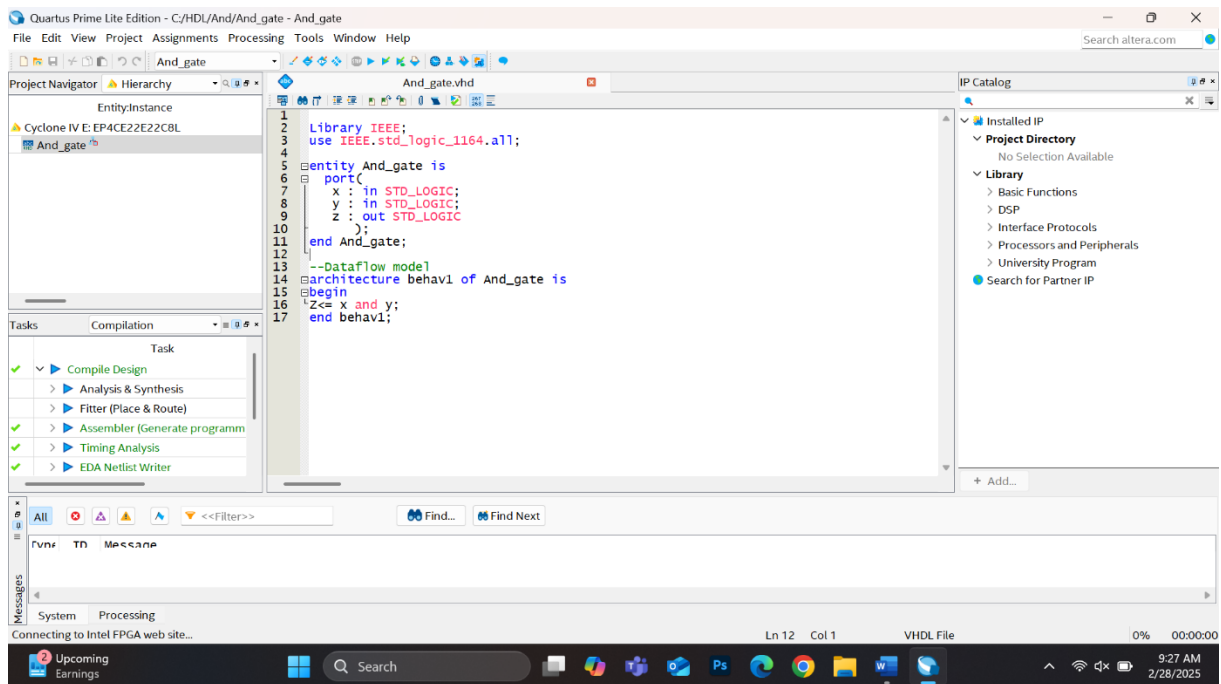
```
end behav2;
```

OUT PUT WAVE FORM:

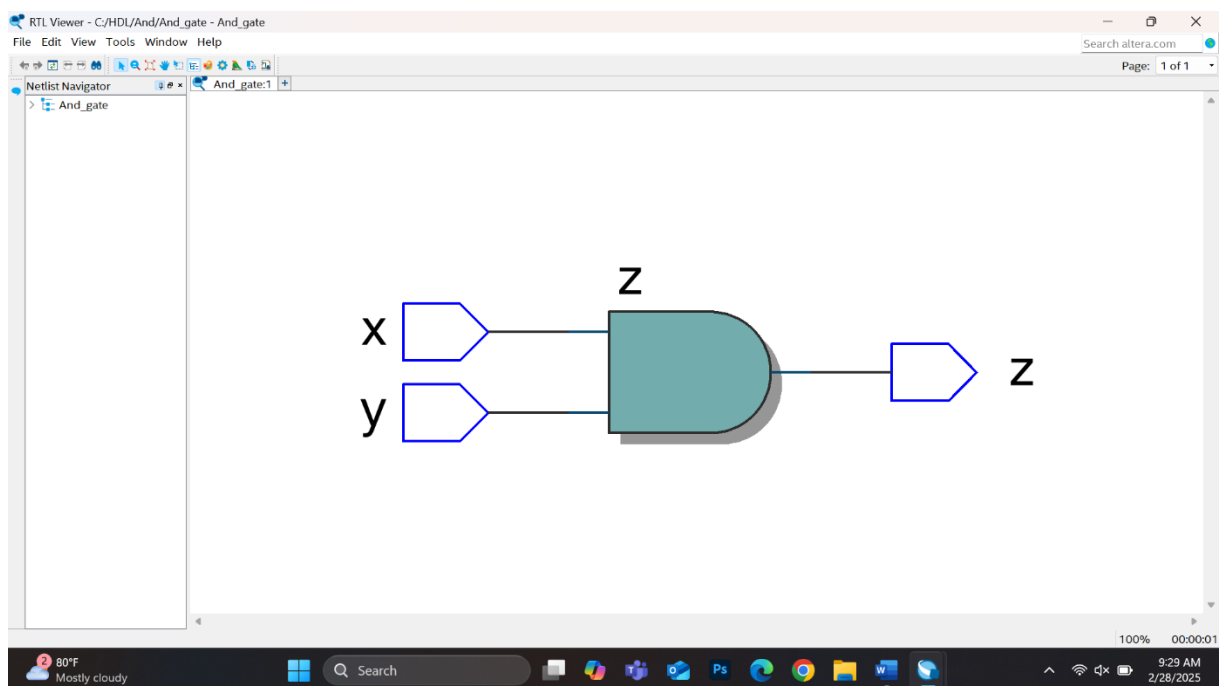


Experiment results:

CODE



LOGIC GATES



The screenshot shows the Quartus Prime Lite Edition software interface. The main window displays a timing diagram for a circuit. The left pane shows a list of signals: `/and_gate/x`, `/and_gate/y`, and `/and_gate/z`. The main area shows a timing diagram with a vertical yellow cursor line at 26 ps. The bottom status bar indicates "Now: 400 ps Delta: 0".