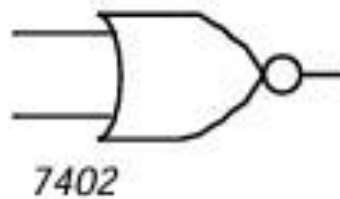


Name: Richard Raymond J. Canda

C.Y.S.: BSCpE-3A

#5- TITLE: NOR gate

LOGIC GATE SYMBOL:



TRUTH TABLE:

x	y	z
0	0	1
0	1	0
1	0	0
1	1	0

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity nor2 is
  Port (
    X: in STD_LOGIC;
    Y: in STD_LOGIC;
    Z: out STD_LOGIC
  );
end nor2;
```

--Dataflow model

```
architecture behav1 of nor2 is  
begin
```

```
    Z<= x nor y; --Signal Assignment Statement
```

```
end behav1;
```

-- Behavioral model

```
architecture behav2 of nor2 is  
begin
```

```
    process (x, y)  
    begin
```

```
        If (x='0' and y='0') then -- Compare with truth table
```

```
            Z <= '1';
```

```
        else
```

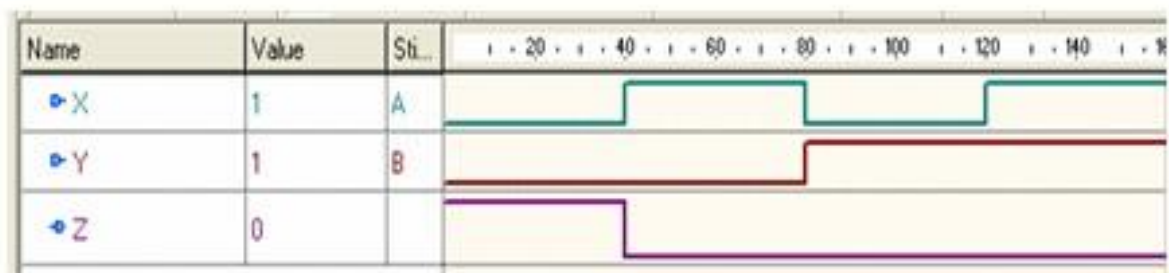
```
            Z <= '0';
```

```
        end if;
```

```
    end process;
```

```
end behav2;
```

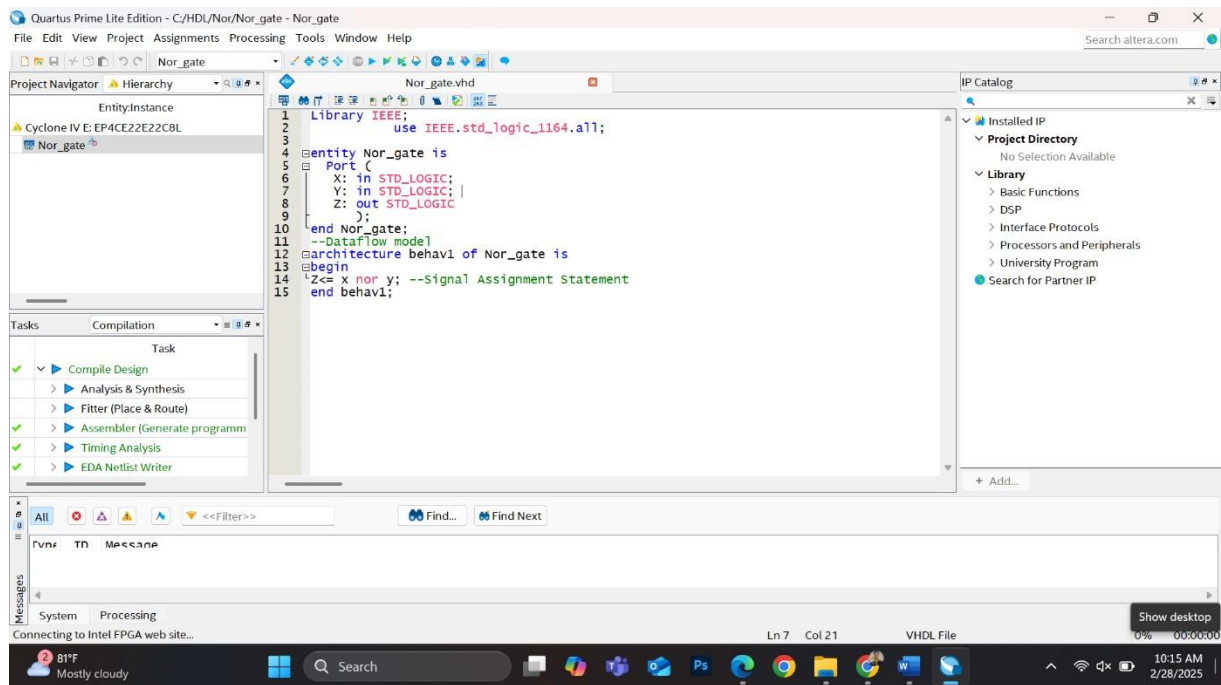
OUTPUT WAVEFORM:



Experiment results:

DATA FLOW MODEL EXPERIMENTS:

CODE:

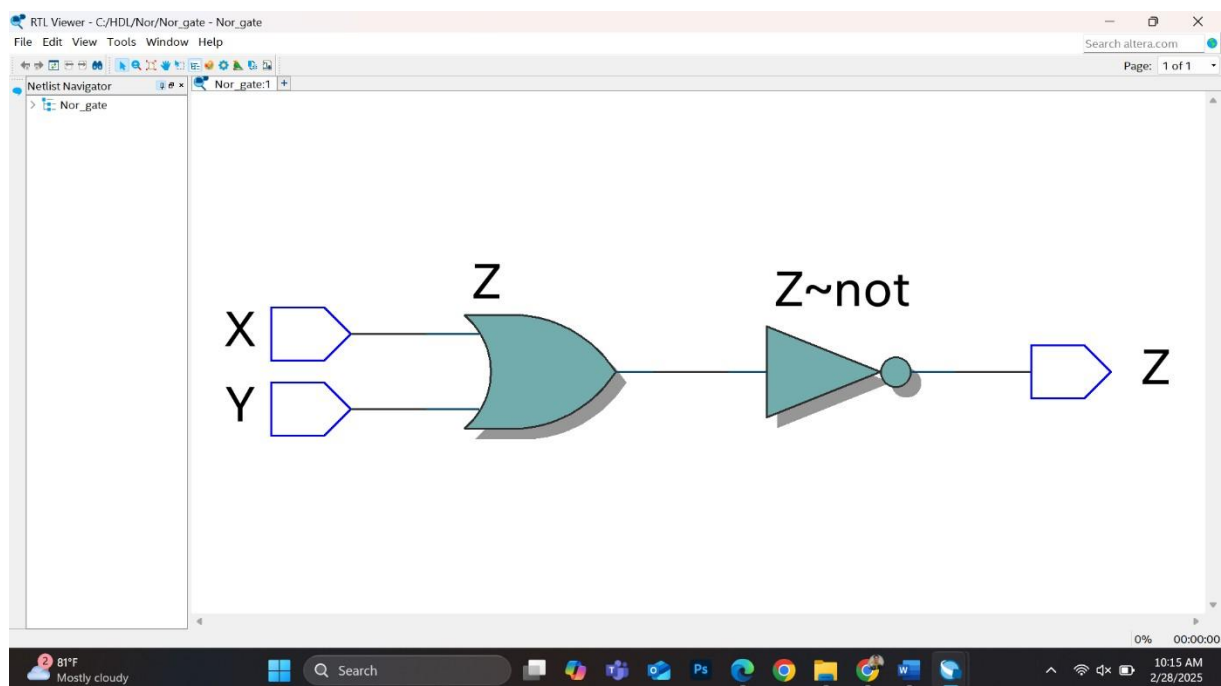


The screenshot shows the Quartus Prime Lite Edition interface. The main window displays the VHDL code for a NOR gate. The code is as follows:

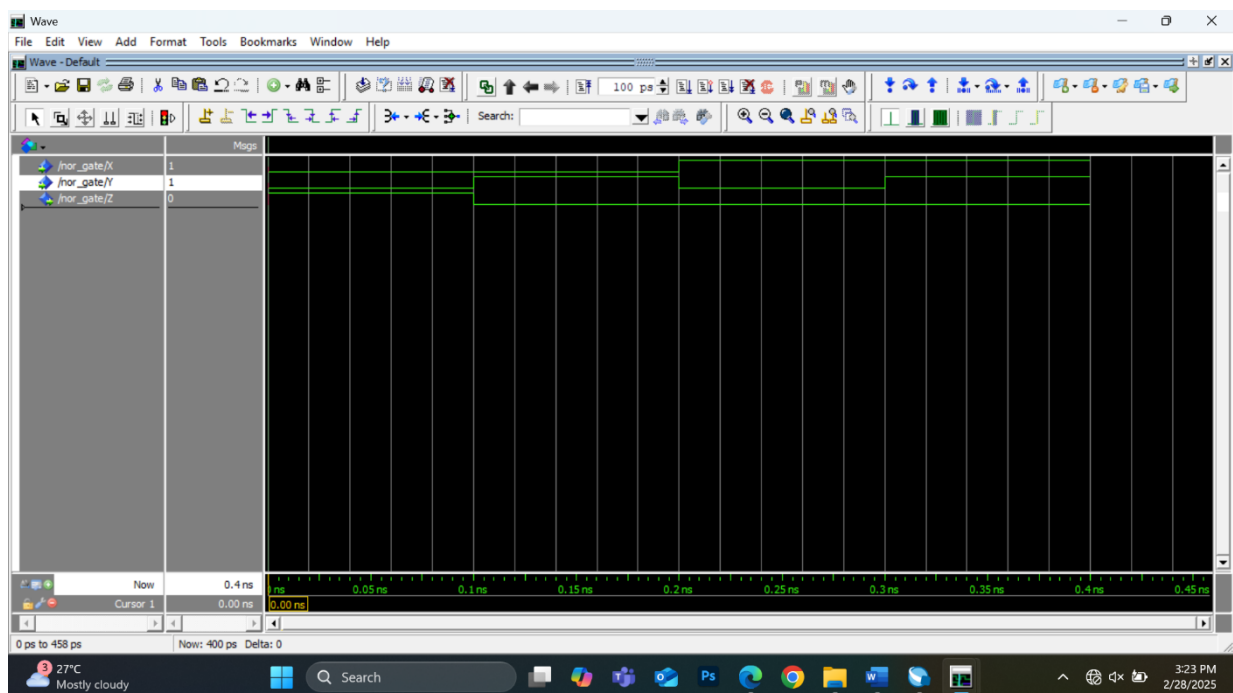
```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  Entity Nor_gate is
5  Port (
6  X: in STD_LOGIC;
7  Y: in STD_LOGIC;
8  Z: out STD_LOGIC
9  );
10 end Nor_gate;
11 --DataFlow model
12 Architecture behavi of Nor_gate is
13 begin
14   Z<= X nor Y; --Signal Assignment Statement
15 end behavi;
```

The interface also shows the Project Navigator on the left, the Tasks window, and the IP Catalog on the right. The status bar at the bottom indicates the file is at Line 7, Column 21.

LOGIC GATE:



WAVEFORM:



BEHAVIORAL MODEL EXPERIMENTS:

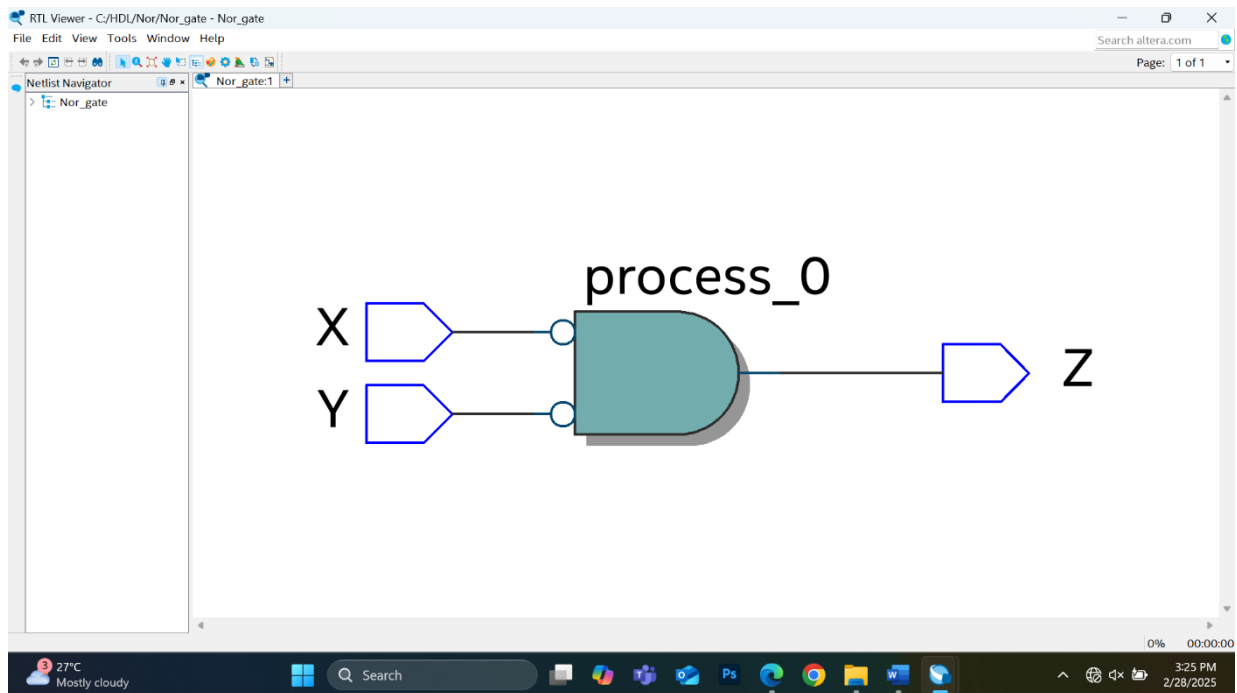
CODE:

```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity Nor_gate is
5  Port (
6    X: in STD_LOGIC;
7    Y: in STD_LOGIC;
8    Z: out STD_LOGIC
9  );
10 end Nor_gate;
11
12 -- Behavioral model
13 architecture behav2 of Nor_gate is
14 begin
15   process (X, Y)
16   begin
17     if (X='0' and Y='0') then -- Compare with truth table
18       Z <= '1';
19     else
20       Z <= '0';
21     end if;
22   end process;
23 end behav2;
```

The messages pane at the bottom shows the following output:

```
Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
293000 Quartus Prime Full Compilation was successful. 0 errors, 14 warnings
```

LOGIC GATE:



WAVEFORM:

