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#6-TITLE: EX-OR gate

LOGIC GATE SYMBOL:



7486

TRUTH TABLE:

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity xor2 is
  Port (
    X: in STD_LOGIC;
    Y: in STD_LOGIC;
    Z: out STD_LOGIC
  );
end xor2;

--Dataflow model

architecture behav1 of xor2 is
begin

  Z<= x xor y;  --Signal Assignment Statement

end behav1;
```

-- Behavioral model

```
architecture behav2 of xor2 is  
begin
```

```
    process (x, y)  
    begin
```

```
        If (x/=y) then    -- Compare with truth table  
            Z <= '1';  
        else  
            Z <= '0';  
        end if;
```

```
    end process;
```

```
end behav2;
```

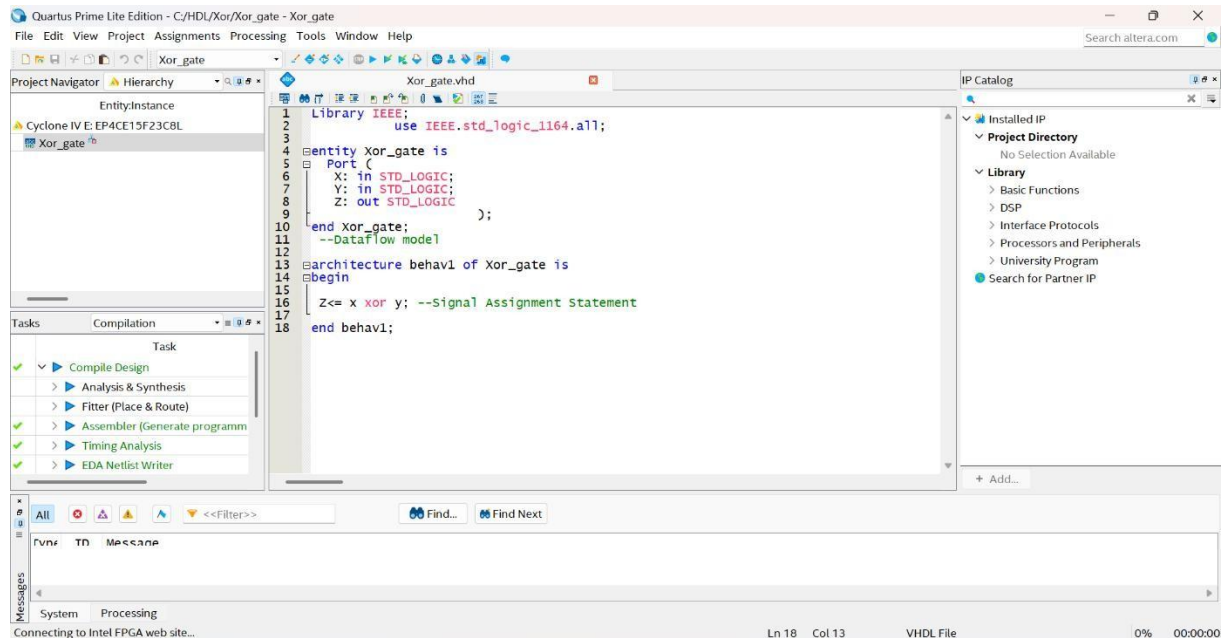
OUTPUT WAVEFORM:



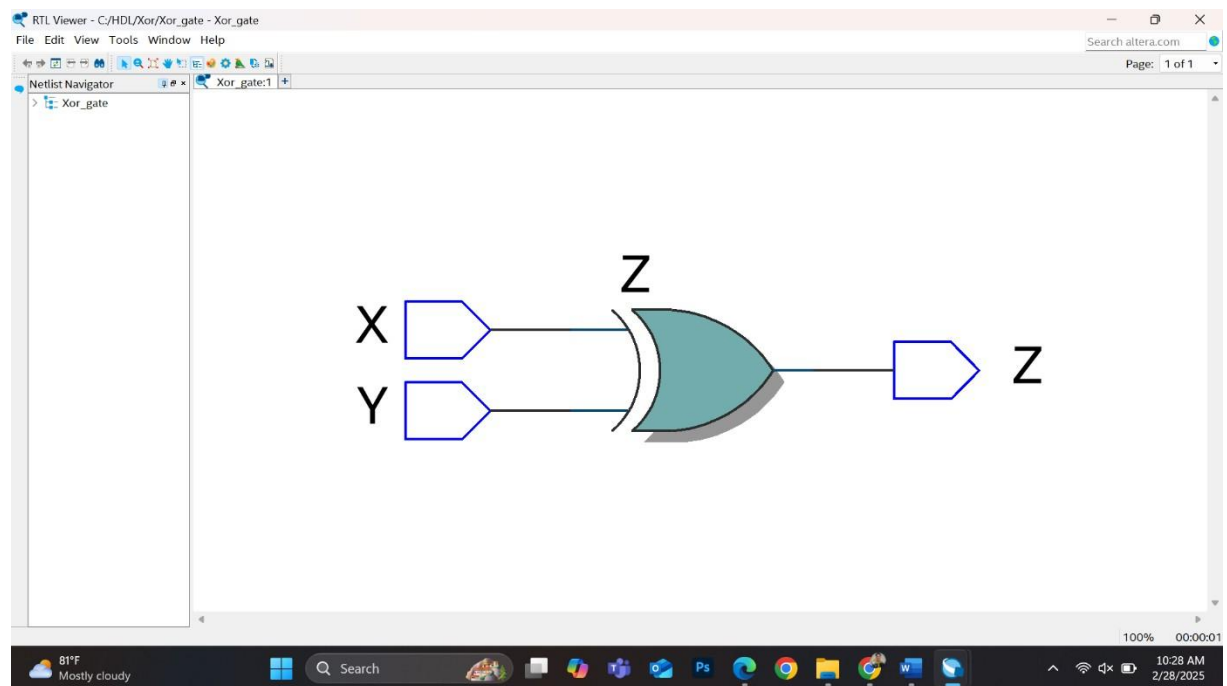
Experiment results:

DATA FLOW EXPERIMENTS:

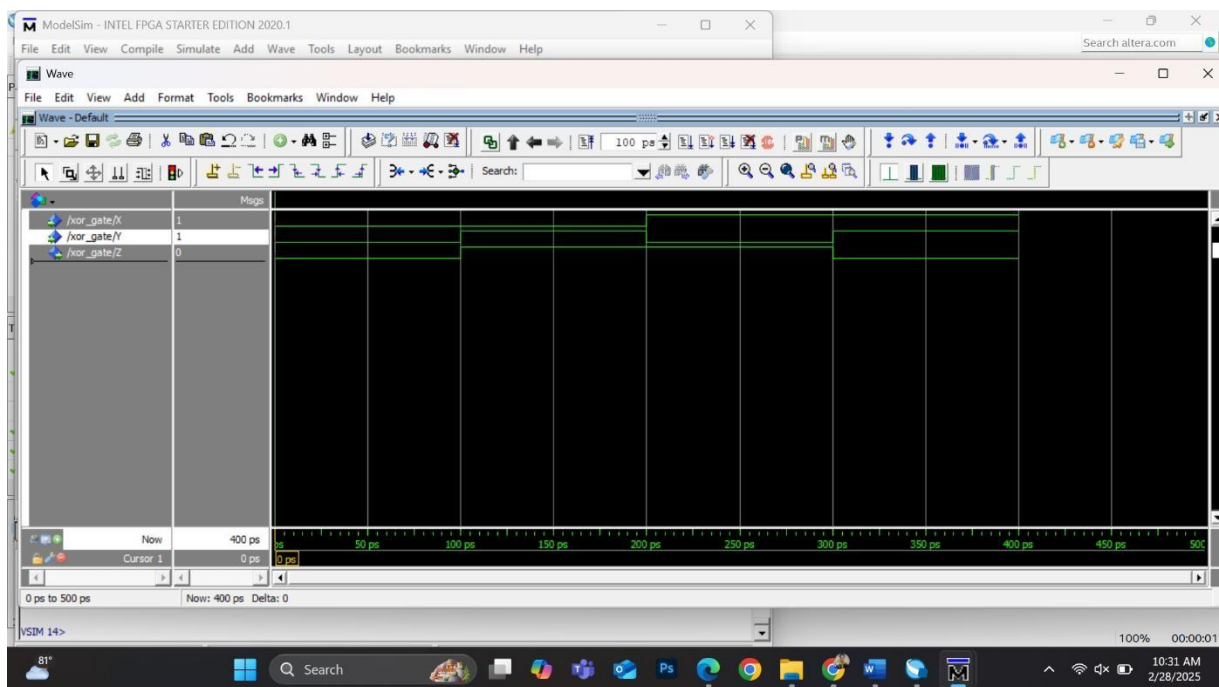
CODE:



LOGIC GATE:



WAVE FORM:



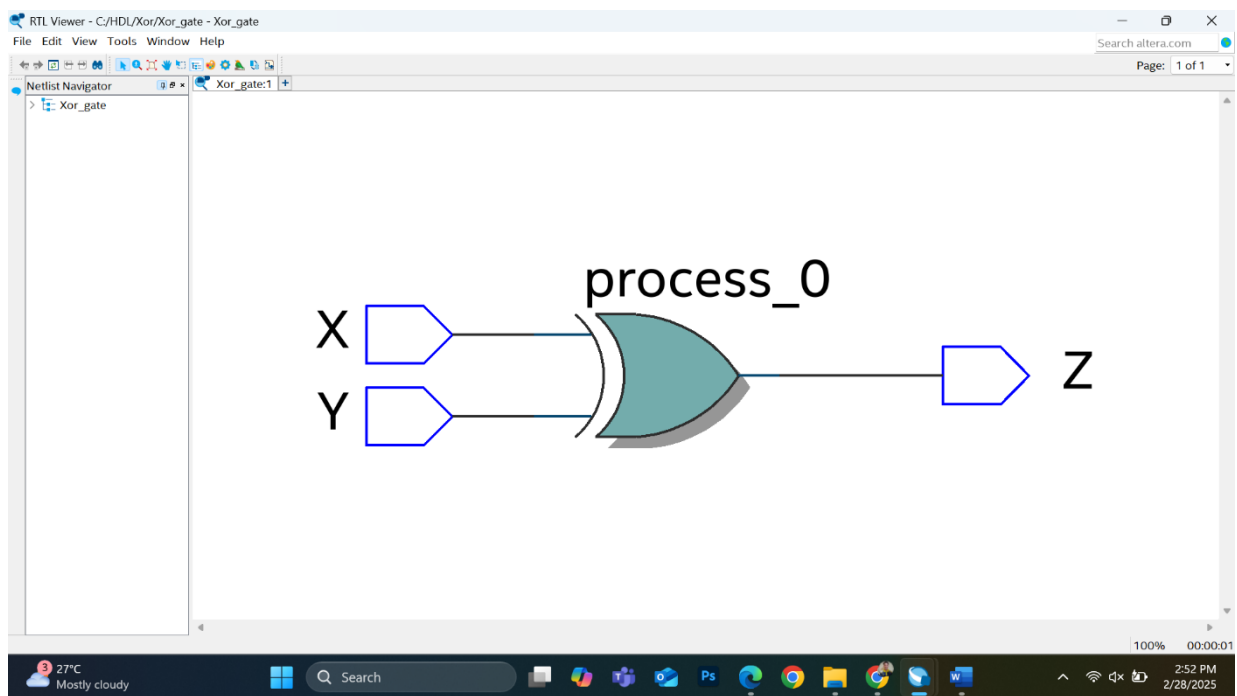
DATA FLOW EXPERIMENTS:

CODE:

```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity Xor_gate is
5  Port (
6    X: in STD_LOGIC;
7    Y: in STD_LOGIC;
8    Z: out STD_LOGIC
9  );
10 end Xor_gate;
11
12 architecture behav2 of Xor_gate is
13 begin
14   process (X, Y)
15   begin
16     if (X=Y) then
17       Z <= '1';
18     else
19       Z <= '0';
20     end if;
21   end process;
22 end behav2;
```

The screenshot shows the Quartus Prime Lite Edition interface with the code for `Xor_gate.vhd` open. The code defines an entity `Xor_gate` with three ports: `X`, `Y`, and `Z`. The architecture `behav2` implements the XOR logic using a process block. The code is titled "Xor_gate.vhd" and includes a toolbar with various editing tools. The IP Catalog on the right shows the installed IP and the project directory. The Messages window at the bottom shows the compilation results.

LOGIC GATE:



WAVE FORM:

