Name: Richard Raymond J. Canda

C.Y.S.: BSCpE-3A

#6-TITLE: EX-OR gate

LOGIC GATE SYMBOL:

7486

TRUTH TABLE:

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

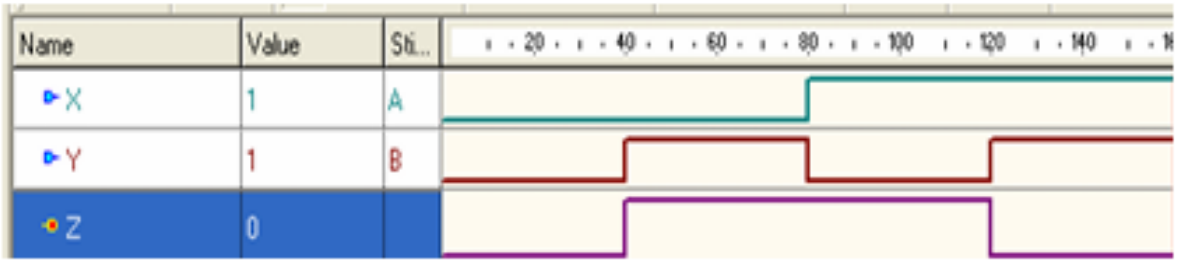
VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity xor2 is
        Port (
                X: in STD_LOGIC;
                Y: in STD_LOGIC;
                Z: out STD_LOGIC
              );
end xor2;

--Dataflow model

architecture behav1 of xor2 is
begin

        Z<= x xor y;    --Signal Assignment Statement

end behav1;
```

-- Behavioral model

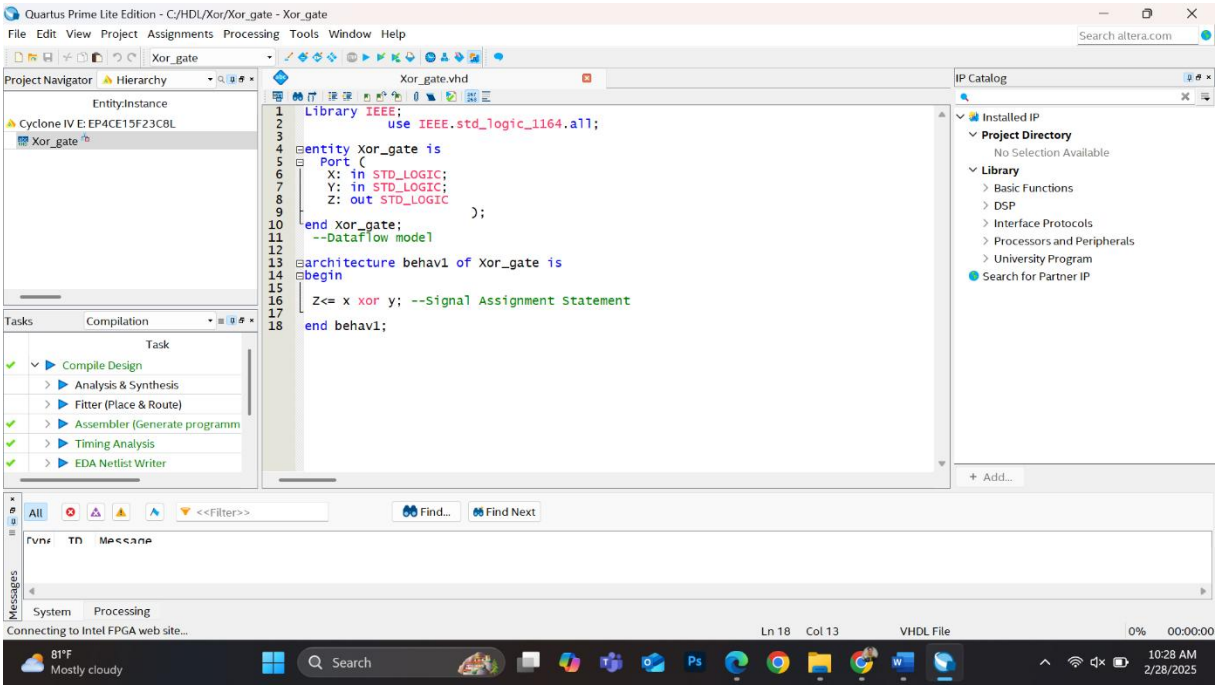
```
architecture behav2 of xor2 is
begin

   process (x, y)
    begin

       If (x/=y) then      -- Compare with truth table
          Z <= '1';
        else
          Z<= '0';
       end if;

    end process;

end behav2;
```

OUTPUT WAVEFORM:

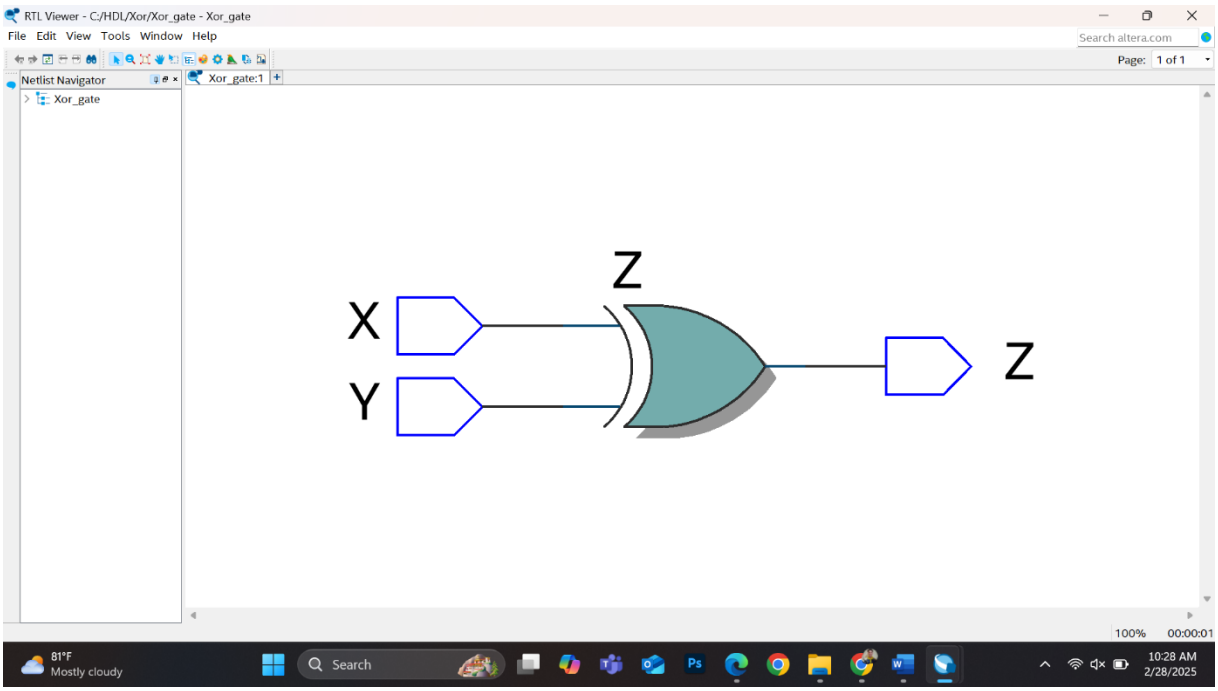


Experiment results:

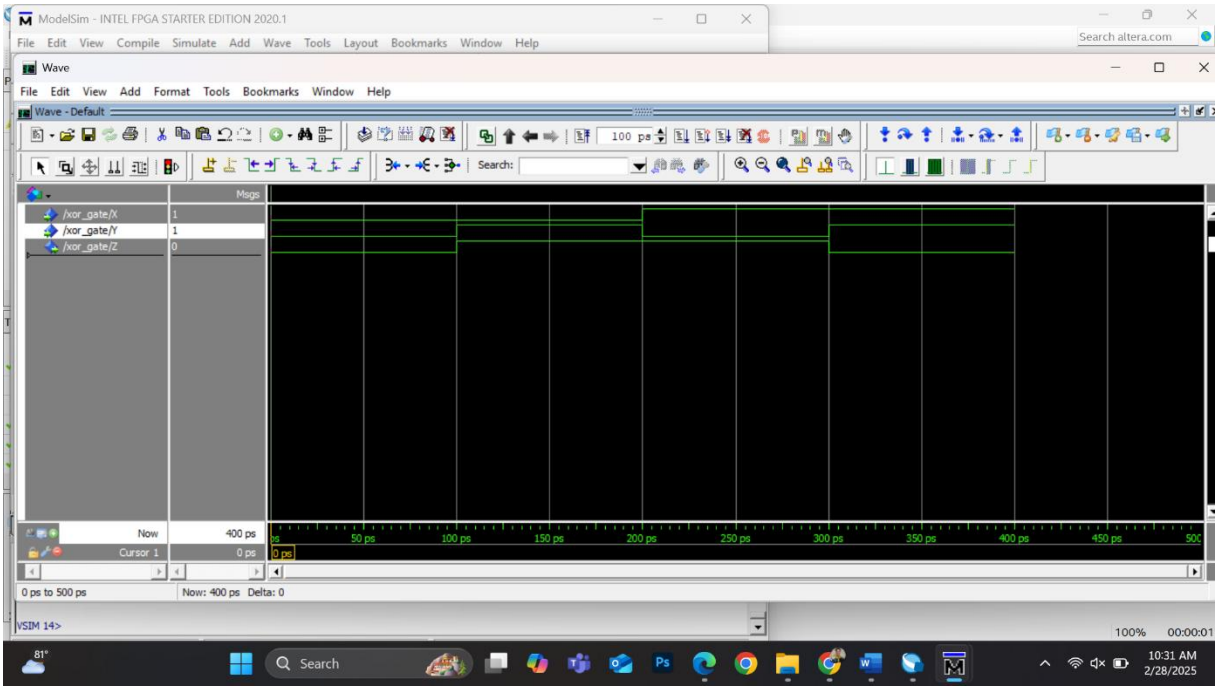
CODE



LOGIC GATE



WAVE


ModelSim - INTEL FPGA STARTER EDITION 2020.1
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/xor_gate/Y
/xor_gate/Z
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Now
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Cursor 1
0 ps
50 ps
100 ps
150 ps
200 ps
250 ps
300 ps
350 ps
400 ps
450 ps
0 ps to 500 ps
Now: 400 ps Delta: 0
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