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C.Y.S.: BSCpE-3A

#4-TITLE: NAND gate

LOGIC GATE SYMBOL:

7400

TRUTH TABLE:

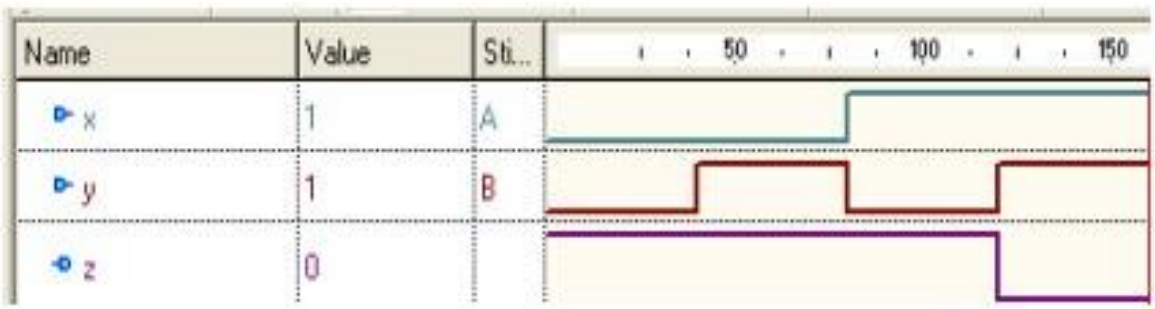
x	y	z
0	0	1
0	1	1
1	0	1
1	1	0

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity nand2 is
        port(
                x : in STD_LOGIC;
                y : in STD_LOGIC;
                z : out STD_LOGIC
            );
end nand2;
```

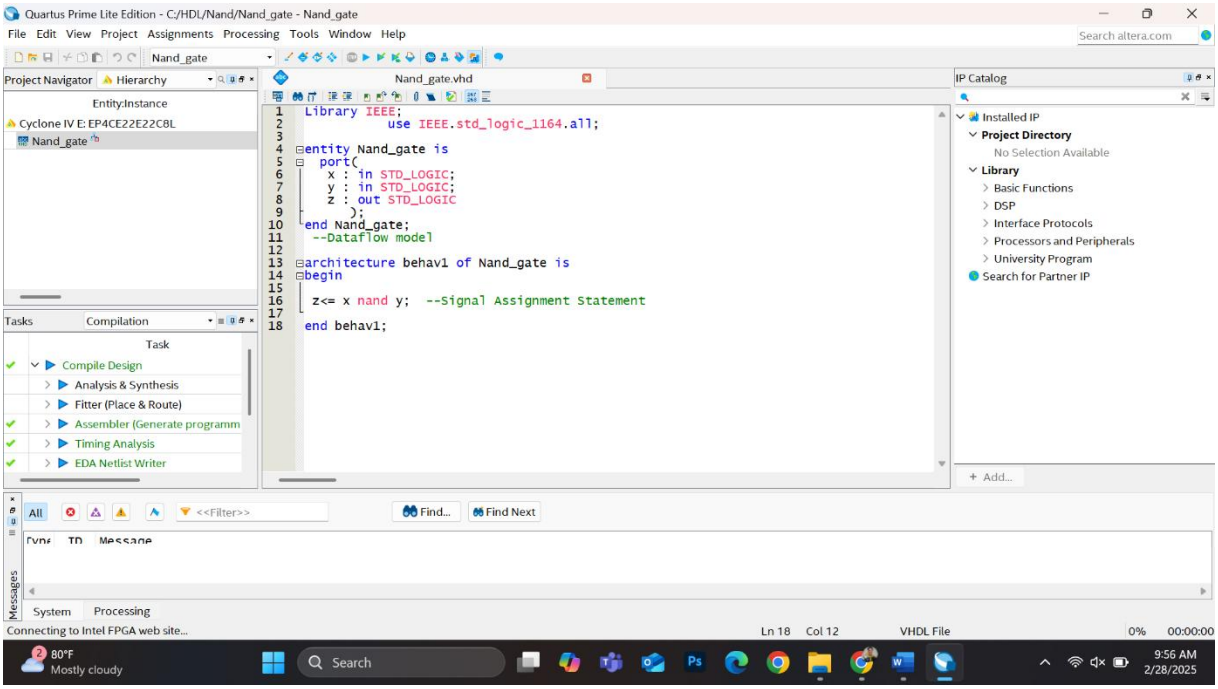
```
--Dataflow model

        architecture behav1 of nand2 is
        begin

                z<= x nand y;          --Signal Assignment Statement

        end behav1;


-- Behavioral model

        architecture behav2 of nand2 is
        begin

         Process (x, y)
          Begin

            If (x='1' and y='1') then  -- Compare with truth table
                Z <= '0';
            else
                Z <= '1';
            end if;

         end process;

       end behav2;
```

OUTPUT WAVEFORM:

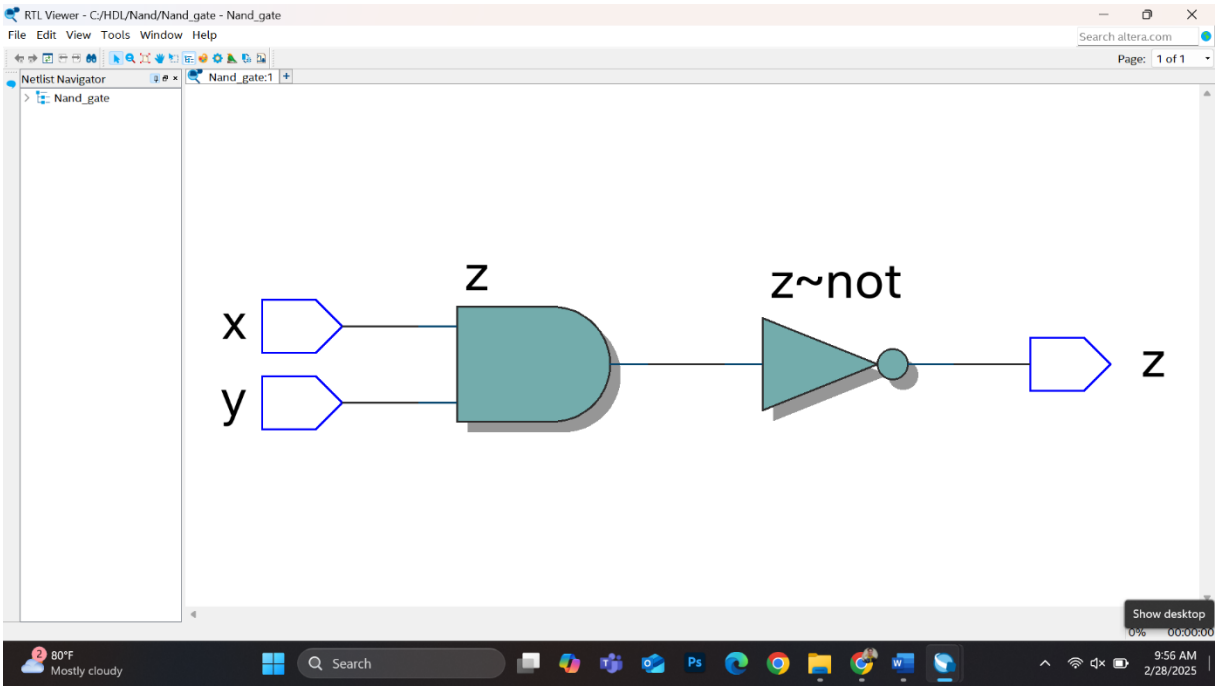


Experiment results:

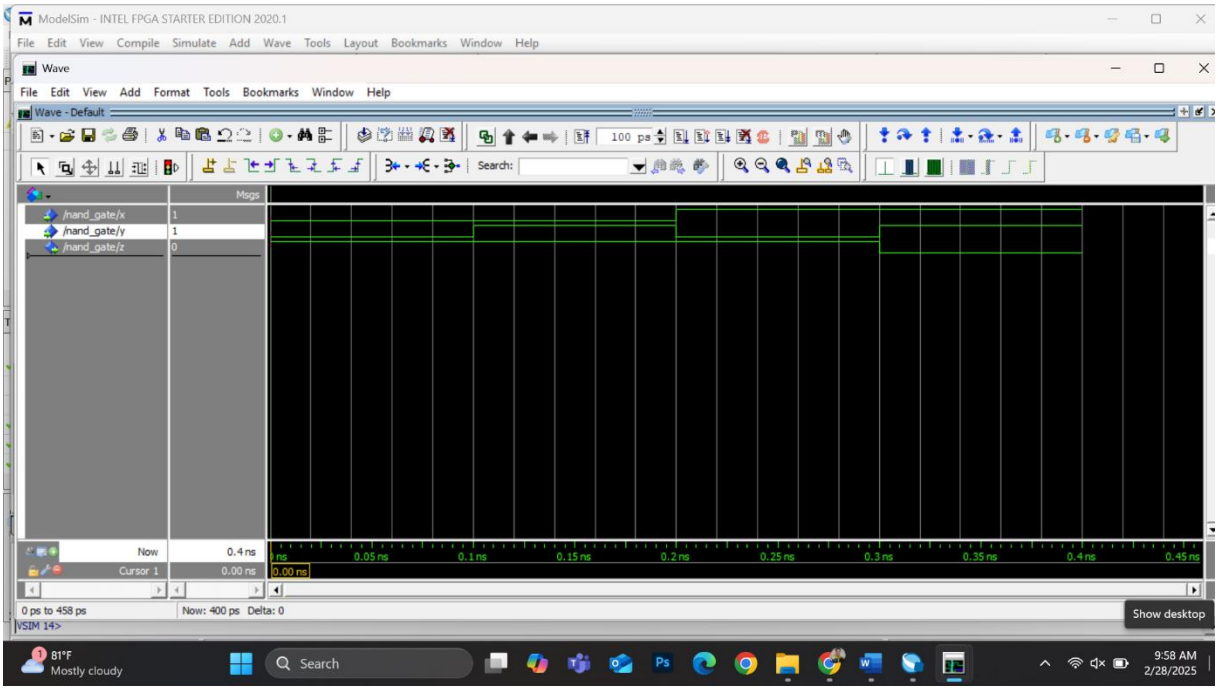
CODE



LOGIC GATE



WAVE


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/nand_gate/x
/nand_gate/y
/nand_gate/z
1
1
0
Now
0.4 ns
Cursor 1
0.00 ns
0.05 ns
0.1 ns
0.15 ns
0.2 ns
0.25 ns
0.3 ns
0.35 ns
0.4 ns
0.45 ns
0 ps to 458 ps
Now: 400 ps Delta: 0
VSIM 14>
Show desktop
81°F
Mostly cloudy
Search
9:58 AM
2/28/2025