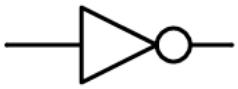
Name: Richard Raymond J. Canda

C.Y.S.: BSCpE-3A

#3-TITLE: NOT gate

LOGIC GATE SYMBOL:



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TRUTH TABLE:

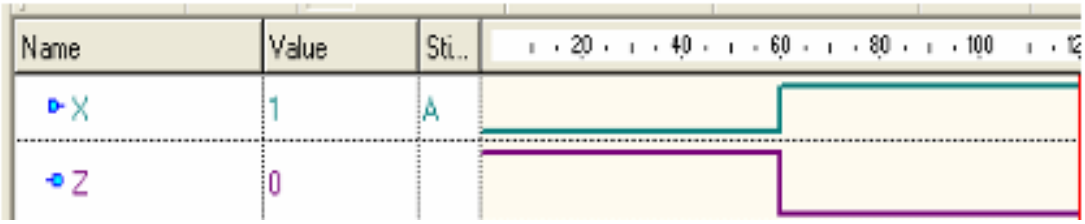
x	z
0	1
1	0

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity not1 is
        port(
                X:  in STD_LOGIC;
                Z:  out STD_LOGIC
            );
        end not1;
```

```
--Dataflow model
        architecture behav1 of not1 is
         begin

          Z<= not X;   --Signal Assignment Statement

        end behav1;

-- Behavioral model
        architecture behav2 of not1 is
         begin

           process (X)
            begin

              if (x='0') then  -- Compare with truth table
                Z <= '1';
             else
                Z<= '0';

             end if;

          end process;

       end behav2;
```

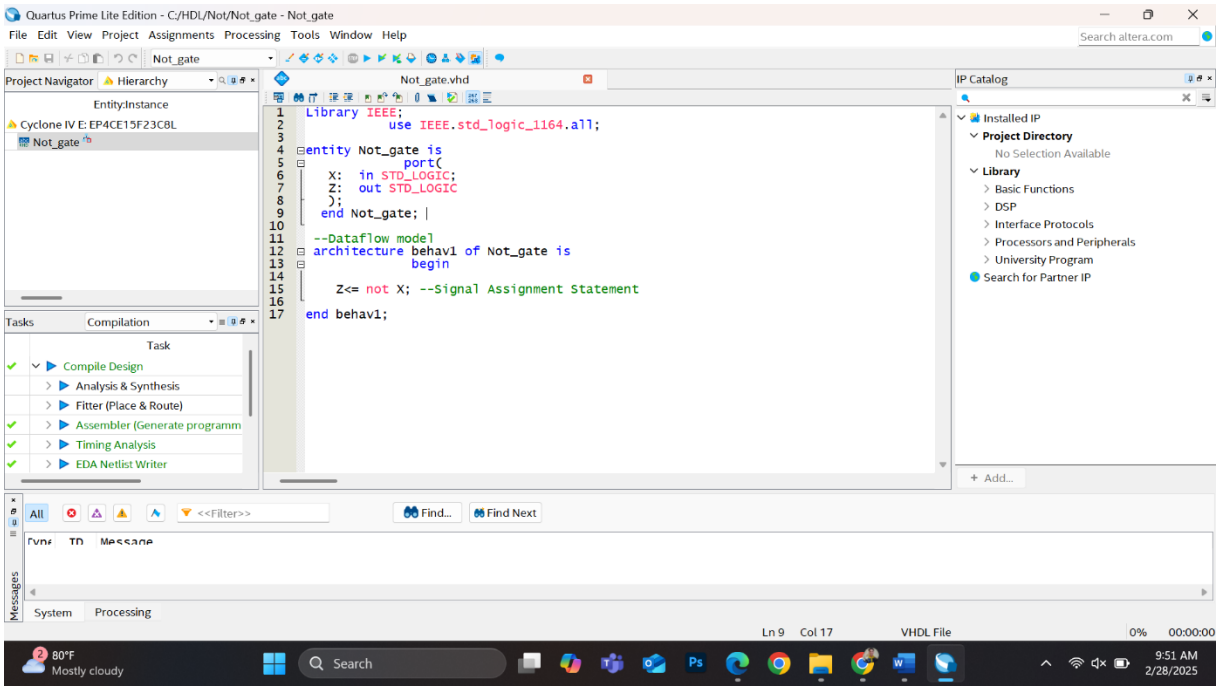
OUTPUT WAVEFORM:



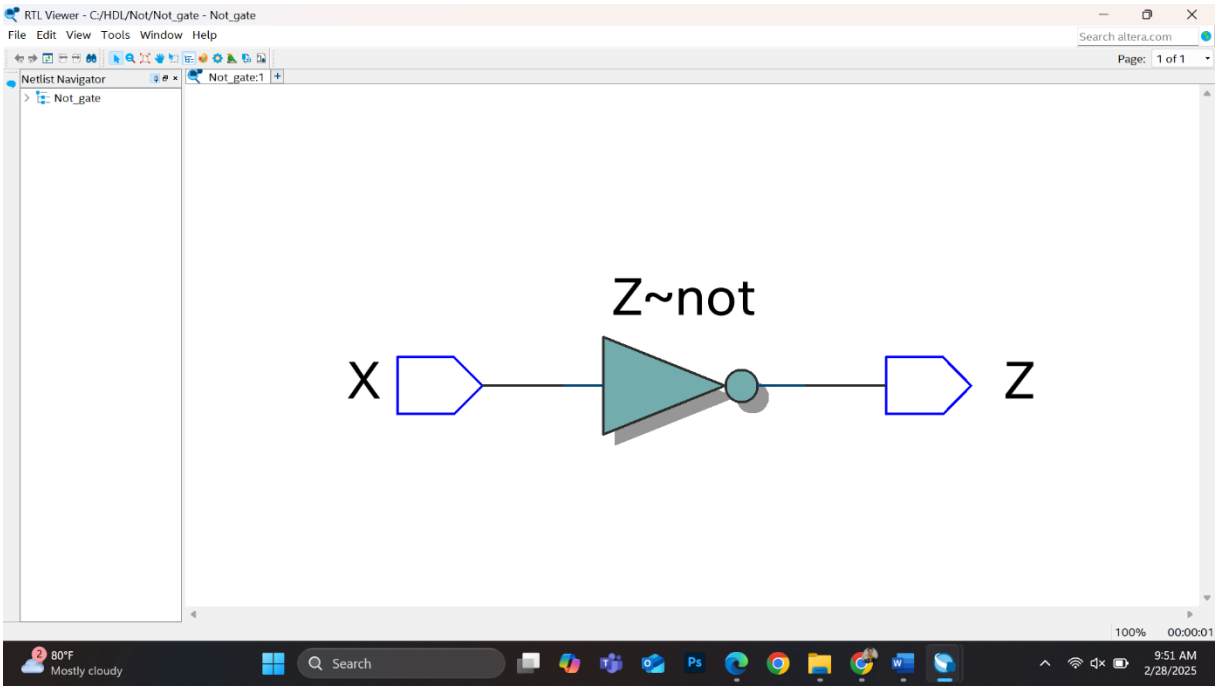
Experiment results:

DATA FLOW MODEL EXPERIMENTS:

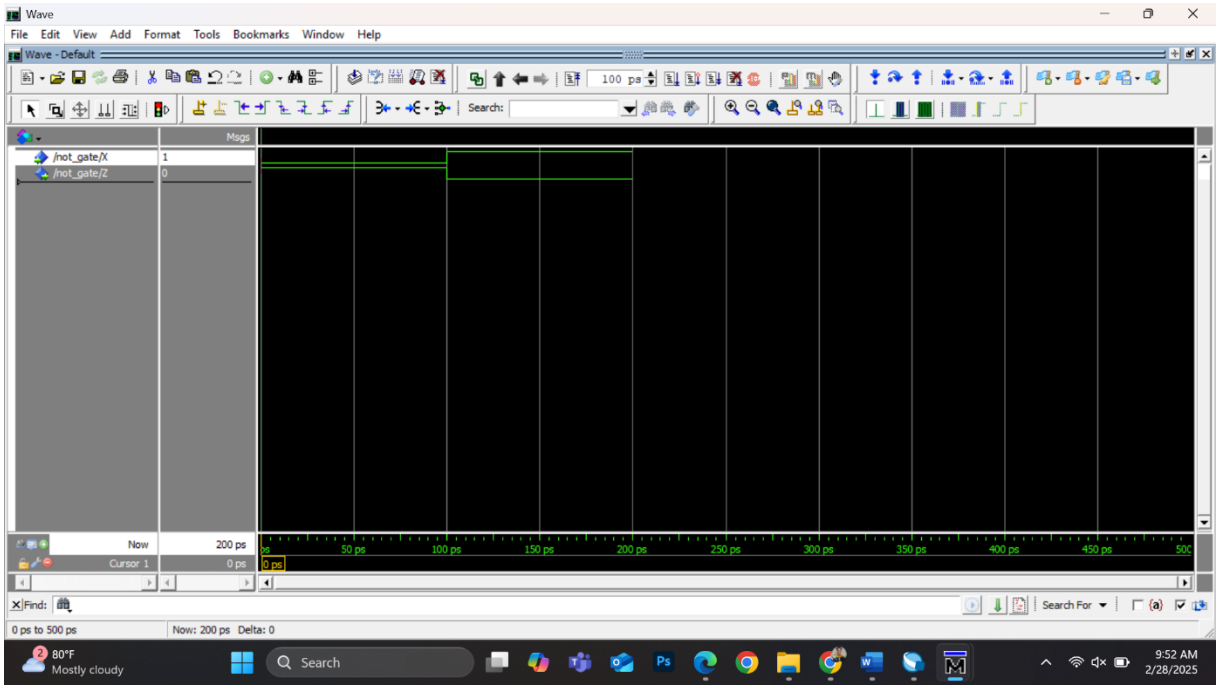
CODE



LOGIC GATE:

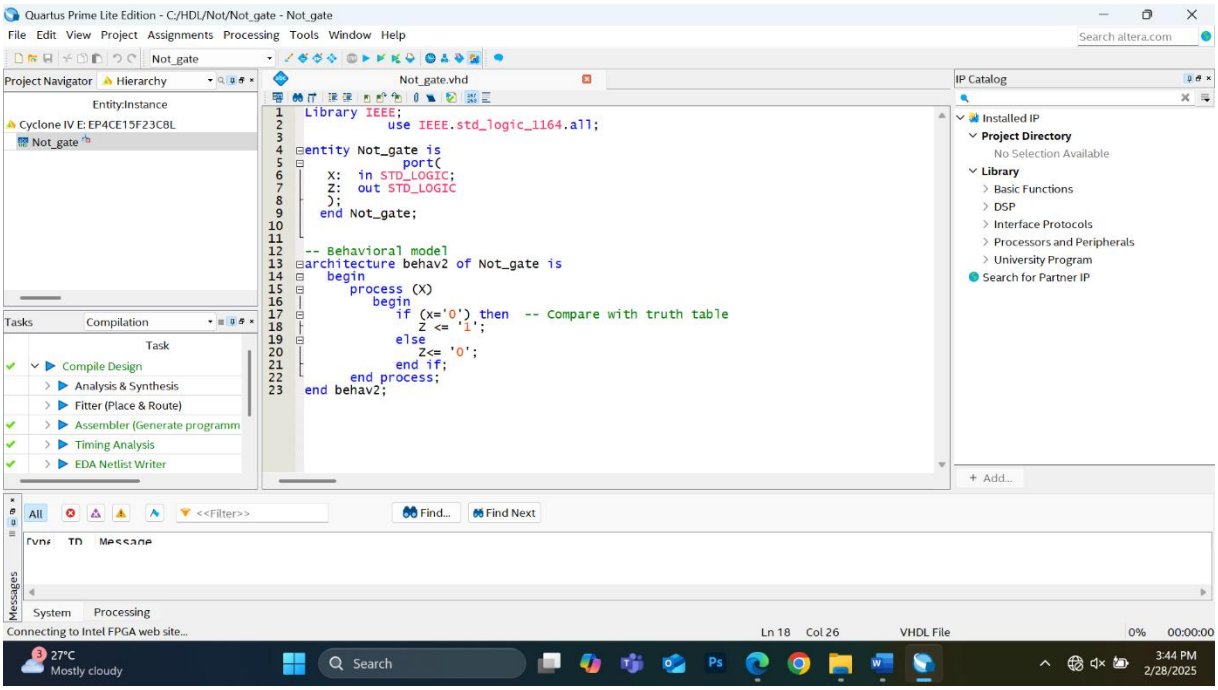


WAVEFORM:

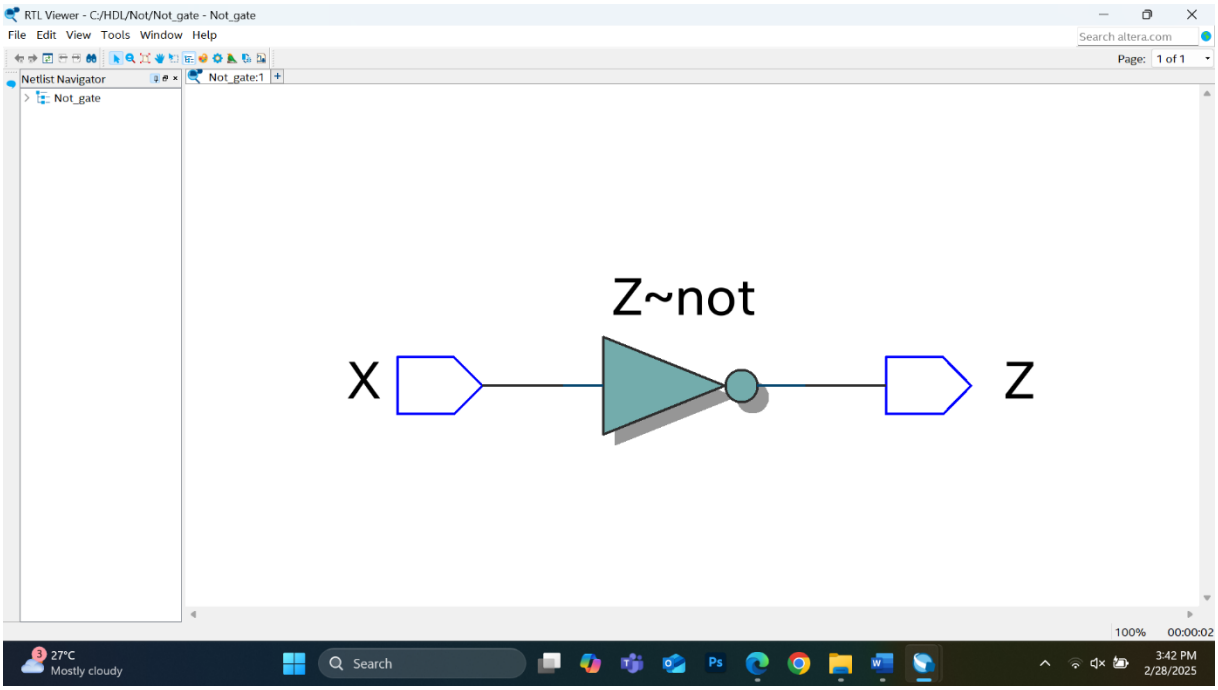


BEHAVIORAL MODEL EXPERIMENTS:

CODE:



LOGIC GATE:



WAVEFORM: