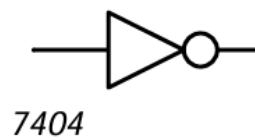


Name: Richard Raymond J. Canda

C.Y.S.: BSCpE-3A

**#3-TITLE:** NOT gate

**LOGIC GATE SYMBOL:**



**TRUTH TABLE:**

X	Z
0	1
1	0

**VHDL CODE:**

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity not1 is
    port(
        X: in STD_LOGIC;
        Z: out STD_LOGIC
    );
end not1;
```

--Dataflow model

```
architecture behav1 of not1 is
begin
```

```
    Z<= not X;  --Signal Assignment Statement
```

```
end behav1;
```

-- Behavioral model

```
architecture behav2 of not1 is
begin
```

```
    process (X)
    begin
```

```
        if (x='0') then  -- Compare with truth table
```

```
            Z <= '1';
```

```
        else
```

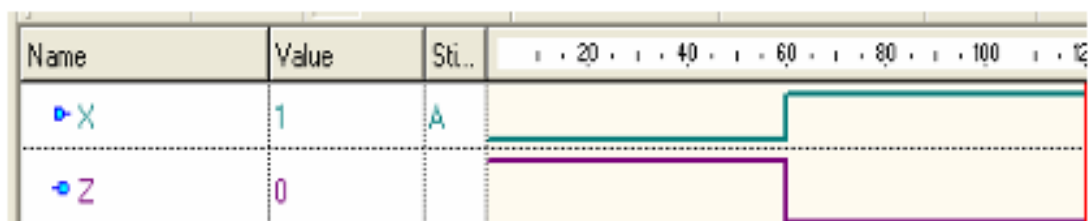
```
            Z<= '0';
```

```
        end if;
```

```
    end process;
```

```
end behav2;
```

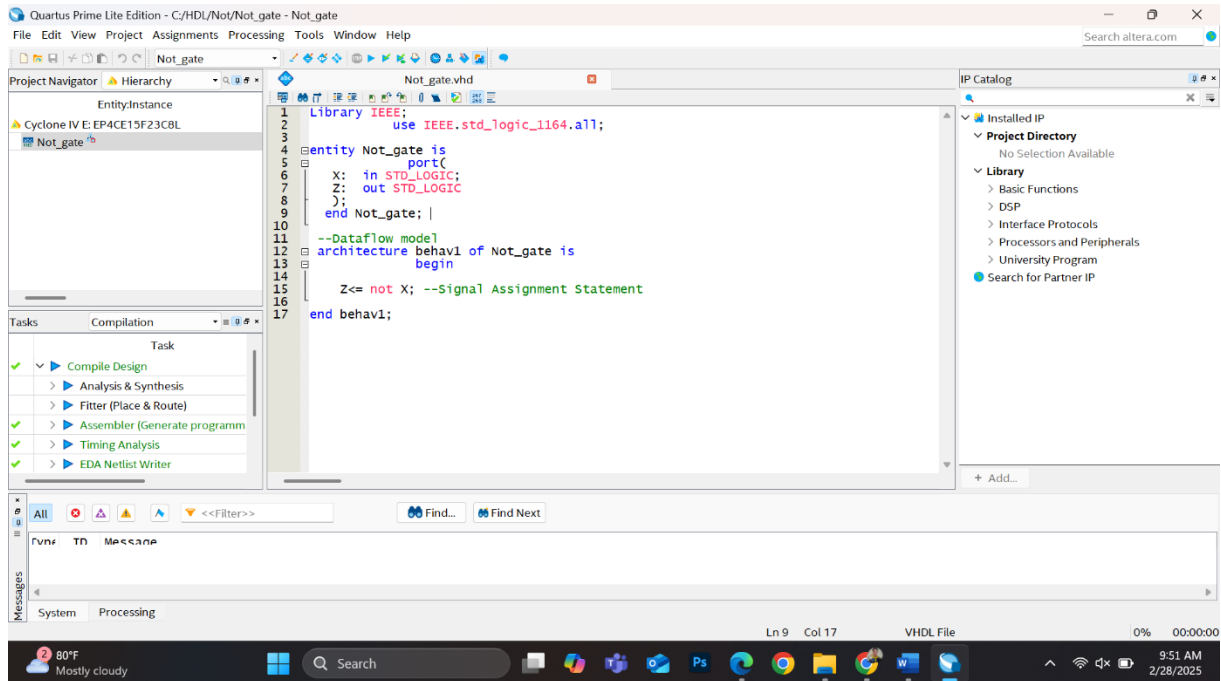
**OUTPUT WAVEFORM:**



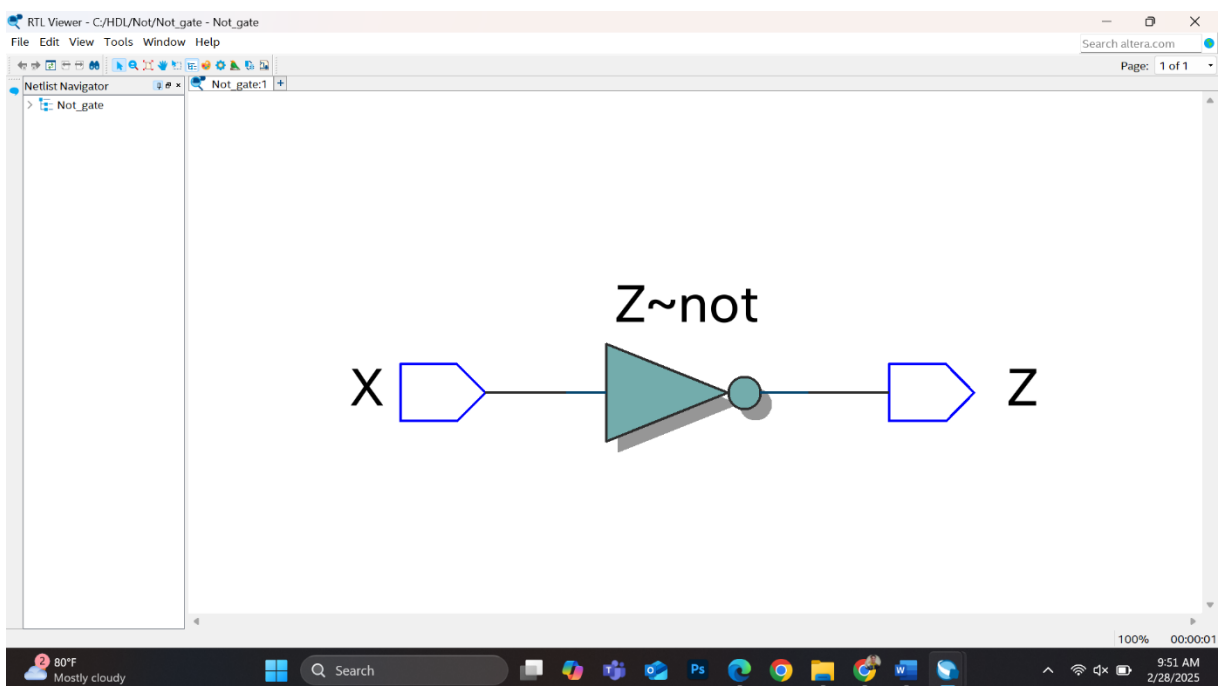
## Experiment results:

## DATA FLOW MODEL EXPERIMENTS:

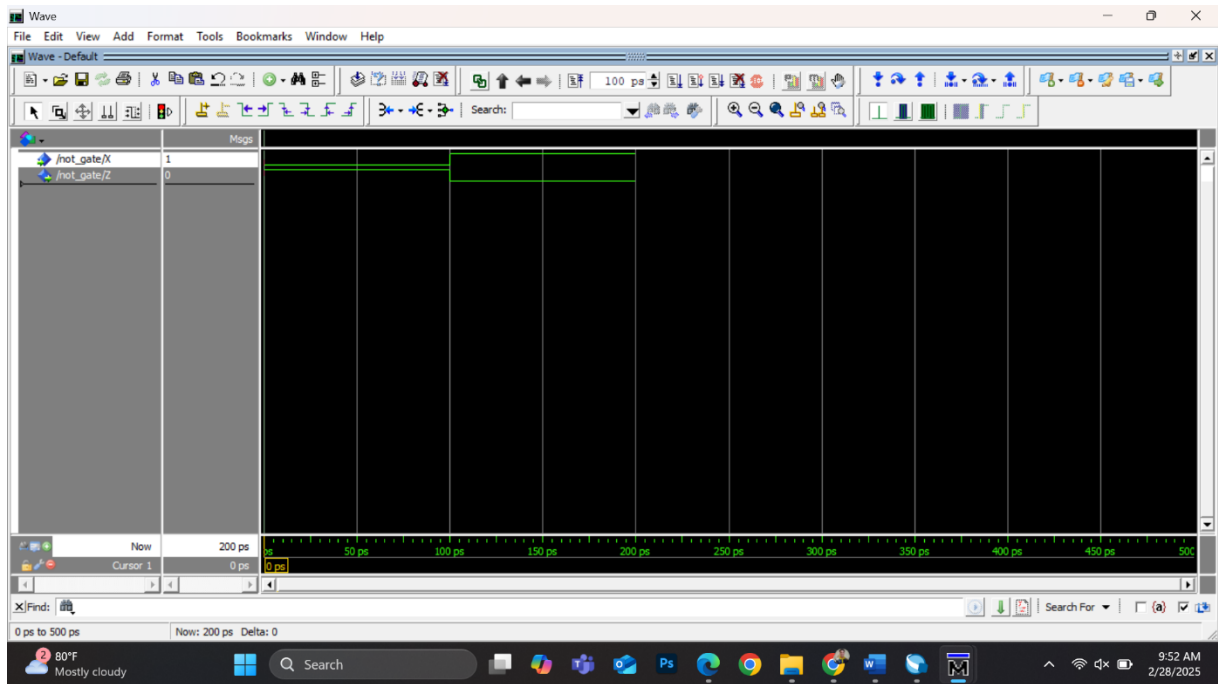
## CODE



## LOGIC GATE:



## WAVEFORM:



## BEHAVIORAL MODEL EXPERIMENTS:

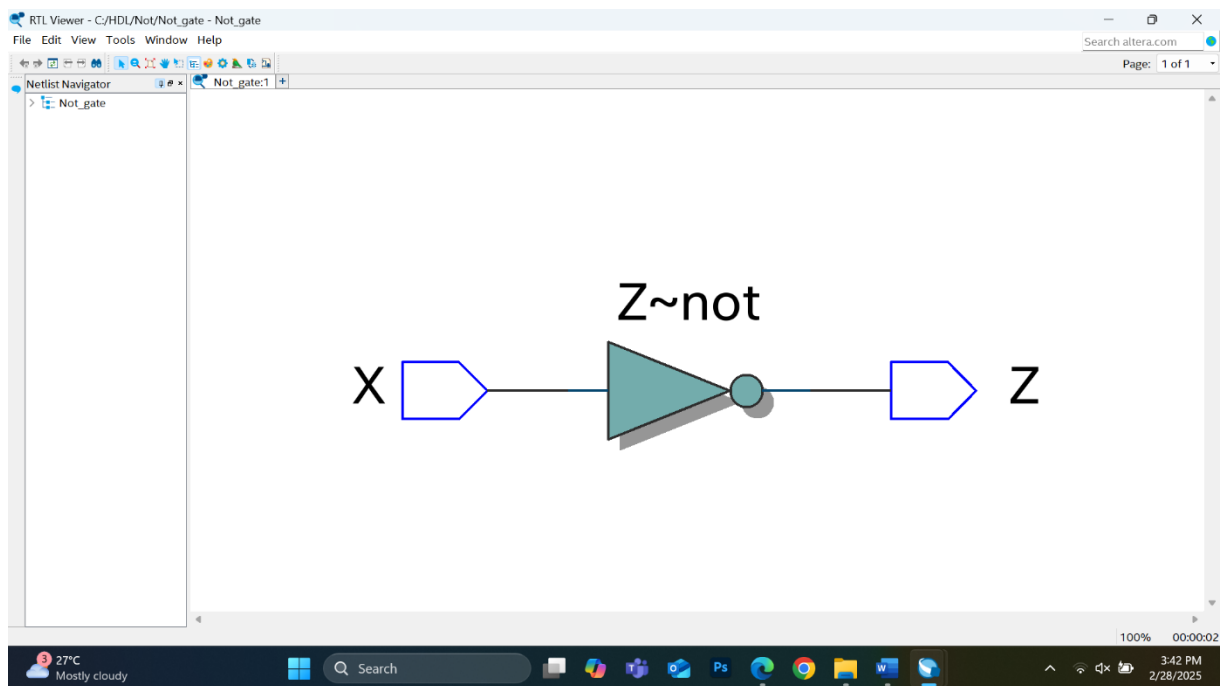
## CODE:

The screenshot shows the Quartus Prime Lite Edition IDE. The main window displays the VHDL code for a `Not_gate` entity. The code is as follows:

```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity Not_gate is
5  port(
6    X: in STD_LOGIC;
7    Z: out STD_LOGIC
8  );
9  end Not_gate;
10
11 -- Behavioral model
12
13 architecture behav2 of Not_gate is
14 begin
15   process (X)
16   begin
17     if (X='0') then -- Compare with truth table
18       Z <= '1';
19     else
20       Z <= '0';
21     end if;
22   end process;
23 end behav2;
```

The left pane shows the Project Navigator with the `Not_gate` entity selected. The right pane shows the IP Catalog. The bottom status bar indicates the current line is 18, column 26, and the file is `VHDL File`. The system tray at the bottom indicates a temperature of 27°C and a date of 2/28/2025.

## LOGIC GATE:



## WAVEFORM:

