

Name: Richard Raymond J. Canda

C.Y.S.: BSCpE-3A

#6-TITLE: EX-OR gate

LOGIC GATE SYMBOL:



7486

TRUTH TABLE:

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity xor2 is
  Port (
    X: in STD_LOGIC;
    Y: in STD_LOGIC;
    Z: out STD_LOGIC
  );
end xor2;
```

--Dataflow model

```
architecture behav1 of xor2 is
begin

  Z<= x xor y;  --Signal Assignment Statement

end behav1;
```

-- Behavioral model

```
architecture behav2 of xor2 is
begin

    process (x, y)
    begin

        If (x/=y) then    -- Compare with truth table
            Z <= '1';
        else
            Z <= '0';
        end if;

    end process;

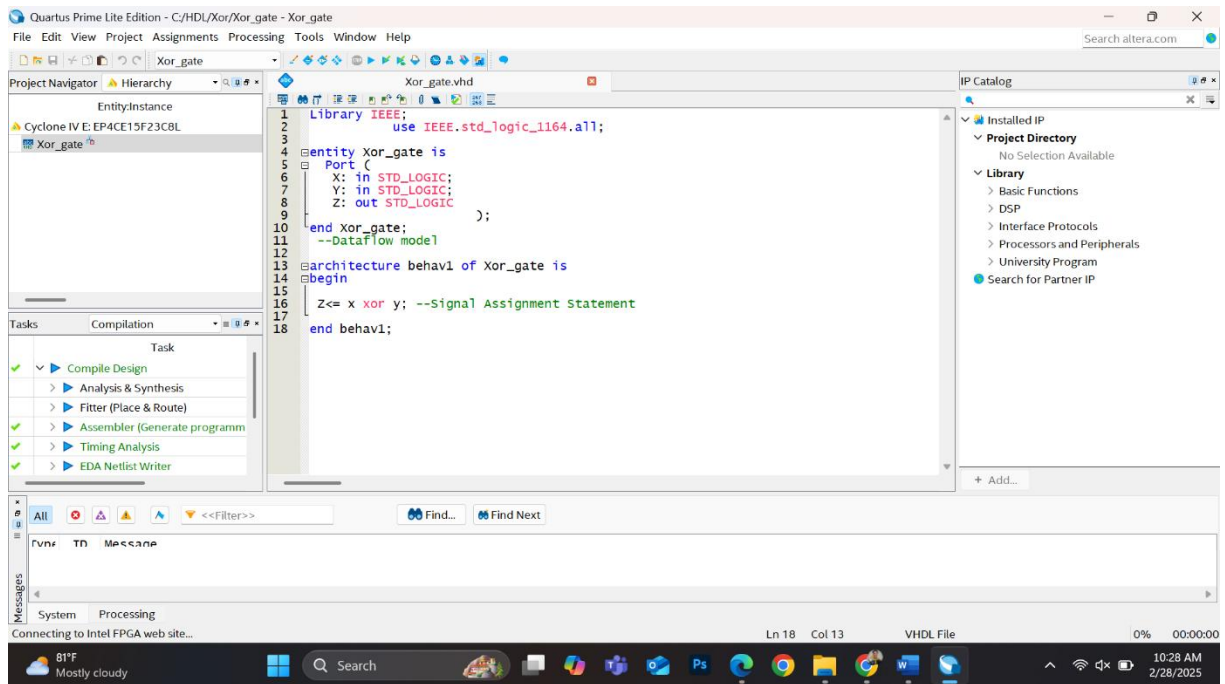
end behav2;
```

OUTPUT WAVEFORM:



Experiment results:

CODE

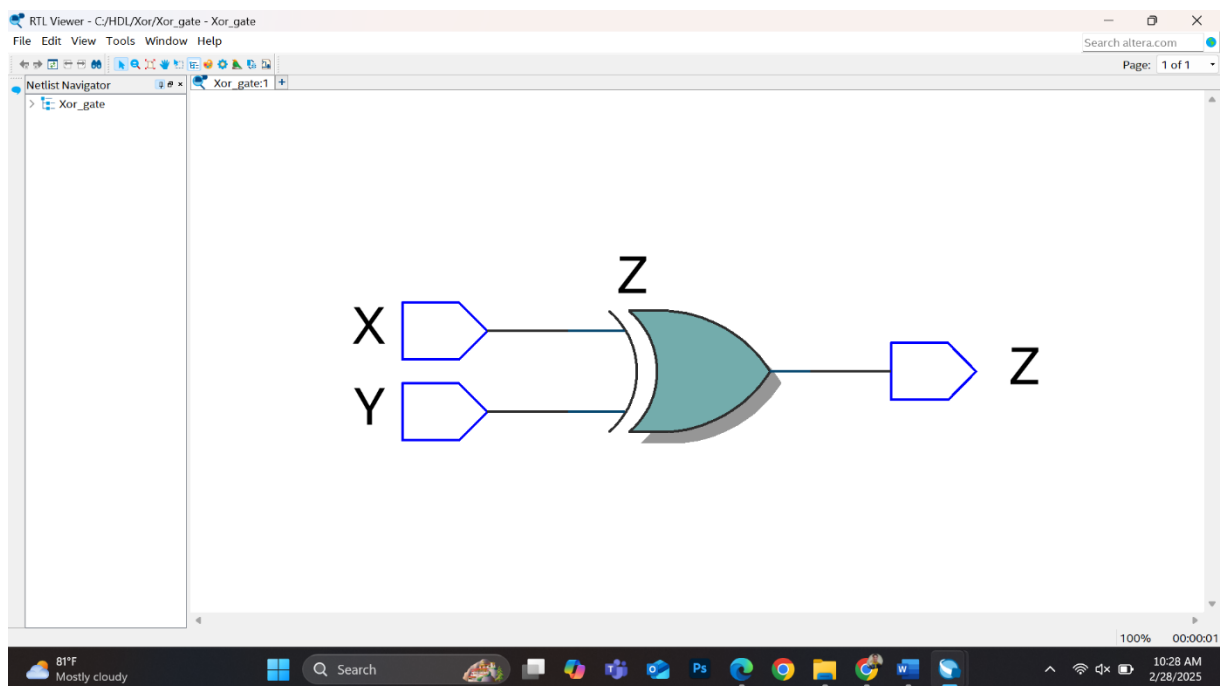


The screenshot shows the Quartus Prime Lite Edition interface. The main window displays the VHDL code for an XOR gate named 'Xor_gate.vhd'. The code is as follows:

```
1  Library IEEE;
2  use IEEE.std_logic_1164.all;
3
4  entity Xor_gate is
5      Port (
6          X: in STD_LOGIC;
7          Y: in STD_LOGIC;
8          Z: out STD_LOGIC
9      );
10 end Xor_gate;
11 --Dataflow model
12
13 architecture behav1 of Xor_gate is
14 begin
15     Z <= x xor y; --Signal Assignment Statement
16
17 end behav1;
```

The interface also shows the Project Navigator on the left with the 'Xor_gate' entity selected. The Tasks window on the left lists compilation tasks: Compile Design, Analysis & Synthesis, Fitter (Place & Route), Assembler (Generate program), Timing Analysis, and EDA Netlist Writer. The IP Catalog on the right shows the installed IP and project directory. The status bar at the bottom indicates the file is 'Xor_gate.vhd' and the current line is 18, column 13.

LOGIC GATE



WAVE

