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C.Y.S.: BSCpE – 3A

The **CODE:**

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity en_wout is
   Port ( i : in  STD_LOGIC_VECTOR (7 downto 0);
        y : out  STD_LOGIC_VECTOR (2 downto 0));
end en_wout;
architecture Behavioral of en_wout is
begin
with i select
y<="000" when "00000001",
"001" when "00000010",
"010" when "00000100",
"011" when "00001000",
"100" when "00010000",
"101" when "00100000",
"110" when "01000000",
"111" when others;
end Behavioral;
```
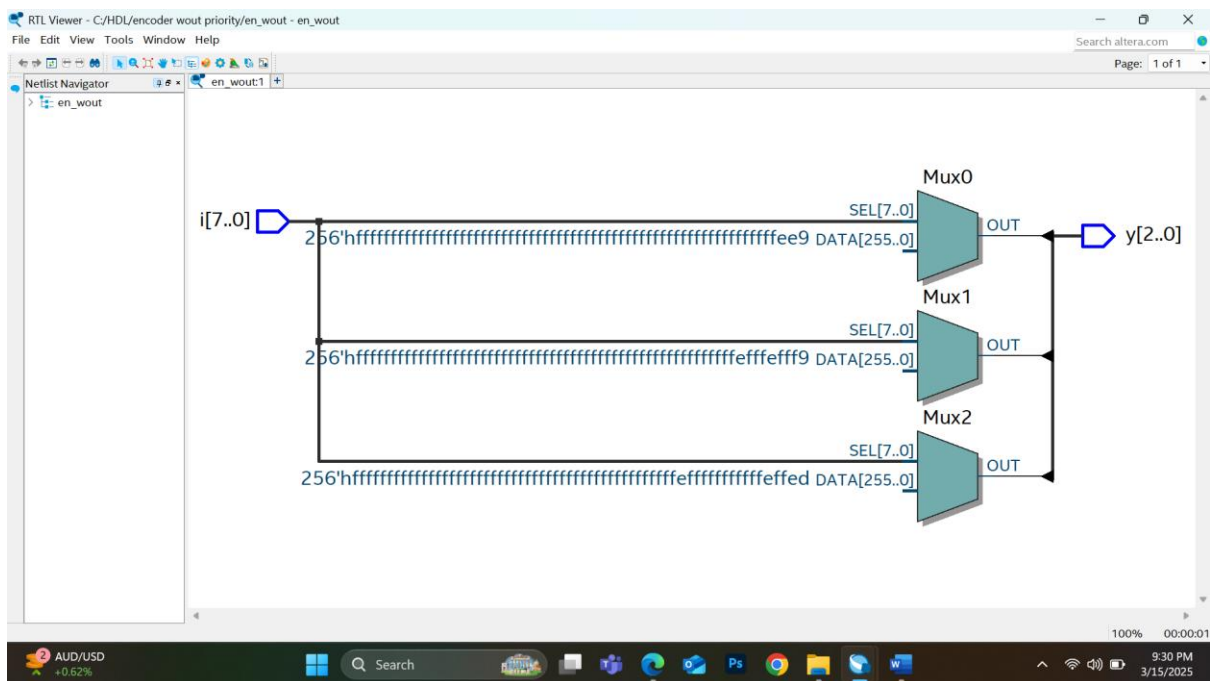
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity en_wout is
    Port ( i : in  STD_LOGIC_VECTOR (7 downto 0);
               y : out  STD_LOGIC_VECTOR (2 downto 0));
end en_wout;
architecture Behavioral of en_wout is
begin
with i select
y<="000" when "00000001",
"001" when "00000010",
"010" when "00000100",
"011" when "00001000",
"100" when "00010000",
"101" when "00100000",
"110" when "01000000",
"111" when others;
end Behavioral;
```

The LOGIC GATE:

The **WAVEFORM**: