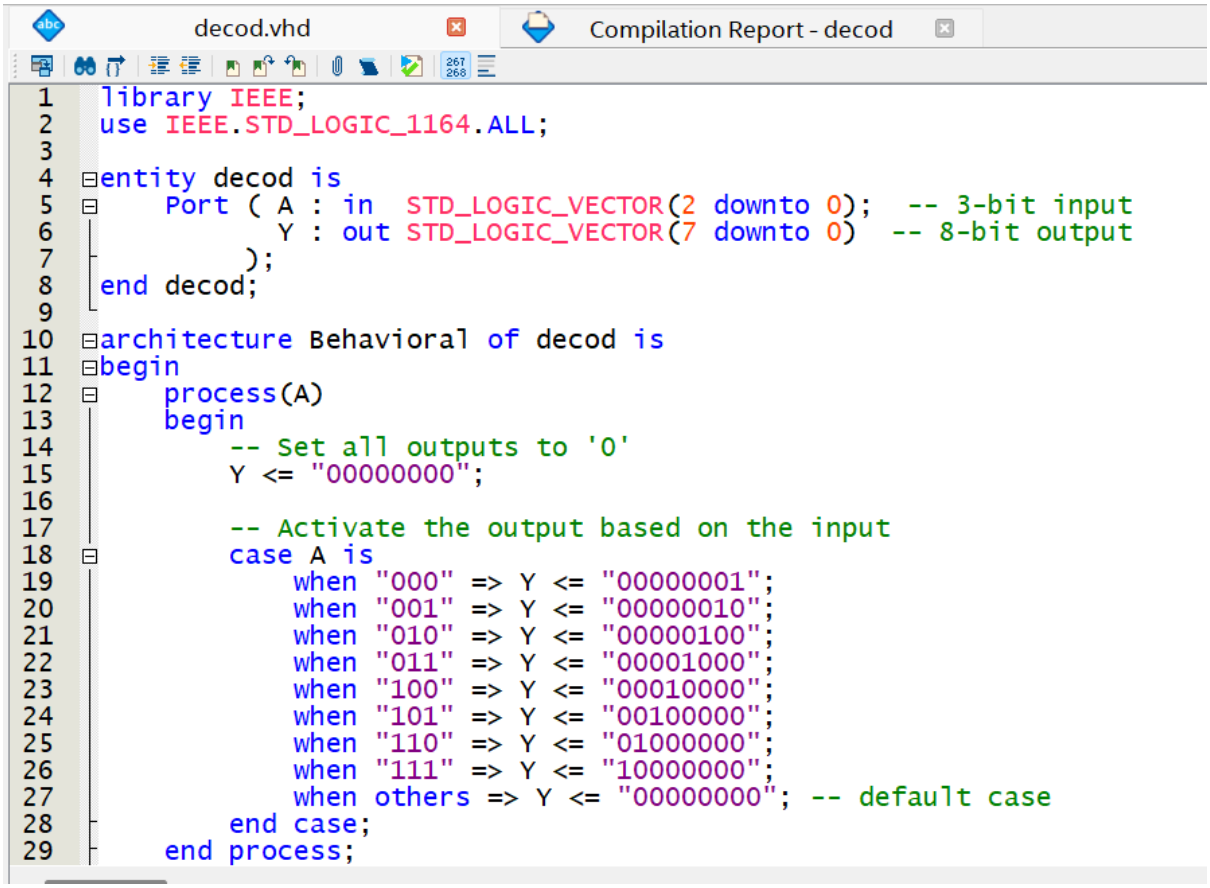
Name: Richard Raymond J. Canda

C.Y.S.: BSCpE – 3A

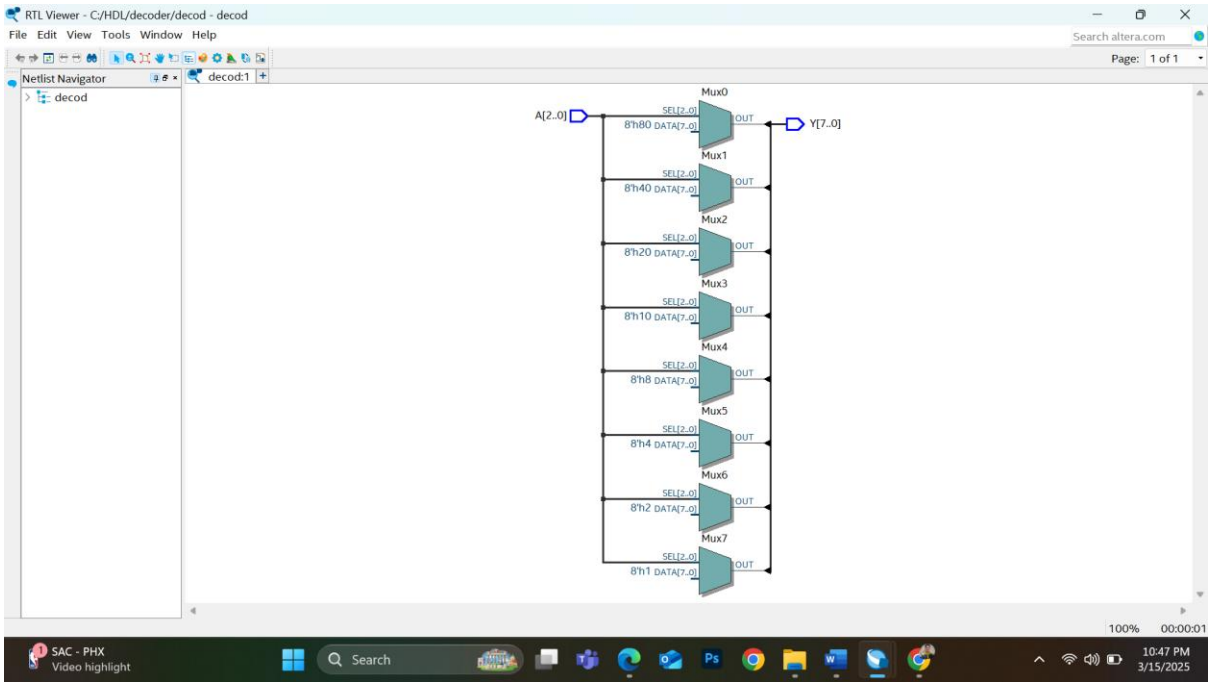
The CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity decod is
    Port ( A : in  STD_LOGIC_VECTOR(2 downto 0);  -- 3-bit input
           Y : out STD_LOGIC_VECTOR(7 downto 0)  -- 8-bit output
         );
end decod;

architecture Behavioral of decod is
begin
    process(A)
    begin
        -- Set all outputs to '0'
        Y <= "00000000";

        -- Activate the output based on the input
        case A is
            when "000" => Y <= "00000001";
            when "001" => Y <= "00000010";
            when "010" => Y <= "00000100";
            when "011" => Y <= "00001000";
            when "100" => Y <= "00010000";
            when "101" => Y <= "00100000";
            when "110" => Y <= "01000000";
            when "111" => Y <= "10000000";
```

```
        when others => Y <= "00000000"; -- default case
    end case;
end process;
end Behavioral;
```



The LOGIC GATE:



The WAVEFORM: