Name: Richard Raymond J. Canda

C.Y.S.: BSCpE-3A

#5- TITLE: NOR gate

LOGIC GATE SYMBOL:

7402

TRUTH TABLE:

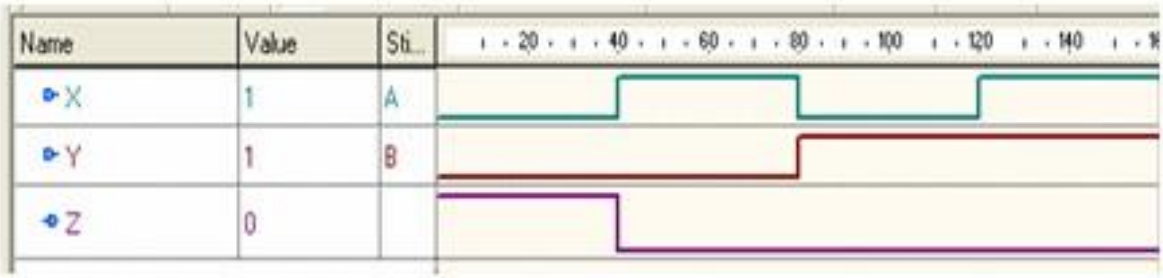
x	y	z
0	0	1
0	1	0
1	0	0
1	1	0

VHDL CODE:

```
Library IEEE;
use IEEE.std_logic_1164.all;

entity nor2 is
        Port (
                X: in STD_LOGIC;
                Y: in STD_LOGIC;
                Z: out STD_LOGIC
            );
end nor2;
```

```
--Dataflow model

        architecture behav1 of nor2 is
        begin

                Z<= x nor y;    --Signal Assignment Statement

        end behav1;

-- Behavioral model

architecture behav2 of nor2 is
begin

        process (x, y)
         begin

           If (x='0' and y='0') then   -- Compare with truth table
             Z <= '1';
           else
             Z <= '0';
           end if;

         end process;

        end behav2;
```

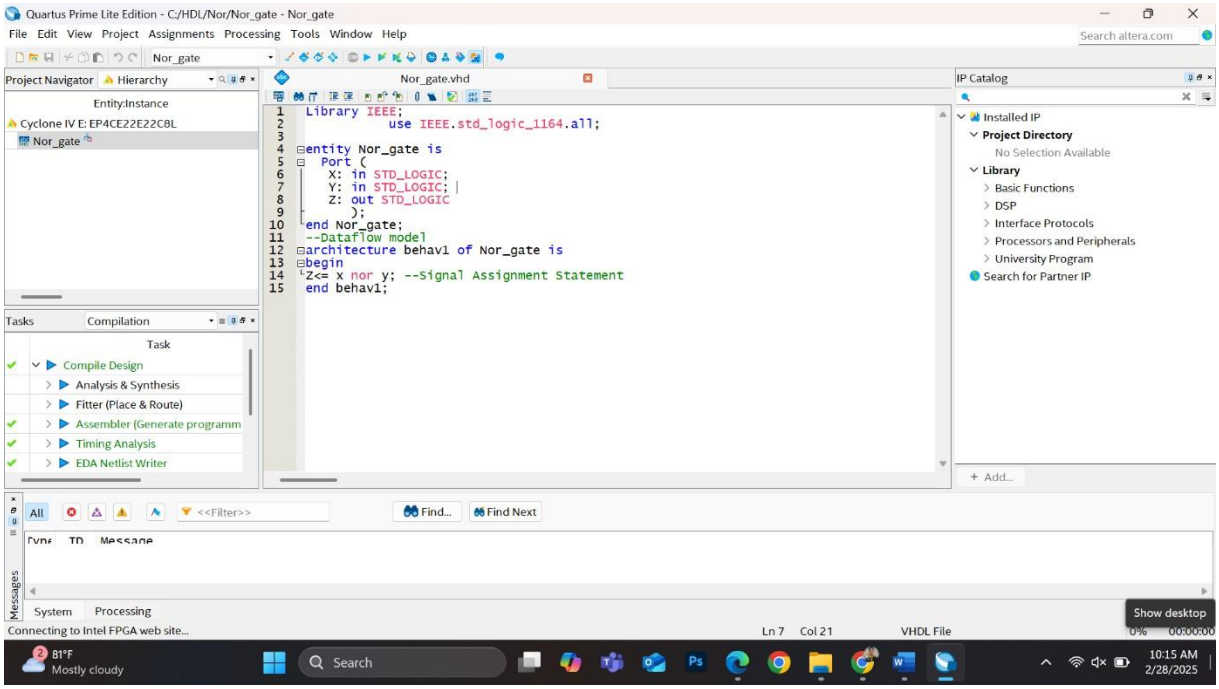
OUTPUT WAVEFORM:



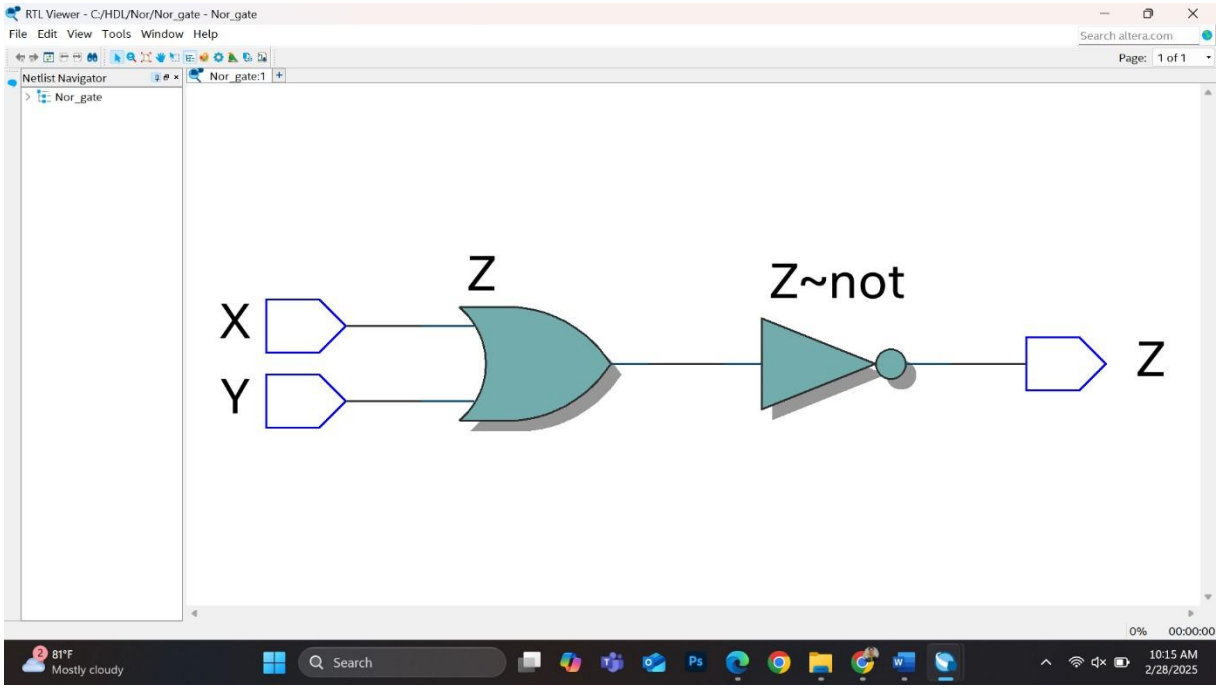
Experiment results:

DATA FLOW MODEL EXPERIMENTS:

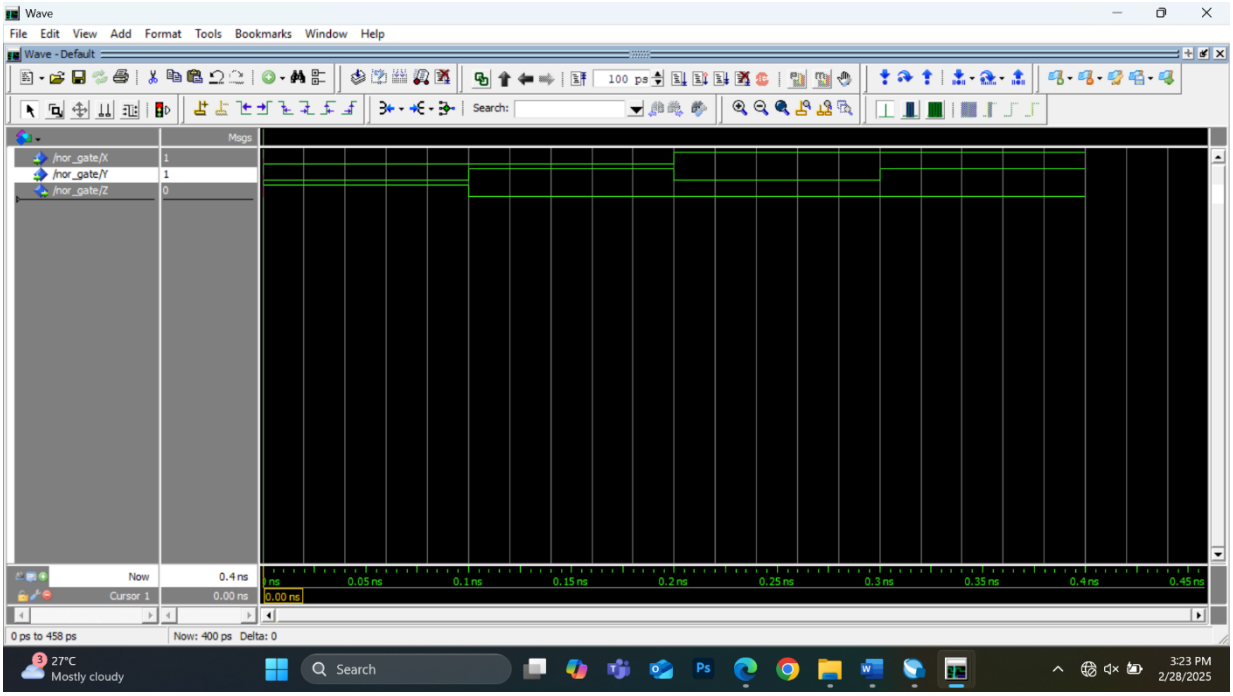
CODE:



LOGIC GATE:

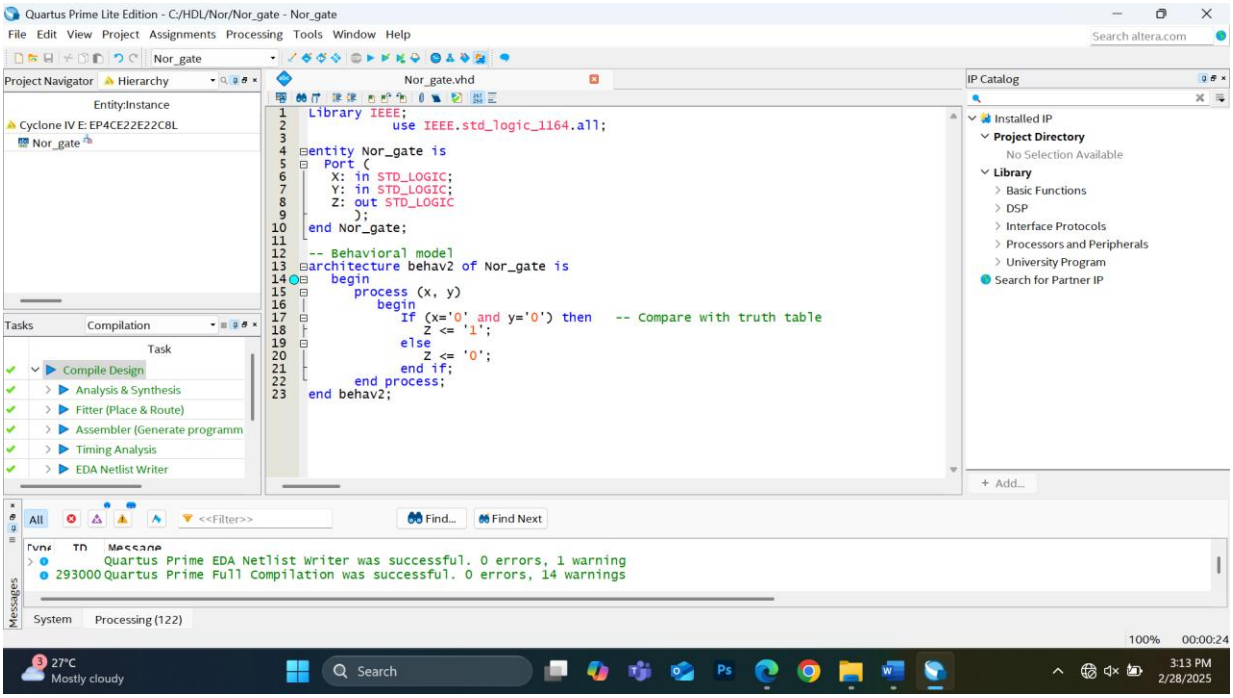


WAVEFORM:

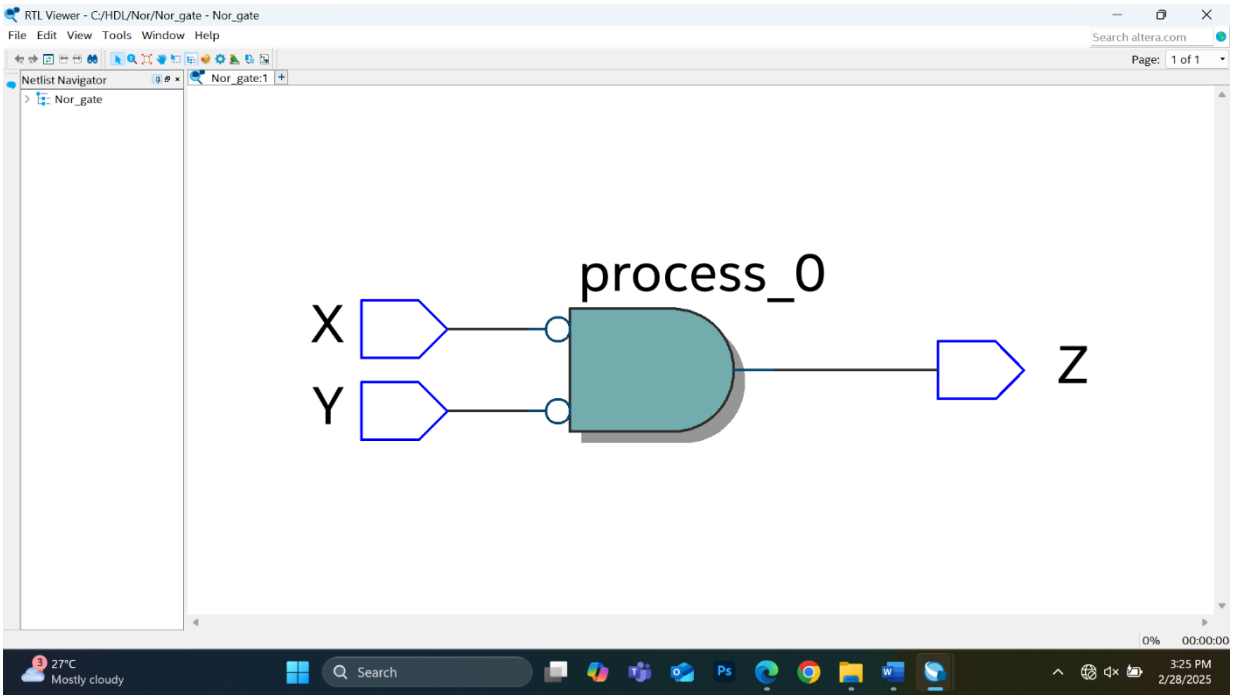


BEHAVIORAL MODEL EXPERIMENTS:

CODE:



LOGIC GATE:



WAVEFORM: