Name: Richard Raymond J. Canda
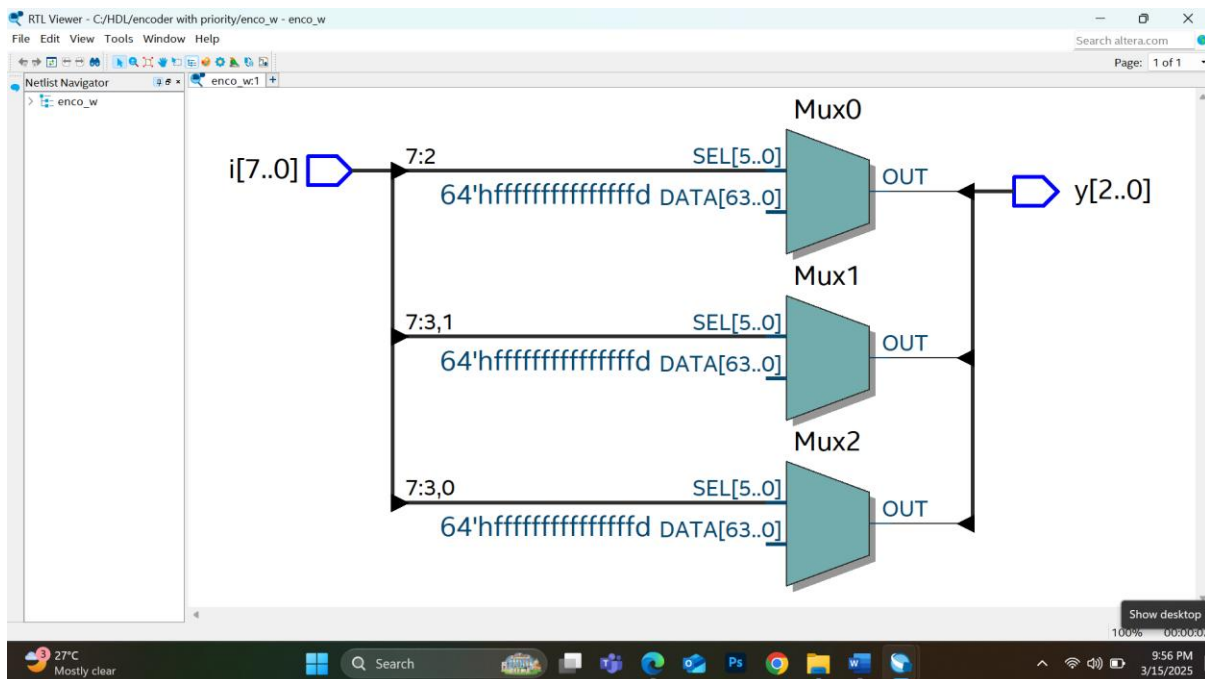
C.Y.S.: BSCpE – 3A

The CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity enco_w is
   Port ( i : in  STD_LOGIC_VECTOR (7 downto 0);
        y : out  STD_LOGIC_VECTOR (2 downto 0));
end enco_w;
architecture Behavioral of enco_w is
begin
with i select
y<="000" when "00000111",
"001" when "00000110",
"010" when "00000101",
"011" when "00000100",
"100" when "00000011",
"101" when "00000010",
"110" when "00000001",
"111" when others;
end Behavioral;
```

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity enco_w is
    Port ( i : in  STD_LOGIC_VECTOR (7 downto 0);
           y : out  STD_LOGIC_VECTOR (2 downto 0));
end enco_w;
architecture Behavioral of enco_w is
begin
with i select
y<="000" when "00000111",
"001" when "00000110",
"010" when "00000101",
"011" when "00000100",
"100" when "00000011",
"101" when "00000010",
"110" when "00000001",
"111" when others;
end Behavioral;
```

The LOGIC GATE:

The WAVEFORM: