EAST WEST UNIVERSITY
DEPT. OF EEE

SECTION: 01

COURSE CODE: EEE 416

COURSE NAME: VLSI CIRCUITS & SYSTEM

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LAB REPORT 04

EXPERIMENT NAME: NOR 2 INPUT SCHEMATIC, SYMBOL & LAYOUT GENERATION

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Objective: The objective is to design a NOR gate with two inputs, including creating a schematic, symbol and layout for fabrication. The schematic will illustrate the circuitry, the sysbol will represent it in diagrams, and the layout will depict physical placement of component on a chip. This process ensure accurate representation & functionality of the NOR gate in electronic system.

Introduction: A schematic diagram shows the function of a circuit with little emphasis on its physical characteristics. The primary goal of the schematic diagram is to show the functional relationships between components like MOSFETS, allowing the circuit to be easily analysed. Schematics for electronic circuits are prepared by designers using EDA tools such as Schematic XL to Virtuoso from Cadence.

Methodology: To generate a NOR two inputs schematic, symbol & layout, begin by using Electronic Design Automation (EDA) software like Cadence Virtuoso Design Compiler.

→ We will drag and drop NOR gates from the component library onto the schematic canvas. We will connect the inputs & outputs of the NOR gates using wires or busses, ensuring correct logic component.

→ We will generate a symbol for the NOR gate by arranging standard logic sysbols for inputs & outputs in a way that clearly represents the gate's function. Ensure consistency with industry standards for symbol representation.

→ We will translate the schematic into a layout by placing transistors & interconnects according to the design rules of the fabrication process.

Theory: A NOR gate is a digital logic gate that performs NOR operation. It has two or more inputs & one one output signals. The output of NOR gate is "high" only when none of its inputs are "high". In other words, the output is "low" if any of the inputs are high. The NOR gate is characterized by its truth table, which shows the relationship between its inputs and output. It is widely used in digital electronics for various applications such as Boolean logic operations, digital circuit design & building more complex logic functions.

Truth Table:

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Specifications:

→ V_{dc} = 1.8V [DC Voltage]

→ V_{pulse_1}:

$Voltage_1$ = 0V

$Voltage_2$ = 1.8V [connected to "a"]

Period = 200 ns

Pulse Width = 100 ns

→ V_{pulse_2}:

$Voltage_1$ = 0V

$Voltage_2$ = 1.8V [Connected to "b"]

Period = 100 ns

Pulse Width = 50 ns

Process: Generating a NOR gate with two inputs typically severals steps, including designing the schematic, creating a symbol for the gate & laying out the psiysical components on a chip or boaard.

→ We will staart by creating a schematic diagram using a CAD tool like Cadence OrCAD, Altium Designer or KiCad. We'll place two inputs nodes & one output nodes. We'll connect the inputs to the gate logic & connect the output to the appropriate gate.

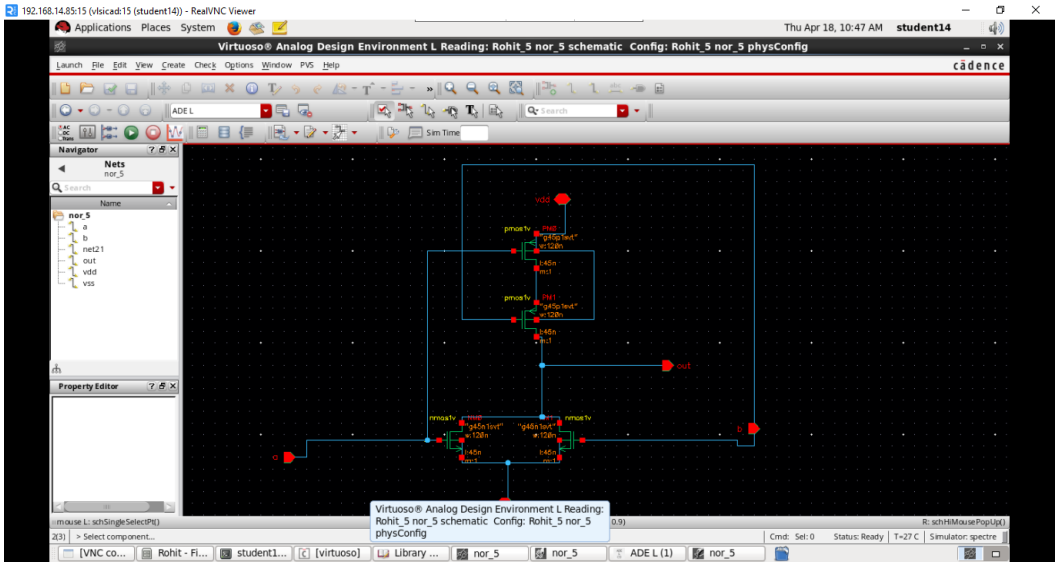
→ We'll design a graphically symbol to represent the NOR gate in circuit diagrams. This symbol typically consists of a triangle with a bubble at the output, representation the logical negation. The symbol should be easily recognizable & conform to standard conventions.

→ We'll layout the physical components of the NOR gate on a chip. We'll define the placement & routing of transistors, resistors & other components according the schematic design. We'll ensure proper spacing & routing to minimize signal interface and optimize performace & pay attention to factors like power consumption, signal propagation delay & noise immunity.

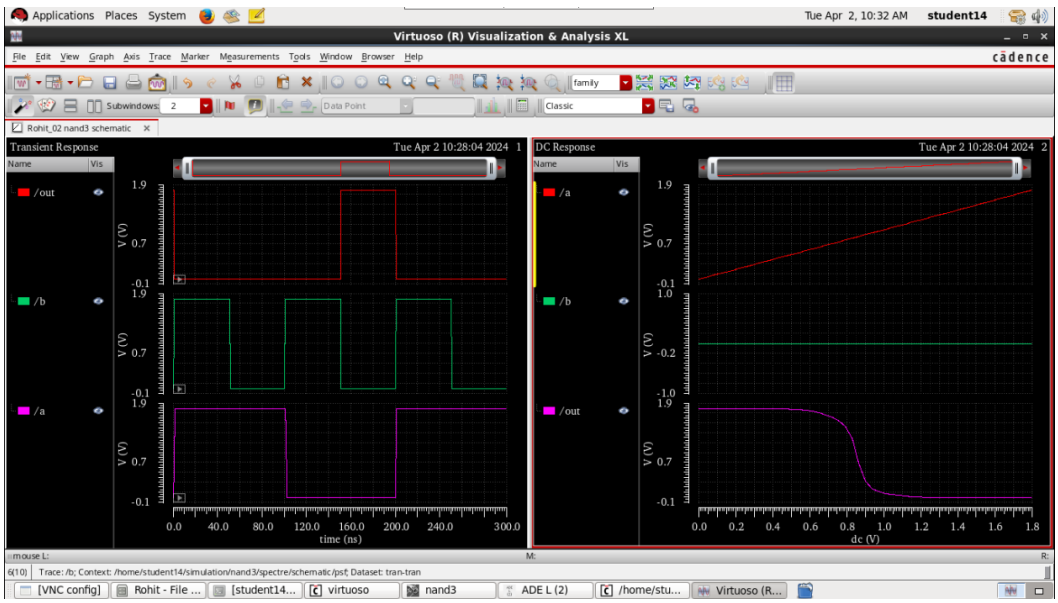
→ We'll verify the correctness of the schematic, symbol, layout by simulating the behaviour of the NOR gate using specialized CAD tools. We'll test the gate in both & real world conditions to ensure it operates as expected. We'll iterate on the design as necessary to address any issues or optimize performance.

→ We'll fabricate the NOR gate according to the finalized design files. We'll integrate the gate into larger systems or circuits as needed. We'll be performed quality assurance checks to verify that the manufactured gates meet the specified requirements.

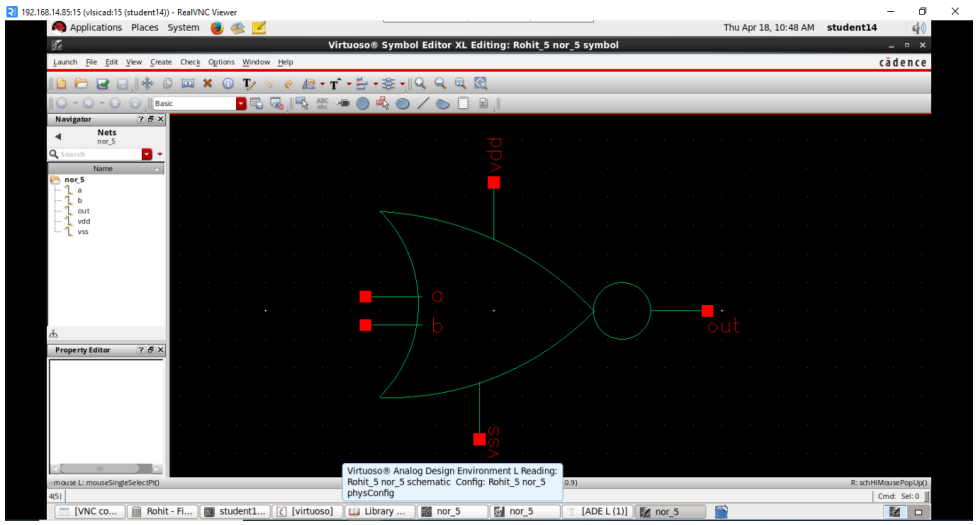
Schematic Draw NORx2



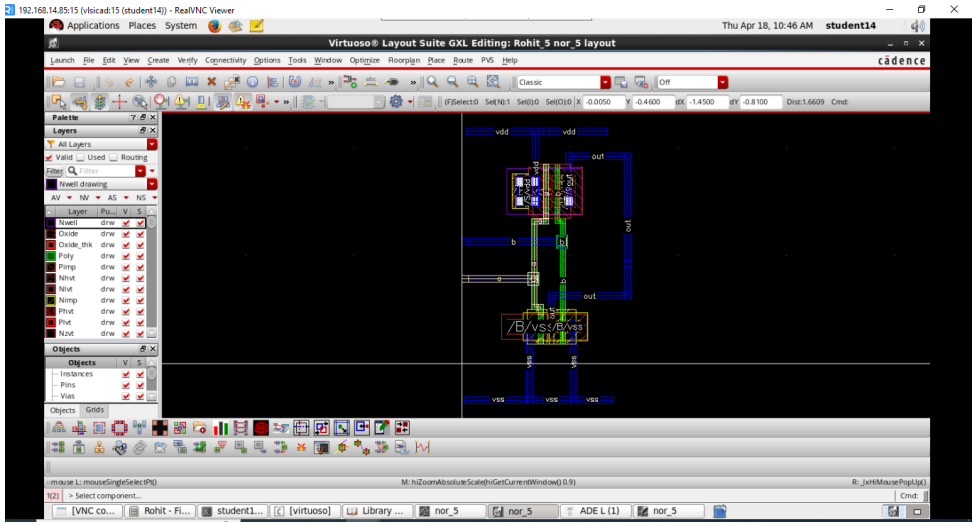
Signal Output



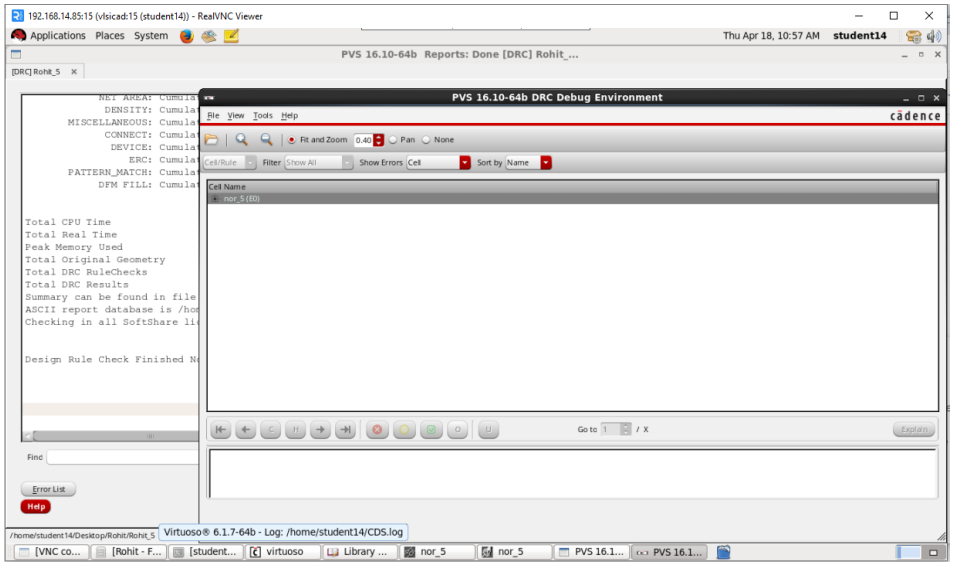
Symbol Draw



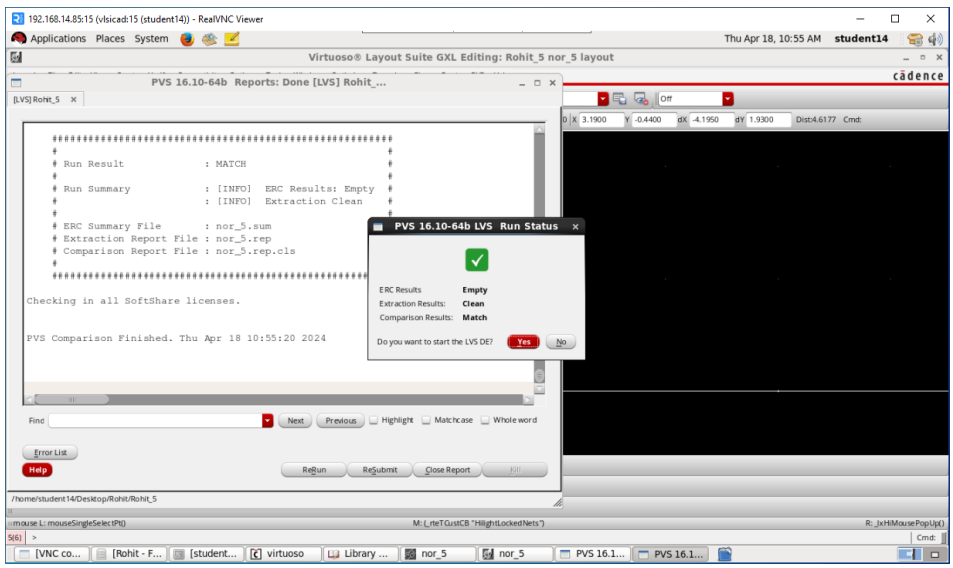
Layout



DRC RUN



LVS RUN



Description of the possible process steps of this 45nm NMOS device using the layers of the obtained layout individually in a sequential manner.

To elucidate the process steps involved in fabrication a 45nm NMOS device, it typically begins with substrate preparation, followed by a series of sequencial processes meticulously executed on individual layers obtained from the layer. The substrate undergoes cleaning & primming steps to ensure uniformly & purity. Next, the gate oxide layer is deposited & patterned to define the transistor's channel region. Subsequently the polysilicon layer is deposited & patterned to form the gate electrode. Dopant ions are implaned into the silicon substrate to create the source & drain regions. A dielectric layer is then deposited & etched to create contact openings for source, drain & gate electrodes. Metal layers are deposited & patterned to form interconnects, connecting various components of the NMOS device. Finally, a passivation layers is deposited to protect the device from external environmental factors. Each of these sequential steps, meticulously executed on individual layers derived from the layout, contributes to the preaise fabrication of the 45nm NMOS device, ensuring its functionality & performance

Comments about the 45Nm technology: The 45 nm technology represents a significant milestone in semiconductor fabrication. characterized by its miniaturization & enhanced performance capabilities. By shrinking the transistors size to 45nm, manufacturing achieve greater transistor density, enabling more functionality on a single chip while consuming less power. This technology facilitates the production of faster, more energy efficient electronic devices including processors

chips & integrated circuits, driving advantage in computing, communication & consumer electronics industries. The 45nm technology, has paved the way for further innovation & development in semiconductor manufacturing, serving as a foundation for further generation of even smaller & more powerful electronic devices.

Discussion: The process of generating a NOR gate with two inputs involves several key steps: first, creating a schematic diagram that outlines the logical connections between the inputs & the outputs. Next, a symbolic representation of the NOR gate is designed, typically featuring a triangle with a bubble at the output to denote the design. The physical layout of the gate is then generated, considering factors such as component placement, signal routing & optimization for performance metrics like power consumption & signal integrity. This layout is verified through simulation & testing to ensure functionality & adherence to design specification. Collaboration & adherence to standards are crucial throughout the process, from initial design to final fabrication & assembly, to ensure the successful implementation of the NOR gate in electronic systems.

Conclusion: In conclusion, the process of generating a NOR gate with two inputs involves designing a schematic representing the logical operation creating a symbol for easy representation in circuit diagram & laying out the physical components on a chip. This process requires meticulous attention to detail, adherence to design guildliness & throug verification through simulation & testing. By following these steps, designers can create NOR gate that meet the required specifications & integrate seamlessly into larger systems.