Indian Institute of Technology Kharagpur

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DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Computer Organization and Architecture Laboratory

Addendum: FPGA Implementation Guidelines for Processor Design

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Instructions: *This document provides the final, simplified guidelines for the FPGA demonstration part of Objective 3 of the main assignment,* ***"Experiment: Design and Synthesize a 32-bit Processor using Verilog"****. This instruction supersedes any previous addendum.*

Context and Objective

The main assignment requires you to design a full 32-bit RISC-like processor. Objective 3 specifically asks you to implement the register bank, integrate it with the ALU, and test operations of the form:

$$R_x = R_y \ \texttt{op} \ R_z$$

These guidelines detail a focused plan to demonstrate this 32-bit functionality on the Nexys 4 DDR FPGA board, which has limited physical I/O.

FPGA Task: Demonstrating the 32-bit Datapath

For the mandatory demonstration, you must implement your **complete 32-bit processor datapath** on the FPGA. To simplify the demonstration and focus on the core logic, the I/O requirements have been streamlined.

Key Implementation Requirements:

- **Full 32-bit Core:** The processor core implemented on the FPGA (ALU, Register File, buses) must be the same 32-bit version that you will submit to Moodle.
- **Pre-loaded Registers (No Switch Input):** To simplify the setup, you are **not** required to load data from the switches. Instead, you must **pre-load the general-purpose registers** with some non-trivial initial values directly within your Verilog code.
- **Switch-based Control:** The 16 switches are to be used exclusively for controlling the operation. You must devise a scheme to use the switches to select the instruction components.
  - **Choosing ALU Operations:** Your full design may support more than eight register-to-register ALU operations. To fit the opcode into 3 bits on the switches, you are required to select a representative subset of **eight** of these operations for the FPGA demonstration. You should choose a good mix to showcase your ALU's capability (e.g., 'ADD', 'SUB', 'AND', 'OR', 'XOR', 'SL', 'SRL', and 'SLT').
  - **Selecting Registers:** The remaining switches must be used to provide the addresses for the two source registers ('Ry', 'Rz') and the destination register ('Rx').

  A push-button should be used to trigger the execution of the selected instruction.

- **Simplified Instruction Set (for Demo Only):** Since you are not loading external data, you may **omit the implementation of immediate-addressing instructions** (like 'ADDI') for the FPGA demonstration.
- **Multiplexed Output for Testability:** To view the 32-bit result from a register, you must implement a multiplexed display. This is a common Design for Testability (DFT) technique used in industry to observe wide internal buses with limited physical pins. Use a dedicated switch to select whether the 16 LEDs display the **lower half (bits [15:0])** or the **upper half (bits [31:16])** of the result register.

Example Switch Configuration

To help you get started, here is a suggested mapping for the 16 switches. You are free to use a different mapping as long as it is logical and meets the requirements.

Table 1: Suggested Mapping of Switches to Control Signals

Switch(es)	Bits	Function
'SW[15]'	1	**DFT Display Select**: '0' for lower 16 bits, '1' for upper 16 bits.
'SW[14:12]'	3	**ALU Operation Select**: Selects one of your 8 chosen operations.
'SW[11:8]'	4	**Destination Register ('Rx') Address** (0000 to 1111 for R0-R15).
'SW[7:4]'	4	**Source Register 1 ('Ry') Address** (0000 to 1111 for R0-R15).
'SW[3:0]'	4	**Source Register 2 ('Rz') Address** (0000 to 1111 for R0-R15).

Submission and Evaluation Summary

Your design submission and the FPGA demonstration must both be based on the same 32-bit processor core.

Table 2: Deliverable Requirements

Component	Specification	Platform
Moodle Submission	**Full 32-bit Processor Design** (Complete Verilog source code, including all instructions, and a comprehensive testbench.)	**Simulation**
TA Demonstration	**Full 32-bit Processor Design** (With pre-loaded registers and a top-level DFT module for switch-based control and multiplexed output.)	**Nexys 4 DDR FPGA**