



GW1NR series of FPGA products

Package & Pinout User Guide

UG119-1.8.1E, 06/13/2025

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Revision History

Date	Version	Description
04/03/2018	1.04E	Initial version Published.
06/25/2018	1.05E	MG81 package info. Added.
09/13/2018	1.06E	The pins distribution view and package outline of MG81added.
12/12/2018	1.07E	<ul style="list-style-type: none"> ● LVDS pairs added in Table 2-1; ● Packages of the devices embedded with PSRAM added.
01/09/2019	1.08E	<ul style="list-style-type: none"> ● QN88 of GW1NR4 embedded with PSRAM added; ● View of pin distribution and I/O bank description updated.
07/09/2019	1.09E	The GW1NR-9 MG100 package added.
04/16/2020	1.1E	GW1NR-9c added.
05/18/2020	1.1.1E	GW1NR-9 MG100PF added.
06/12/2020	1.1.2E	GW1NR-9C revised to GW1NR-9.
06/30/2020	1.2E	GW1NR-1 added.
07/28/2020	1.3E	GW1NR-9 MG100PD added.
09/27/2020	1.4E	<ul style="list-style-type: none"> ● GW1NR-9 MG100PA, MG100PT, and MG100PS added; ● GW1NR-9 MG100PD removed.
02/02/2021	1.5E	GW1NR-2 MG49P/MG49PG/MG49G added.
10/26/2021	1.6E	GW1NR-1 EQ144G and QN48G added.
01/20/2022	1.7E	<ul style="list-style-type: none"> ● GW1NR-1 QN48X, LQ100G, and QN32X added; ● GW1NR-1 QN48G removed.
12/14/2023	1.7.1E	<ul style="list-style-type: none"> ● “Figure 3-7 View of GW1NR-9 QN88 Pins Distribution (Top View)” in “3.3 View of GW1NR-9 Pins Distribution” updated. ● “Figure 4-1 Package Outline QN88/QN88P” and the note in “4.1 QN88/QN88P Package Outline (10mm x 10mm)” updated. ● Recommended PCB Layout in “4 Package Diagrams” added.
10/25/2024	1.8E	<ul style="list-style-type: none"> ● All of the packages information for GW1NR-1 devices removed. ● The Max. user IO of FN32G/EQ144G/QN32X packages for GW1NR-1 devices, QN88/QN88P packages for GW1NR-4/9 devices, and LQ144P package for GW1NR-9 devices in “Table 2-1 Package and Max. User I/O Information, LVDS Pairs” updated. ● The description of “2.5 Introduction to the I/O BANK” optimized.
06/13/2025	1.8.1E	The LVDS and True LVDS output pairs of MG100P and MG100PF packages for GW1NR-9 devices in “Table 2-1 Package and Max. User I/O Information, LVDS Pairs” and “Table 2-6 Quantity of GW1NR-9 Pins” updated.

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1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW1NR series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The latest user guidelines are available on the GOWIN website at www.gowinsemi.com:

- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [UG290, Gowin FPGA Products Programming and Configuration User Guide](#)
- [UG805, GW1NR-2 Pinout](#)
- [UG116, GW1NR-4 Pinout](#)
- [UG803, GW1NR-9 Pinout](#)

1.3 Abbreviations and Terminology

The abbreviations and terminologies that are used in this manual are delineated in Table 1-1.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Full Name
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable IO
LQ	LQFP Package
MG	MBGA Package
PSRAM	Pseudo Static Random Access Memory
QN	QFN Package
SDRAM	Synchronous Dynamic RAM

Abbreviations and Terminology	Full Name
SIP	System in Package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The GW1NR series of FPGA Products are the 1 series products of GOWINSEMI LittleBee family. They are available in various forms that offer high I/O compatibility and flexible usage.

2.1 PB-Free Package

The GW1NR series of FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1NR series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package and Max. User I/O Information, LVDS Pairs

Package	Pitch(mm)	Size (mm)	GW1NR-2	GW1NR-4	GW1NR-9
MG49P	0.5	3.8 x 3.8	30 (8)	–	–
MG49PG	0.5	3.8 x 3.8	30 (8)	–	–
MG49G	0.5	3.8 x 3.8	30 (8)	–	–
QN88	0.4	10 x 10	–	71 (11)	71 (19)
QN88P	0.4	10 x 10	–	71 (11)	71 (18)
MG81P	0.5	4.5 x 4.5	–	68 (10)	–
MG100P	0.5	5 x 5	–	–	87 (17)
MG100PF ^[1]	0.5	5 x 5	–	–	87 (17)
MG100PA	0.5	5 x 5	–	–	87 (17)
MG100PT	0.5	5 x 5	–	–	87 (17)
MG100PS	0.5	5 x 5	–	–	87 (17)
LQ144P	0.5	20 x 20	–	–	121 (20)

Note!

- ^[1] MG100PF: The pinout of ball C1/C2/D2/F1/F9/A7/A6 adjusted on the basis of MG100P.
- In this manual, abbreviations are employed to refer to the package types. See [1.3 Abbreviations and Terminology](#).

- See GW1NR series Pinouts for more details.
- The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously.

2.3 Power Pin

Table 2-2 Other Pins in the GW1NR Series

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCX	VSS	NC

2.4 Pin Quantity

2.4.1 Quantity of GW1NR-2 Pins

Table 2-3 Quantity of GW1NR-2 Pins

Pin Type		GW1NR-2		
		MG49P	MG49PG	MG49G
I/O Single end/Differential pair/LVDS ^[1]	BANK0	14/7/4	14/7/4	14/7/4
	BANK1	0/0/0	0/0/0	0/0/0
	BANK2	8/4/2	8/4/2	8/4/2
	BANK3	4/2/1	4/2/1	4/2/1
	BANK4	4/2/1	4/2/1	4/2/1
	BANK5	0/0/0	0/0/0	0/0/0
	BANK6	10/5/0	10/5/0	10/5/0
Max. User I/O ^[2]		40	40	40
Differential Pair		20	20	20
True LVDS output		8	8	8
VCC		1	1	1
VCCX		1	1	1
VCCIO0		1	1	1
VCCIO1		1	1	1
VCCIO2/VCCIO3/VCCIO4/VCCIO5 ^[3]		1	1	1
VCCD		1	1	1
VCCIOD		1	1	1
VSS		2	2	2
MODE0		0	0	0
MODE1		0	0	0
MODE2		0	0	0
JTAGSEL_N		0	0	0

Note!

- ^[1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins.
- ^[2] The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as

- I/O.
^[3] Pin multiplexing.

2.4.2 Quantity of GW1NR-4 Pins

Table 2-4 Quantity of GW1NR-4 Pins (SDRAM embedded)

Pin Type		GW1NR-4
		QN88
I/O Single end/Differential pair/LVDS ^[1]	BANK0	20/5/0
	BANK1	15/6/2
	BANK2	23/9/7
	BANK3	12/4/2
Max. User I/O ^[2]		70
Differential Pair		24
True LVDS output		11
VCC		4
VCCX		0
VCCIO0		0
VCCIO1		1
VCCIO2		2
VCCIO3		1
VCCX/VCCIO0 ^[3]		3
VSS		6
MODE0		1
MODE1		1
MODE2		0
JTAGSEL_N		1

Table 2-5 Quantity of GW1NR-4 Pins (PSRAM embedded)

Pin Type		GW1NR-4	
		MG81P	QN88P
I/O Single end/Differential pair/LVDS ^[1]	BANK0	13/6/0	20/5/0
	BANK1	17/3/0	15/6/2
	BANK2	21/10/10	23/9/7
	BANK3	17/2/0	12/4/2
Max. User I/O ^[2]		68	70
Differential Pair		21	24
True LVDS output		10	11
VCC		3	4
VCCX		1	0
VCCIO0		1	0
VCCIO1		1	1

Pin Type	GW1NR-4	
	MG81P	QN88P
VCCIO2	1	2
VCCIO3	1	1
VCCX/VCCIO0 ^[3]	0	3
VSS	4	6
MODE0	0	1
MODE1	1	1
MODE2	0	0
JTAGSEL_N	1	1

Note!

- ^[1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins.
- ^[2] The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O.
- ^[3] Pin multiplexing.

2.4.3 Quantity of GW1NR-9 Pins

Table 2-6 Quantity of GW1NR-9 Pins

Pin Type		GW1NR-9							
		QN88	QN88P	LQ144P	MG100P	MG100PF	MG100PA	MG100PT	MG100PS
I/O Single end/Differential pair/LVDS ^[1]	BANK0	0/0/0	0/0/0	18/9/0	12/6/0	12/6/0	12/6/0	12/6/0	12/6/0
	BANK1	25/11/4	25/11/4	32/12/4	22/5/1	22/6/1	22/6/1	22/5/1	22/6/1
	BANK2	23/11/11	23/11/11	40/19/14	32/15/14	32/15/14	32/15/14	32/15/14	32/15/14
	BANK3	22/8/4	22/6/3	30/8/2	21/4/2	21/6/2	21/6/2	21/4/2	21/6/2
Max. User I/O ^[2]		70	70	120	87	87	87	87	87
Differential Pair		30	28	48	30	33	33	30	33
True LVDS output		19	18	20	17	17	17	17	17
VCC		4	4	4	3	3	3	3	3
VCCX		0	0	2	1	1	1	1	1
VCCIO0		0	0	2	1	1	1	1	1
VCCIO1		1	1	2	1	1	1	1	1
VCCIO2		2	2	2	1	1	1	1	1
VCCIO3		1	1	2	1	1	1	1	1
VCCX/VCCIO0 ^[3]		3	3	0	0	0	0	0	0
VSS		6	6	9	4	4	4	4	4
MODE0		1	1	1	0	0	0	0	0
MODE1		1	1	1	1	1	1	1	1
MODE2		0	0	0	0	0	0	0	0
JTAGSEL_N		1	1	1	1	1	1	1	1

Note!

- ^[1] Quantity of single end/ differential/LVDS I/O include CLK pins, and download pins.
- ^[2] The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O.
- ^[3] Pin multiplexing.











2.5 Introduction to the I/O BANK

GW1NR-4/9 includes four I/O Banks.

GW1NR-2 MG49P/MG49PG/MG49G includes seven I/O Banks.

This manual provides an overview of the distribution view of the pins in the GW1NR series of FPGA products. Please refer to [3 View of Pin Distribution > 2.4 Input/Output Blocks](#) for further details. Different IO Banks in the GW1NR series FPGA products are marked with different colors.

User I/O, power, and ground are also marked with different symbols and colors. The various symbols and colors used for the various pins are defined as follows:

-  denotes I/Os in BANK0.
-  denotes I/Os in BANK1.
-  denotes I/Os in BANK2.
-  denotes I/Os in BANK3.
-  denotes I/Os in BANK4.
-  denotes I/Os in BANK5.
-  denotes I/Os in BANK6 and DIOs in MIPI.
-  denotes VCC, VCCX, and VCCIO. The filling color does not change.
-  denotes VCC. The filling color does not change.
-  denotes NC.

3 View of Pin Distribution

3.1 View of GW1NR-2 Pins Distribution

3.1.1 View of MG49P Pins Distribution (PSRAM Embedded)

Figure 3-1 View of GW1NR-2 MG49P Pins Distribution (Top View, PSRAM Embedded)

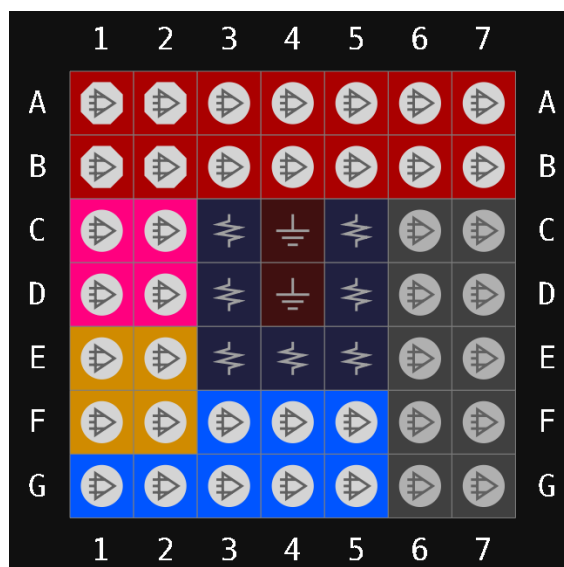


Table 3-1 Other pins in GW1NR-2 MG49P (PSRAM Embedded)

VCC	C3
VCCD	E4
VCCIOD	E5
VCCIO0	C5
VCCIO1	D5
VCCIO2/VCCIO3/VCCIO4/VCCIO5	D3
VCCX	E3
VSS	C4,D4

3.1.2 View of MG49PG Pins Distribution (PSRAM and Flash Embedded)

Figure 3-2 View of GW1NR-2 MG49PG Pins Distribution (Top View, PSRAM and Flash Embedded)

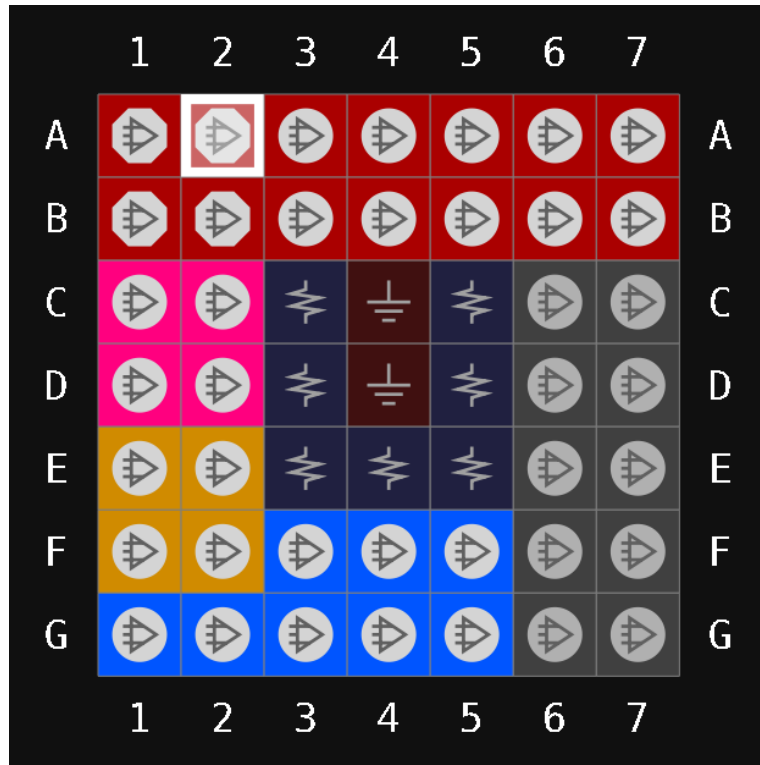


Table 3-2 Other pins in GW1NR-2 MG49PG (PSRAM and Flash Embedded)

VCC	C3
VCCD	E4
VCCIOD	E5
VCCIO0	C5
VCCIO1	D5
VCCIO2/VCCIO3/VCCIO4/VCCIO5	D3
VCCX	E3
VSS	C4,D4

3.1.3 View of MG49G Pins Distribution (Flash Embedded)

Figure 3-3 View of GW1NR-2 MG49G Pins Distribution (Top View, Flash Embedded)

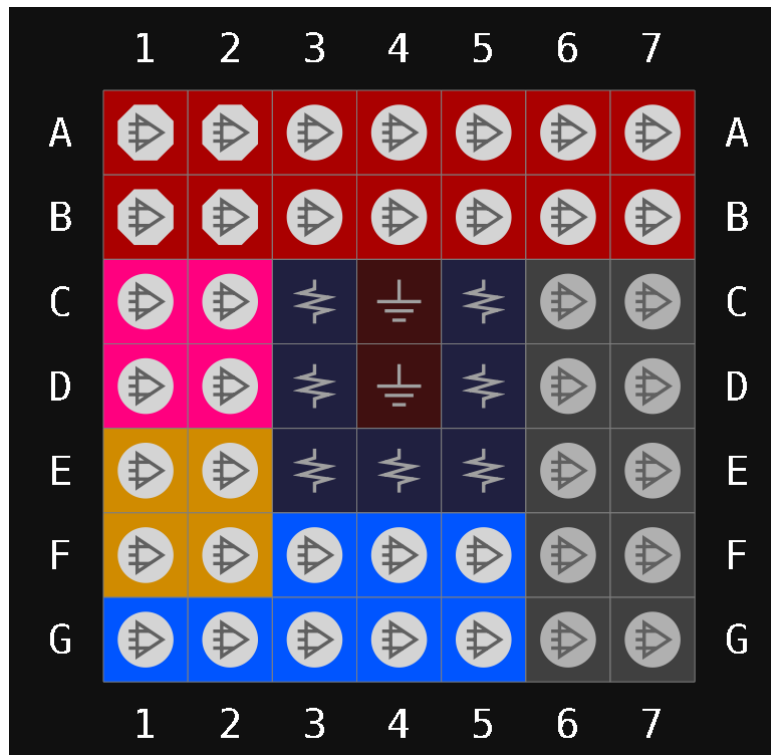


Table 3-3 Other pins in GW1NR-2 MG49G (Flash Embedded)

VCC	C3
VCCD	E4
VCCIOD	E5
VCCIO0	C5
VCCIO1	D5
VCCIO2/VCCIO3/VCCIO4/VCCIO5	D3
VCCX	E3
VSS	C4,D4

3.2 View of GW1NR-4 Pins Distribution

3.2.1 View of MG81P Pins Distribution (PSRAM Embedded)

Figure 3-4 View of GW1NR-4 MG81P Pins Distribution (Top View, PSRAM Embedded)

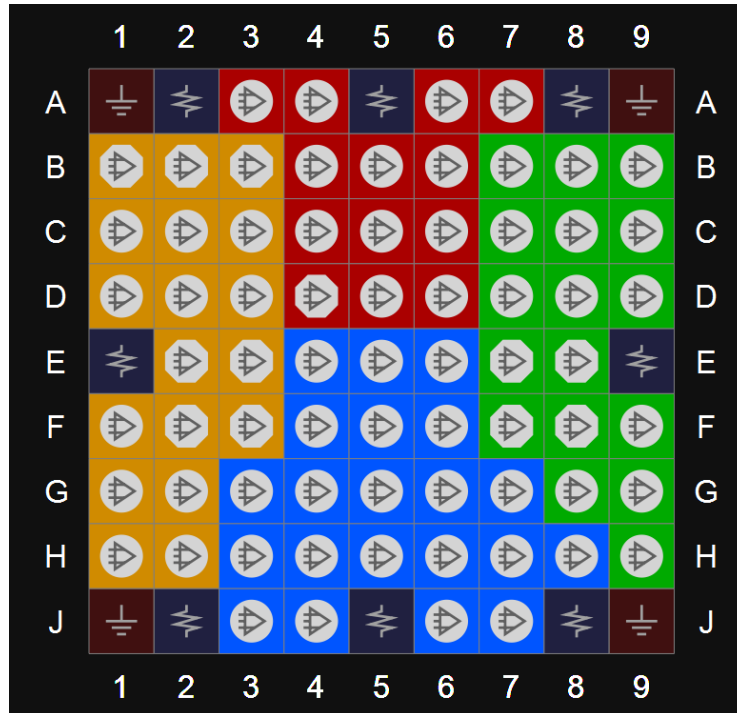


Table 3-4 Other pins in GW1NR-4 MG81P (PSRAM Embedded)

VCC	A2, A8, J2
VCCX	J8
VCCIO0	A5
VCCIO1	E9
VCCIO2	J5
VCCIO3	E1
VSS	A1, A9, J1, J9

3.2.2 View of QN88P Pins Distribution (PSRAM Embedded)

Figure 3-5 View of GW1NR-4 QN88P Pins Distribution (Top View, PSRAM Embedded)



Table 3-5 Other pins in GW1NR-4 QN88P (PSRAM Embedded)

VCC	1, 22, 45, 66
VCCX/VCCIO0	64, 67, 78
VCCIO1	58
VCCIO2	23, 44
VCCIO3	12
VSS	2, 21, 24, 43, 46, 65

3.2.3 View of QN88 Pins Distribution (SDRAM Embedded)

Figure 3-6 View of GW1NR-4 QN88 Pins Distribution (Top View, SDRAM Embedded)

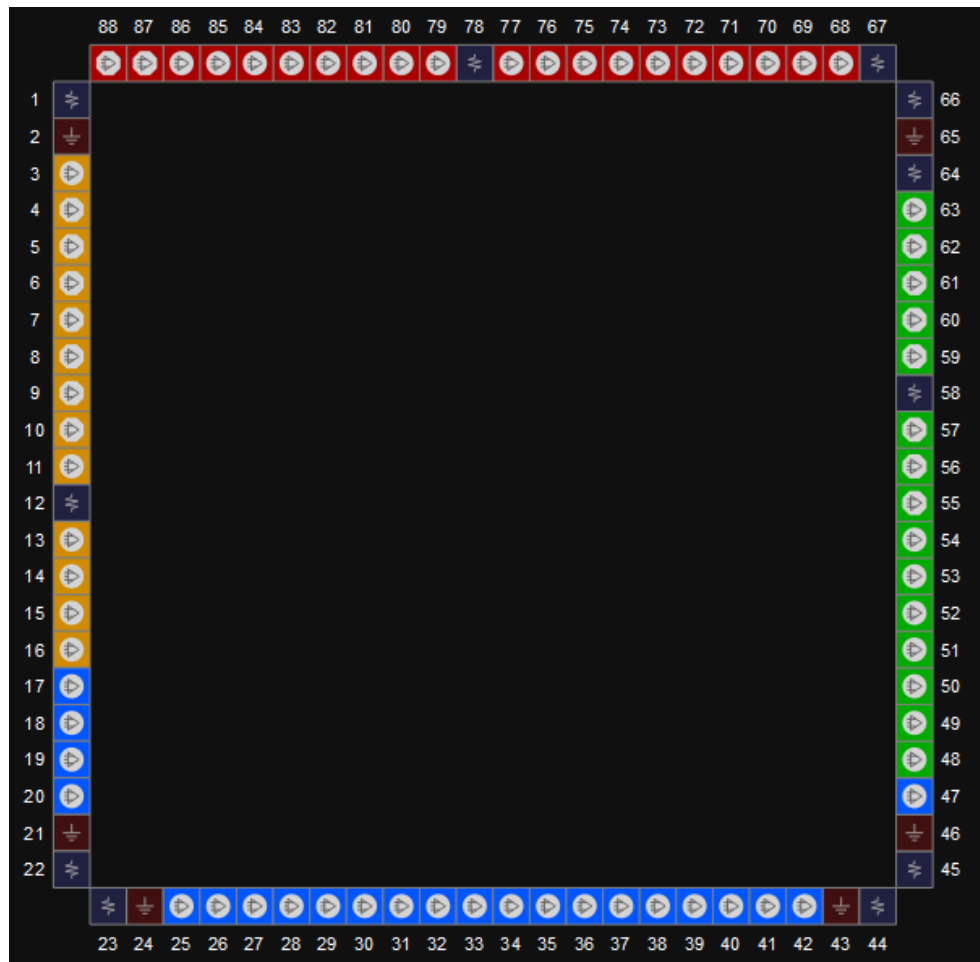


Table 3-6 Other pins in GW1NR-4 QN88 (SDRAM Embedded)

VCC	1, 22, 45, 66
VCCX/VCCIO0	64, 67, 78
VCCIO1	58
VCCIO2	23, 44
VCCIO3	12
VSS	2, 21, 24, 43, 46, 65

3.3 View of GW1NR-9 Pins Distribution

3.3.1 View of QN88 Pins Distribution

Figure 3-7 View of GW1NR-9 QN88 Pins Distribution (Top View)

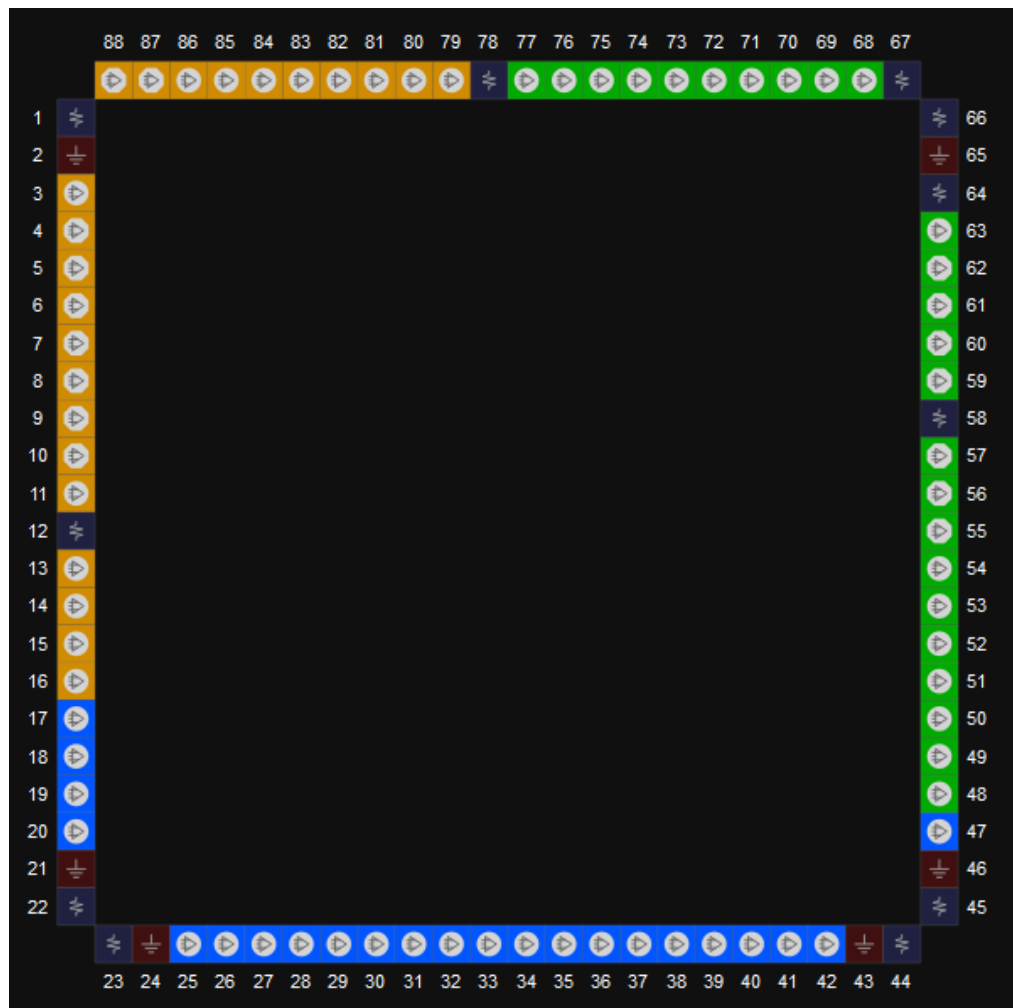


Table 3-7 Other pins in GW1NR-9 QN88

VCC	1, 22, 45, 66
VCCX/VCCIO0	64, 67, 78
VCCIO1	58
VCCIO2	23, 44
VCCIO3	12
MODE	87, 88
VSS	2, 21, 24, 43, 46, 65

3.3.2 View of QN88P Pins Distribution

Figure 3-8 View of GW1NR-9 QN88P Pins Distribution (Top View)

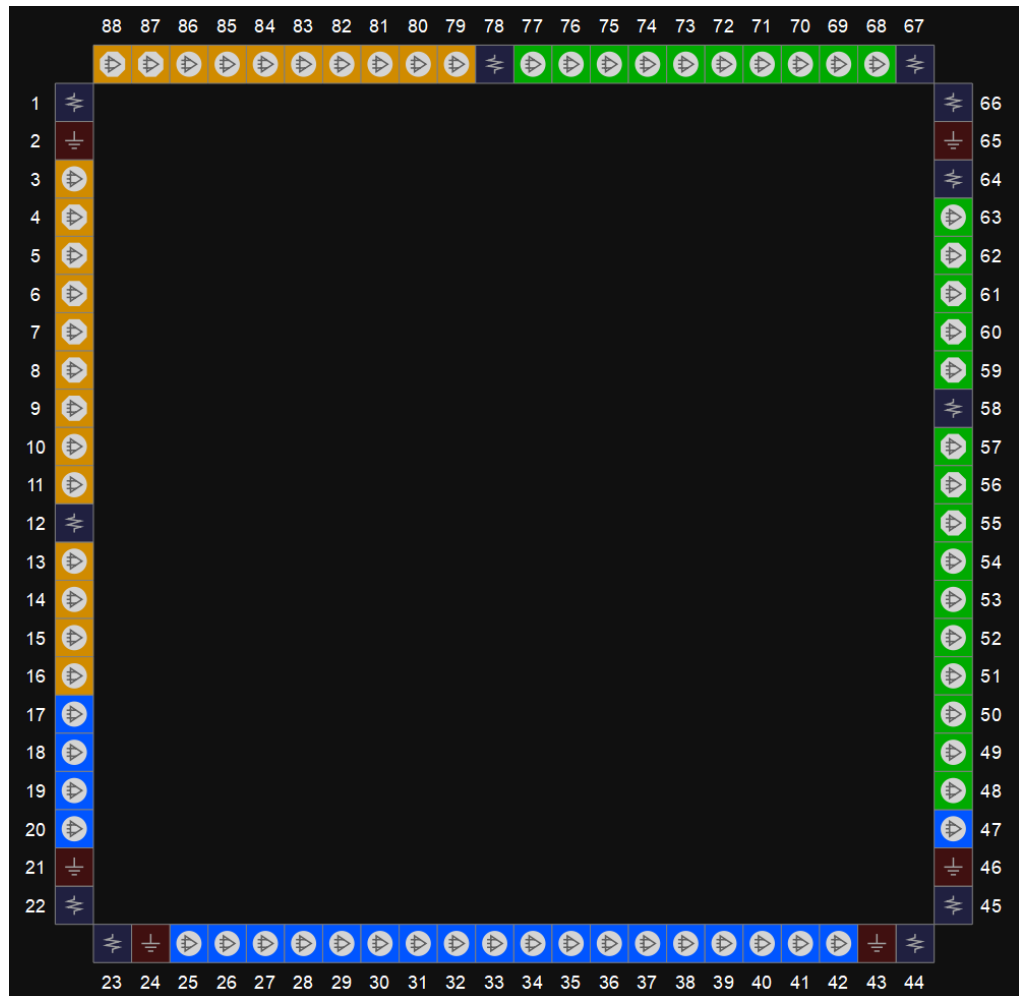


Table 3-8 Other pins in GW1NR-9 QN88P

VCC	1, 22, 45, 66
VCCX/VCCIO0	64, 67, 78
VCCIO1	58
VCCIO2	23, 44
VCCIO3	12
MODE	87, 88
VSS	2, 21, 24, 43, 46, 65

3.3.3 View of MG100P Pins Distribution

Figure 3-9 View of GW1NR-9 MG100P Pins Distribution (Top View)

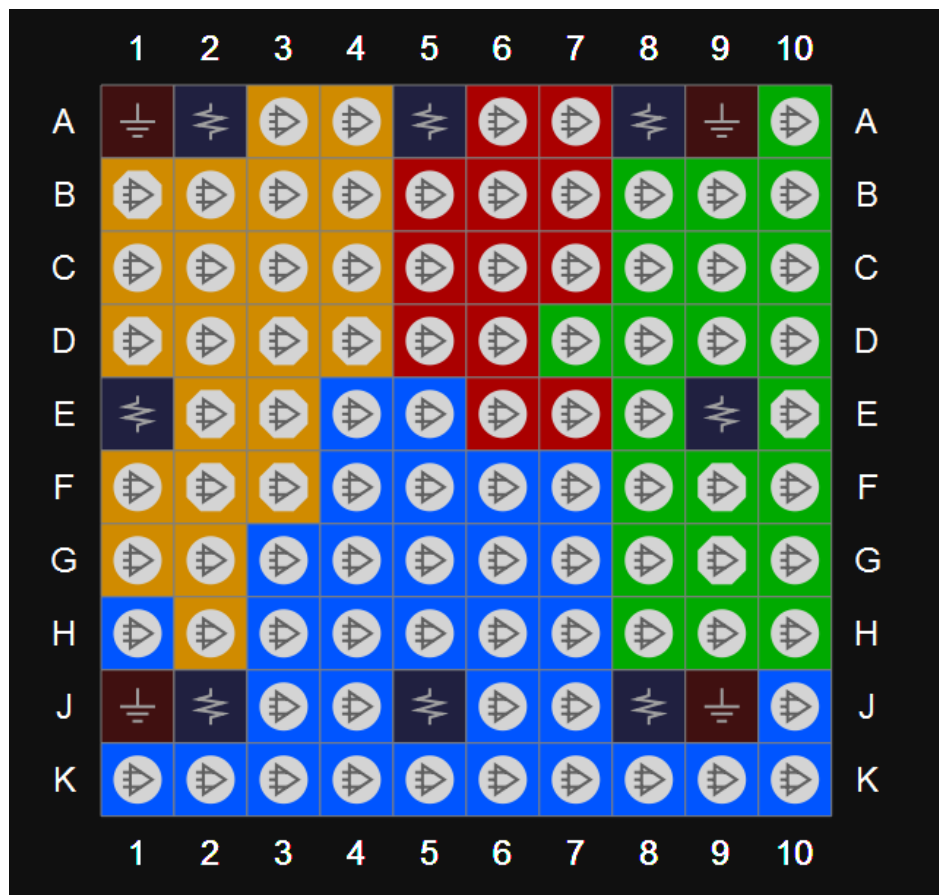


Table 3-9 Other pins in GW1NR-9 MG100P

VCC	A2,J2,A8
VCCIO0	A5
VCCIO1	E9
VCCIO2	J5
VCCIO3	E1
VCCX	J8
MODE	D4
VSS	A1,A9,J1,J9

3.3.4 View of MG100PF Pins Distribution

Figure 3-10 View of GW1NR-9 MG100PF Pins Distribution (Top View)

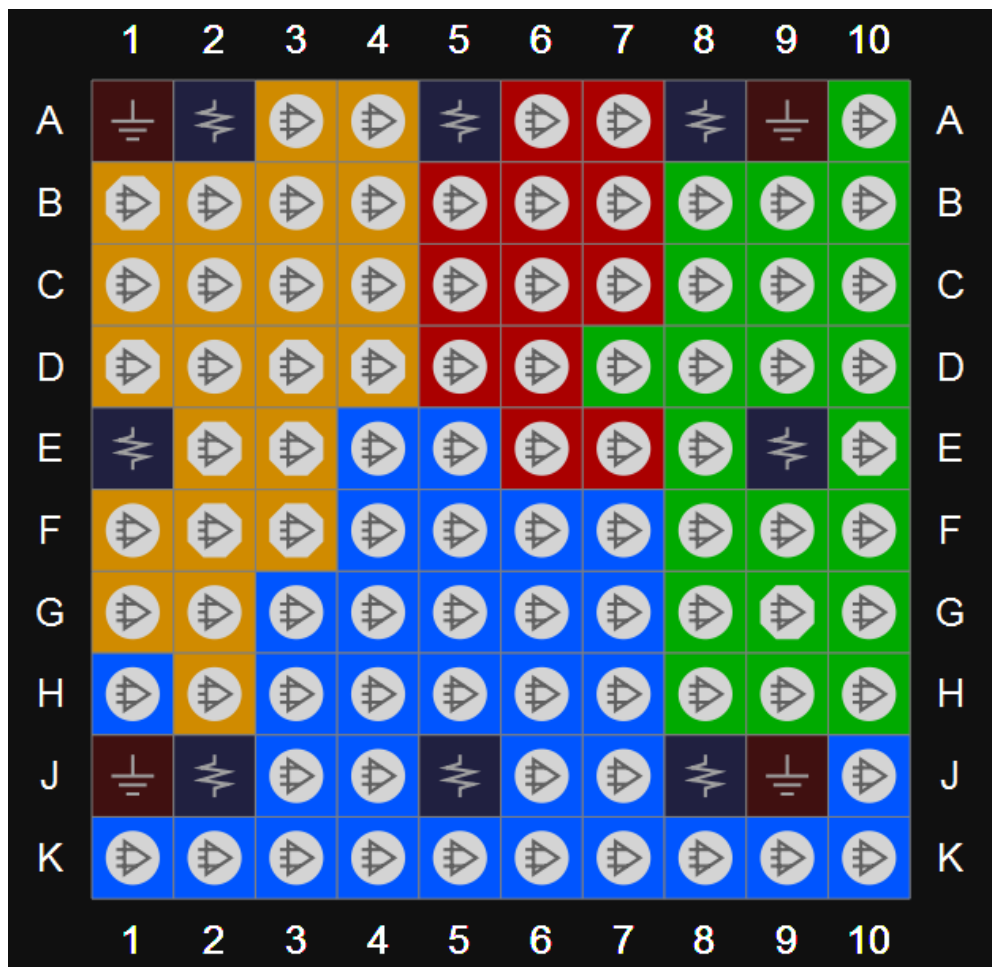


Table 3-10 Other pins in GW1NR-9 MG100PF

VCC	A2,J2,A8
VCCIO0	A5
VCCIO1	E9
VCCIO2	J5
VCCIO3	E1
VCCX	J8
MODE	D4
VSS	A1,A9,J1,J9

3.3.5 View of LQ144P Pins Distribution

Figure 3-11 View of GW1NR-9 LQ144P Pins Distribution (Top View)



Table 3-11 Other pins in GW1NR-9 LQ144P

VCC	1, 36, 73, 108
VCCIO0	109, 127
VCCIO1	91, 103
VCCIO2	37, 55
VCCIO3	9, 19
VCCX	31, 77
MODE	143, 144
VSS	2, 17, 33, 35, 53, 74, 89, 105, 107

3.3.6 View of MG100PA Pins Distribution

Figure 3-12 View of GW1NR-9 MG100PA Pins Distribution (Top View)

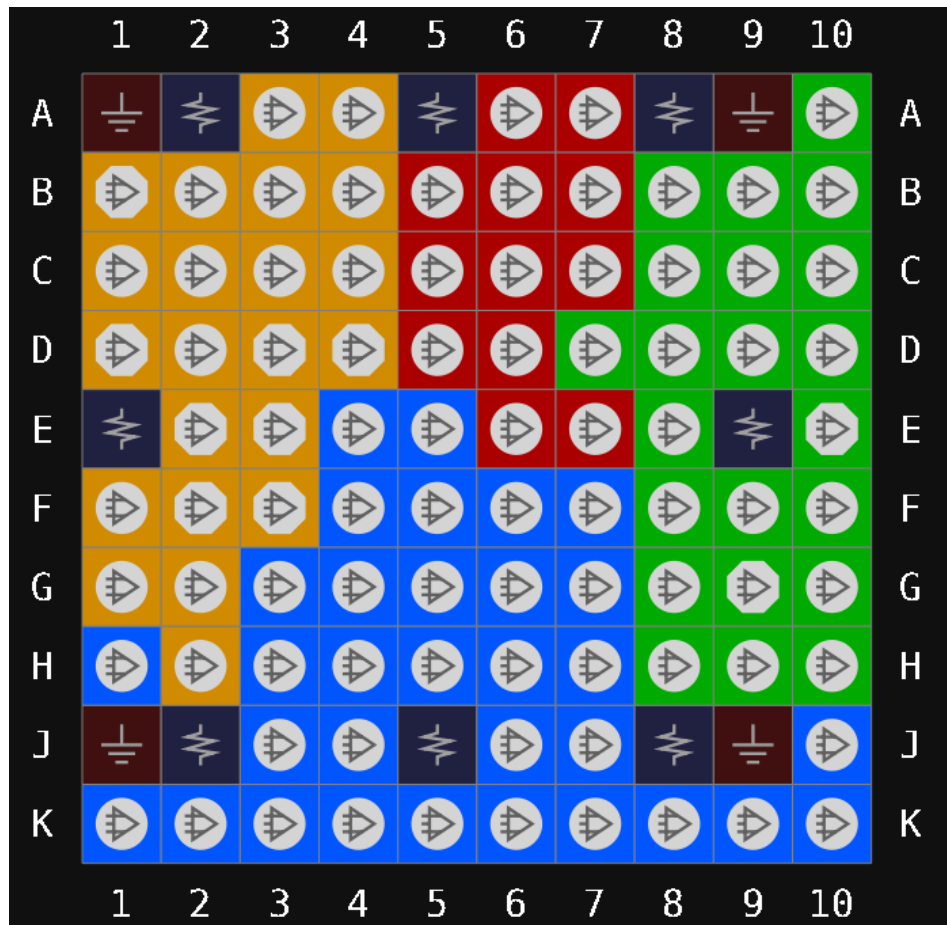


Table 3-12 Other pins in GW1NR-9 MG100PA

VCC	A2,J2,A8
VCCIO0	A5
VCCIO1	E9
VCCIO2	J5
VCCIO3	E1
VCCX	J8
MODE	D4
VSS	A1,A9,J1,J9

3.3.7 View of MG100PS Pins Distribution

Figure 3-13 View of GW1NR-9 MG100PS Pins Distribution (Top View)

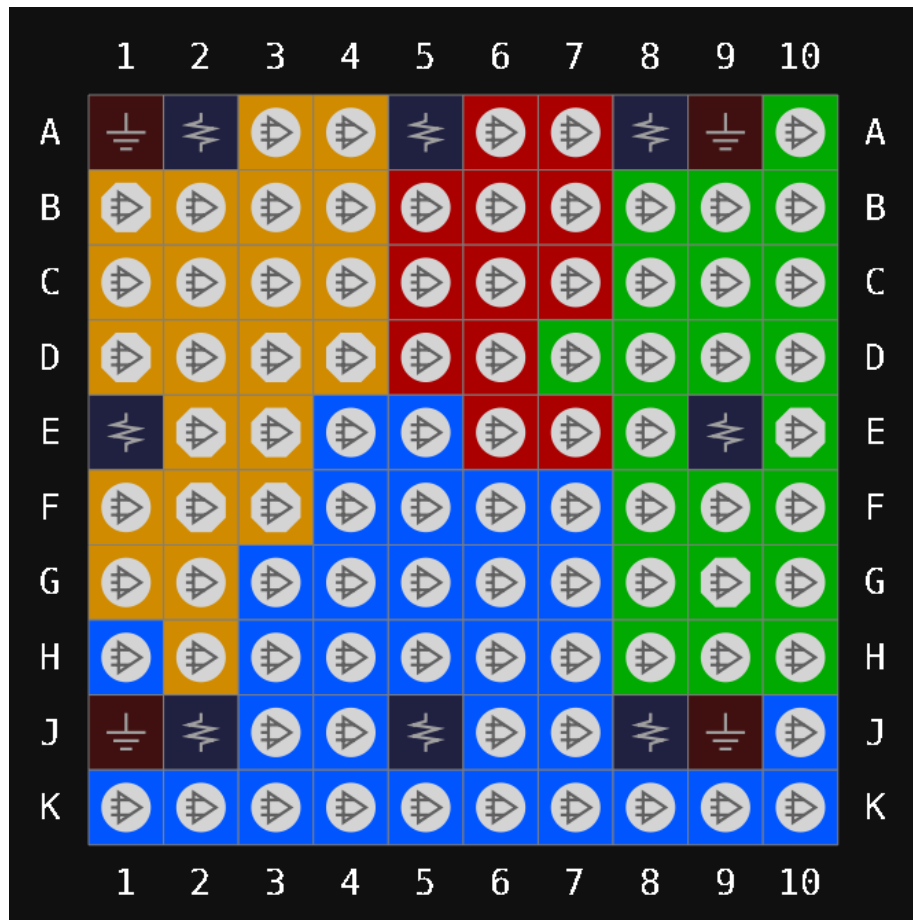


Table 3-13 Other pins in GW1NR-9 MG100PS

VCC	A2,A8,J2
VCCIO0	A5
VCCIO1	E9
VCCIO2	J5
VCCIO3	E1
VCCX	J8
MODE	D4
VSS	A1,A9,J1,J9

3.3.8 View of MG100PT Pins Distribution

Figure 3-14 View of GW1NR-9 MG100PT Pins Distribution (Top View)

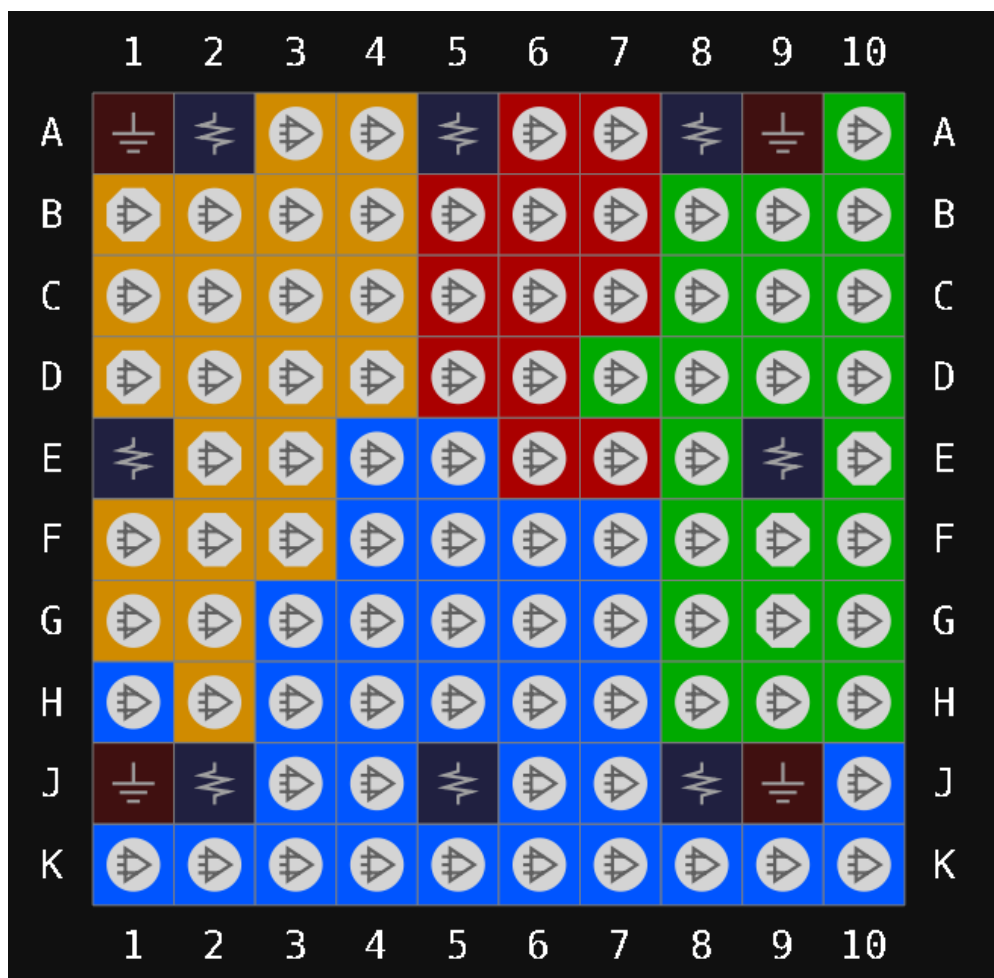


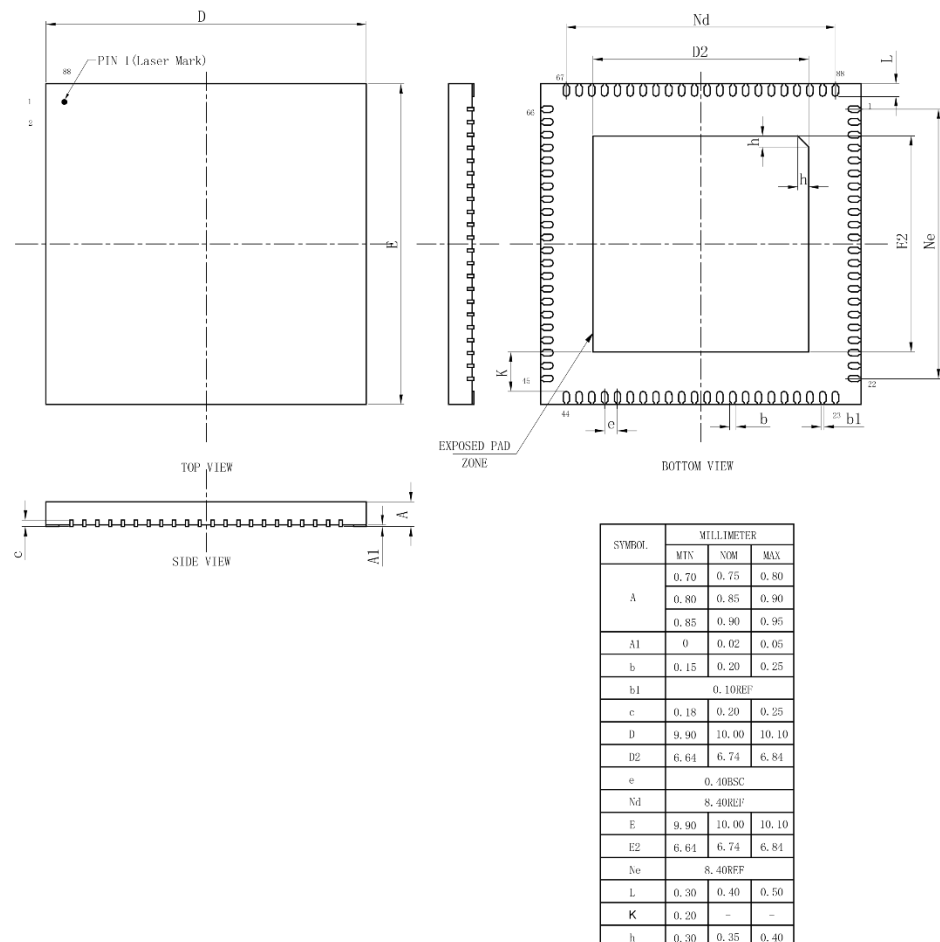
Table 3-14 Other pins in GW1NR-9 MG100PT

VCC	A2,A8,J2
VCCIO0	A5
VCCIO1	E9
VCCIO2	J5
VCCIO3	E1
VCCX	J8
MODE	D4
VSS	A1,A9,J1,J9

4 Package Diagrams

4.1 QN88/QN88P Package Outline (10mm x 10mm)

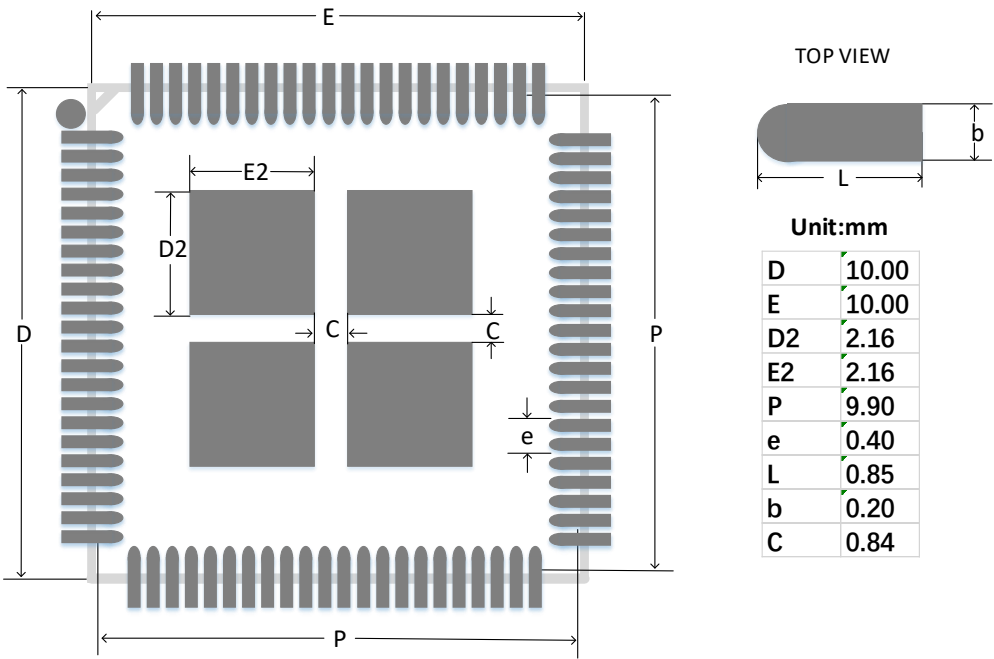
Figure 4-1 Package Outline QN88/QN88P



注!

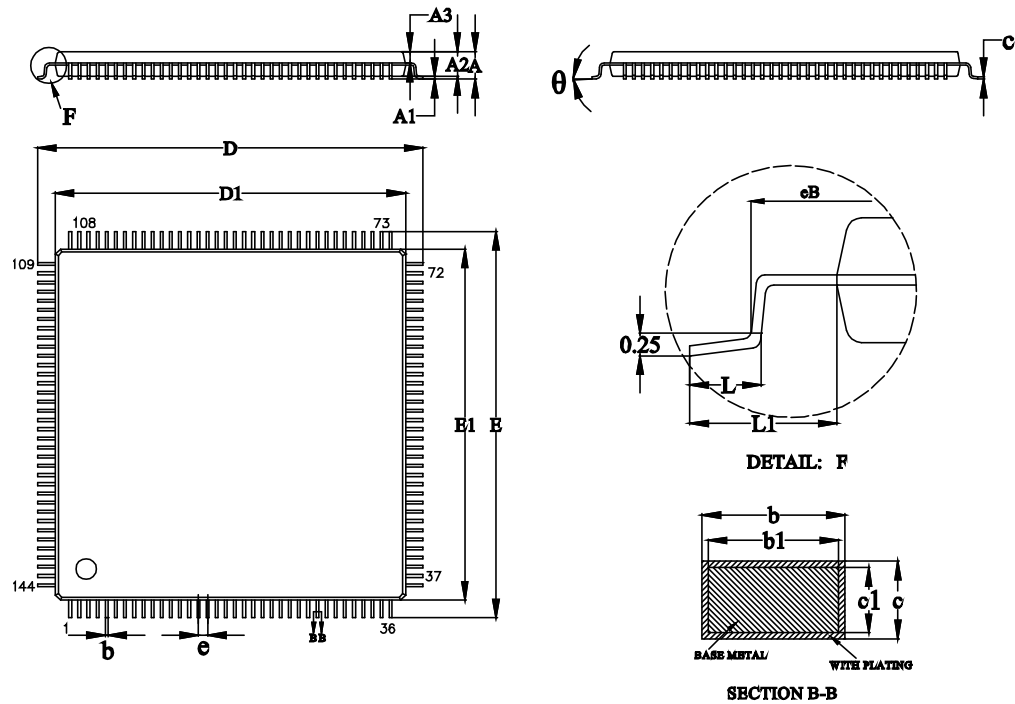
- For GW1NR-LV4QN88, GW1NR-UV4QN88, and GW1NR-LV9QN88, the value of A(NOM) is 0.85mm.
- For GW1NR-LV4QN88P, GW1NR-UV4QN88P, GW1NR-LV9QN88P, and GW1NR-UV9QN88P, the value of A(NOM) is 0.75mm.

Figure 4-2 Recommended PCB Layout QN88/QN88P



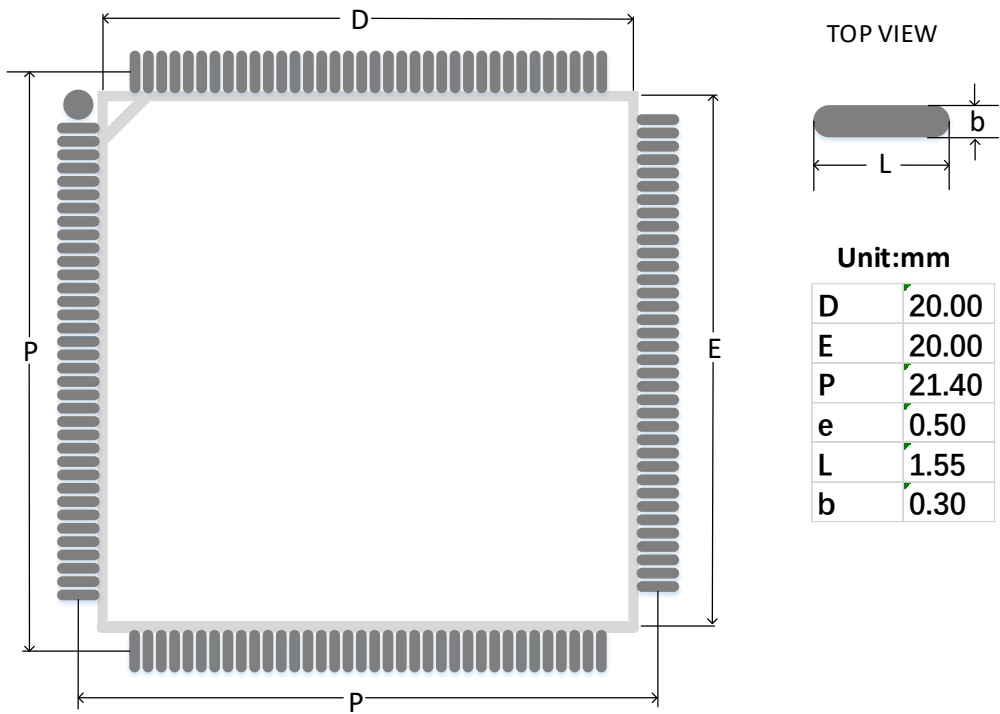
4.2 LQ144/LQ144P Package Outline (20mm x 20mm)

Figure 4-3 Package Outline LQ144/LQ144P



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 4-4 Recommended PCB Layout LQ144/LQ144P



4.3 MG49P/MG49PG/MG49G Package Outline (3.8mm x 3.8mm)

Figure 4-5 Package Outline MG49P/ MG49PG/MG49G

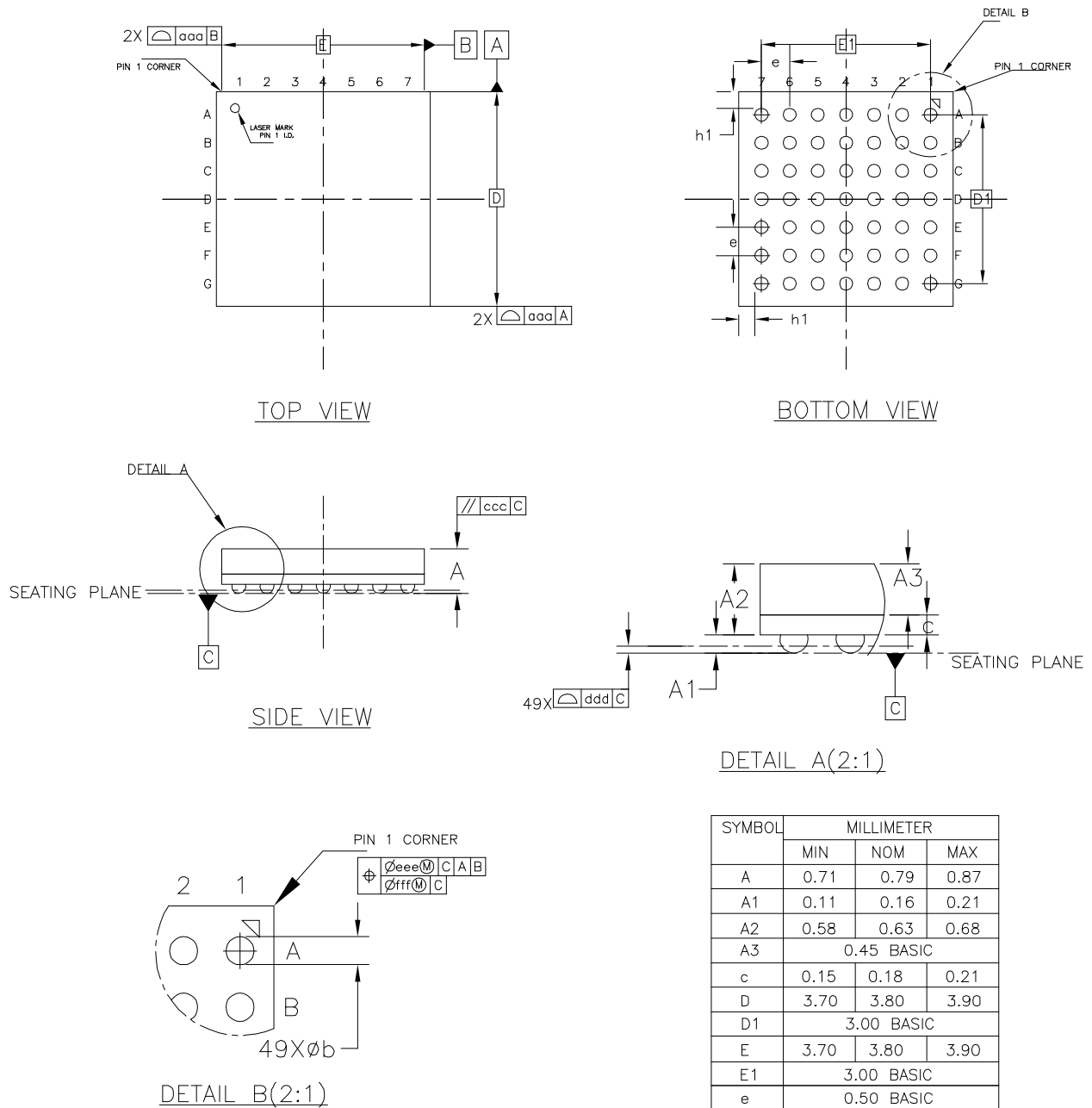
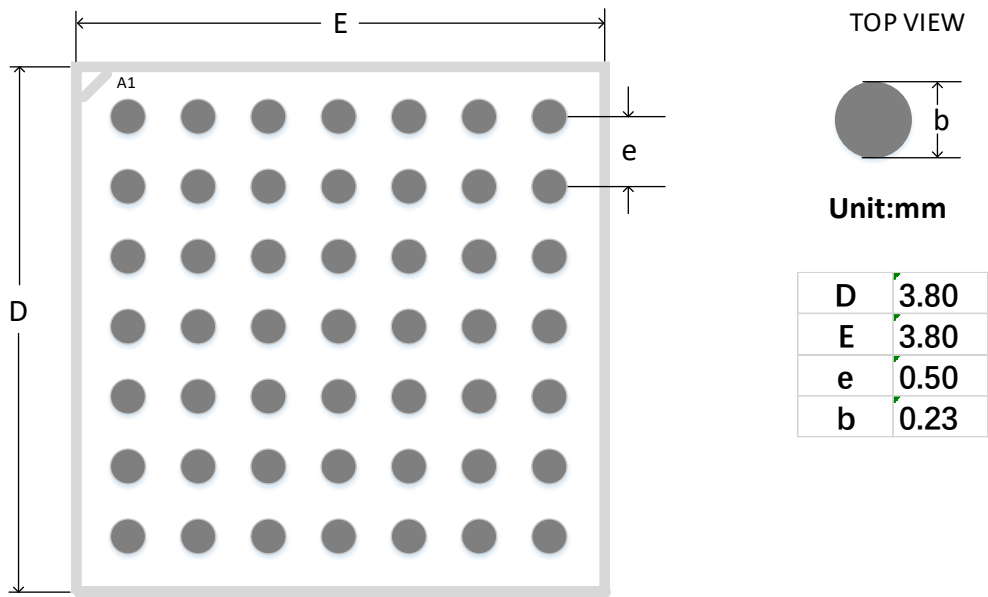
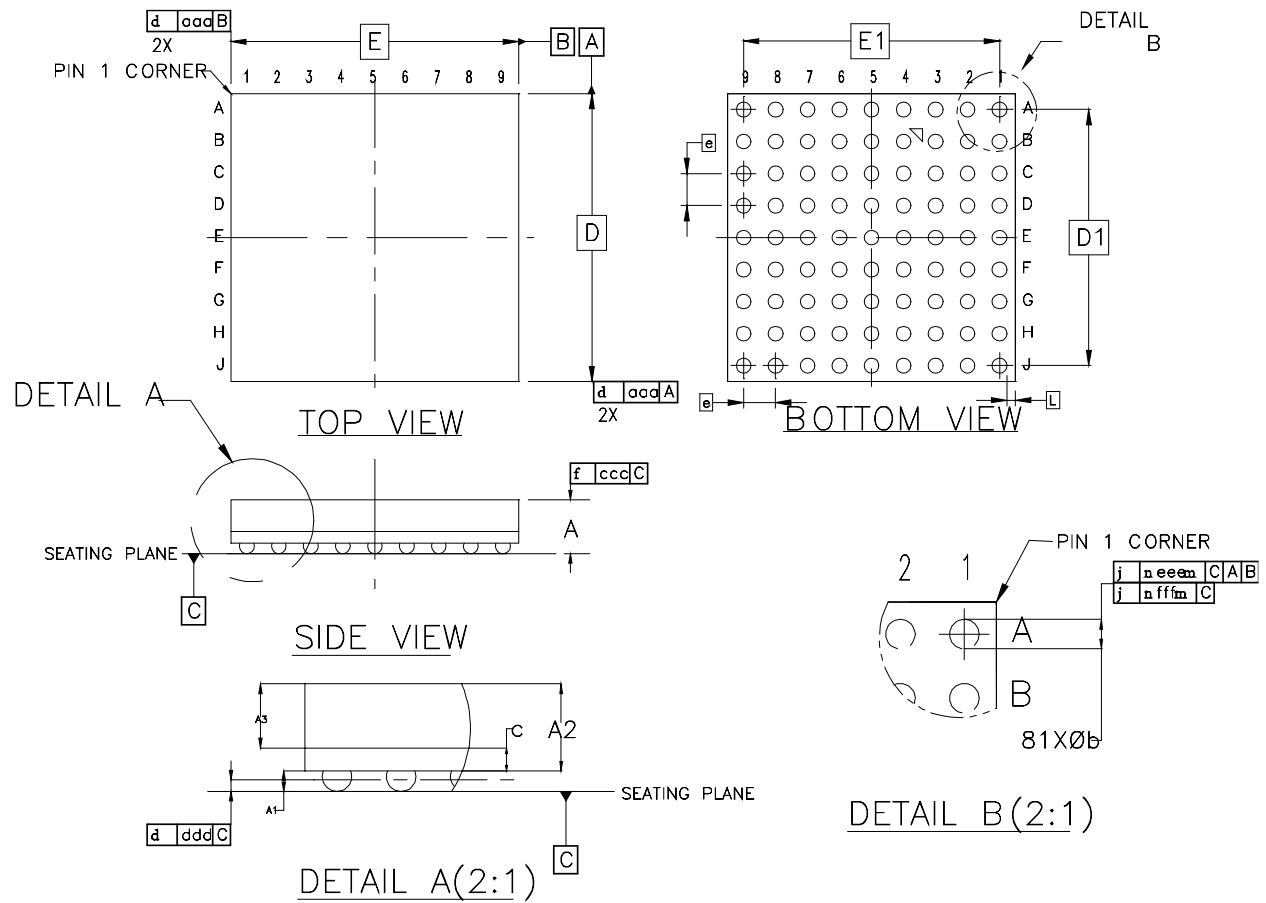


Figure 4-6 Recommended PCB Layout MG49P/MG49PG/MG49G



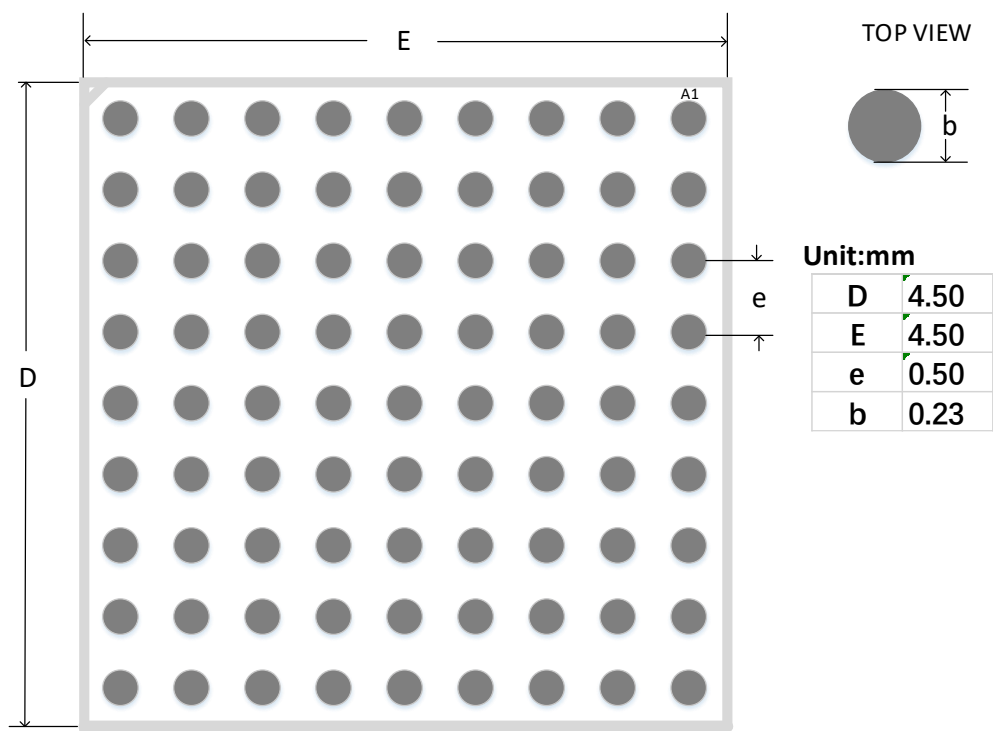
4.4 MG81P Package Outline (4.5mm x 4.5mm)

Figure 4-7 Package Outline MG81P



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	0.84	0.90
A1	0.11	0.16	0.21
A2	0.63	0.68	0.73
A3	0.50 BASIC		
c	0.15	0.18	0.21
D	4.40	4.50	4.60
D1	4.00 BASIC		
E	4.40	4.50	4.60
E1	4.00 BASIC		
e	0.50 BASIC		
b	0.18	0.23	0.28
L	0.135 TYP		
aaa	0.10		
ccc	0.15		
ddd	0.10		
eee	0.15		
fff	0.05		

Figure 4-8 Recommended PCB Layout MG81P



4.5 MG100P/MG100PF/MG100PA/MG100PT MG100PS Package Outline (5mm x 5mm)

Figure 4-9 Package Outline MG100P/MG100PF/MG100PA/ MG100PT

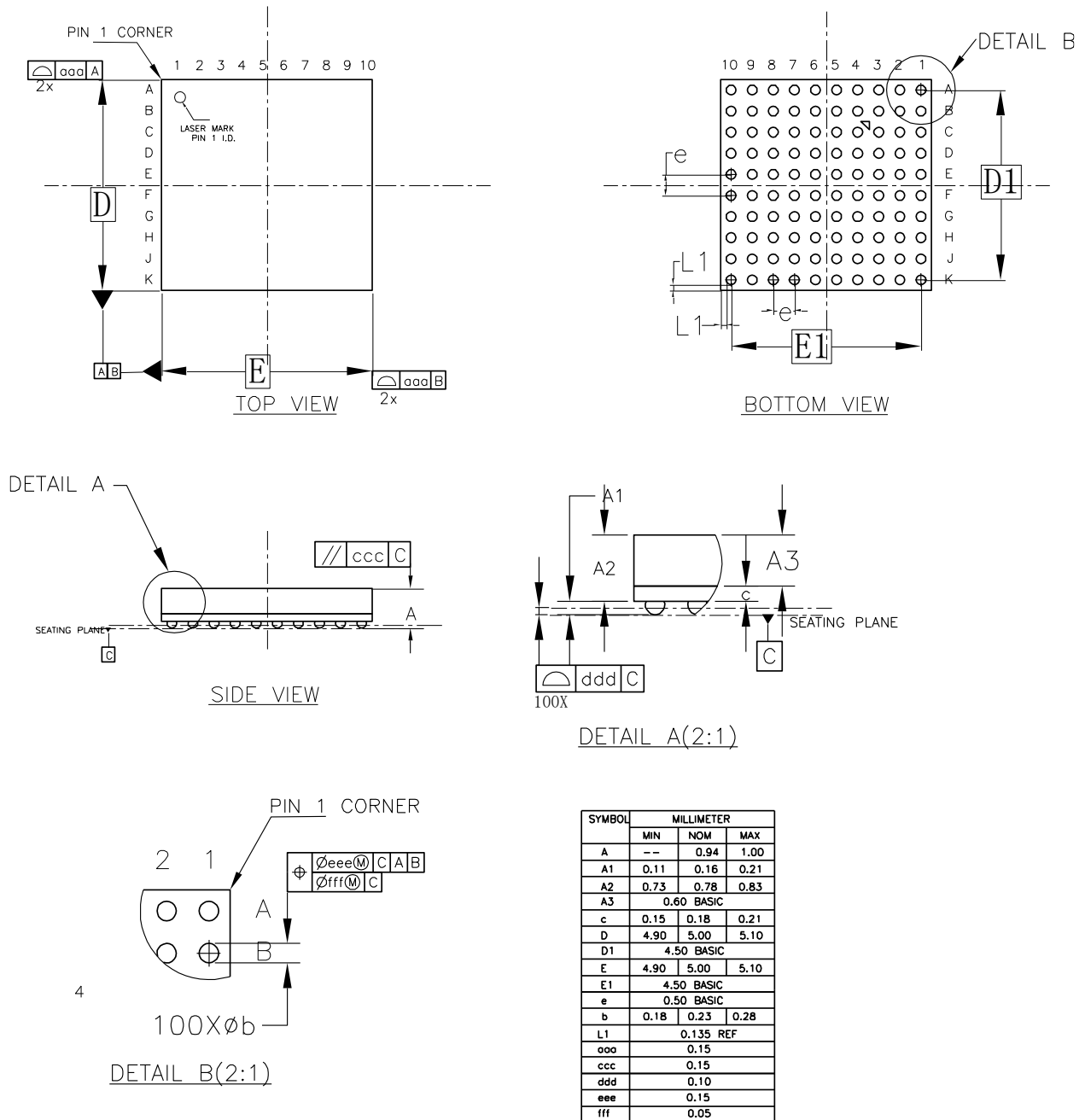


Figure 4-10 Recommended PCB Layout
MG100P/MG100PF/MG100PA/MG100PT/MG100PS

