

第七組

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郭家偉

lab1

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[輸入文件副標題]

1. din = 4’b1111時，dout[0] 的K-map

din[1], din[0]

din[3], din[2]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | 00 | 01 | 11 | 10 |
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 |
| 11 | 0 | 0 | 1 | 0 |
| 10 | 0 | 0 | 0 | 0 |

由K-map可以發現dout[0] = din[3] & din[2] & din[1] & din[0]。

以此類推:

dout[1] = din[3] & din[2] & din[1] & not(din[0])

dout[2] = din[3] & din[2] & not(din[1]) & din[0]

dout[3] = din[3] & din[2] & not(din[1]) & not(din[0])

dout[4] = din[3] & not(din[2]) & din[1] & din[0]

dout[5] = din[3] & not(din[2]) & din[1] & not(din[0])

dout[6] = din[3] & not(din[2]) & not(din[1]) & din[0]

dout[7] = din[3] & not(din[2]) & not(din[1]) & not(din[0])

dout[8] = not(din[3]) & not(din[2]) & not(din[1]) & not(din[0])

dout[9] = not(din[3]) & not(din[2]) & not(din[1]) & din[0]

dout[10] = not(din[3]) & not(din[2]) & din[1] & not(din[0])

dout[11] = not(din[3]) & not(din[2]) & din[1] & din[0]

dout[12] = not(din[3]) & din[2] & not(din[1]) & not(din[0])

dout[13] = not(din[3]) & din[2] & not(din[1]) & din[0]

dout[14] = not(din[3]) & din[2] & din[1] & not(din[0])

dout[15] = not(din[3]) & din[2] & din[1] & din[0]

Verilog Question 4

(Gate-level) 4-bit ripple-carry adder (RCA)

4-BIT RIPPLE-CARRY ADDER 可以由四個 1-BIT 的FullAdder 組成，因此我翻了翻以前的筆記，複習一下。

1-BIT FullAdder的運作原理如下:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| a | b | Cin | Cout | sum |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

由表格可以發現 Cout 就是a, b, Cin 的majority，

即 Cout = (a&b) | (a&cin) | (b&cin)

而 sum 就是如果a, b, cin當中有奇數個1那sum就等於1，也就是說sum = a, b, cin三個input做XOR。

有了這樣的基礎知識，接下來我們只需要將四個1-BIT FullAdder 的Cout 以及Cin做前後連接，4-BIT RIPPLE-CARRY ADDER 就完成啦。