3EJ4 Lab4

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Part1:

Q1. (10 Points) (1) Based on the simulation data obtained in Step 1.2, what is the low-frequency (i.e., f = 100 Hz) voltage gain in dB for the first stage differential amplifier A_{d1}, the second state CE amplifier A_{d2}, and the third stage CC amplifier A_{d3}, respectively for the differential-mode signal? (2) What is the overall voltage gain for the differential-mode signal? (3) Which input (V_1 or V_2) is the non-inverting input of the operational amplifier? (4) What is the upper 3-dB frequency f_H of the amplifier?

(1)

Frequency	vm(vo1)	|vm(vo2)|	|vm(vo)|	i(cp_q1.0)	ph(v(vo1))	ph(v(vo2))	ph(v(vo))	i(ph(cp_q1.0))	Ad1	Ad2	Ad3	Ad	Ad	Rin
Hz	Volts	Volts	Volts	Amps	deg	deg	deg	deg	dB	dB	dB	dB	V/V	Ohm
1.00E+02	4.68E-03	1.49E+01	1.49E+01	2.45E-08	-4.90E-01	1.79E+02	1.79E+02	1.90E-02	7.38	70.05	0.00	77.42	7432.9	81760.2

Ad1 = 7.38dB, Ad2 = 70.5dB, Ad3 = 0dB.

(2) The overall voltage gain in phase is Ad = 77.42dB. And Ad = 7432.9 in magnitude.

(3) The non-inverting input is V2 since it is in phase of the output Vo.

(4) For the upper 3-dB frequency, it can be obtained by subtracting 45degress from the phase observed at low frequency(100Hz). Which is 179 – 45 = 134deg. The corresponding frequency is 6.34kHz as shown below.

6.34E+03	0.0036314	10.391615	10.391154	2.44678E-08	-19.961013	134.27406	134.26961	1.20276405	5.18	69.13	0.00	74.31	5195.6	81739.9

Q2. (5 Points) Compare the simulated differential-mode gain A_{d1} found in Q1 and the simulated gain A_d in the Q5 of Lab 3. What causes these two gains to be so different from each other for the same differential amplifier?

Ad1 = 7.38dB. Ad = 78.11dB from Q5 of lab3.
The reason why these two gains are so different is because for Ad1 it is a feedback amplifier which its output Vo1 is connected to the input Vcc through a pnp bjt where its emitter is connected to the emitter of the current mirror and voltage source. And since there is also another npn bjt where its collector is connected to the emitter of Q3 and voltage source, the electric potential at Q8 emitter will be decreased as a result of the huge decrease in the voltage gain of Ad1.

Q3. (5 Points) Based on the simulated results obtained in Steps 1.2 and 1.3, what are the input resistance R_{in} and the output resistance R_o of the Op-Amp?

Rin = 81760.2Ohm. Ro = 460.9Ohm.

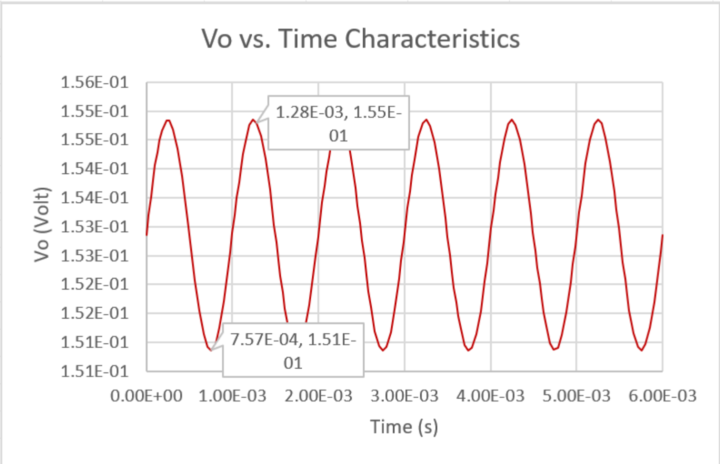
Rin
Ohm
81760.2

Rout
Ohm
460.9

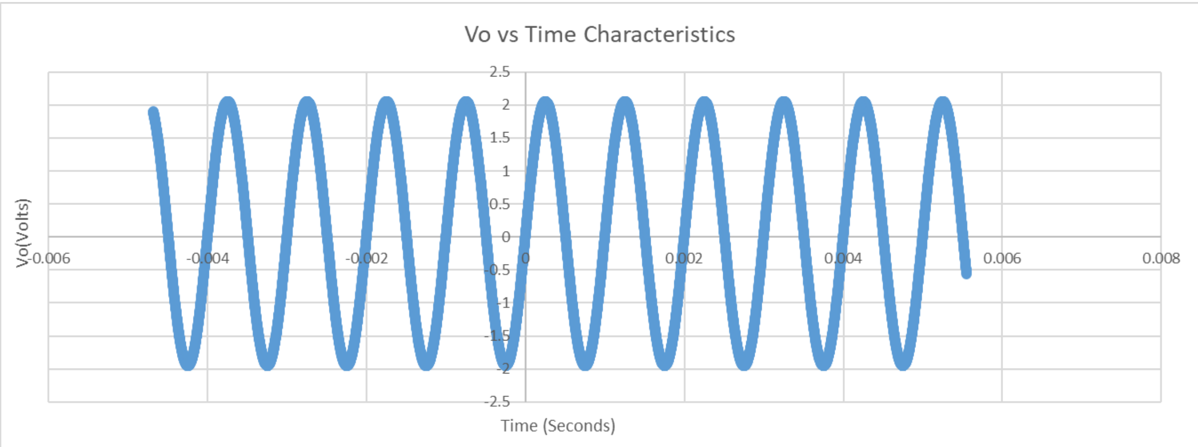
Q4. (10 Points) (1) Based on the simulated and measured results from Steps 1.6 and 1.13, plot the simulated and measured output voltages V_o vs. time characteristics at 1 kHz. (2) Calculate the simulated and measured peak to peak voltage V_{pp}, the AC amplitude V_p, and the dc voltage V_{dc} of V_o, and compare the simulation and measurement results.

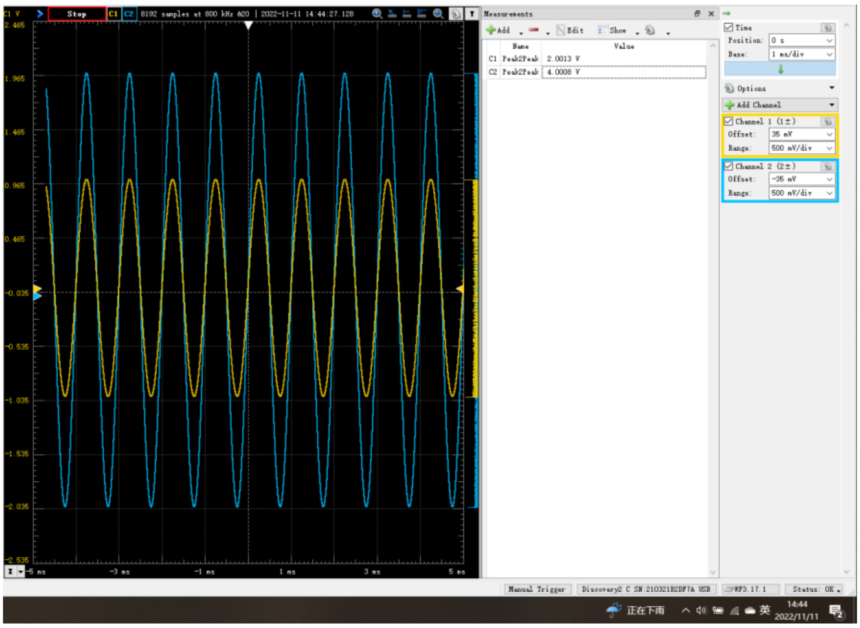
(1)

Step 1.6:



Step 1.13:

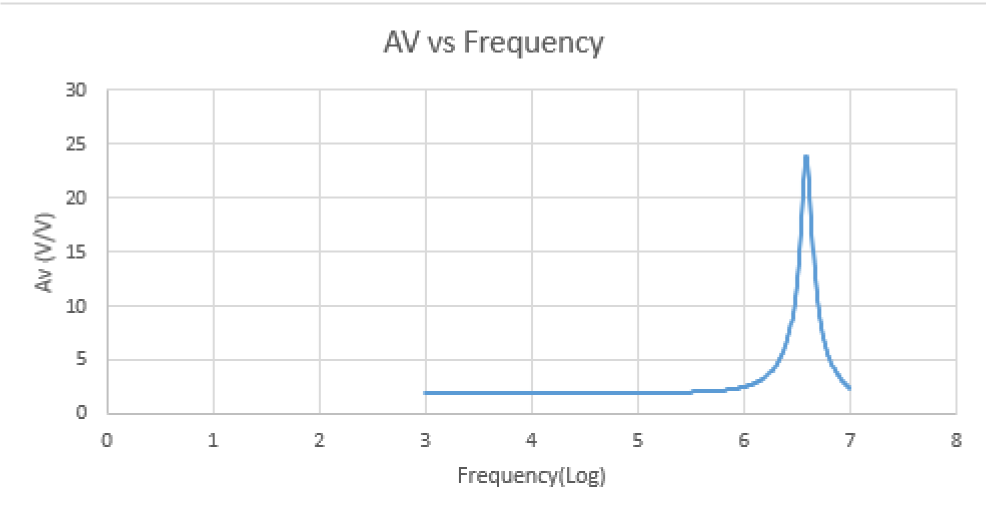




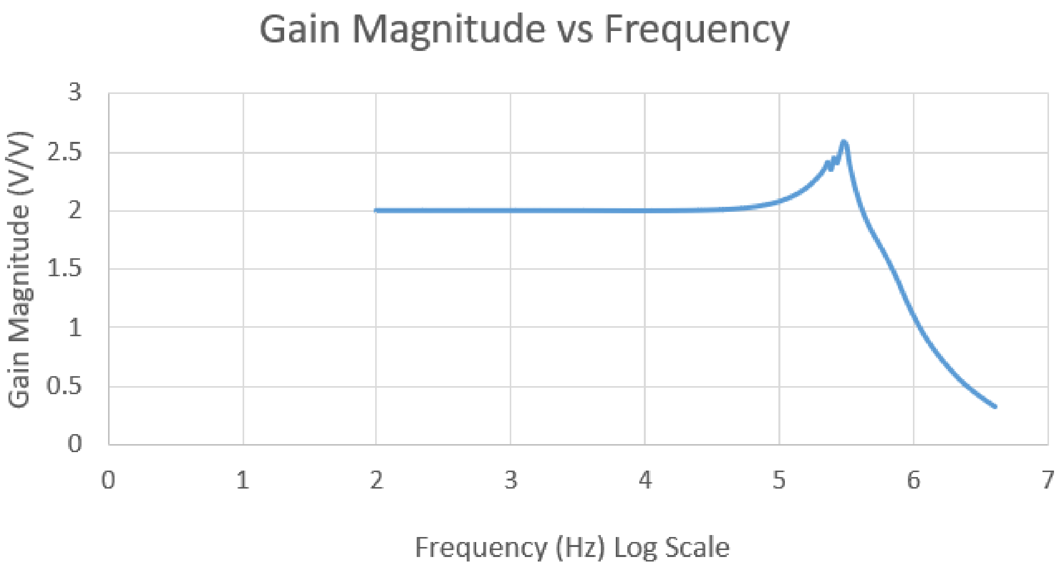
(2) The simulated Vpp is 1.55E-01 – 1.51E-01 = 0.004V, the Vp and Vdc of Vo is 0.002V and 0.002*0.707 = -1.4mV.
The measured Vpp is 4V, the Vp and Vdc of Vo is 2V and 2V and 1.414V.
Because in step 1.6 the ac input is 1mV, but in step1.13 the input ac is 1V. So the result of step 1.13 should be 1000times larger than step1.13 result and since both steps have the same input sine wave frequency with 1kHz, both steps graph are in phase.

Q5. (10 Points) (1) Based on the simulated and measured results from Steps 1.7 and 1.13, plot the simulated and measured voltage gain magnitude and phase vs. frequency characteristics. What is the low-frequency gain of this amplifier? (2) To operate this amplifier, what is its highest operating frequency to provide a constant gain as designed?

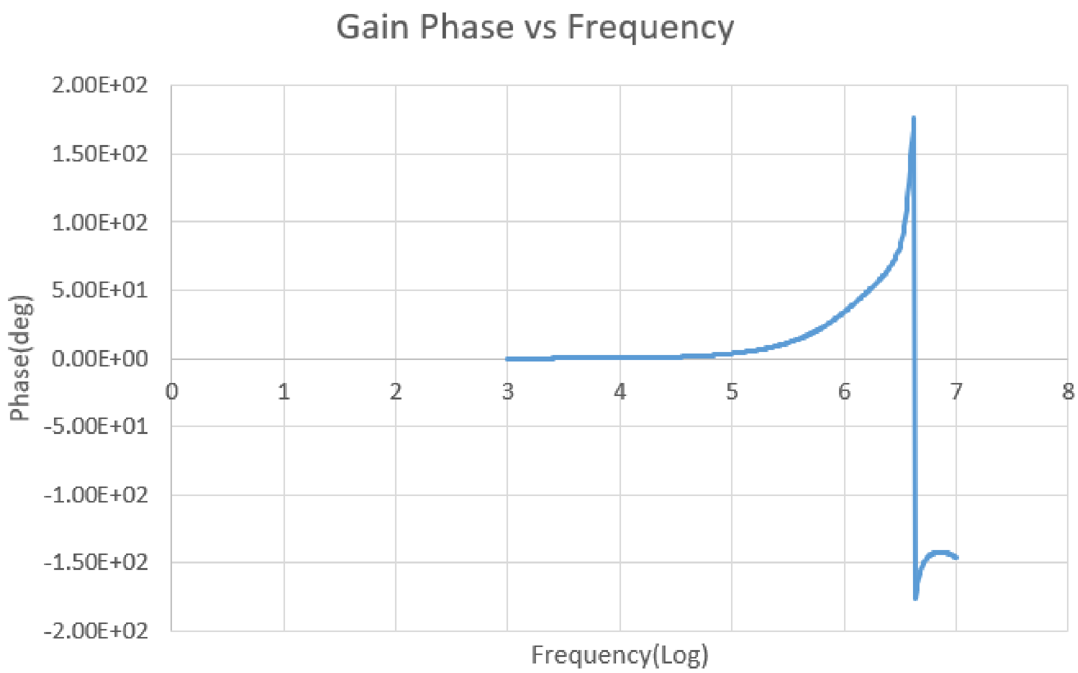
(1)
Simulated voltage gain magnitude vs frequency:



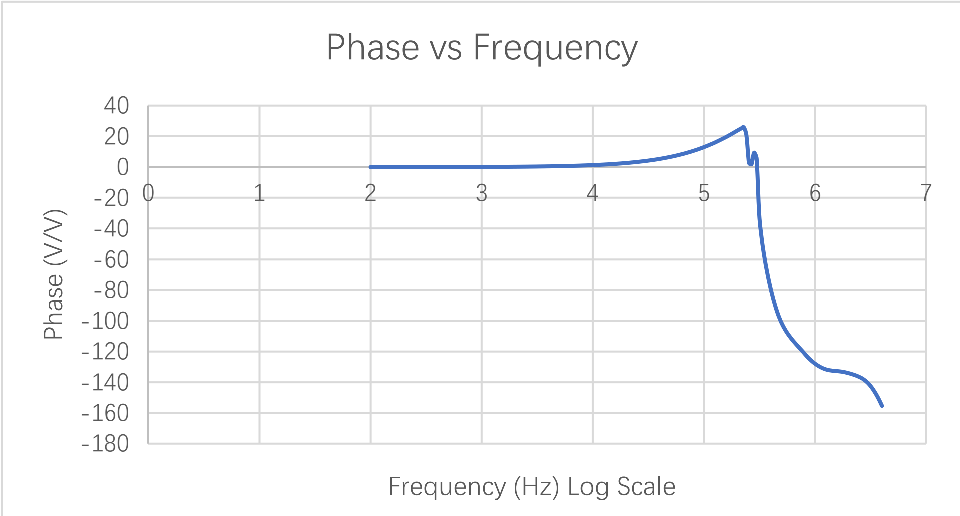
Measured voltage gain magnitude vs frequency:

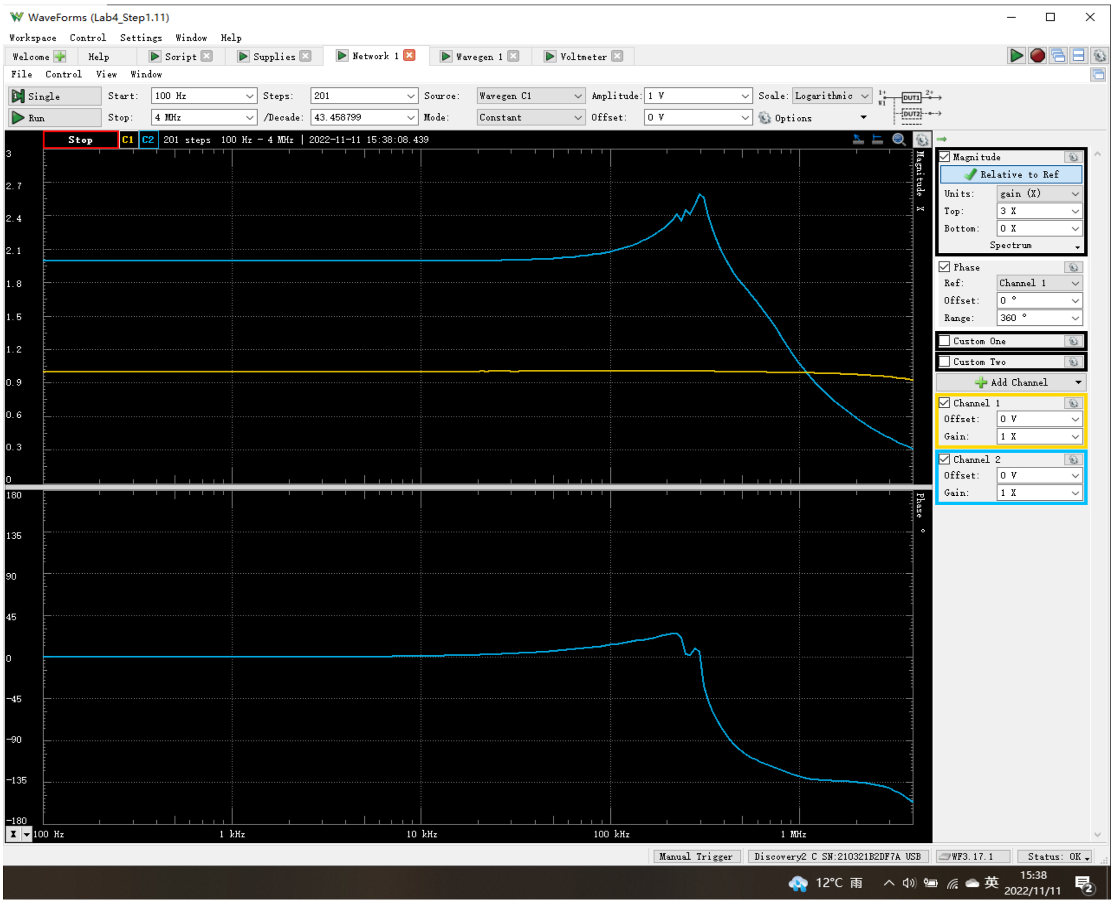


Simulated phase vs frequency:



Measured phase vs frequency:





The low frequency gain of this amplifier is 2.

(2): To provide a constant gain, based on the simulation and experimental results, the gain and phase should be both constant therefore the highest operating frequency should be 100kHz.

Q6. (5 Points) What kind of feedback configurations (e.g., shunt-shunt) is it for the amplifier in Fig. 2?

It uses the series-shunt feedback configuration. The input is connected in series with each directional amplifier, and the output is connected to one of the amplifier which will provide a feedback for the amplifier, resulting in shunt connection.

Q7. (10 Points) Find the beta network and the feedback components β, R_{11}, and R_{22}, respectively.

$$\beta = \frac{R1}{R1 + R2} = \frac{100k}{100k + 100k} = 0.5$$

$$R_{11} = R_1 || R_2 = \frac{100k * 100k}{100k + 100k} = 50k$$

$$R_{22} = R_1 + R_2 = 100k + 100k = 200k$$

Q8. (15 Points) Use the feedback theory and simulation results to find the voltage gain, the input resistance, and the output resistance of the amplifier, respectively.

A'v = 1/h12 = 1/β = 1/0.5 = 2

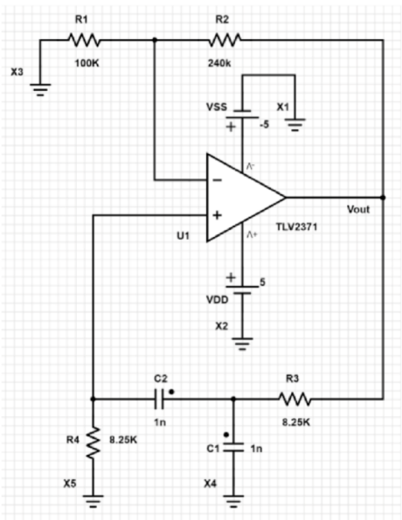
Rin = 81760.2 ohms, Rout = 460.9 ohms

Ri' = Rin + R11 = 81760.2 + 50k = 131.7602k Ohm

Ro' = Rout || R22 || RL = 460.9 || 200k || 240k = 458.96 Ohm

Part2:

Q9. (15 Points) For the oscillator circuit in Fig. 9, find its loop gain $L(s)$, the frequency for the zero loop phase, and R_2/R_1 for oscillation.



Q9. $R = R_3 = R_4$, $C = C_1 = C_2$

$$V_o = V_+ \left(1 + \frac{1}{sCR}\right) + RV_+\left[\frac{1}{R} + sC\left(1 + \frac{1}{sCR}\right)\right]$$

$$= V_+\left(1 + \frac{1}{sCR}\right) + V_+ (2 + sCR)$$

$$= V_+ \left(3 + \frac{1}{sCR} + sCR\right)$$

$$\frac{V_+}{V_o} = \frac{s/CR}{s^2 + s\left(\frac{3}{CR}\right) + \left(\frac{1}{CR}\right)^2}$$

$$L(s) = \left(1 + \frac{R_2}{R_1}\right) \frac{s/CR}{s^2 + s\left(\frac{3}{CR}\right) + \left(\frac{1}{CR}\right)^2}$$

zero loop frequency $w_o = \frac{1}{CR}$.

At zero loop frequency, $|L(j\omega)| = \frac{1}{3}\left(1 + \frac{R_2}{R_1}\right)$, hence for oscillation it requires $\frac{1}{3}\left(1 + \frac{R_2}{R_1}\right) \geq 1$ which occurs when $\frac{R_2}{R_1} \geq 2$.

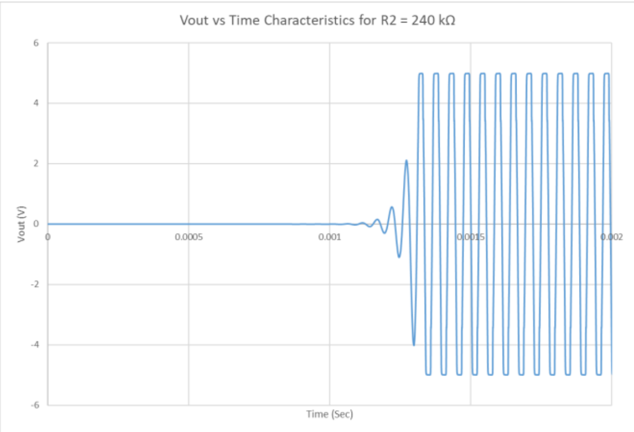
Q10. (5 Points) Based on the simulated results in Step 2.5, what are the settling times for R_2 = 220 kΩ, 240 kΩ, and 280 kΩ, respectively? What do you observe? Explain the observed trend.

R2 = 220 kΩ	R2 = 240 kΩ	R2 = 280 kΩ
Settling Time (ms)	Settling Time (ms)	Settling Time (ms)
2.6622819	1.327	0.60509607

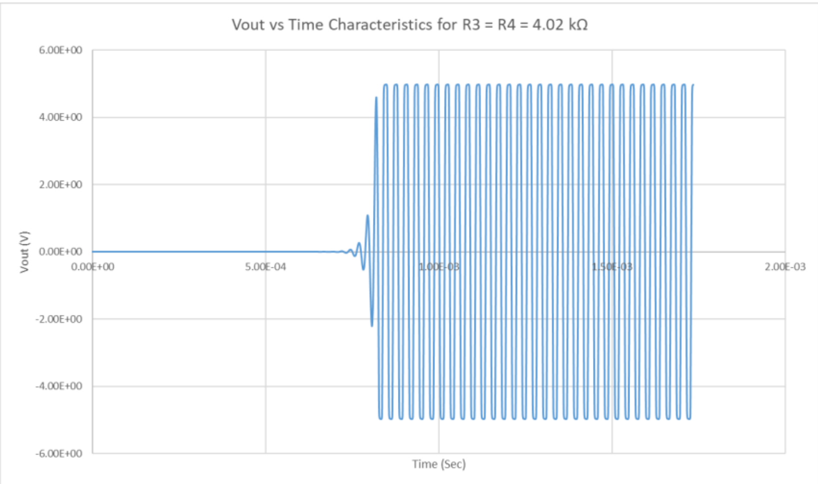
With the increase of the resistance of R2, the settling time will decrease.
The increase of the R2 will increase the loop gain L(s) based on the formula derived from Q9, hence it will result the decrease in the amount of time that circuit requires to react saturation(5V).

Q11. (10 Points) (1) Based on the setup in Steps 2.4, 2.6, 2.9, and 2.10, plot the simulated and measured V_o. (2) Calculate the simulated and measured oscillation frequencies in each case. Compare and discuss them with the results from the theory.

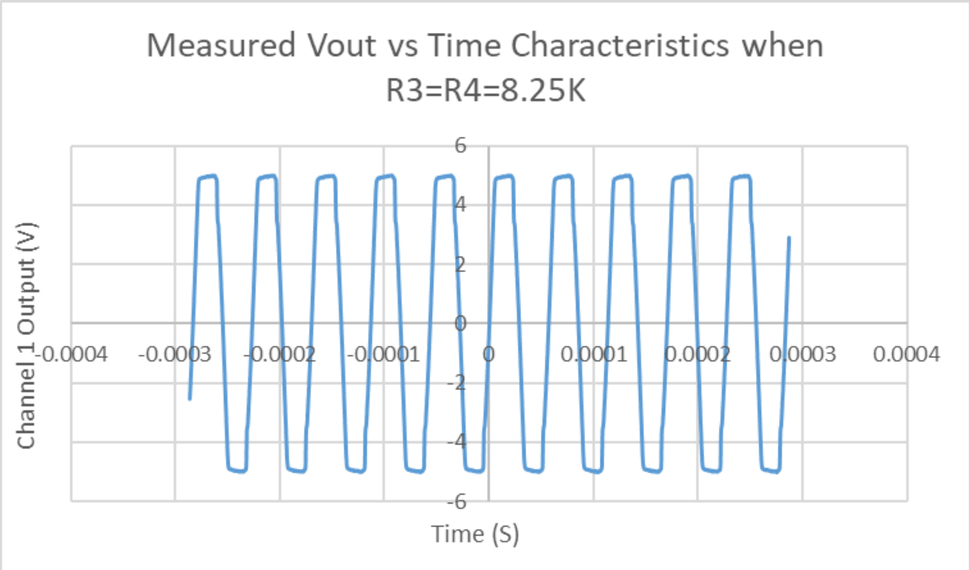
2.4:

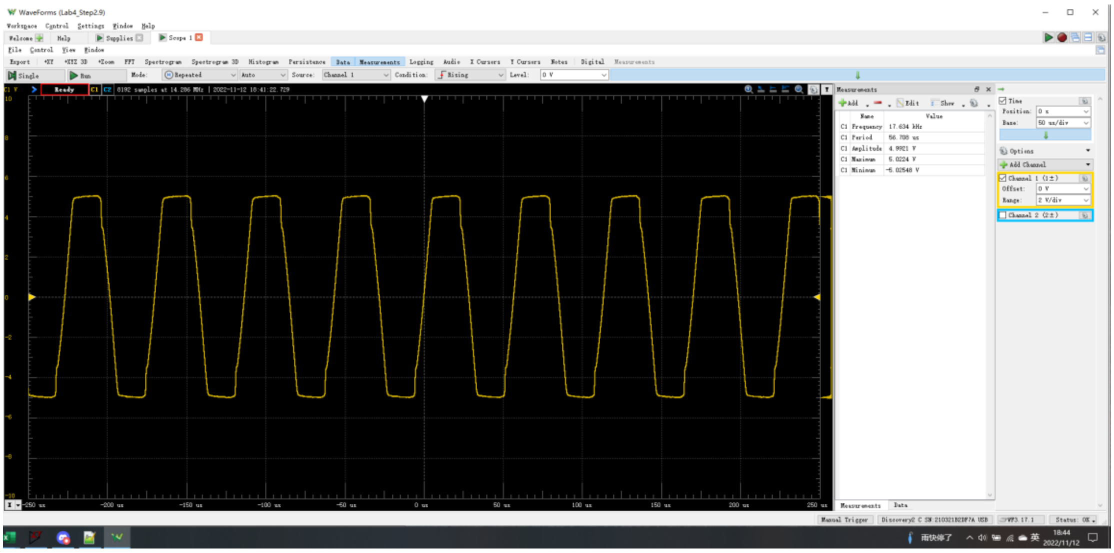


2.6:

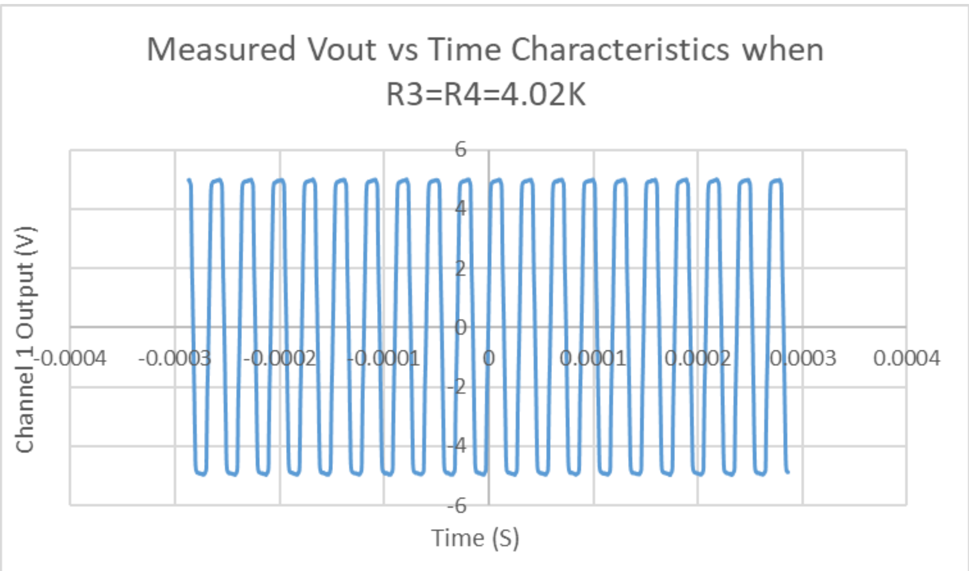


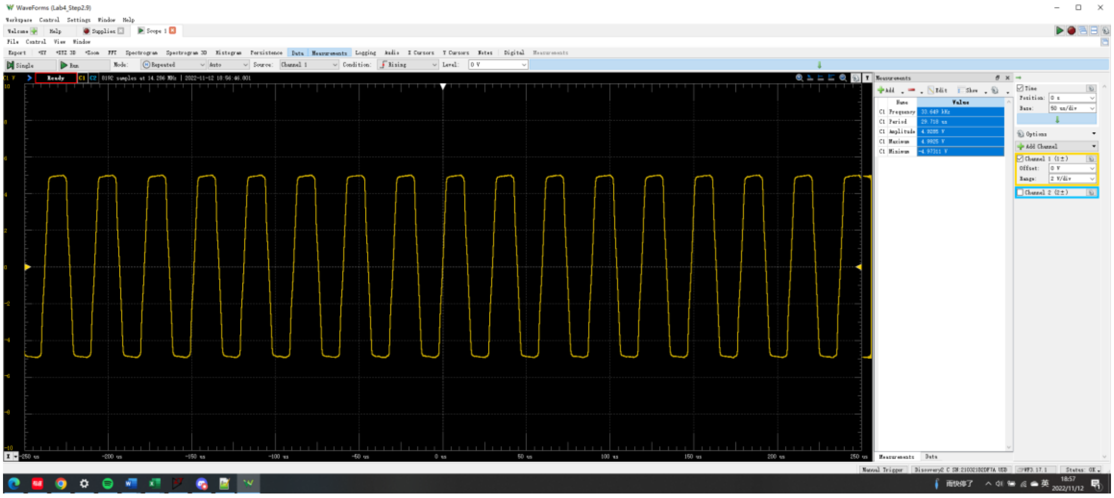
2.9:


Measured Vout vs Time Characteristics when
R3=R4=8.25K
Channel 1 Output (V)
Time (S)
6
4
2
0
-2
-4
-6
-0.0004
-0.0003
-0.0002
-0.0001
0
0.0001
0.0002
0.0003
0.0004



2.10:


Measured Vout vs Time Characteristics when
R3=R4=4.02K
Channel 1 Output (V)
Time (S)
6
4
2
0
-2
-4
-6
-0.0004
-0.0003
-0.0002
-0.0001
0
0.0001
0.0002
0.0003
0.0004



Step 2.4 = 17.989 kHz
Step 2.6 = 33.862 kHz
Step 2.9 = 17.634 kHz
Step 2.10 = 33.649 kHz

As we calculated above for each step frequency, these values are close enough to match the results from theory from Q10, as we nearly doubled the resistance R3 and R4 from 4.02k to 8.25k, the oscillation frequency will nearly get doubled from 17kHz to 34kHz.