3EJ4 Lab2

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<u>Part1:</u>

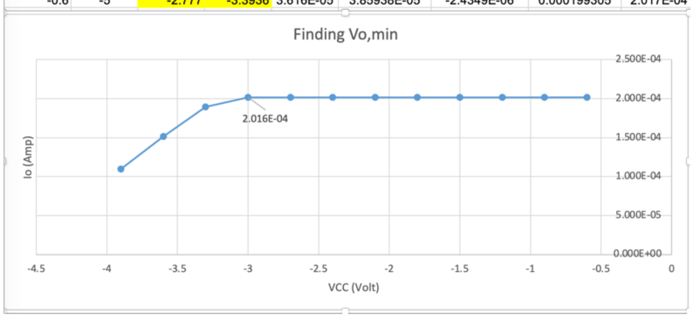
Q1. (10 Points) (1) Based on the simulation data obtained in Step 1.2, what are the $V_{o,min}$, and I_o of the current sink? Use the measurement data obtained in Step 1.10 to verify the $V_{o,min}$ and I_o. (2) Based on the simulation data obtained in Step 1.2 and the measurement data obtained in Step 1.10, what are the <u>ranges of the simulated and measured output resistance R_o</u> of the current sink for VCC larger than $V_{o,min}$?

(1):

VCC	IC	VE	Ro
-3	1.85E-04	-3.490808	7.19E+06

, the Vo,min = -3V and Io = 1.85*10^-4 A.

VCC	VEE	CH1 (VB)	CH2 (VE)	IR1	IR2	IB = IR1 - IR2	IE	IC = IE - IB
Volts	Volts	Volts	Volts	Amps	Amps	Amps	Amps	Amps
-3.9	-5	-3.3836	-3.987	4.406E-05	2.80625E-05	1.59948E-05	0.000125682	1.097E-04
-3.6	-5	-3.106	-3.717	4.044E-05	3.28819E-05	7.56076E-06	0.000159181	1.516E-04
-3.3	-5	-2.8596	-3.4716	3.723E-05	3.71597E-05	7.46528E-08	0.000189628	1.896E-04
-3	-5	-2.7774	-3.3946	3.616E-05	3.85868E-05	-2.42274E-06	0.000199181	2.016E-04
-2.7	-5	-2.7774	-3.3942	3.616E-05	3.85868E-05	-2.42274E-06	0.000199231	2.017E-04
-2.4	-5	-2.7776	-3.3944	3.617E-05	3.85833E-05	-2.41667E-06	0.000199206	2.016E-04
-2.1	-5	-2.7778	-3.395	3.617E-05	3.85799E-05	-2.41059E-06	0.000199132	2.015E-04
-1.8	-5	-2.777	-3.3956	3.616E-05	3.85938E-05	-2.4349E-06	0.000199057	2.015E-04
-1.5	-5	-2.777	-3.3952	3.616E-05	3.85938E-05	-2.4349E-06	0.000199107	2.015E-04
-1.2	-5	-2.7774	-3.3942	3.616E-05	3.85868E-05	-2.42274E-06	0.000199231	2.017E-04
-0.9	-5	-2.7776	-3.3942	3.617E-05	3.85833E-05	-2.41667E-06	0.000199231	2.016E-04
-0.6	-5	-2.777	-3.3936	3.616E-05	3.85938E-05	-2.4349E-06	0.000199305	2.017E-04



The verified result from the Step 1.10. The corresponding Io(Ic) is 2.016E-04.

(2):

Simulated result ranges of <u>Ro: 7.19E+06 to 7.69E+07 ohm.</u>

Experimental result ranges of <u>Ro: Neglect the negative resistance values because the uncertainty of circuit behaviors, the experimental ranges should between the range of 2.68E+06ohm and 6.05E+06ohm.</u>

Q2. (10 Points) What are the values of V_{o1} and V_{o2} obtained in Step 1.5? Check the Q-points of Q_2 under these two conditions and explain/justify the results obtained qualitatively.

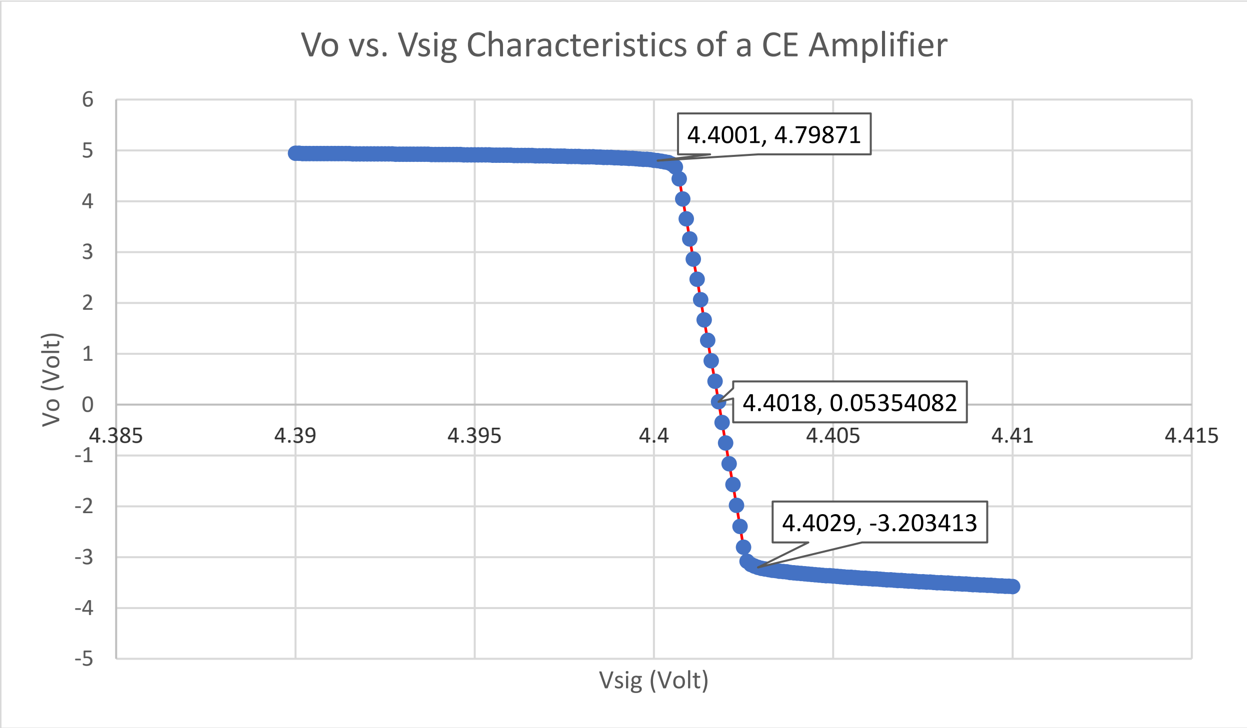
$V_{o1} = 4.94029V$ $V_{o2} = -3.57892V$

Vo1 (V)	Vo2 (V)
4.94029	-3.57892

Explain/justify: As the value of Vo1 and Vo2 obtained from Step 1.5, the value of Vo1 is pushing towards the saturation region of 5V. Since there is a huge jump from Vo1 to Vo2, which can conclude that Vo2 is in the cut-off region.

Q3. (15 Points) Based on the simulation data obtained in Step 1.6, (1) plot the simulated DC V_o vs. V_{sig} characteristics. Discuss/justify the simulated characteristics. (2) For the circuit to work as an amplifier, find the DC input range for V_{sig} and the output voltage range for V_o. (3) Find the V_{sig} value and its corresponding collector current I_{C2} that results in $V_o \approx 0$ V. (4) Based on the measurement data obtained in Step 1.16, plot the measured DC V_o vs. V_{sig} characteristics.

(1):

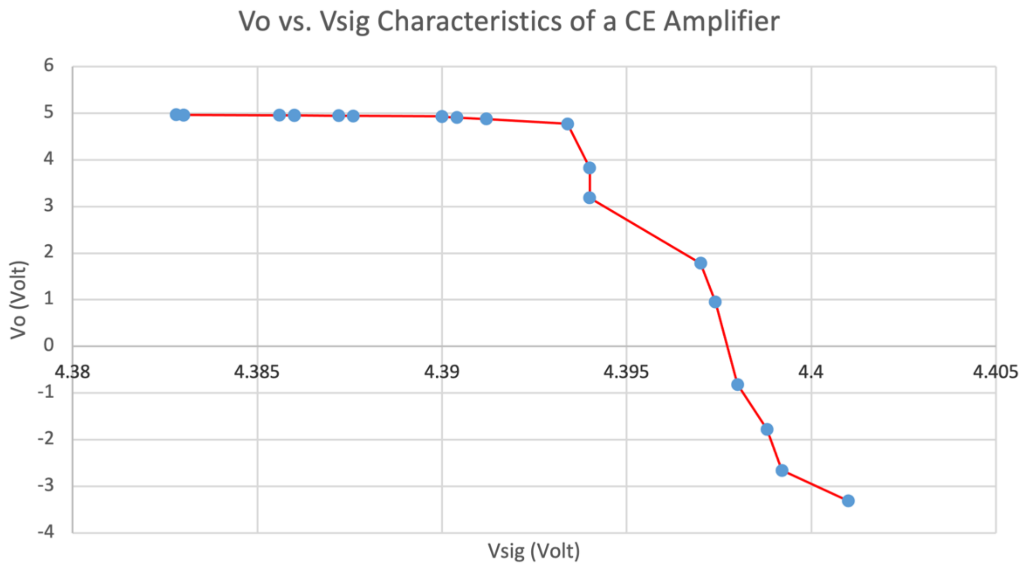


Discuss/justify: As the graph shown above, there are three regions plotted of the CE Amplifier, the upper bond shows an approximately horizontal line is the saturation region of the Q-point which means the transistor is fully on, the lower bond shows an approximately horizontal line is the cut-off region of the Q-point which means the transistor is fully off, the linear line between the upper bond and lower bond is the active region of the Q-point which can amplify upper and lower part of the input signal.

(2): For the circuit to work as an amplifier, the DC input range for Vsig is 4.4001 to 4.4029, and the output voltage range for Vo is 4.79871 to -3.203413

(3): Vsig = 4.4018V and Ic = -0.000184882, when $V_o \approx 0$ V.

(4):



Q4. (10 Points) (1) Based on the simulation data obtained in Step 1.7, what are the magnitude (in dB) and phase of intrinsic voltage gain A_{vo} at low frequency (i.e., 100 Hz) and the upper 3-dB frequency f_{3dB} (i.e., the frequency at which the amplitude become 1 2 = 0.707 of its low-frequency value, or the phase changes 45°) of this CE amplifier? (2) Verify the voltage gain A_{vo} using the measurement data obtained in Steps 1.18 and 1.19. (3) Increase the frequency of W1 to the upper 3-dB frequency f_{3dB} obtained from the simulation, check the value of A_{vo}, and see if it is about 0.707 of its low-frequency value obtained at 100 Hz. Provide WaveForms screenshots of your measurement results.

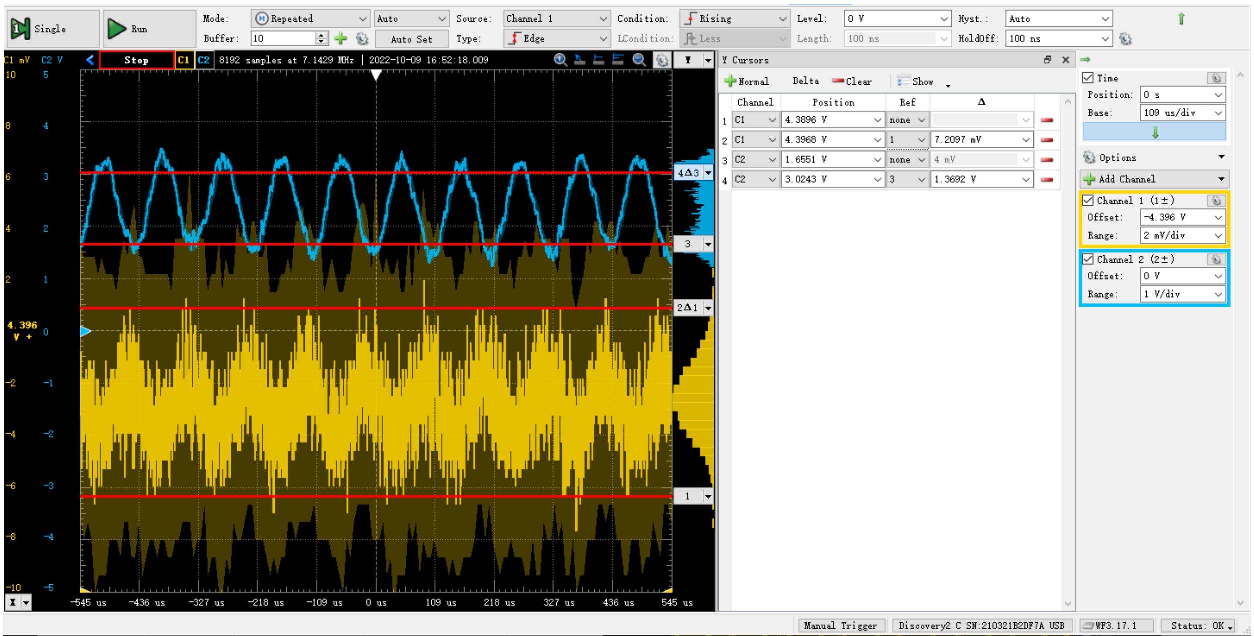
(1): The magnitude (in dB) and phase of intrinsic voltage gain A_{vo} at low frequency (i.e., 100 Hz) is, 72.14662238dB and 179.5968243deg. The upper 3-dB frequency f3dB = 9128.428949Hz.

(2):

ΔC1 (V)	ΔC2 (V)	Gain Av (dB)
2.41E-03	2.5596	60.5

It is close enough to the simulation result.

(3): WaveForms screenshot result:



The gain of Avo is equal to =20*LOG10(1.3692/7.21E-03) = 45.6 which is approximately equal to 0.707 * 60.5 = 42.7735 the gain of low frequency.

Part2:

Q5. (15 Points) Based on the simulation data obtained in Step 2.2, (1) what are the voltages of V_o and V_E, and I_{C2} of Q_2 when V_{CM} = 0V, (2) what is the input common-mode range (i.e., the voltage range of V_{CM} to maintain the same out voltage), and (3) what determines the upper and lower bounds of the input common-mode range? (4) Based on the measurement data obtained in Steps 2.7 and 2.8, verify the common-mode range by experimental data.

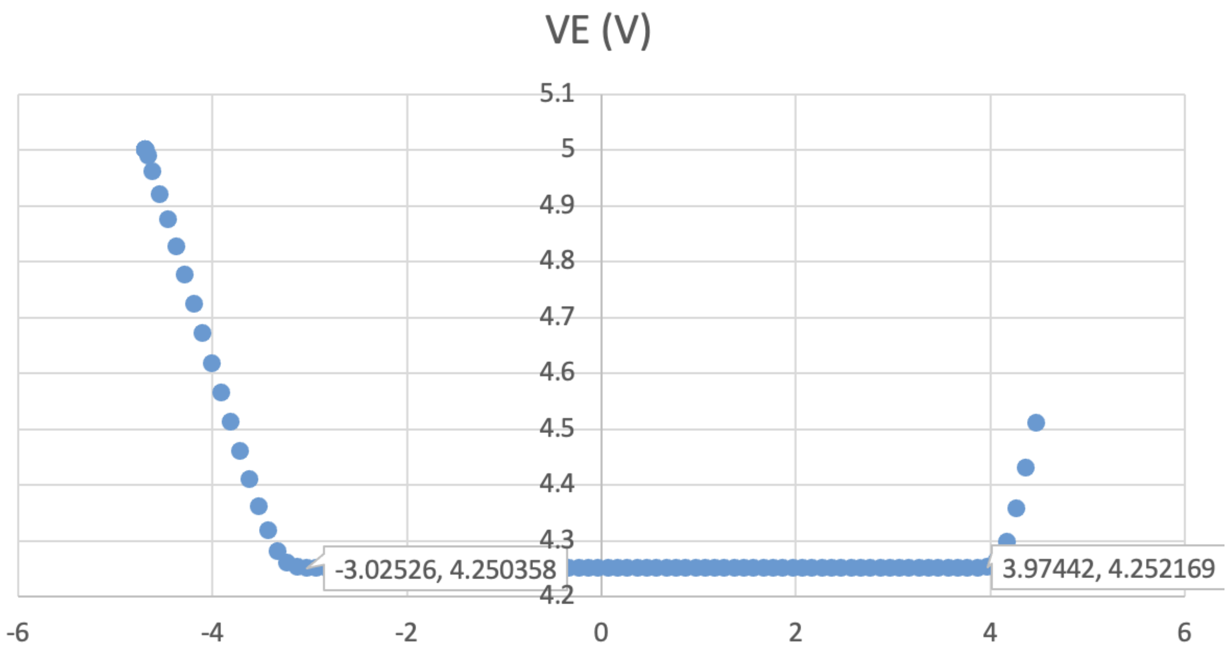
(1): Vo = -0.5253805, VE = 4.249999, Ic2 = 9.09093*10^-5 when Vcm = 0V.

Vo (V)	VE (V)	IC2 (A)		Vcm
-0.5253805	4.249999	9.09093E-05		-1.027E-15

(2): The input common-mode range of Vcm to stay constant is between -2.5V to 4.5V.

Vo (V)	VE (V)	IC2 (A)		Vcm
-3.02526	4.250358	9.0865E-05		-2.5

Vo (V)	VE (V)	IC2 (A)		Vcm
3.97442	4.252169	9.0646E-05		4.5

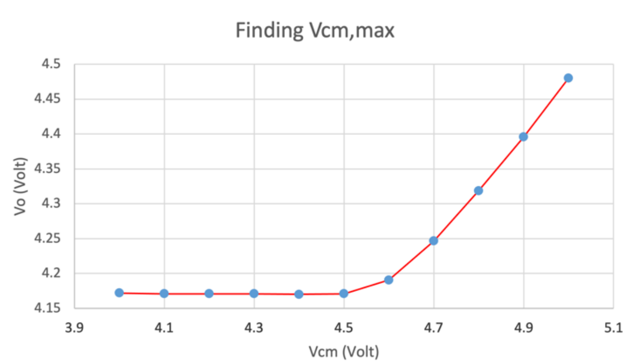


(3): what determines the upper and lower bounds of the input common-mode range?

The common-mode input voltage Vcm will determine the upper and lower bounds of the range which will keep Vov the same as long as Q1&Q2 are in saturation region which is the flat line as shown. When there is not sufficient Vcm supplies to meet the saturation condition of BJTS, it will act as an amplifier and shows an active region (linear increase or decrease line) from the graph.

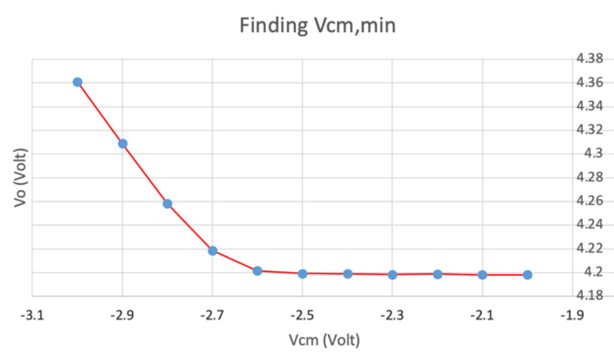
(4): Steps 2.7:

W1 Setting	Channel 1 (VE)	Channel 2 (Vo)	IC2 = (5 V - Vo)/8.25 kohm
Volts	Volts	Volts	Amps
4	3.395	4.172	1.00E-04
4.1	3.4922	4.171	1.00E-04
4.2	3.5936	4.171	1.00E-04
4.3	3.694	4.171	1.00E-04
4.4	3.7926	4.1702	1.01E-04
4.5	3.8934	4.171	1.00E-04
4.6	3.99	4.1906	9.81E-05
4.7	4.091	4.2466	9.13E-05
4.8	4.188	4.3188	8.26E-05
4.9	4.286	4.3956	7.33E-05
5	4.383	4.48	6.30E-05



Steps 2.8:

W1 Setting	Channel 1 (VE)	Channel 2 (Vo)	IC2 = (5 V - Vo)/8.25 kohm
Volts	Volts	Volts	Amps
-2	-2.6024	4.1982	9.72E-05
-2.1	-2.7048	4.1982	9.72E-05
-2.2	-2.803	4.1988	9.71E-05
-2.3	-2.904	4.1984	9.72E-05
-2.4	-3.002	4.1992	9.71E-05
-2.5	-3.103	4.1994	9.70E-05
-2.6	-3.2044	4.2016	9.68E-05
-2.7	-3.301	4.2188	9.47E-05
-2.8	-3.402	4.2582	8.99E-05
-2.9	-3.499	4.309	8.38E-05
-3	-3.5978	4.361	7.75E-05



Both data confirmed the range of Vcm.

Q6. (10 Points) Based on the simulated data obtained in Step 2.3, what is the low-frequency voltage gain A_{cm} in dB for the common-mode signal?

The gain of Acm is -86.90dB.

Part3:

Q7. (10 Points) Based on the simulation data obtained in Step 3.2 and the description in Section 9.2.3 Large-Signal Operation of the textbook, (1) what is the input differential-mode range? (2) How do we determine the upper and lower bounds of the input differential-mode range?

(1): T=25mV, 2/T=12.5mV, The differential-mode range is from -12.5mV to 12.5mV.

(2): The input differential-mode range is determined by the range needed to make the amplification linear, if it is outside that range, the amplification is not linear anymore.

Q8. (10 Points) (1) Based on the simulation data obtained in Step 3.3, what is the voltage gain A_d in dB for the differential-mode signal? (2) Estimate its upper 3-dB frequency f_{3dB} (i.e., the frequency at which the amplitude becomes 1/sqrt(2) = 0.707 of its low-frequency value or the phase changes 45°) and calculate the gain-bandwidth product (GBW) in hertz (Hz). (3) Compare the upper 3-dB frequency f_{3dB} of this differential amplifier with that of the CE amplifier obtained in Q4. (4) Based on the measurement data obtained in Step 3.6, calculate the measured low-frequency differential voltage gain A_d in dB.

(1): The voltage gain Ad is 19.63dB.

(2): The upper 3-dB frequency is 5655555.22514252Hz. The calculated gain-bandwidth product (GBW) is calculated by 10^(16.59/20) = 6.755392.

(3): The upper 3-dB frequency is f3dB = 9128.428949Hz from question (4) by using the CE amplifier. The upper 3-dB frequency is 5655555.22514252Hz from question (8) by using the differential amplifier. The difference is the CE amplifier is used in the low-frequency voltage amplifier and well-suited for voltage amplification so it also provides a higher gain than differential amplifier. The differential amplifier is used mainly to suppress noise, generally the open loop gain can be as high as 100dB at DC(zero Hz). The output gain decreases linearly as frequency increases down to “Unity Gain” or 1, at about 1MHz, that’s why the upper 3-dB frequency of differential amplifier is much higher than the CE amplifier.

(4): The measured low-frequency differential voltage gain Ad is 21.8dB.

Q9. (10 Points) Based on the simulation data, what is the common-mode rejection ratio (CMRR) of the amplifier in dB?

The common mode gain is -86.90dB.

The differential mode gain is 19.63dB.

The common-mode rejection ratio (CMRR) is |19.63dB|/|-86.90dB| = 0.2258918297 ≈ 0.2359