3EJ4 Lab3

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*Part1:*

Text

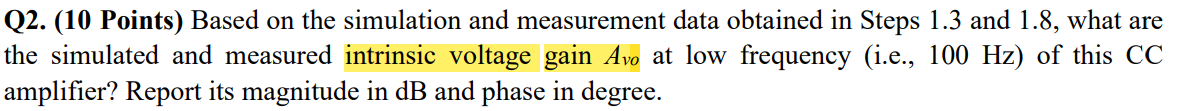
Description automatically generated with medium confidence

(1)

Discuss/Justify:

(2) To ensure the circuit work as a common-collector amplifier, Vsig should be greater than -4.5V and Vo should be greater than -4.683226V.

(3) The Vsig values results in Vo = 0V is Vsig = 0.5V.



The simulated intrinsic voltage gain Avo at low frequency is 0dB with phase -8.47E-5deg.

The measured intrinsic voltage gain Avo at low frequency is 0.8dB with phase 0.97deg.

*Part2:*

Text

Description automatically generated with medium confidence

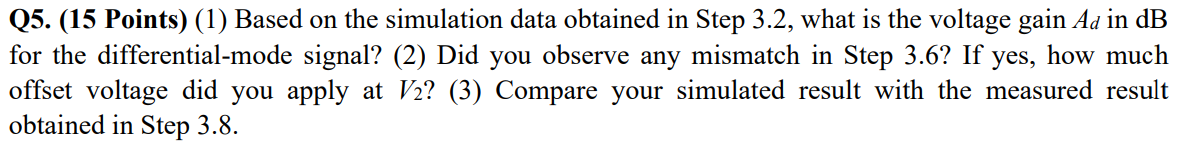
The most difficult one.

Text

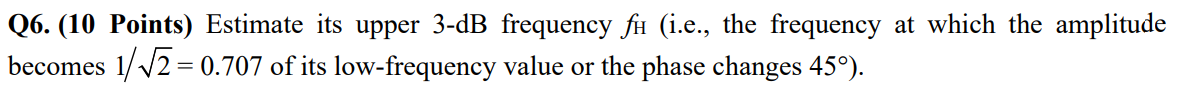
Description automatically generated

1. Input impedance Rin = 389.12ohm. The current gain Ai = 1.048.
2. Output impedance Ro = 1.58E+06ohm.
3. A picture:

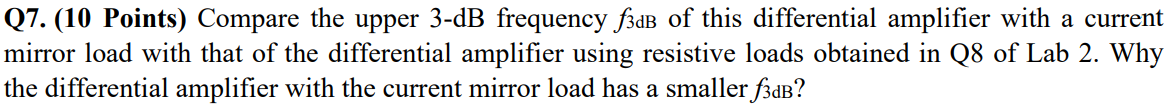
*Part3:*



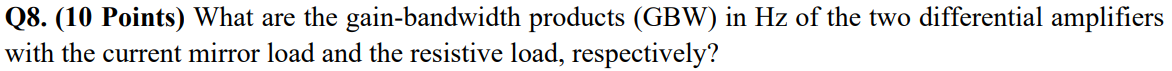
1. The voltage gain is 78.11dB.
2. Yes, the offset I applied at V2 is -0.00065V.
3. The simulated result is 58.94dB and the measured result is 56.2dB which they are close enough.



The upper 3-dB frequency should around 1.54E+04 hz which will have the Vm(vo) amplitude close to 11.37861354V.



The upper 3-dB frequency is 5655555.22514252Hz from question (8) of lab2 by using the differential amplifier. The upper 3-dB frequency from Q6 is around 15400Hz. The reason of the differential amplifier with the current mirror load has a smaller f3dB is because ..



What formulas should use to find GBW?