3EJ4 Lab4

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*Part1:*

Text

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(1)



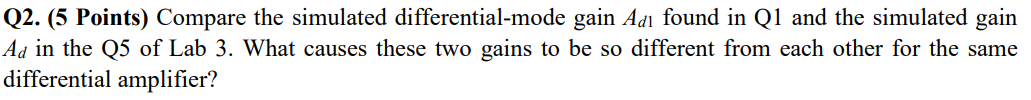
Ad1 = 7.38dB, Ad2 = 70.5dB, Ad3 = 0dB.

(2) The overall voltage gain in phase is Ad = 77.42dB. And Ad = 7432.9 in magnitude.

(3) The non-inverting input is V2 since it is in phase of the output Vo.

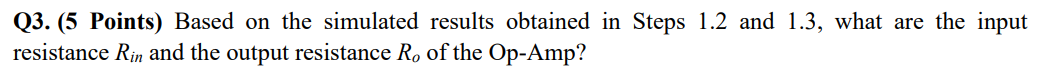
(4) For the upper 3-dB frequency, it can be obtained by subtracting 45degress from the phase observed at low frequency(100Hz). Which is 179 – 45 = 134deg. The corresponding frequency is 6.34kHz as shown below.





Ad1 = 7.38dB. Ad = 78.11dB from Q5 of lab3.

The reason why these two gains are so different is because for Ad1 it is a feedback amplifier which its output Vo1 is connected to the input Vcc through a pnp bjt where its emitter is connected to the emitter of the current mirror and voltage source. And since there is also another npn bjt where its collector is connected to the emitter of Q3 and voltage source, the electric potential at Q8 emitter will be decreased as a result of the huge decrease in the voltage gain of Ad1.



Rin = 81760.2Ohm. Ro = 460.9Ohm.

Graphical user interface

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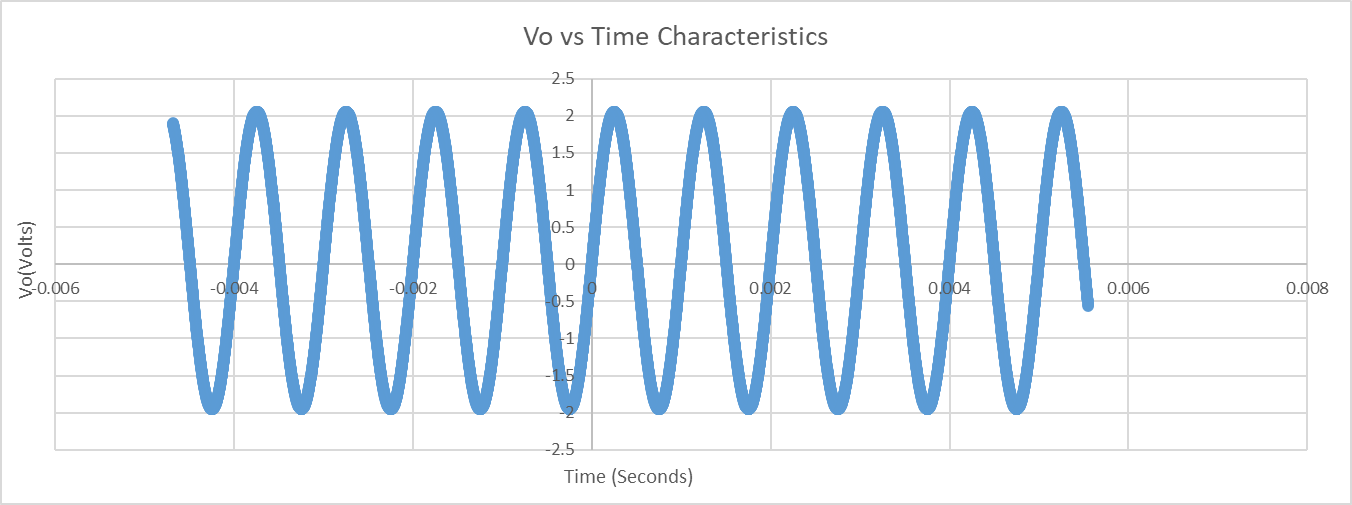
(1)

Step 1.6:

Chart, line chart

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Step 1.13:



Graphical user interface

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(2) The simulated Vpp is 1.55E-01 – 1.51E-01 = 0.004V, the Vp and Vdc of Vo is 0.002V and 0.002\*0.707 = -1.4mV.

The measured Vpp is 4V, the Vp and Vdc of Vo is 2V and 2V and 1.414V.

Because in step 1.6 the ac input is 1mV, but in step1.13 the input ac is 1V. So the result of step 1.13 should be 1000times larger than step1.13 result and since both steps have the same input sine wave frequency with 1kHz, both steps graph are in phase.

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(1)

Simulated voltage gain magnitude vs frequency:

Chart

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Measured voltage gain magnitude vs frequency:

Chart, scatter chart

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Simulated phase vs frequency:

Chart, line chart

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Measured phase vs frequency:

Graphical user interface

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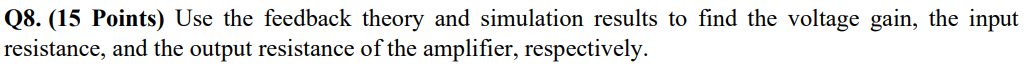
The low frequency gain of this amplifier is 2.

(2): To provide a constant gain, based on the simulation and experimental results, the gain and phase should be both constant therefore the highest operating frequency should be 100kHz.



It uses the series-shunt feedback configuration. The input is connected in series with each directional amplifier, and the output is connected to one of the amplifier which will provide a feedback for the amplifier, resulting in shunt connection.





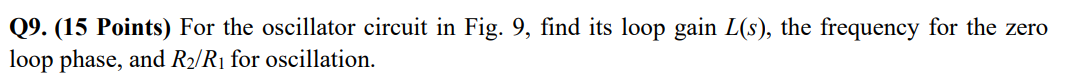
A’v = 1/h12 = 1/β = 1/0.5 = 2

Rin = 81760.2 ohms, Rout = 460.9 ohms

Ri’ = Rin + R11 = 81760.2 + 50k = 131.7602k Ohm

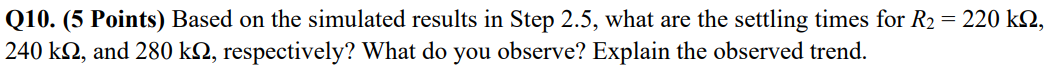
Ro’ = Rout || R22 || RL = 460.9 || 200k || 240k = 458.96 Ohm

*Part2:*



Diagram, schematic

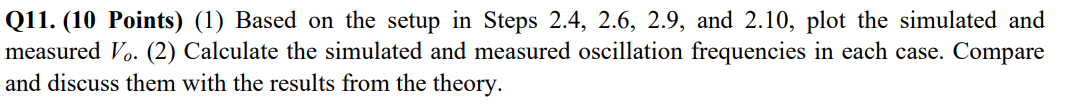
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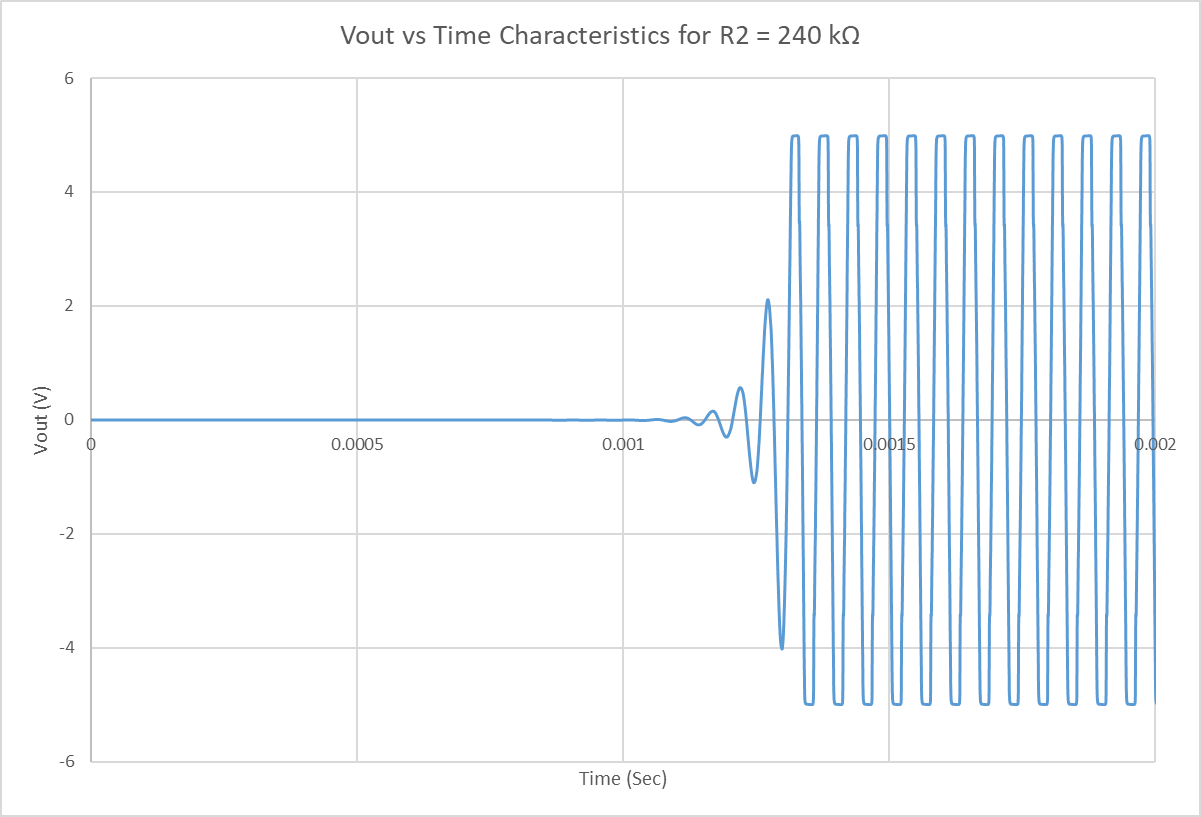


With the increase of the resistance of R2, the settling time will decrease.

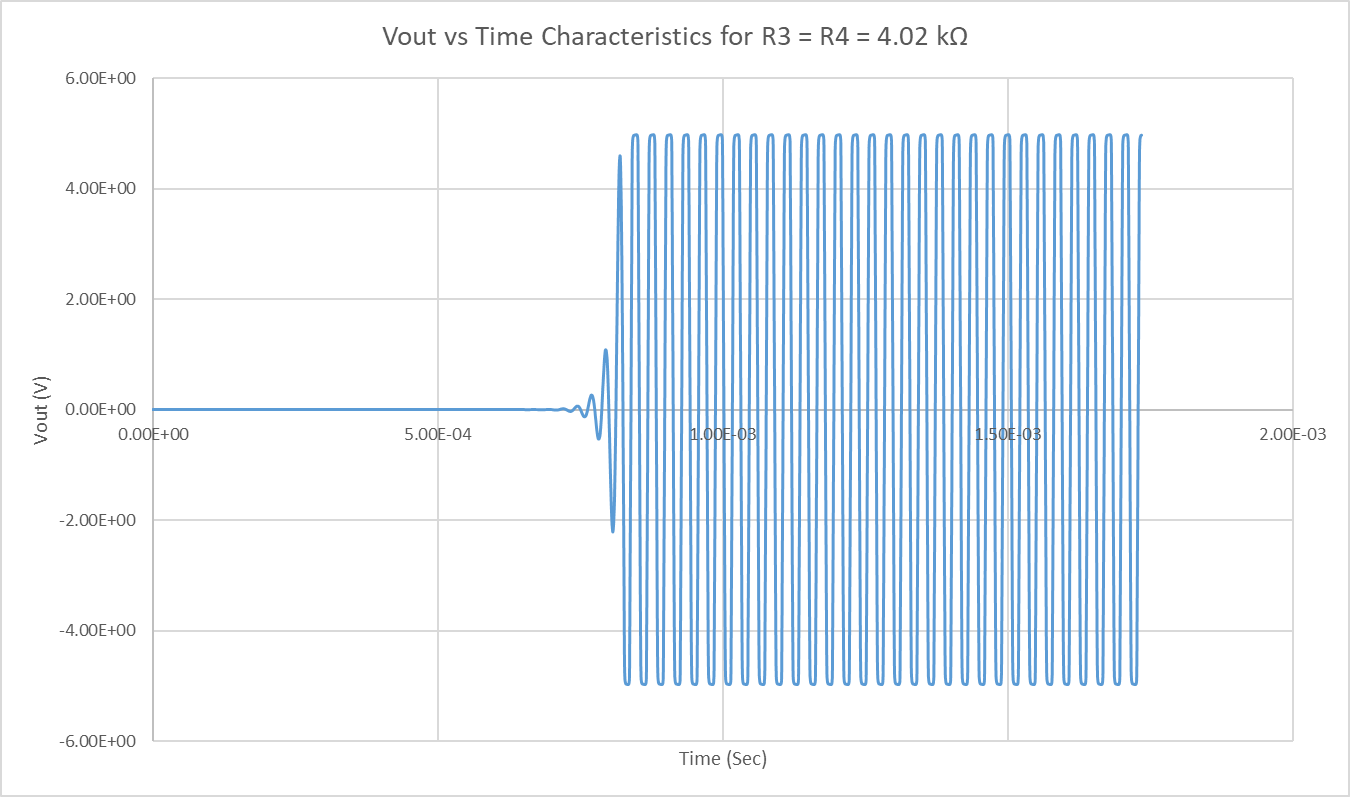
The increase of the R2 will increase the loop gain L(s) based on the formula derived from Q9, hence it will result the decrease in the amount of time that circuit requires to react saturation(5V).



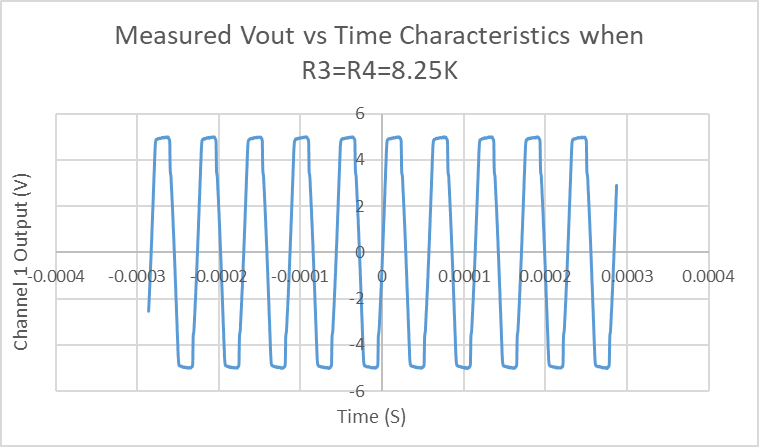
2.4:



2.6:



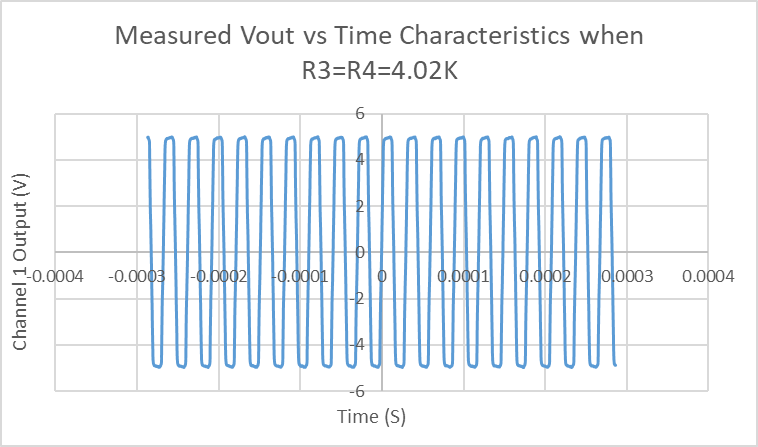
2.9:



A screenshot of a computer

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2.10:



Graphical user interface

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Step 2.4 = 17.989 kHz

Step 2.6 = 33.862 kHz

Step 2.9 = 17.634 kHz

Step 2.10 = 33.649 kHz

As we calculated above for each step frequency, these values are close enough to match the results from theory from Q10, as we nearly doubled the resistance R3 and R4 from 4.02k to 8.25k, the oscillation frequency will nearly get doubled from 17kHz to 34kHz.