

CMPE 315: Principles of VLSI Design

Project Cover Page

Lab # : Project Submission 2
Project Title : Two-Way, Set-Associative Cache

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Section : 01

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Comments to student:

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INTRODUCTION

The purpose of this lab is to be able to utilize Cadence software to design a two-way, set associative cache to hone VHDL coding skills while learning about functionality behind cache systems. The overall development process of the cache involves design, implementation and simulation.

Each of the sets of caches have 8 blocks, with four bytes per block. 3 bits are used to select one of the 8 blocks and 2 bits are used to select the correct byte from the block. The remaining 3 bits in the 8-bit address are used as a tag. The cache will be able to store 64 bytes by utilizing two sets of 32-byte cache.

The following symbols and acronyms for various signals will be used frequently throughout this document:

RH – Read Hit

M_A – Memory Address

RM – Read Miss

M_D – Memory Data

WH – Write Hit

RD_WR – Read/(not)Write

WM – Write Miss

clk – Clock

C_A – CPU Address

LRU – Least Recently Used

C_D – CPU Data

The two-way, set associative cache supports read miss, read hit, write miss and write hit handling in a manner described in Table 1.

	Description	Clock Cycles
Read Hit	Access data in cache addressed by C_A , which originates from the CPU. The data will be then sent back to the CPU via C_D bus.	2
Read Miss	After checking if tag bits & valid bits in the cache match the corresponding bits of C_A , and finding that no blocks contain the desired data, memory data access will occur after a period of wait cycles. The data will be stored in the least recently used cache, and the data block of interest will be sent back to the CPU via C_D bus.	19
Write Hit	The address sent from the CPU via C_A bus is seen to be currently supported by the cache, so the block addressed by C_A will be overwritten with the contents of C_D .	3
Write Miss	C_A is not currently supported in the cache sets, so no operation will occur. (NOP)	3

DESIGN APPROACH

VHDL CODE:

The general approach to create the cache system was to start with basic functionality, such as basic, gate entities and working up to multiplexers, decoders then registers, then finally the state machine until everything that was required of the cache chip was created.

To understand what to build for each of the entities, block diagrams and basic conceptualization was done on paper before implementing in code.

Using the decoders in a simple example, a basic 1-to-2 decoder was designed on paper, and this block is used to design a 2-to-4 decoder, and again for a 3-to-8 decoder. Details regarding specific design processes for the more complicated entities will follow in later sections. To effectively tackle the task, basic entities were divided amongst the team members and the more difficult entities were discussed, designed, and debugged as a team, but coding was mainly accomplished by a single person due to inefficiency and complexity in multiple access & simultaneous editing of code for a complicated system.

CADENCE LAYOUTS:

To approach the layouts, each entity was designed as standard-cell instances, or combinations of standard-cell instances for ease of interfacing.

HIERARCHICAL CHIP DESIGN

All higher-level tier entities depended on lower-tier entities. In the hierarchy diagram shown in Figure 1, the general organization has higher-level tier entities at the top and the low-level tiers are at the bottom; however, some relatively independent entities are in the mid-section of the figure.

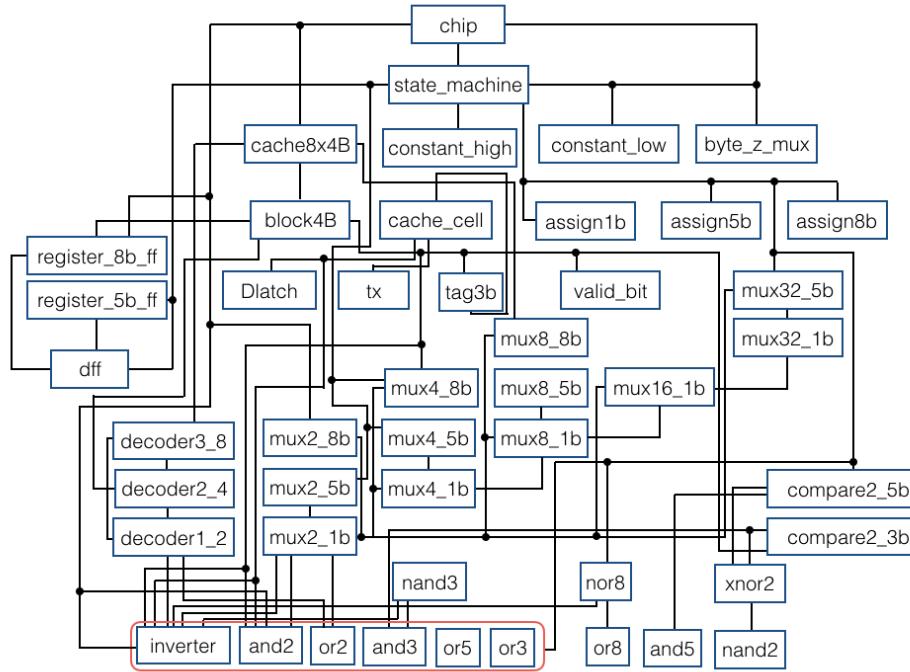


Figure 1: Chip Hierarchy Diagram

The connections describe which entities depend on what other entities; furthermore, if an entity block is at a higher placement in the diagram, all entities that are connected to this entity block and are lower in placement are its dependencies.

Below is a list of brief descriptions of all the blocks shown on the Chip Hierarchy Diagram:

Entity	Description
inverter	Invert one bit from 0 to 1 or 1 to 0
and2	AND two single-bit inputs
or2	OR two single-bit inputs
and3	AND three single-bit inputs
or5	OR five single-bit inputs
or3	OR three single-bit inputs
or 8	OR eight single-bit inputs
and5	AND five single-bit inputs
nand2	AND two single-bit inputs then invert the result
nand3	AND three single-bit inputs then invert the result
nor8	OR eight single-bit inputs then invert the result
xnor2	XNOR two single-bit inputs
decoder1_2	Enables one of the two output signals (active low) depending on the single-bit input
decoder2_4	Enables one of the four output signals (active low) depending on the two single-bit inputs

decoder3_8	Enables one of the eight output signals (active low) depending on the three single-bit inputs
mux2_1b	Outputs one of the two single-bit inputs depending on a single-bit select signal
mux2_5b	Outputs one of the two five-bit inputs depending on a single-bit select signal
mux2_8b	Outputs one of the two eight-bit inputs depending on a single-bit select signal
mux4_1b	Outputs one of the four single-bit inputs depending on a two-bit select signal
mux4_5b	Outputs one of the four five-bit inputs depending on a two-bit select signal
mux4_8b	Outputs one of the four eight-bit inputs depending on a two-bit select signal
mux8_1b	Outputs one of the eight single-bit inputs depending on a three-bit select signal
mux8_5b	Outputs one of the eight five-bit inputs depending on a three-bit select signal
mux8_8b	Outputs one of the eight eight-bit inputs depending on a three-bit select signal
mux16_1b	Outputs one of the sixteen single-bit inputs depending on a four-bit select signal
mux32_1b	Outputs one of the thirty-two single-bit inputs depending on a five-bit select signal
mux32_5b	Outputs one of the thirty-two five-bit inputs depending on a five-bit select signal
compare2_3b	Compares two three-bit inputs and outputs a high signal if the values are equivalent
compare2_5b	Compares two five-bit inputs and outputs a high signal if the values are equivalent
dff	Single-bit input & output, negative-edge-triggered D Flip-Flop that operates on a clock and outputs the input and its inverse
Register5b_ff	Five-bit input & output, negative-edge-triggered D Flip-Flop that operates on a clock and outputs the input and its inverse
register8b_ff	Eight-bit input & output, negative-edge-triggered D Flip-Flop that operates on a clock and outputs the input and its inverse
Dlatch	Positive-level triggered D latch that outputs the input and its inverse
tx	Transmission-gate-based switch
tag3b	Three-bit cache cell that can be written and read from when utilizing a negative-edge triggered clock
valid_bit	Single-bit cache cell that can be written and read from when utilizing a negative-edge triggered clock
block4B	Combines four
cache_cell	Combines a transmission gate and a D latch to store
assign1b	Assigns a single-bit value to another single-bit signal

assign5b	Assigns five single-bit values to a five-bit signal
assign8b	Assigns eight single-bit values to a eight-bit signal
cache8x4B	Provides read and write access and structure for a 4- by 8-byte cache
constant_high	Assign a single-bit value high signal to another single-bit value
constant_low	Assign a single-bit value low signal to another single-bit value
byte_Z_mux	Outputs seven-bits of high signals or impedance
state_machine	Outputs necessary control signals, based on the current state, to properly drive the functionality for the cache chip
chip	The entity interfaced directly by the CPU and memory that encompasses all other entities

The entities in the hierarchy are all structural except for the provided behavioral entities. The byte_Z_mux is also behavioral because from research, there seemed to be no way to output a byte of impedance values without using behavioral logic; however, switching this entity to structural or not using the entity does not really affect the behavior of the cache chip.

REGISTERS

In the design, the registers are used to store values for multiple cycles. There are two types of registers: five-bit and eight-bit. The functionality is shared between the two types of registers except that the eight-bit holds three more bits than the five-bit register. The registers use d flip-flops to retain the values.

The register takes in an input D, and the clock, and outputs whatever is stored from the signal D through Q.

CACHE CELL

The cache cell is designed with a D Latch and a transmission gate; furthermore, the cache cell provides simultaneous read and write capability at the expense of extra area. The inputs are read, write, data and clock, and the output is Q which should reflect the data stored in the cell. The cache cell stores a single-bit value. To store the value for several cycles a sub-clock is used to latch until a write signal occurs.

FOUR-BYTE BLOCK

The four-byte block is comprised of a valid bit, three-bit tag, and four 8-bit registers. The inputs to the block are validate, data, tag, byte select, read, write, reset and clock.

The validate bit, and the write signal create the actual write signal to the registers because if the block is not valid, then it cannot be written to. In addition to the valid-bit checking, tag checking is also necessary so a three-bit comparator is used to see if the correct data block is accessed from memory and is in the cache. Decoders are used to access one of eight registers at a time.

The block will also report if there was a hit or a miss, so if the validate process or tag check had failed, a miss signal will be outputted. Also, eight-bits of data can be outputted if data is being read.

32-BYTE CACHE

The 32-byte cache is comprised of eight four-byte blocks, which are described above and pass the input signals valid bit, three-bit tag, data, address, read, write, reset and clock signals to one of the eight blocks.

Similar to the four-byte block entity, decoders are used by utilizing the address to determine which block and byte should be accessed.

The validate bit, and the write signal create the actual write signal to the registers because if the block is not valid, then it cannot be written to. In addition to the valid-bit checking, tag checking is also necessary so a three-bit comparator is used to see if the correct data block is accessed from memory and is in the cache.

When the block reports a hit/miss, and obtains appropriate data to output, the 32-byte cache will pass it to the rest of the system.

STATE MACHINE

State machine controls signals that are inputted to the other entities. The control signals outputted are dependent on the state. The state machine is implemented with multiplexers and the previous state and outputs of some entities comprise the inputs to the various multiplexers. The only branching within the state machine, besides for reset are when read misses, read hits, write misses or write hits occur.

When the reset signal is set, the current state is set to a five-bit low signal that forces the next state to be the initialize/reset state, which also acts as our idle state.

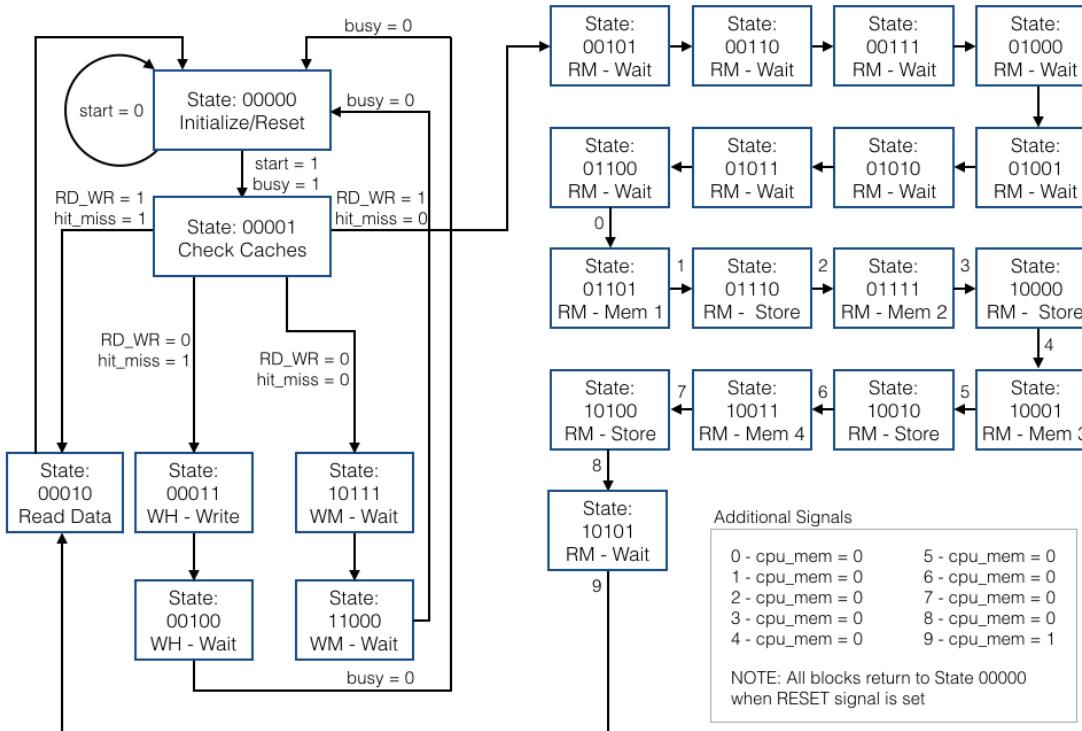


Figure 2: Cache Chip State Machine

TABLE 3: State Transition Diagram

State Description (clk cycle)	State	Next State(s)	Dependencies
Init/Reset	00000	00001	RST Busy/Start
Check Caches (1)	00001	00010 or 00011 or 00101 or 11001	Busy/Start
Read Hit (2)	00010	00000	RM/RH1, RM/RH2, LRU
Write Hit - Write (2)	00011	00100	RM/RH1, RM/RH2, LRU
Write Hit - Wait 1 (3)	00100	00000	
Read Miss - Wait 1 (11)	00101	00110	RM/RH1, RM/RH2, LRU
Read Miss - Wait 2 (12)	00110	00111	
Read Miss - Wait 3 (13)	00111	01000	
Read Miss - Wait 4 (14)	01000	01001	

Read Miss - Wait 5 (15)	01001	01010	
Read Miss - Wait 6 (16)	01010	01011	
Read Miss - Wait 7 (17)	01011	01100	
Read Miss - Wait 8 (18)	01100	01101	
Read Miss - Get Mem 1 (2)	01101	01110	
Read Miss - Store Mem 1 (3)	01110	01111	
Read Miss - Get Mem 2 (4)	01111	10000	
Read Miss - Store Mem 2 (5)	10000	10001	
Read Miss - Get Mem 3 (6)	10001	10010	
Read Miss - Store Mem 3 (7)	10010	10011	
Read Miss - Get Mem 4 (8)	10011	10100	
Read Miss - Store Mem 4 (9)	10100	10101	
Read Miss - Wait 9 (18)	10101	10110	
Read Miss - Return data (10)	10110	00000	
Write Miss - Wait 1 (2)	10111	11000	RM/RH1, RM/RH2, LRU
Write Miss - Wait 2 (3)	11000	00000	

TABLE 4: State Descriptions

State Name	State	Description
Init/Reset	00000	Idle state until CPU signals (start, C _D , C _A , etc) are sent to the cache chip
Check Caches	00001	Check both Cache 0 and Cache 1
Read Hit	00010	One of the Caches recognized that there is a valid block of data with a matching tag and data is returned to the CPU.

Write Hit - Write	00011	One of the Caches recognized that there is a valid block of data with a matching tag and data is returned to the CPU.
Write Hit - Wait 1	00100	NOP to make sure correct timing occurs between the cache chip and the CPU
Read Miss - Wait 1	00101	None of the caches found a valid block with a matching tag so, to operate properly, the chip must wait until inputs are prepared.
Read Miss - Wait 2	00110	None of the caches found a valid block with a matching tag so, to operate properly, the chip must wait again until inputs are prepared.
Read Miss - Wait 3	00111	None of the caches found a valid block with a matching tag so, to operate properly, the chip must wait again until inputs are prepared.
Read Miss - Wait 4	01000	None of the caches found a valid block with a matching tag so, to operate properly, the chip must wait again until inputs are prepared.
Read Miss - Wait 5	01001	None of the caches found a valid block with a matching tag so, to operate properly, the chip must wait again until inputs are prepared.
Read Miss - Wait 6	01010	None of the caches found a valid block with a matching tag so, to operate properly, the chip must wait again until inputs are prepared.
Read Miss - Wait 7	01011	None of the caches found a valid block with a matching tag so, to operate properly, the chip must wait again until inputs are prepared.
Read Miss - Wait 8	01100	None of the caches found a valid block with a matching tag so, to operate properly, the chip must wait again until inputs are prepared.
Read Miss - Get Mem 1	01101	The cache chip can request memory read access to obtain the first byte of data so that the tag in the address matches the tag of the block
Read Miss - Store Mem 1	01110	The first byte of data obtained from the memory is stored in the cache block

Read Miss - Get Mem 2	01111	The cache chip can request memory read access to obtain the second byte of data so that the tag in the address matches the tag of the block
Read Miss - Store Mem 2	10000	The second byte of data obtained from the memory is stored in the cache block
Read Miss - Get Mem 3	10001	The cache chip can request memory read access to obtain the third byte of data so that the tag in the address matches the tag of the block
Read Miss - Store Mem 3	10010	The third byte of data obtained from the memory is stored in the cache block
Read Miss - Get Mem 4	10011	The cache chip can request memory read access to obtain the fourth byte of data so that the tag in the address matches the tag of the block
Read Miss - Store Mem 4	10100	The fourth byte of data obtained from the memory is stored in the cache block
Read Miss - Wait 9	10101	For the read to operate properly, the chip must wait until the CPU is ready to receive data
Read Miss - Return data	10110	Return the byte of data originally requested by the CPU
Write Miss - Wait 1	10111	NOP wait for one cycle
Write Miss - Wait 2	11000	NOP wait for an additional cycle so that the CPU is ready

The tables above describe the state machine behavior and the various states involved. Below are all signals involved in the state machine:

Inputs

<i>start</i>	indicates the start of an operation.
<i>rd_wr</i>	read/write enable; when this signal is 1, a read operation is requested, and when this signal is 0, a write operation is requested
<i>address</i>	eight-bit address associated with the data to be accessed from or written to memory.
<i>hit_miss_0</i>	whether the operation on cache 0 was a hit or miss; when this signal is 1, it is a hit, and when this signal is a 0, it is a miss
<i>hit_miss_1</i>	whether the operation on cache 1 was a hit or miss; when this signal is 1, it is a hit, and when this signal is a 0, it is a miss
<i>rst</i>	reset signal to reset the state machine to its default state

<i>clk</i>	master clock signal
Outputs	
<i>validate</i>	signal to enable validation of a block in the cache
<i>cpu_mem</i>	whether data from the CPU or memory is being used for an operation; when this signal is a 1, data is coming from the CPU, and when this signal is 0, data is coming from the memory
<i>mem_add</i>	the current address of the memory being used
<i>wr_from_mem_addr</i>	the current address in the memory from which the data is being accessed to write into the cache
<i>wr_from_mem</i>	whether or not data is currently being accessed from memory to write
<i>rd_data</i>	whether or not data is currently being read at the current state
<i>rd_0</i>	read enable for cache 0
<i>rd_1</i>	read enable for cache 1
<i>wr_0</i>	write enable for cache 0
<i>wr_1</i>	write enable for cache 1
<i>busy</i>	whether or not an operation is ongoing

LRU & TWO-WAY SET-ASSOCIATIVE CACHE CHIP

An LRU scheme is implemented to create a two-way, set-associative cache. A single-bit signal within the chip, LRU, is used to select the cache that will be overwritten when a read miss occurs; for example, if the LRU bit is 0 the first cache's block should be overwritten, not the second.

The following table describes the LRU behavior:

TABLE 5: LRU Behavior

Operation	LRU Behavior
Read Miss on Cache 0 or Cache 1	LRU = ~LRU
Read Hit on Cache 0	LRU = 1
Write Hit on Cache 0	LRU = 1
Read Hit on Cache 1	LRU = 0
Write Hit on Cache 1	LRU = 0
Write Miss on Cache 0 or Cache 1	LRU = LRU

To briefly describe the contents of the table, the LRU bit toggles when a read miss occurs because a read miss operation depends on the LRU to determine which cache to access. Since the read miss operation uses the LRU cache, the new LRU cache will be the other

one; therefore, toggling the bit is appropriate. During any kind of hit operation, the LRU becomes the value opposite of what was hit, so the LRU may not necessarily change during these operations. For example, if the LRU bit is 1, and cache 0 is read, then the LRU will remain 1. For a write miss operation, nothing will occur because during a write miss operation, there is no operation or actions taken.

Utilizing the LRU scheme, our system supports two 32-byte caches, creating a 64-byte cache.

SIMULATION RESULTS

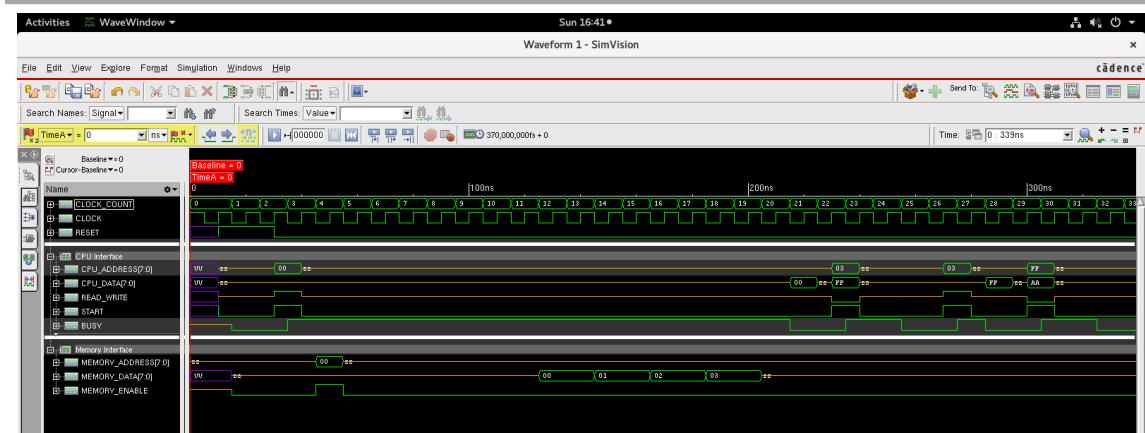


Figure 3: Full Test Bench Output Waveform

The first operation is a read, which misses, and the operation starts during clock cycle 2 ends at clock cycle 20, so the read miss is 19 cycles long. The next operation is a write miss, which starts at cycle 22 and ends at cycle 24, so the write miss is 3 cycles long. The third operation is a read hit which starts at clock cycle 26 and ends at clock cycle 27, so the write hit is 2 cycles long. The final operation is a write miss, which occurs during clock cycles 29 through 31, so the write miss operation is 3 cycles long.

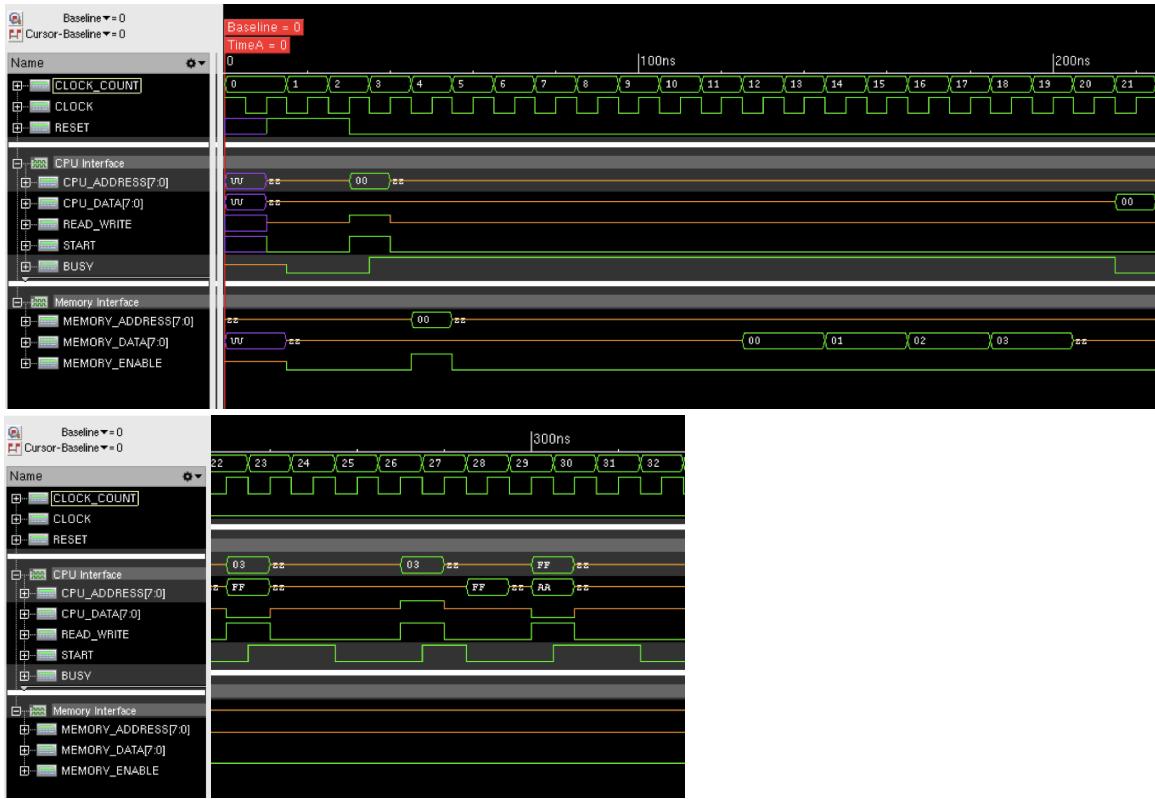


Figure 4: Zoomed-In Test Bench Output Waveform in Similar Format as Dr. Patel's Waveform

LAYOUT RESULTS

The layouts of interest within this project are block4b, cache_cell, cache8x4b, decoder1_2, decoder2_4, decoder3_8, mux2_1b, mux4_1b, mux4_8b, mux8_1b, mux8_8b, tag3b, register8b, register8b_ff, and valid_bit. Their area sizes are described in Table 6.

TABLE 6: Component Sizes

	Length (horizontal, μm)	Width (vertical, μm)	area (μm^2)
block4b			0
cache8x4b			0
cache_cell	69.75	24	1674
decoder1_2	26.7	24	640.8
decoder2_4	140.55	24	3373.2

decoder3_8	434.1	24	10418.4
dff	56.1	24	1346.4
dlatch	38.7	24	928.8
mux2_1b	60.3	24	1447.2
mux2_8b	234.6	45	10557
mux4_1b	176.7	24	4240.8
mux4_8b	700.05	45	31502.25
mux8_1b	234.9	45	10570.5
mux8_8b	468.6	171.9	80552.34
register8b	541.2	24	12988.8
register8b_ff	433.05	24	10393.2
tag3b	204.45	24	4906.8
tx	10.5	24	252
valid_bit	69.75	24	1674

The components listed above rely on basic entities such as inverters, NAND gates, etc, and all the components and entities passed LVS checking tests. The major LVS output test files are shown in Appendix B. The layouts and schematics of all of the components, including the lowest-level ones, are shown in Appendix A.

CONCLUSION

The focus of this portion of the project was designing layouts that will support the logic described above that is embedded in vhdl code from the previous part of the project. The state machine was not included in the layout design due to time constraints; however, the remainder of the chip was designed entirely and successfully in the layouts.

The layouts utilized up to the metal3 layer and followed standard-cell approach. All of the layouts successfully built and provided the team with a large amount of VLSI layout experience.

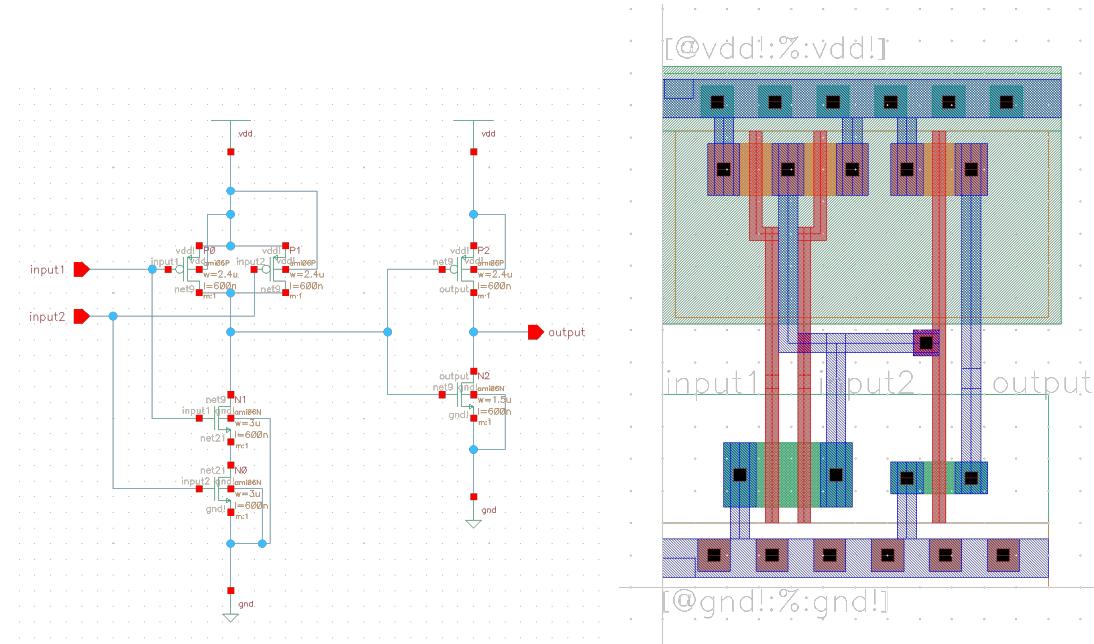
LAYOUT WORK DISTRIBUTION

The successful two-way, set-associative cache was designed by Dang-Quang Tran and Ressa Reneth Sarreal. Below describes the work distribution:

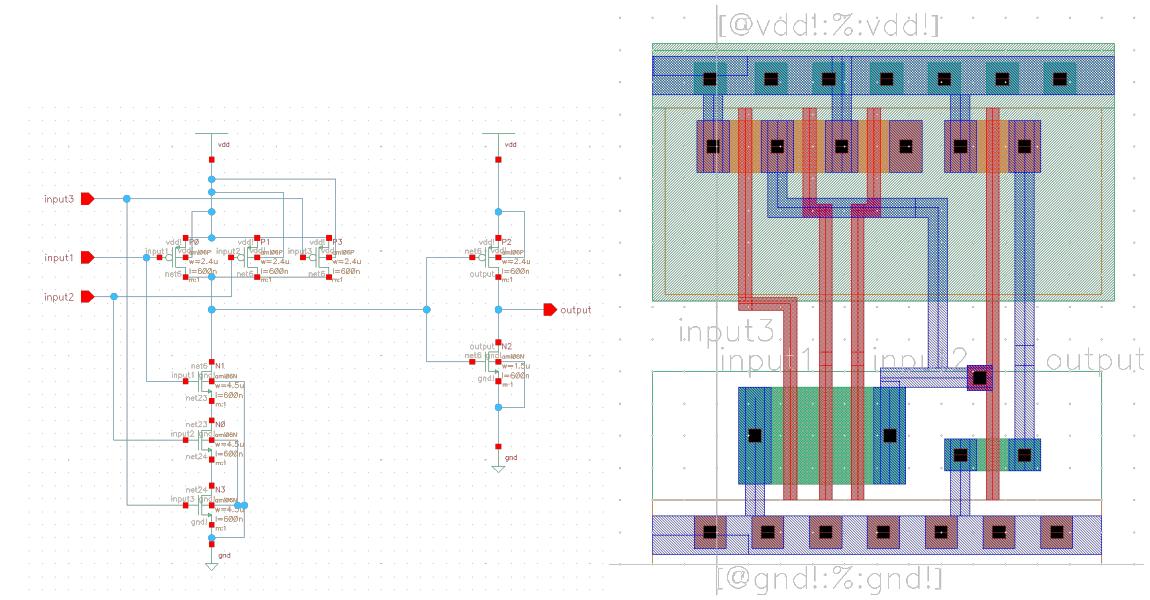
Dang-Quang Tran	Ressa Reneth Sarreal
<ul style="list-style-type: none"> Xnor2 Decoder1_2 Decoder2_4 Decoder3_8 Mux4_1 Dff Register8b 	<ul style="list-style-type: none"> Register8b_ff Dlatch Tx Valid_bit Block4b Cache_cell <ul style="list-style-type: none"> Inverter And2 And3 Or2 Or3 Nand2 Mux2_1b Mux2_8b Mux4_8b Mux8_1b Mux8_8b Cache8x4b Report

APPENDIX A – LAYOUTS & SCHEMATIC

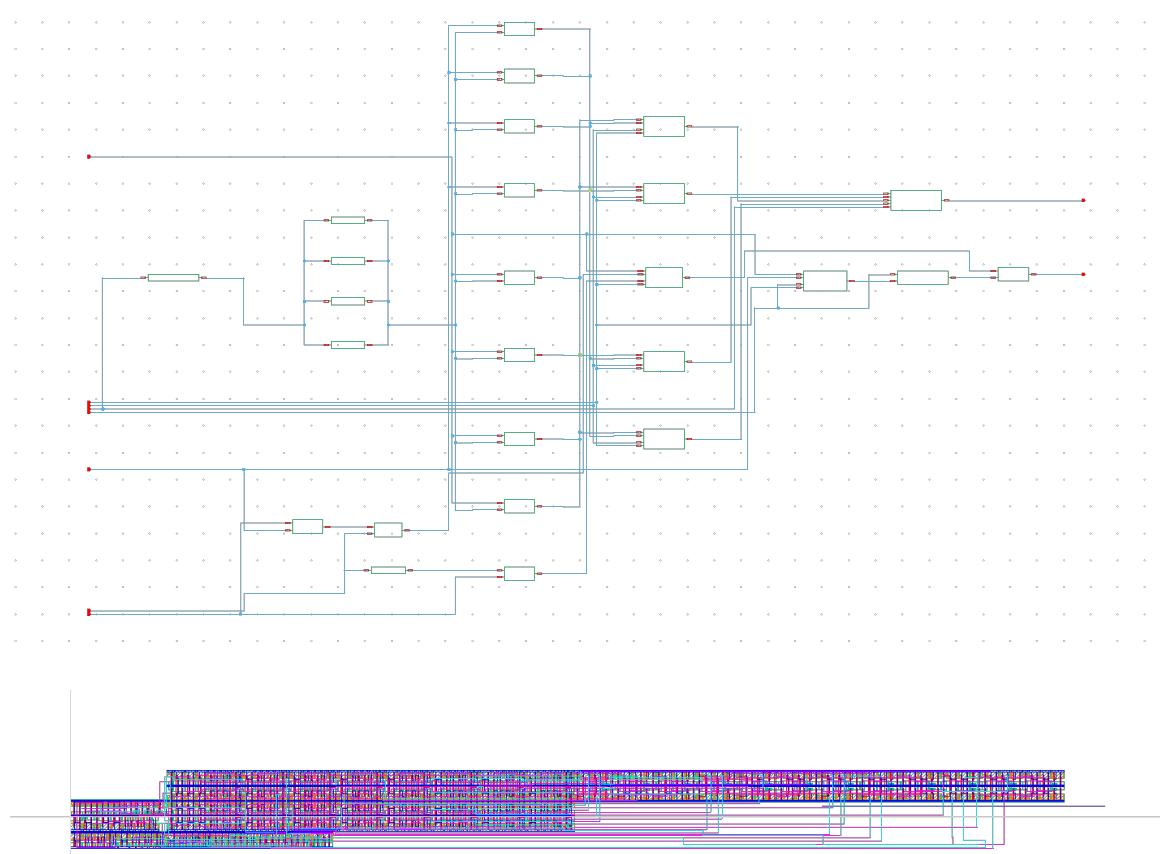
and2



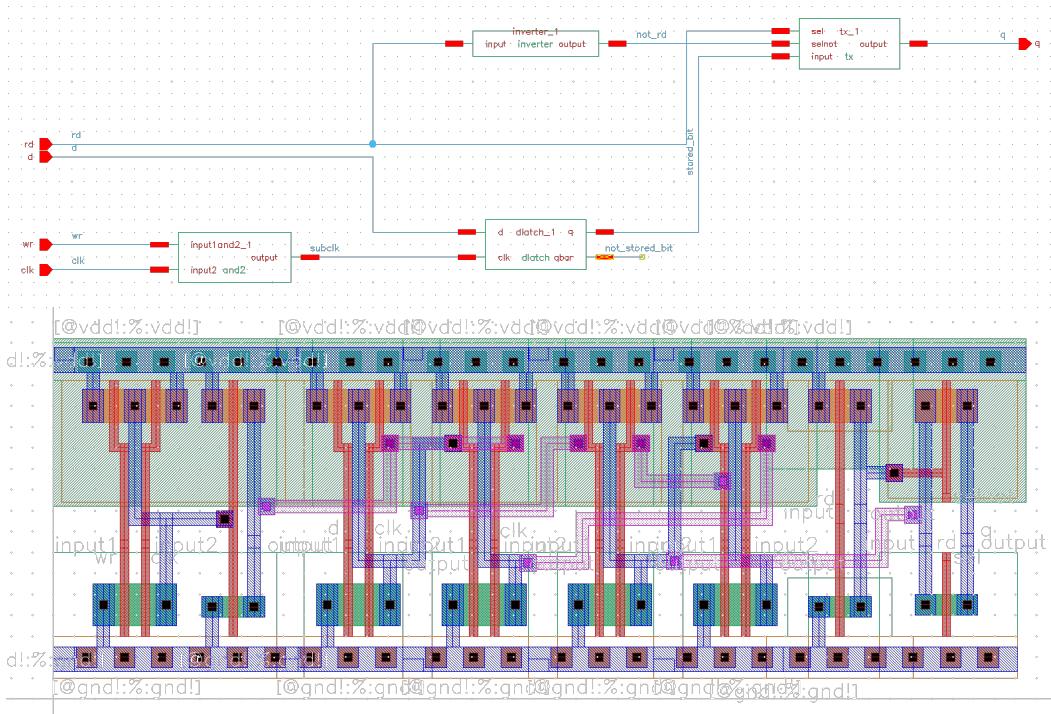
and3



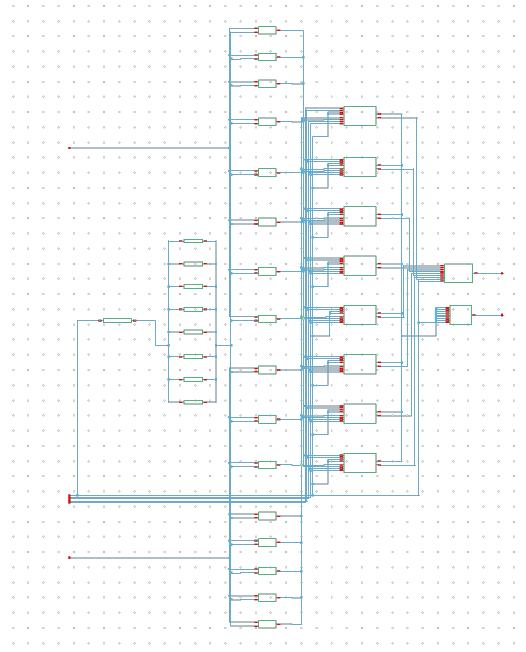
block4b

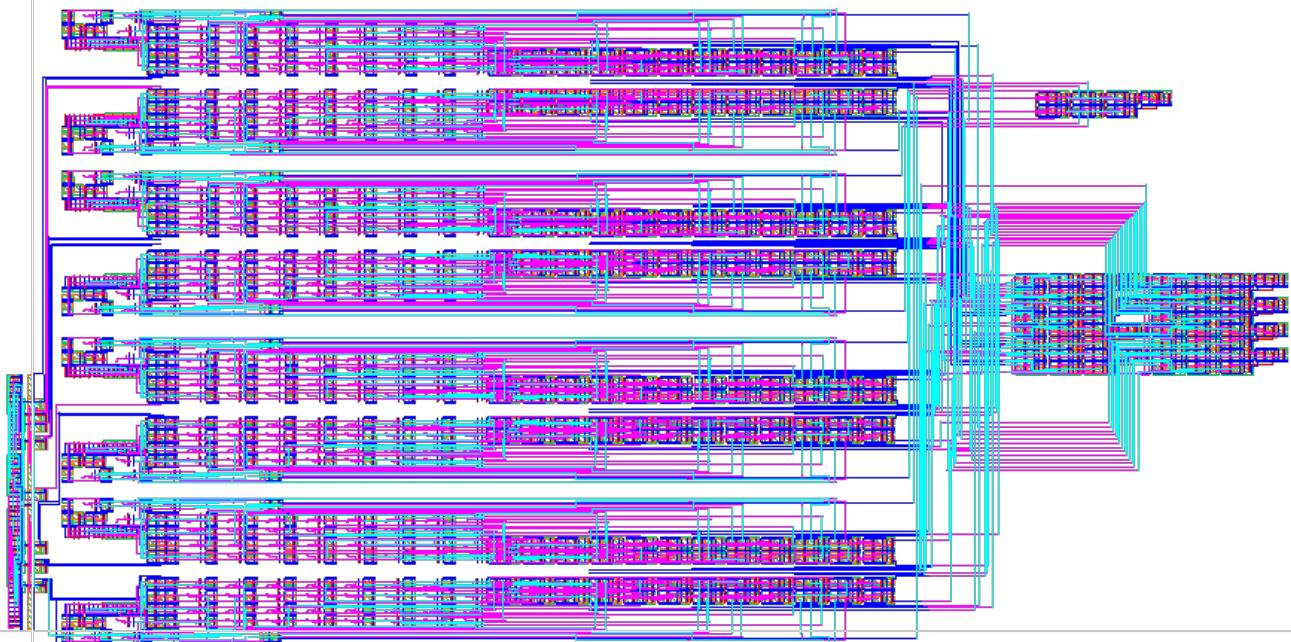


cache_cell

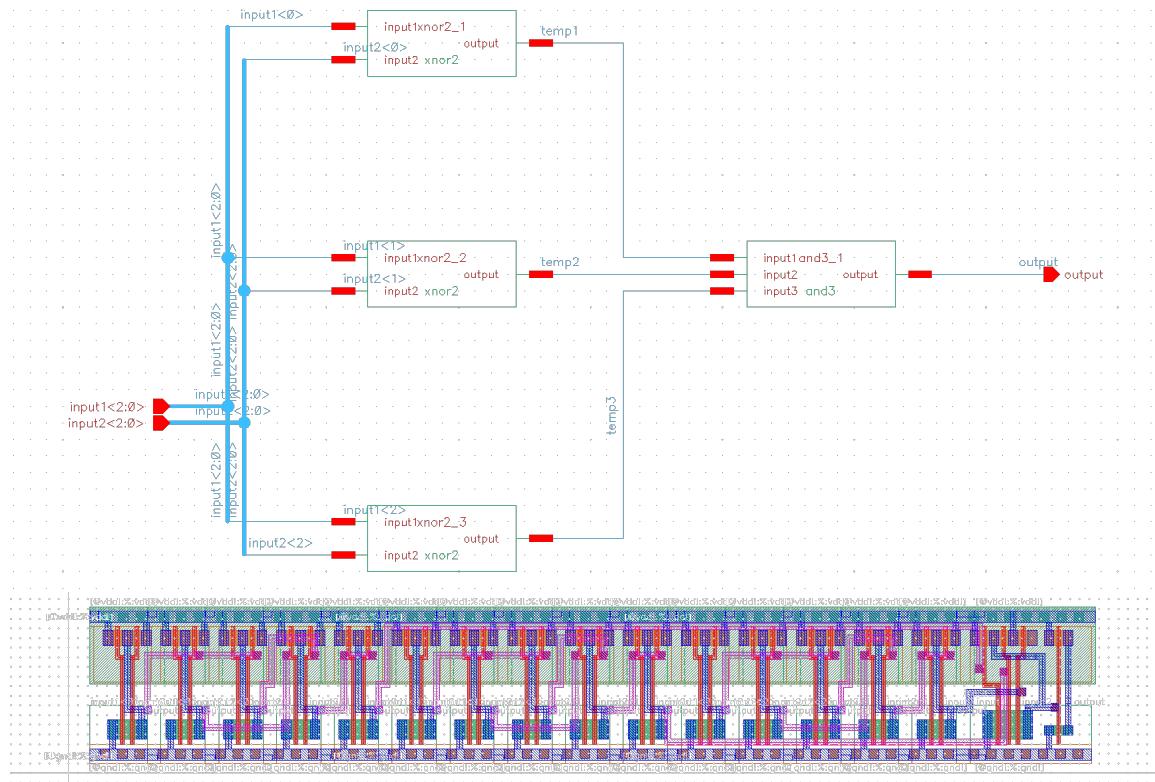


cache8x4b

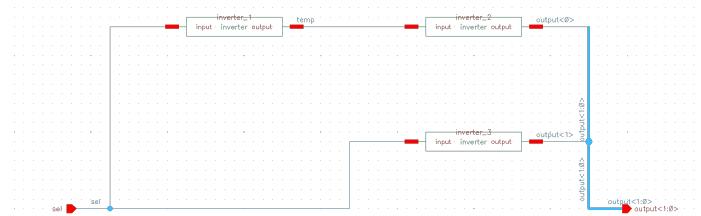


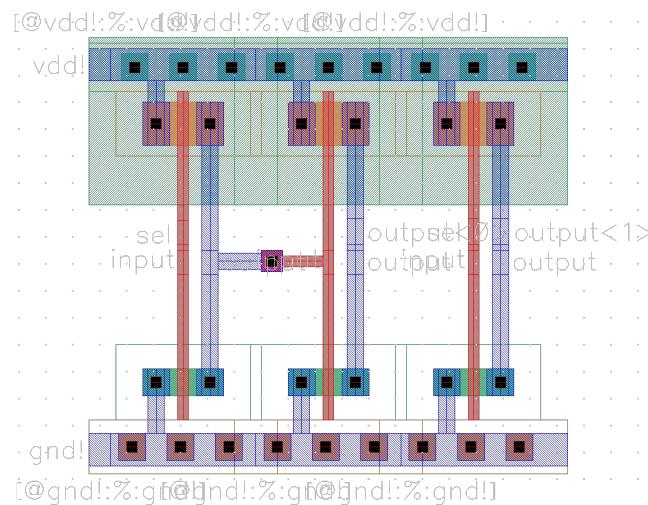


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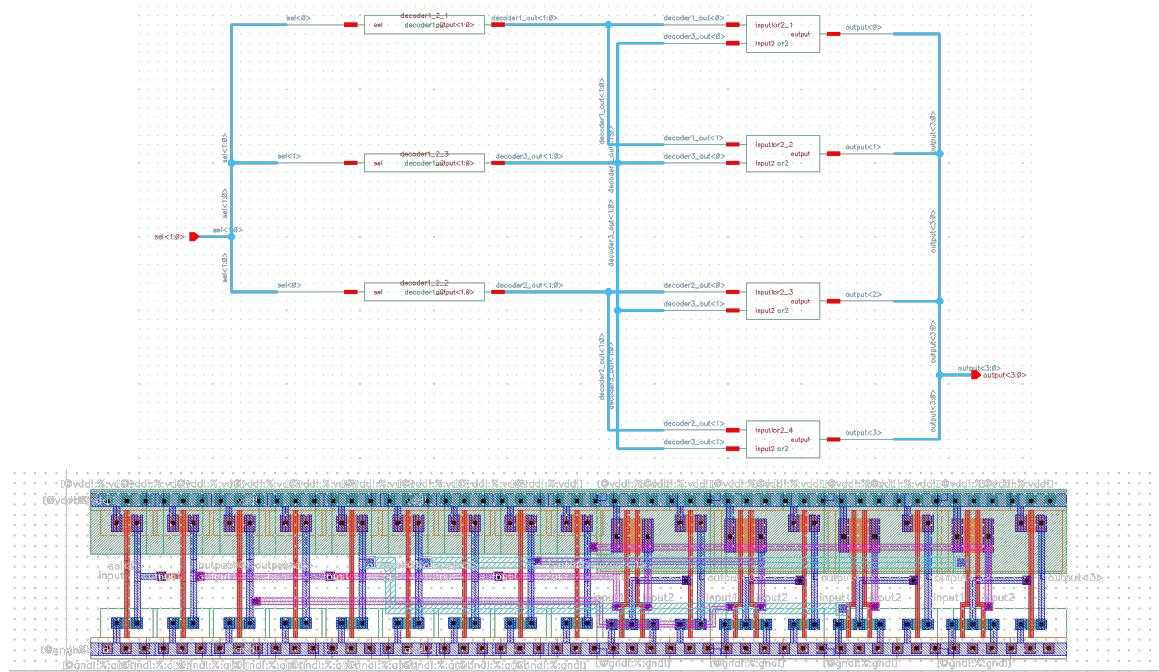


decoder1_2

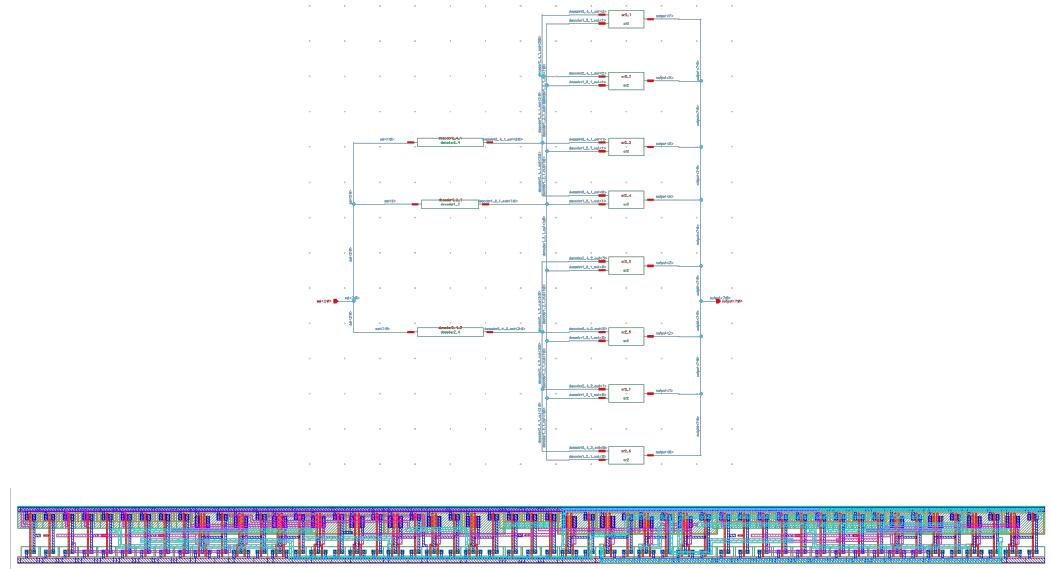




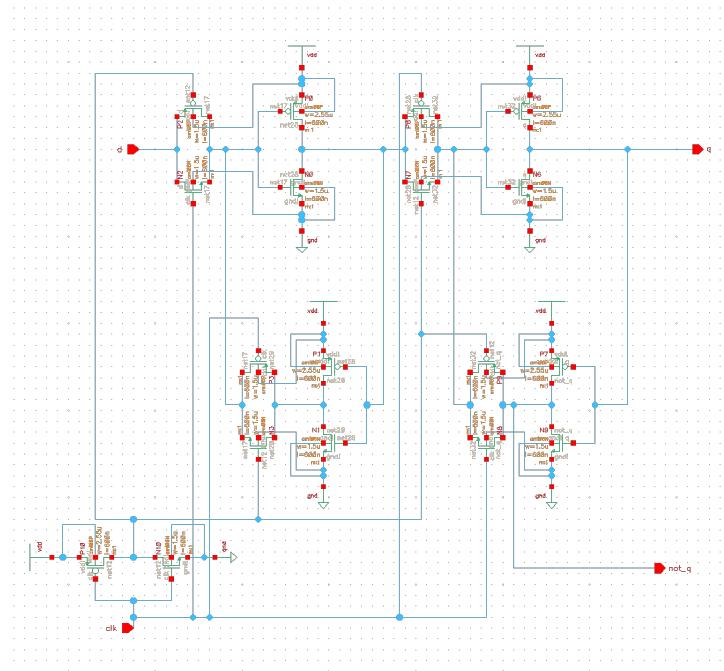
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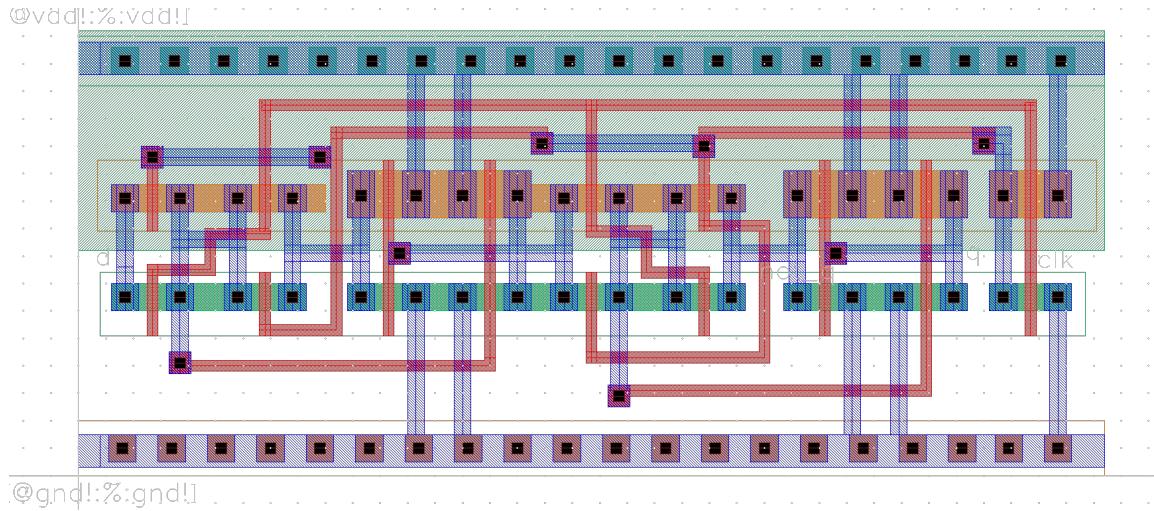


decoder3_8

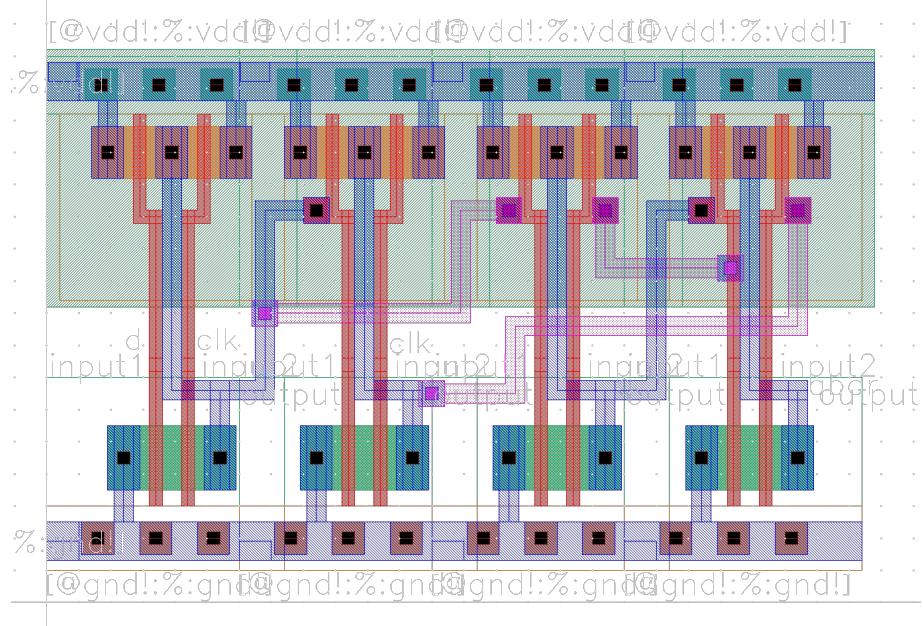
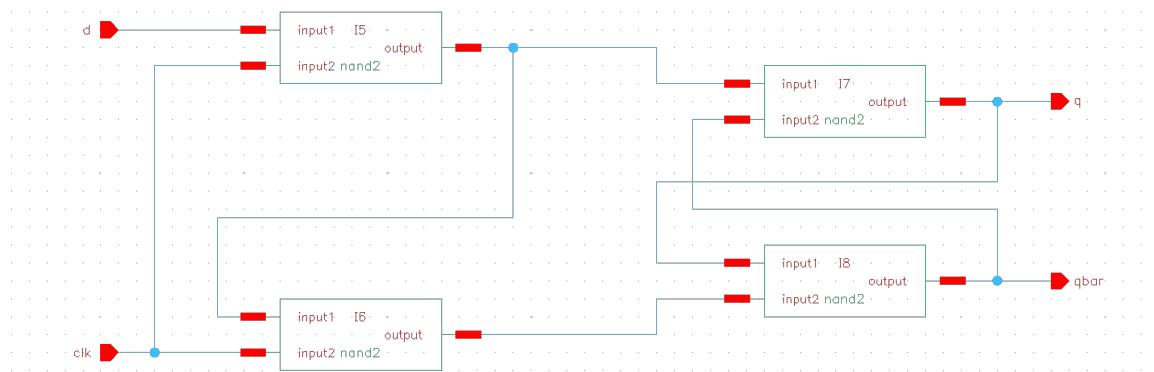


dff

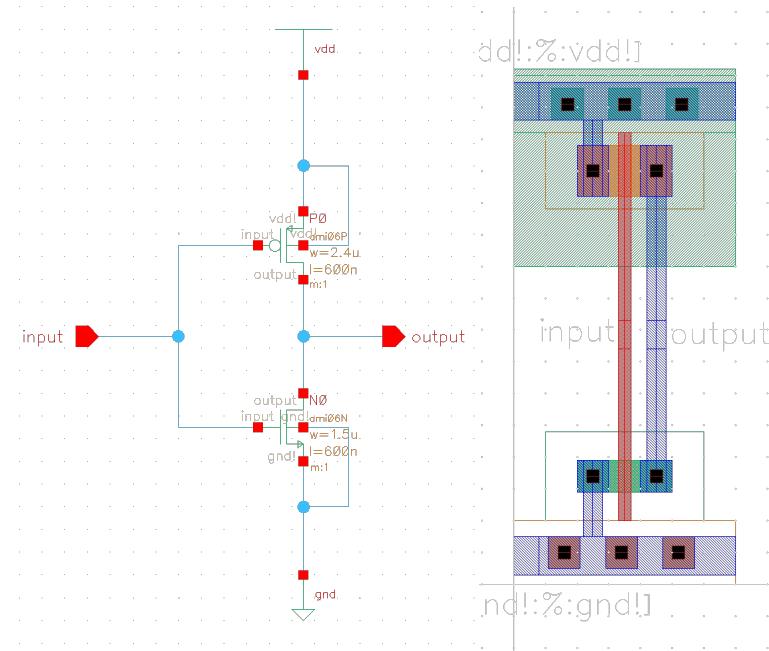




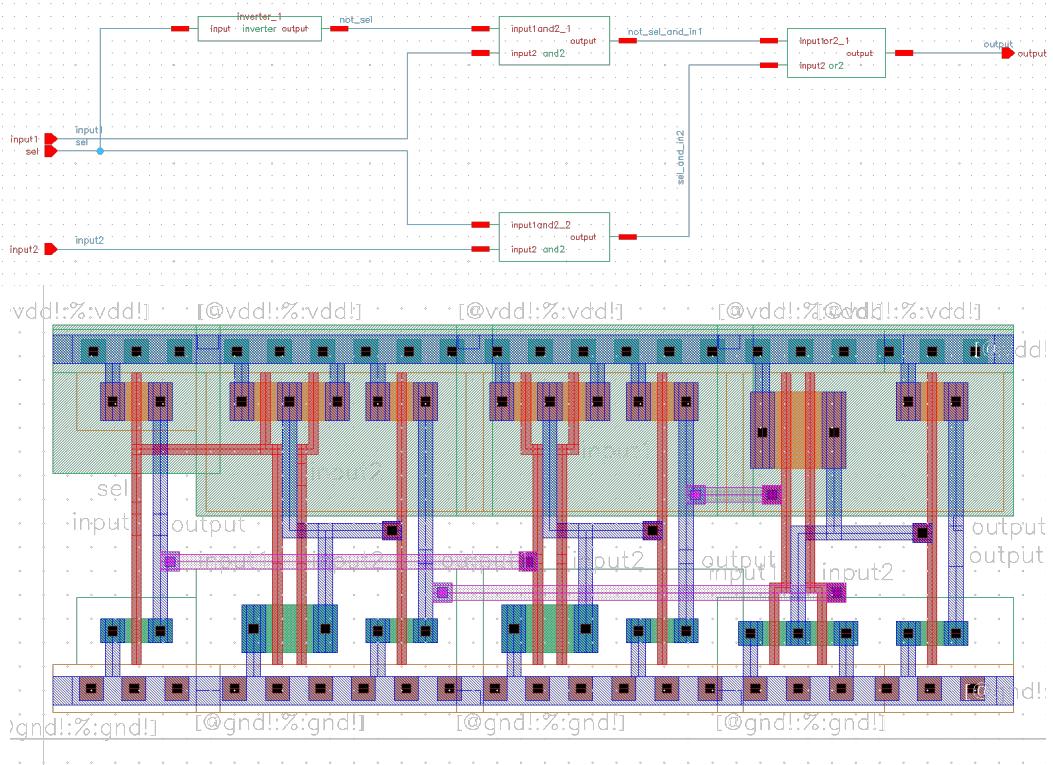
dlatch



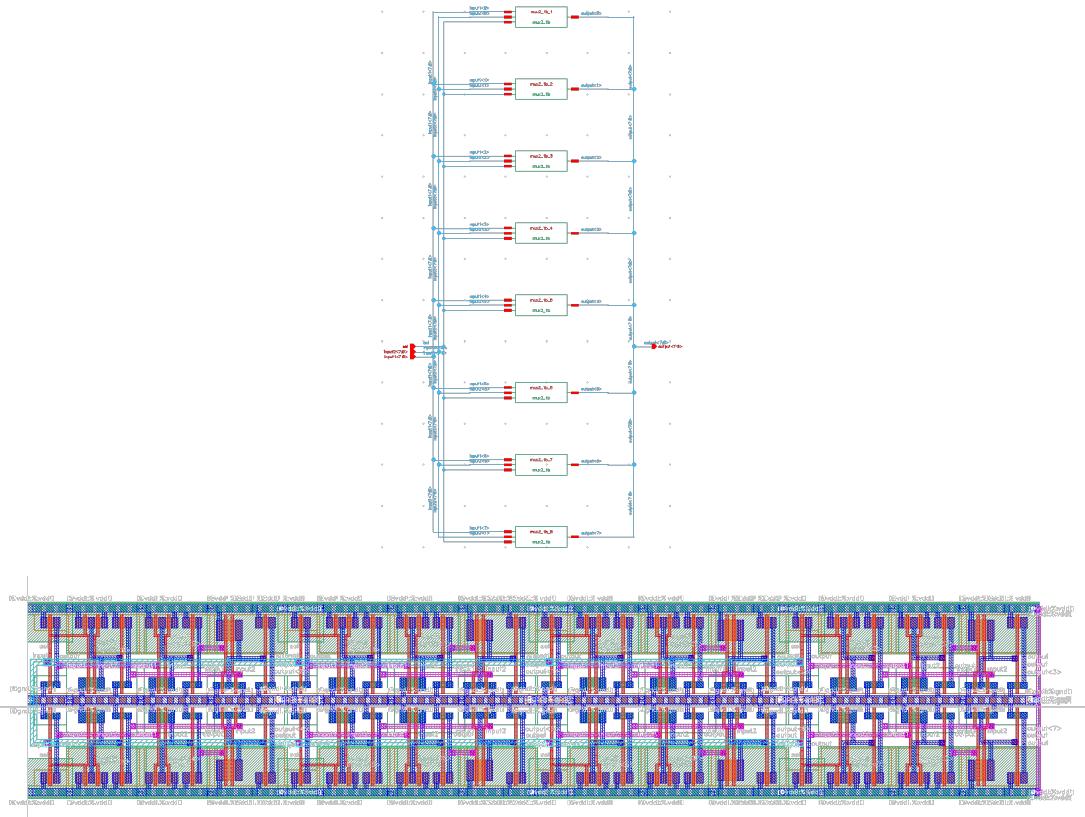
inverter



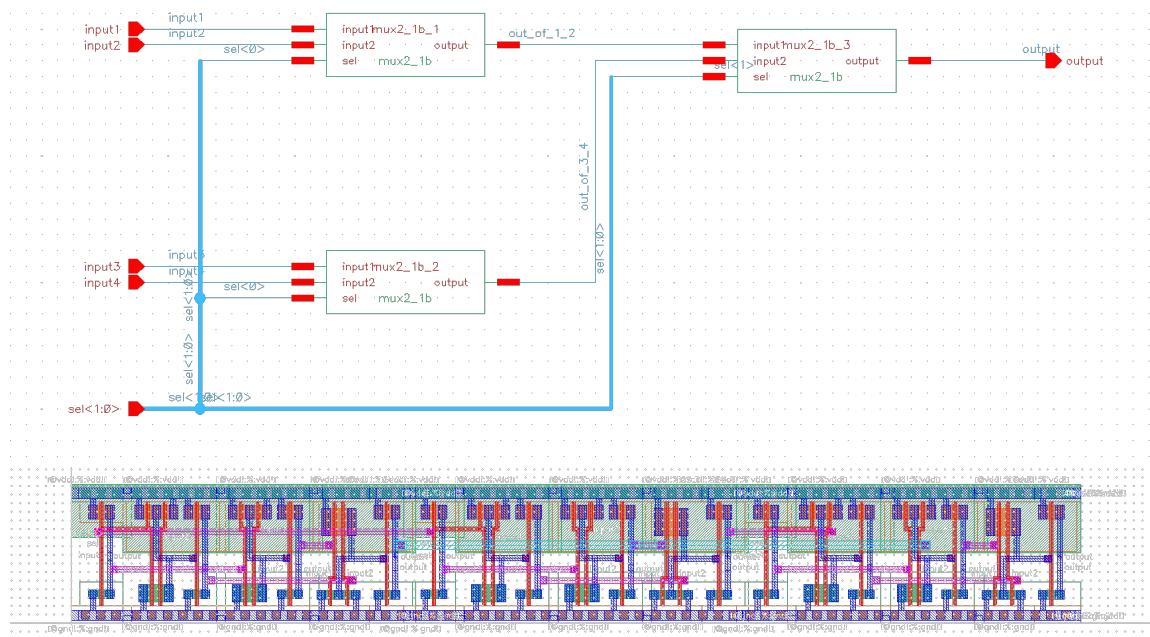
mux2_1b



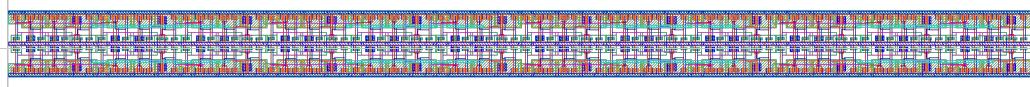
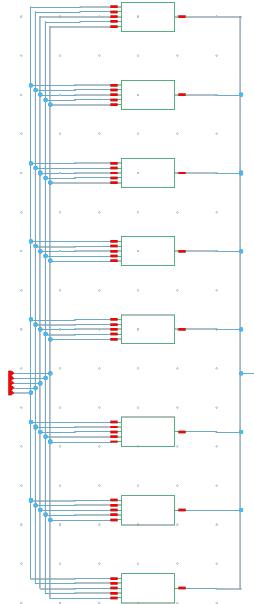
mux2_8



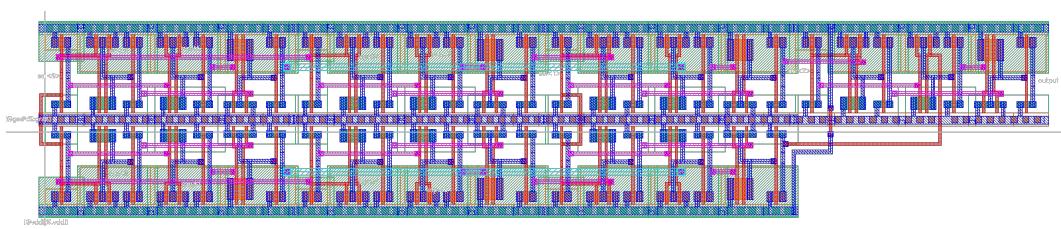
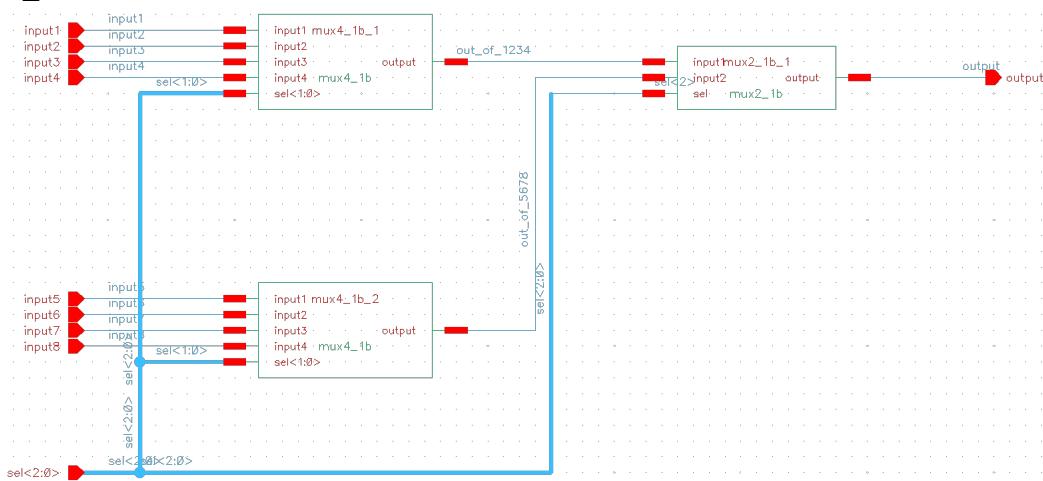
mux4_1b



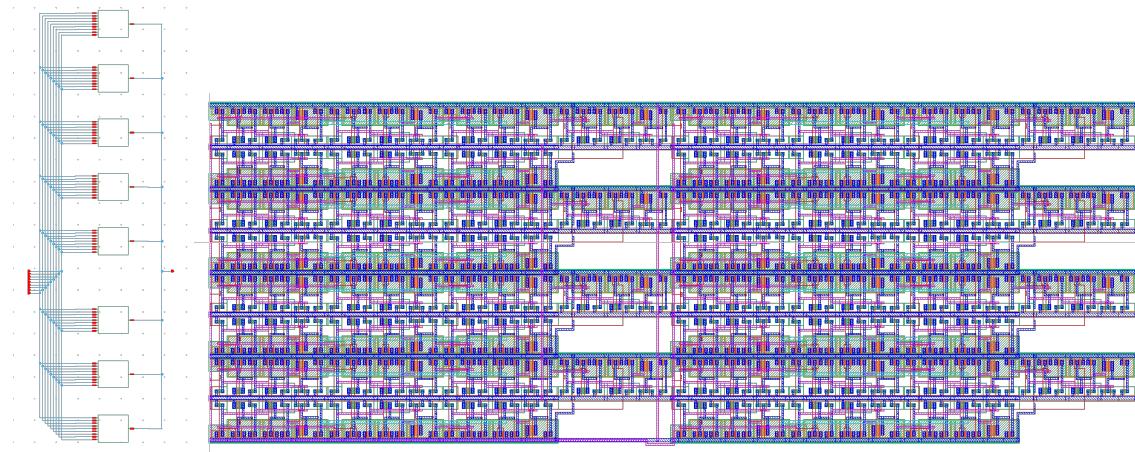
mux4_8b



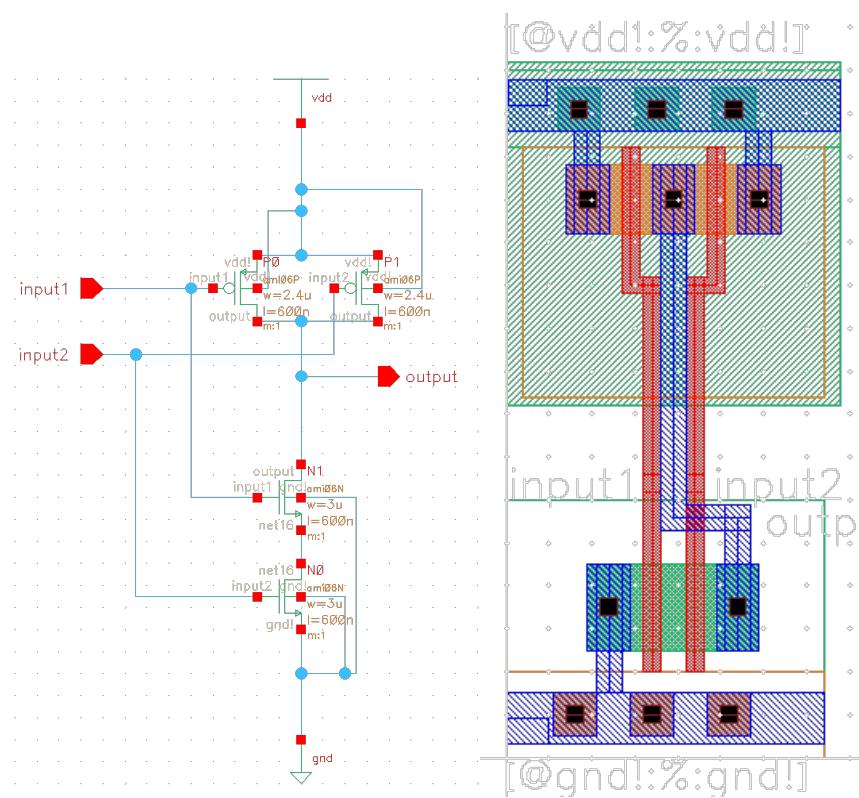
mux8_1b



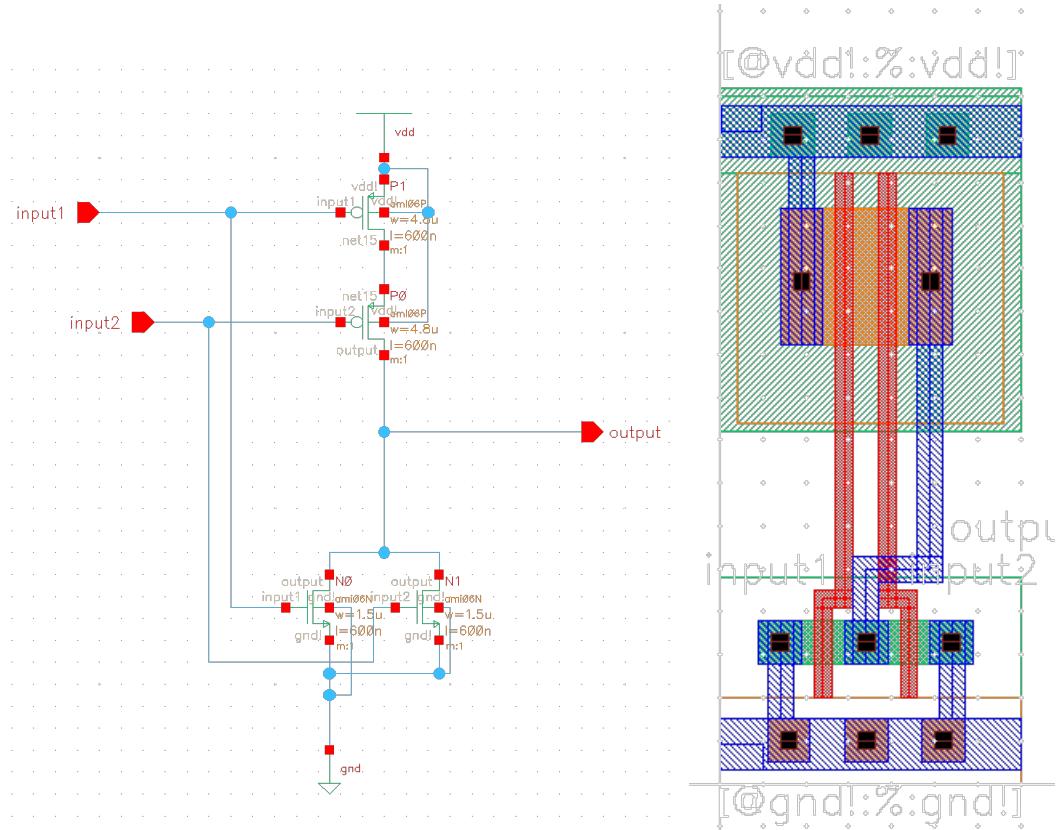
mux8_8b



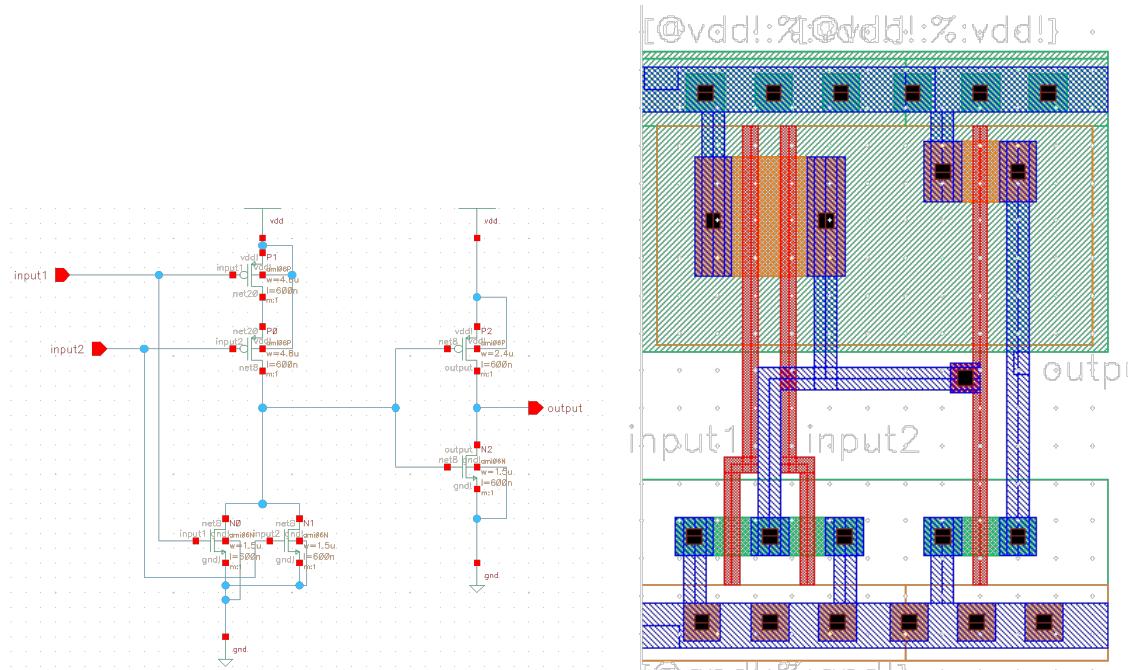
nand2



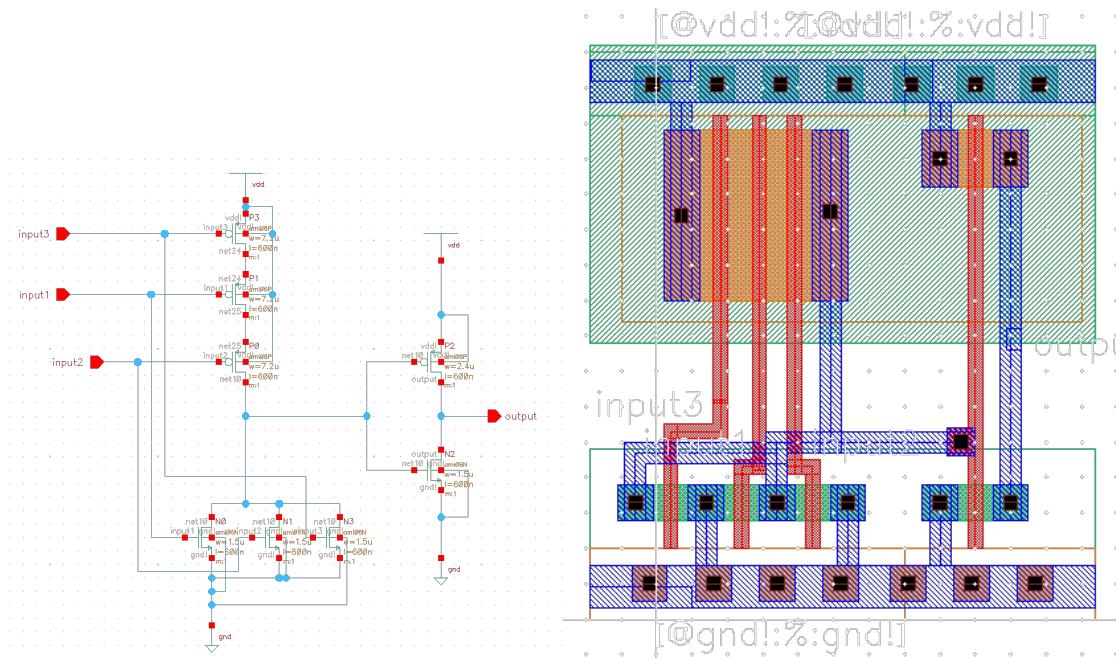
nor2



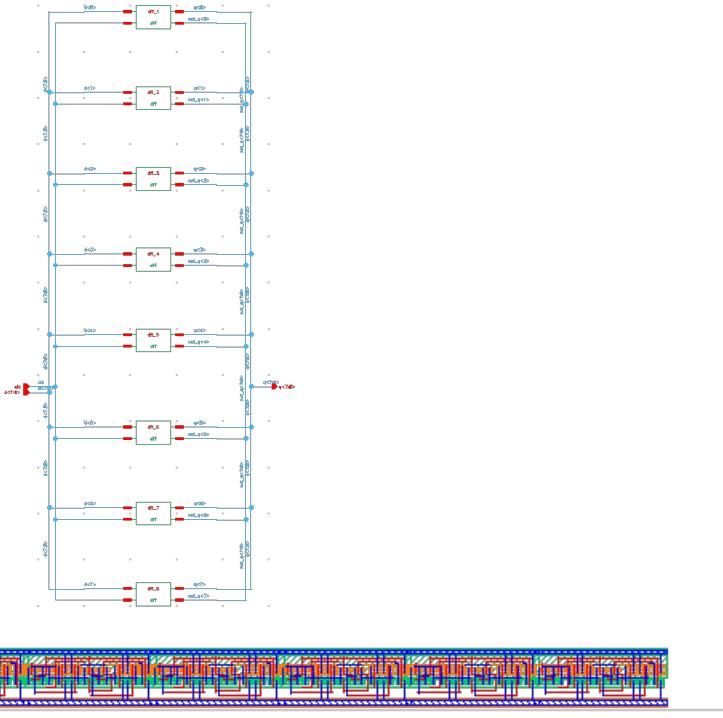
or2



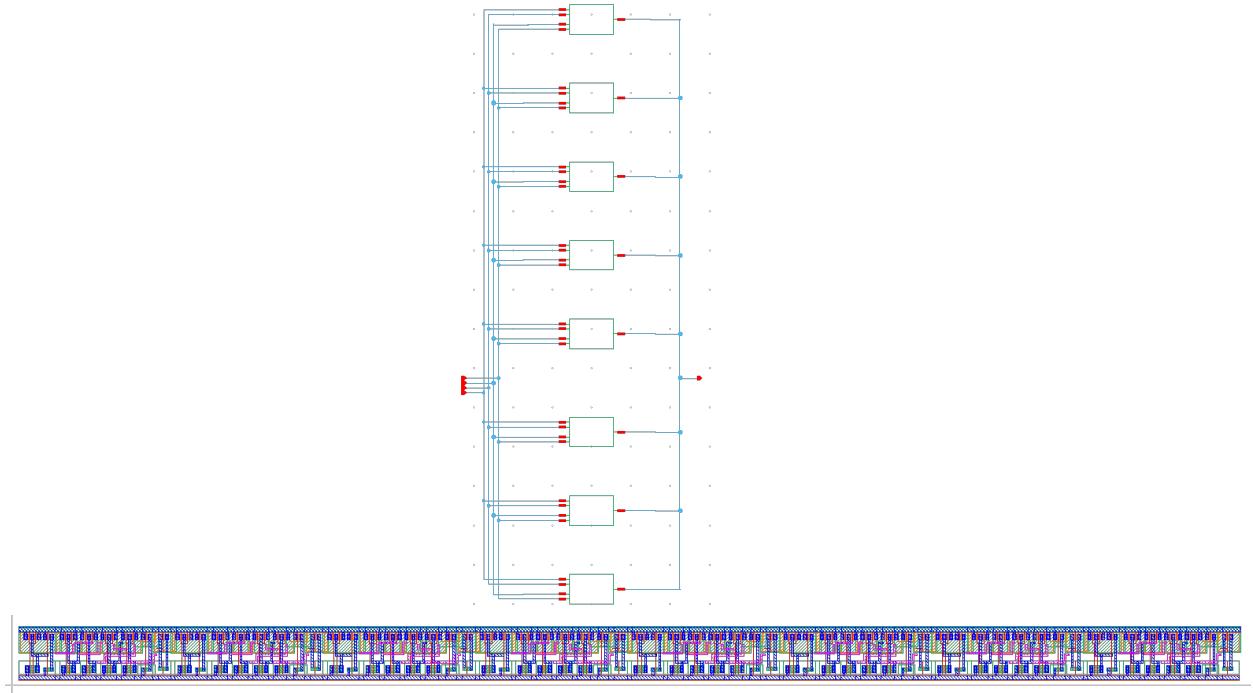
or3



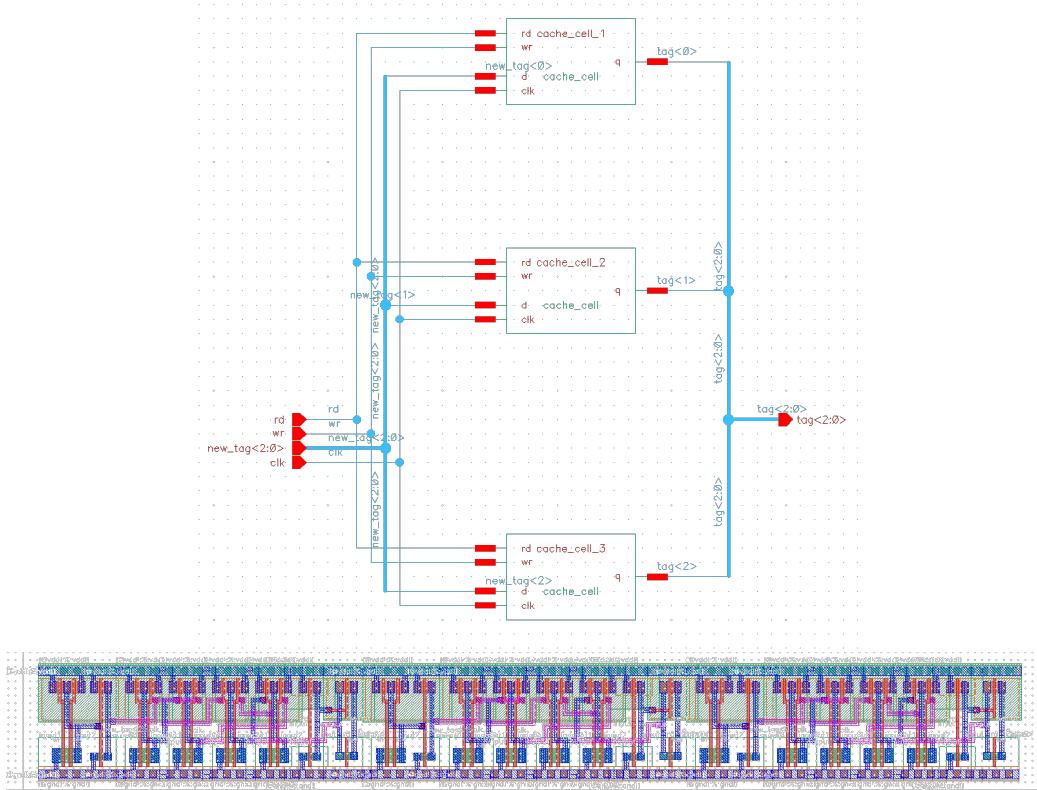
register8b_ff



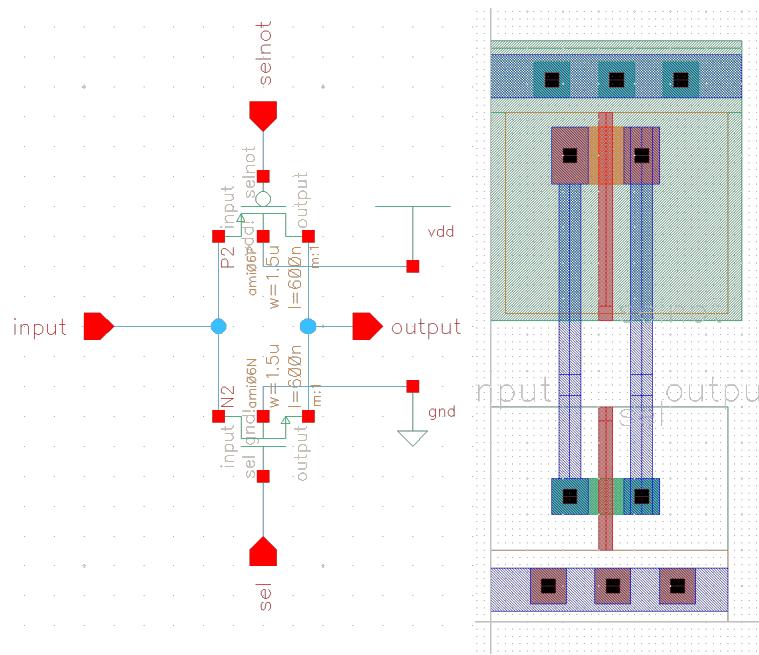
register8b



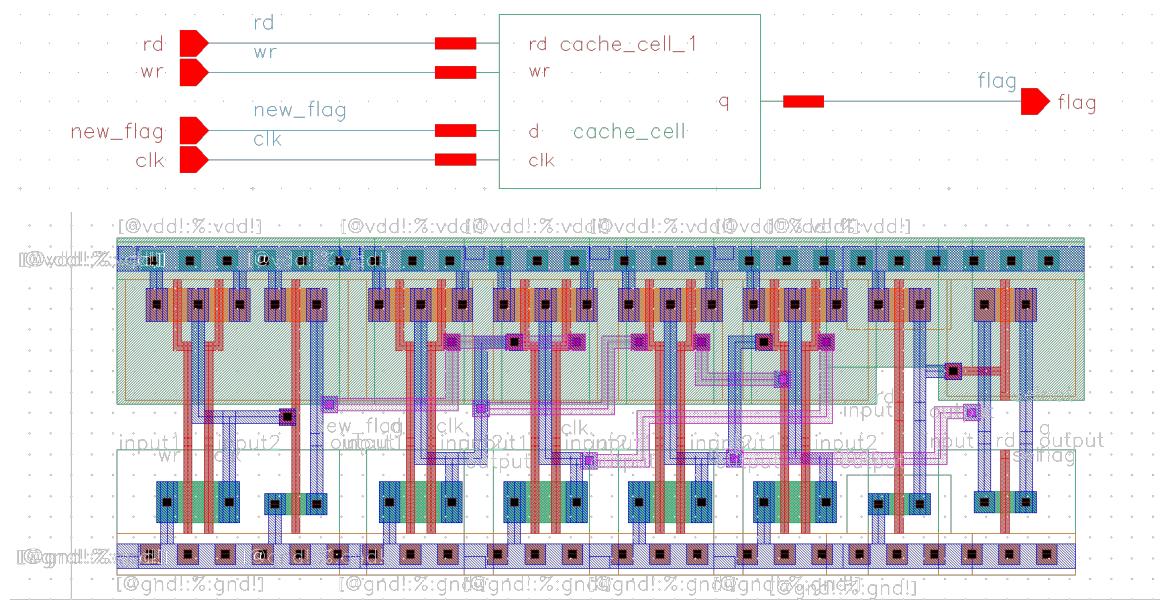
tab3b



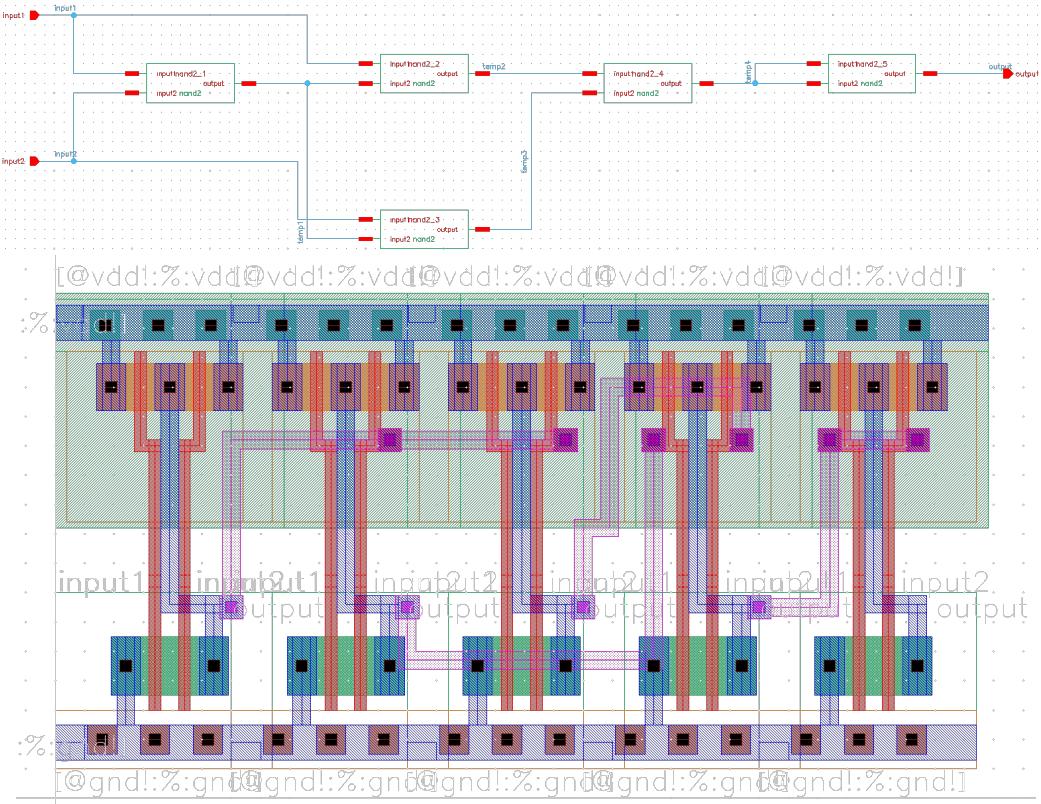
tx



valid_bit



xnor2



APPENDIX B – LVS SI.OUT OUTPUT FILES

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc  
.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/  
CMPE315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Using terminal names as correspondence points.  
7: Compiling Diva LVS rules...  
8:  
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
10:    count  
11:      824      nets  
12:      29       terminals  
13:      804      pmos  
14:      804      nmos  
15:  
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
17:    count  
18:      824      nets  
19:      29       terminals  
20:      804      pmos  
21:      804      nmos  
22:  
23:  
24: Terminal correspondence points  
25: N798   N75   byte_sel<0>  
26: N823   N76   byte_sel<1>  
27: N814   N71   clk  
28: N797   N80   data_in<0>  
29: N822   N46   data_in<1>  
30: N820   N47   data_in<2>  
31: N818   N48   data_in<3>  
32: N816   N49   data_in<4>  
33: N812   N58   data_in<5>  
34: N808   N59   data_in<6>  
35: N804   N60   data_in<7>  
36: N809   N50   data_out<0>  
37: N805   N51   data_out<1>  
38: N801   N52   data_out<2>  
39: N796   N53   data_out<3>  
40: N821   N54   data_out<4>  
41: N819   N55   data_out<5>  
42: N817   N56   data_out<6>  
43: N815   N57   data_out<7>  
44: N800   N0    gnd!  
45: N811   N70   hit_miss  
46: N824   N74   rd  
47: N803   N72   rst  
48: N807   N77   tag<0>  
49: N802   N78   tag<1>  
50: N799   N79   tag<2>  
51: N813   N61   validate  
52: N810   N1    vdd!  
53: N806   N73   wr  
54:  
55: Devices in the netlist but not in the rules:  
56:     pcapacitor  
57: Devices in the rules but not in the netlist:
```

	cap	nfet	pfet	nmos4	pmos4
58:					
59:					
60:	The net-lists match.				
61:					
62:	layout schematic				
63:					instances
64:	un-matched			0	0
65:	rewired			0	0
66:	size errors			0	0
67:	pruned			0	0
68:	active			1608	1608
69:	total			1608	1608
70:					
71:	nets				
72:	un-matched			0	0
73:	merged			0	0
74:	pruned			0	0
75:	active			824	824
76:	total			824	824
77:					
78:	terminals				
79:	un-matched			0	0
80:	matched but			0	0
81:	different type			0	0
82:	total			29	29
83:					
84:	Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic				
85:					
86:	devbad.out:				
87:					
88:	netbad.out:				
89:					
90:	mergenet.out:				
91:					
92:	termbad.out:				
93:					
94:	prunenet.out:				
95:					
96:	prunedev.out:				
97:					
98:	audit.out:				
99:					
100:	101:				
101:	Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout				
102:					
103:	104:				
104:	devbad.out:				
105:					
106:	netbad.out:				
107:					
108:	mergenet.out:				
109:					
110:	termbad.out:				
111:					
112:	prunenet.out:				
113:					
114:	prunedev.out:				
115:					
116:	audit.out:				

```
1: @(#) $CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
2:
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc
.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/
CMPE315/LVS/schematic
4: Like matching is enabled.
5: Net swapping is enabled.
6: Using terminal names as correspondence points.
7: Compiling Diva LVS rules...
8:
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay
out/netlist
10:    count
11:      7262      nets
12:      32       terminals
13:      7187      pmos
14:      7187      nmos
15:
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch
ematic/netlist
17:    count
18:      7210      nets
19:      32       terminals
20:      7187      pmos
21:      7187      nmos
22:
23:
24: Terminal correspondence points
25: N7240  N122  address<0>
26: N7268  N121  address<1>
27: N7265  N120  address<2>
28: N7262  N119  address<3>
29: N7259  N118  address<4>
30: N7254  N117  address<5>
31: N7250  N116  address<6>
32: N7246  N115  address<7>
33: N7256  N110  clk
34: N7239  N114  data_in<0>
35: N7267  N127  data_in<1>
36: N7264  N126  data_in<2>
37: N7261  N125  data_in<3>
38: N7258  N124  data_in<4>
39: N7253  N123  data_in<5>
40: N7248  N83   data_in<6>
41: N7244  N82   data_in<7>
42: N7249  N91   data_out<0>
43: N7245  N92   data_out<1>
44: N7242  N93   data_out<2>
45: N7238  N96   data_out<3>
46: N7266  N97   data_out<4>
47: N7263  N98   data_out<5>
48: N7260  N99   data_out<6>
49: N7257  N100  data_out<7>
50: N7241  N0    gnd!
51: N7252  N109  hit_miss
52: N7269  N113  rd
53: N7243  N111  rst
54: N7255  N90   validate
55: N7251  N1    vdd!
56: N7247  N112  wr
57:
58: Devices in the netlist but not in the rules:
59:      pcapacitor
60: Devices in the rules but not in the netlist:
61:      cap nfet pfet nmos4 pmos4
62:
63: Ill-defined correspondence points.
64:
65:      N7265  N120  Accepted because one is a subset of the other
66:      N7259  N118  Accepted because one is a subset of the other
67:      N7251  N1   Accepted because one is a subset of the other
68:      N7269  N113  Accepted because one is a subset of the other
69:      N7268  N121  Accepted because one is a subset of the other
70:      N7241  N0   Accepted because one is a subset of the other
71:      N7262  N119  Accepted because one is a subset of the other
72:      N7259  N118  Accepted because one is a subset of the other
73:      N7262  N119  Accepted because one is a subset of the other
74:      N7265  N120  Accepted because one is a subset of the other
75:      N7251  N1   Accepted because one is a subset of the other
76:      N7268  N121  Accepted because one is a subset of the other
77:      N7241  N0   Accepted because one is a subset of the other
78:      N7240  N122  Accepted because one is a subset of the other
79:      N7240  N122  Accepted because one is a subset of the other
80:      N7269  N113  Accepted because one is a subset of the other
81:
82:
83: Device summary for layout
84:           bad  total
85:             pmos  29  7187
86:             nmos  26  7187
87:
88:
89: Device summary for schematic
90:           bad  total
91:             pmos  29  7187
92:             nmos  26  7187
93:
94: 11 net-list ambiguities were resolved by random selection.
95:
96: The net-lists failed to match.
97:
98:           layout  schematic
99:                           instances
100:    un-matched          83   83
101:    rewired            124   0
102:    size errors         0   0
103:    pruned             0   0
104:    active              14374  14374
105:    total               14374  14374
106:
107:           nets
108:    un-matched          68   46
109:    merged              30   0
110:    pruned              0   0
111:    active              7262  7210
112:    total               7262  7210
113:
114:           terminals
115:    un-matched          4    4
116:    matched but          0   0
117:    different type        0   0
118:    total                32   32
119:
```

```
120:  
121: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
122:  
123: devbad.out:  
124: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFil  
e.  
125: To see the complete information please see the file:  
126: /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic/devbad.out  
127:  
128: netbad.out:  
129: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFil  
e.  
130: To see the complete information please see the file:  
131: /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic/netbad.out  
132:  
133: mergenet.out:  
134:  
135: termbad.out:  
136: T -1 address<0> /address<0>  
137: ? Terminal address<0> in the schematic failed to match any terminal in the lay  
out.  
138: T -1 address<1> /address<1>  
139: ? Terminal address<1> in the schematic failed to match any terminal in the lay  
out.  
140: T -1 rd /rd  
141: ? Terminal rd in the schematic failed to match any terminal in the layout.  
142: T -1 vdd! /vdd!  
143: ? Terminal vdd! in the schematic failed to match any terminal in the layout.  
144:  
145: prunenet.out:  
146:  
147: prunedev.out:  
148:  
149: audit.out:  
150:  
151:  
152: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
153:  
154: devbad.out:  
155: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFil  
e.  
156: To see the complete information please see the file:  
157: /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout/devbad.out  
158:  
159: netbad.out:  
160: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFil  
e.  
161: To see the complete information please see the file:  
162: /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout/netbad.out  
163:  
164: mergenet.out:  
165: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFil  
e.  
166: To see the complete information please see the file:  
167: /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout/mergenet.out  
168:  
169: termbad.out:  
170: The no. of lines exceeded than specified by the variable lvsLimitLinesInOutFil  
e.  
171: To see the complete information please see the file:  
172: /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout/termbad.out  
173:
```

```
174: prunenet.out:  
175:  
176: prunedev.out:  
177:  
178: audit.out:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Using terminal names as correspondence points.  
7: Compiling Diva LVS rules...  
8:  
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout/netlist  
10:    count  
11:      19      nets  
12:      7       terminals  
13:      13      pmos  
14:      13      nmos  
15:  
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic/netlist  
17:    count  
18:      19      nets  
19:      7       terminals  
20:      13      pmos  
21:      13      nmos  
22:  
23:  
24:     Terminal correspondence points  
25:     N16    N7    clk  
26:     N12    N8    d  
27:     N13    N0    gnd!  
28:     N18    N2    q  
29:     N17    N10   rd  
30:     N15    N1    vdd!  
31:     N14    N9    wr  
32:  
33: Devices in the rules but not in the netlist:  
34:     cap nfet pfet nmos4 pmos4  
35:  
36: The net-lists match.  
37:  
38:           layout schematic  
39:           instances  
40:     un-matched      0      0  
41:     rewired         0      0  
42:     size errors     0      0  
43:     pruned          0      0  
44:     active          26     26  
45:     total           26     26  
46:  
47:           nets  
48:     un-matched      0      0  
49:     merged           0      0  
50:     pruned          0      0  
51:     active          19     19  
52:     total           19     19  
53:  
54:           terminals  
55:     un-matched      0      0  
56:     matched but  
57:     different type  0      0  
58:     total           7      7  
59:  
60:  
61: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
62:  
63: devbad.out:  
64:  
65: netbad.out:  
66:  
67: mergenet.out:  
68:  
69: termbad.out:  
70:  
71: prunenet.out:  
72:  
73: prunedev.out:  
74:  
75: audit.out:  
76:  
77:  
78: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
79:  
80: devbad.out:  
81:  
82: netbad.out:  
83:  
84: mergenet.out:  
85:  
86: termbad.out:  
87:  
88: prunenet.out:  
89:  
90: prunedev.out:  
91:  
92: audit.out:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s /afs/umbc.ed  
u/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/CM  
E315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Compiling Diva LVS rules...  
7:  
8:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
9:         count  
10:        6          nets  
11:        5          terminals  
12:        3          pmos  
13:        3          nmos  
14:  
15:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
16:         count  
17:        6          nets  
18:        5          terminals  
19:        3          pmos  
20:        3          nmos  
21:  
22: Devices in the rules but not in the netlist:  
23:     cap nfet pfet nmos4 pmos4  
24:  
25: The net-lists match.  
26:  
27:             layout schematic  
28:                 instances  
29:     un-matched      0      0  
30:     rewired        0      0  
31:     size errors    0      0  
32:     pruned         0      0  
33:     active         6      6  
34:     total          6      6  
35:  
36:             nets  
37:     un-matched      0      0  
38:     merged          0      0  
39:     pruned          0      0  
40:     active          6      6  
41:     total          6      6  
42:  
43:             terminals  
44:     un-matched      0      0  
45:     matched but  
46:     different type   0      0  
47:     total          5      5  
48:  
49:  
50: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
51:  
52: devbad.out:  
53:  
54: netbad.out:  
55:  
56: mergenet.out:  
57:  
58: termbad.out:  
59:  
60: prunenet.out:  
61:  
62: prunedev.out:  
63:  
64: audit.out:  
65:  
66:  
67: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
68:  
69: devbad.out:  
70:  
71: netbad.out:  
72:  
73: mergenet.out:  
74:  
75: termbad.out:  
76:  
77: prunenet.out:  
78:  
79: prunedev.out:  
80:  
81: audit.out:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s /afs/umbc.ed  
u/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/CM  
E315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Compiling Diva LVS rules...  
7:  
8:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
9:         count  
10:        25          nets  
11:        8           terminals  
12:        21          pmos  
13:        21          nmos  
14:  
15:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
16:         count  
17:        25          nets  
18:        8           terminals  
19:        21          pmos  
20:        21          nmos  
21:  
22: Devices in the rules but not in the netlist:  
23:     cap nfet pfet nmos4 pmos4  
24:  
25: The net-lists match.  
26:  
27:             layout schematic  
28:                 instances  
29:     un-matched      0      0  
30:     rewired        0      0  
31:     size errors    0      0  
32:     pruned         0      0  
33:     active         42     42  
34:     total          42     42  
35:  
36:             nets  
37:     un-matched    0      0  
38:     merged         0      0  
39:     pruned         0      0  
40:     active         25     25  
41:     total          25     25  
42:  
43:             terminals  
44:     un-matched    0      0  
45:     matched but  
46:     different type 0      0  
47:     total          8      8  
48:  
49:  
50: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
51:  
52: devbad.out:  
53:  
54: netbad.out:  
55:  
56: mergenet.out:  
57:  
58: termbad.out:  
59:  
60: prunenet.out:  
61:  
62: prunedev.out:  
63:  
64: audit.out:  
65:  
66:  
67: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
68:  
69: devbad.out:  
70:  
71: netbad.out:  
72:  
73: mergenet.out:  
74:  
75: termbad.out:  
76:  
77: prunenet.out:  
78:  
79: prunedev.out:  
80:  
81: audit.out:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s /afs/umbc.ed  
u/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/CM  
E315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Compiling Diva LVS rules...  
7:  
8: Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
9:      count  
10:     74      nets  
11:     13      terminals  
12:     69      pmos  
13:     69      nmos  
14:  
15: Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
16:      count  
17:     74      nets  
18:     13      terminals  
19:     69      pmos  
20:     69      nmos  
21:  
22: Devices in the netlist but not in the rules:  
23:      pcapacitor  
24: Devices in the rules but not in the netlist:  
25:      cap nfet pfet nmos4 pmos4  
26:  
27: The net-lists match.  
28:  
29:          layout schematic  
30:          instances  
31: un-matched      0      0  
32: rewired        0      0  
33: size errors    0      0  
34: pruned         0      0  
35: active          138    138  
36: total           138    138  
37:  
38:          nets  
39: un-matched      0      0  
40: merged          0      0  
41: pruned          0      0  
42: active          74     74  
43: total           74     74  
44:  
45:          terminals  
46: un-matched      0      0  
47: matched but  
48: different type  0      0  
49: total           13     13  
50:  
51:  
52: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
53:  
54: devbad.out:  
55:  
56: netbad.out:  
57:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s /afs/umbc.ed  
u/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/CMPE  
E315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Compiling Diva LVS rules...  
7:  
8: Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
9: count  
10: 15 nets  
11: 6 terminals  
12: 10 pmos  
13: 10 nmos  
14:  
15: Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
16: count  
17: 15 nets  
18: 6 terminals  
19: 10 pmos  
20: 10 nmos  
21:  
22: Devices in the rules but not in the netlist:  
23: cap nfet pfet nmos4 pmos4  
24:  
25: The net-lists match.  
26:  
27: layout schematic  
28: instances  
29: un-matched 0 0  
30: rewired 0 0  
31: size errors 0 0  
32: pruned 0 0  
33: active 20 20  
34: total 20 20  
35:  
36: nets  
37: un-matched 0 0  
38: merged 0 0  
39: pruned 0 0  
40: active 15 15  
41: total 15 15  
42:  
43: terminals  
44: un-matched 0 0  
45: matched but  
46: different type 0 0  
47: total 6 6  
48:  
49:  
50: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
51:  
52: devbad.out:  
53:  
54: netbad.out:  
55:  
56: mergenet.out:  
57:  
58: termbad.out:  
59:  
60: prunenet.out:  
61:  
62: prunedev.out:  
63:  
64: audit.out:  
65:  
66:  
67: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
68:  
69: devbad.out:  
70:  
71: netbad.out:  
72:  
73: mergenet.out:  
74:  
75: termbad.out:  
76:  
77: prunenet.out:  
78:  
79: prunedev.out:  
80:  
81: audit.out:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s /afs/umbc.ed  
u/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/CM  
E315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Compiling Diva LVS rules...  
7:  
8: Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
9:      count  
10:     38      nets  
11:     9      terminals  
12:    30      pmos  
13:    30      nmox  
14:  
15: Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
16:      count  
17:     38      nets  
18:     9      terminals  
19:    30      pmos  
20:    30      nmox  
21:  
22: Devices in the netlist but not in the rules:  
23:      pcapacitor  
24: Devices in the rules but not in the netlist:  
25:      cap nfet pfet nmox4 pmos4  
26:  
27: The net-lists match.  
28:  
29:          layout schematic  
30:             instances  
31:      un-matched      0      0  
32:      rewired      0      0  
33:      size errors      0      0  
34:      pruned      0      0  
35:      active      60      60  
36:      total      60      60  
37:  
38:          nets  
39:      un-matched      0      0  
40:      merged      0      0  
41:      pruned      0      0  
42:      active      38      38  
43:      total      38      38  
44:  
45:          terminals  
46:      un-matched      0      0  
47:      matched but  
48:      different type      0      0  
49:      total      9      9  
50:  
51:  
52: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
53:  
54: devbad.out:  
55:  
56: netbad.out:  
57:
```

mux4_8b

si.out

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc  
.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/  
CMPE315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Using terminal names as correspondence points.  
7: Compiling Diva LVS rules...  
8:  
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
10:    count  
11:      276      nets  
12:      44      terminals  
13:      240      pmos  
14:      240      nmos  
15:  
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
17:    count  
18:      276      nets  
19:      44      terminals  
20:      240      pmos  
21:      240      nmos  
22:  
23:  
24:     Terminal correspondence points  
25: N236  N0      gnd!  
26: N263  N36     input1<0>  
27: N258  N35     input1<1>  
28: N253  N34     input1<2>  
29: N248  N33     input1<3>  
30: N242  N32     input1<4>  
31: N237  N31     input1<5>  
32: N232  N30     input1<6>  
33: N272  N29     input1<7>  
34: N245  N37     input2<0>  
35: N240  N23     input2<1>  
36: N234  N28     input2<2>  
37: N274  N2      input2<3>  
38: N267  N27     input2<4>  
39: N261  N26     input2<5>  
40: N256  N25     input2<6>  
41: N252  N24     input2<7>  
42: N269  N38     input3<0>  
43: N264  N22     input3<1>  
44: N259  N21     input3<2>  
45: N254  N20     input3<3>  
46: N247  N19     input3<4>  
47: N243  N18     input3<5>  
48: N238  N17     input3<6>  
49: N233  N16     input3<7>  
50: N250  N39     input4<0>  
51: N246  N15     input4<1>  
52: N241  N14     input4<2>  
53: N235  N13     input4<3>  
54: N273  N12     input4<4>  
55: N268  N11     input4<5>  
56: N262  N10     input4<6>  
57: N257  N9      input4<7>  
58: N275  N43     output<0>  
59: N270  N42     output<1>  
60: N265  N41     output<2>  
61: N260  N40     output<3>  
62: N255  N7      output<4>  
63: N249  N6      output<5>  
64: N244  N5      output<6>  
65: N239  N4      output<7>  
66: N271  N3      sel<0>  
67: N266  N8      sel<1>  
68: N251  N1      vdd!  
69:  
70: Devices in the netlist but not in the rules:  
71:      pcapacitor  
72: Devices in the rules but not in the netlist:  
73:      cap nfet pfet nmos4 pmos4  
74:  
75: The net-lists match.  
76:  
77:                                     layout schematic  
78:                                     instances  
79:     un-matched                      0      0  
80:     rewired                         0      0  
81:     size errors                     0      0  
82:     pruned                          0      0  
83:     active                          480    480  
84:     total                           480    480  
85:  
86:                                     nets  
87:     un-matched                      0      0  
88:     merged                          0      0  
89:     pruned                          0      0  
90:     active                          276    276  
91:     total                           276    276  
92:  
93:                                     terminals  
94:     un-matched                      0      0  
95:     matched but                     0      0  
96:     different type                  0      0  
97:     total                           44    44  
98:  
99:  
100: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
101:  
102: devbad.out:  
103:  
104: netbad.out:  
105:  
106: mergenet.out:  
107:  
108: termbad.out:  
109:  
110: prunenet.out:  
111:  
112: prunedev.out:  
113:  
114: audit.out:  
115:  
116:  
117: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
118:  
119: devbad.out:
```

12/10/17
20:43:11

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si.out

120:
121: netbad.out:
122:
123: mergenet.out:
124:
125: termbad.out:
126:
127: prunenet.out:
128:
129: prunedev.out:
130:
131: audit.out:

2

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc  
.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/  
CMPE315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Using terminal names as correspondence points.  
7: Compiling Diva LVS rules...  
8:  
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
10:    count  
11:      83      nets  
12:      14      terminals  
13:      70      pmos  
14:      70      nmos  
15:  
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
17:    count  
18:      83      nets  
19:      14      terminals  
20:      70      pmos  
21:      70      nmos  
22:  
23:  
24: Terminal correspondence points  
25: N71   N0      gnd!  
26: N77   N15     input1  
27: N76   N14     input2  
28: N75   N13     input3  
29: N74   N12     input4  
30: N73   N11     input5  
31: N72   N8      input6  
32: N70   N7      input7  
33: N69   N2      input8  
34: N78   N4      output  
35: N82   N10    sel<0>  
36: N81   N9      sel<1>  
37: N80   N3      sel<2>  
38: N79   N1      vdd!  
39:  
40: Devices in the netlist but not in the rules:  
41:     pcapacitor  
42: Devices in the rules but not in the netlist:  
43:     cap nfet pfet nmos4 pmos4  
44:  
45: The net-lists match.  
46:  
47:           layout schematic  
48:           instances  
49: un-matched      0      0  
50: rewired        0      0  
51: size errors    0      0  
52: pruned         0      0  
53: active          140    140  
54: total           140    140  
55:  
56:           nets  
57: un-matched      0      0  
58: merged          0      0  
59: pruned          0      0  
60: active          83     83  
61: total           83     83  
62:  
63:           terminals  
64: un-matched      0      0  
65: matched but  
66: different type  0      0  
67: total            14    14  
68:  
69:  
70: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
71:  
72: devbad.out:  
73:  
74: netbad.out:  
75:  
76: mergenet.out:  
77:  
78: termbad.out:  
79:  
80: prunenet.out:  
81:  
82: prunedev.out:  
83:  
84: audit.out:  
85:  
86:  
87: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
88:  
89: devbad.out:  
90:  
91: netbad.out:  
92:  
93: mergenet.out:  
94:  
95: termbad.out:  
96:  
97: prunenet.out:  
98:  
99: prunedev.out:  
100:  
101: audit.out:
```

mux8_8b

si.out

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc  
.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/  
CMPE315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Using terminal names as correspondence points.  
7: Compiling Diva LVS rules...  
8:  
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
10:    count  
11:      629      nets  
12:      77       terminals  
13:      560      pmos  
14:      560      nmos  
15:  
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
17:    count  
18:      629      nets  
19:      77       terminals  
20:      560      pmos  
21:      560      nmos  
22:  
23:  
24:     Terminal correspondence points  
25: N559   N0      gnd!  
26: N606   N64     input1<0>  
27: N598   N63     input1<1>  
28: N587   N62     input1<2>  
29: N579   N61     input1<3>  
30: N568   N60     input1<4>  
31: N561   N59     input1<5>  
32: N552   N58     input1<6>  
33: N621   N57     input1<7>  
34: N573   N65     input2<0>  
35: N566   N50     input2<1>  
36: N554   N56     input2<2>  
37: N624   N55     input2<3>  
38: N612   N54     input2<4>  
39: N604   N53     input2<5>  
40: N594   N43     input2<6>  
41: N586   N51     input2<7>  
42: N616   N66     input3<0>  
43: N608   N41     input3<1>  
44: N596   N49     input3<2>  
45: N589   N48     input3<3>  
46: N577   N47     input3<4>  
47: N570   N46     input3<5>  
48: N560   N45     input3<6>  
49: N553   N44     input3<7>  
50: N582   N67     input4<0>  
51: N575   N38     input4<1>  
52: N564   N42     input4<2>  
53: N556   N3      input4<3>  
54: N622   N40     input4<4>  
55: N614   N39     input4<5>  
56: N603   N30     input4<6>  
57: N595   N37     input4<7>  
58: N626   N68     input5<0>  
59: N618   N28     input5<1>  
60: N607   N36     input5<2>  
61: N599   N35     input5<3>  
62: N588   N34     input5<4>  
63: N580   N33     input5<5>  
64: N569   N32     input5<6>  
65: N562   N31     input5<7>  
66: N592   N69     input6<0>  
67: N584   N23     input6<1>  
68: N574   N29     input6<2>  
69: N567   N52     input6<3>  
70: N555   N27     input6<4>  
71: N625   N26     input6<5>  
72: N613   N25     input6<6>  
73: N605   N24     input6<7>  
74: N558   N70     input7<0>  
75: N627   N16     input7<1>  
76: N617   N22     input7<2>  
77: N609   N21     input7<3>  
78: N597   N20     input7<4>  
79: N590   N19     input7<5>  
80: N578   N18     input7<6>  
81: N571   N17     input7<7>  
82: N601   N71     input8<0>  
83: N593   N15     input8<1>  
84: N583   N14     input8<2>  
85: N576   N13     input8<3>  
86: N565   N12     input8<4>  
87: N557   N11     input8<5>  
88: N623   N10     input8<6>  
89: N615   N9      input8<7>  
90: N628   N76     output<0>  
91: N619   N75     output<1>  
92: N610   N74     output<2>  
93: N600   N73     output<3>  
94: N591   N72     output<4>  
95: N581   N2      output<5>  
96: N572   N8      output<6>  
97: N563   N7      output<7>  
98: N620   N6      sel<0>  
99: N611   N5      sel<1>  
100: N602  N4      sel<2>  
101: N585   N1     vdd!  
102:  
103: Devices in the netlist but not in the rules:  
104:      pcapacitor  
105: Devices in the rules but not in the netlist:  
106:      cap nfet pfet nmos4 pmos4  
107:  
108: The net-lists match.  
109:  
110:          layout schematic  
111:                      instances  
112:      un-matched      0      0  
113:      rewired         0      0  
114:      size errors     0      0  
115:      pruned          0      0  
116:      active          1120   1120  
117:      total           1120   1120  
118:  
119:          nets
```

```
120:      un-matched          0      0
121:      merged              0      0
122:      pruned              0      0
123:      active              629    629
124:      total               629    629
125:
126:                      terminals
127:      un-matched          0      0
128:      matched but
129:      different type       0      0
130:      total               77     77
131:
132:
133: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic
134:
135: devbad.out:
136:
137: netbad.out:
138:
139: mergenet.out:
140:
141: termbad.out:
142:
143: prunenet.out:
144:
145: prunedev.out:
146:
147: audit.out:
148:
149:
150: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout
151:
152: devbad.out:
153:
154: netbad.out:
155:
156: mergenet.out:
157:
158: termbad.out:
159:
160: prunenet.out:
161:
162: prunedev.out:
163:
164: audit.out:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc  
.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/  
CMPE315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Using terminal names as correspondence points.  
7: Compiling Diva LVS rules...  
8:  
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
10:    count  
11:      67      nets  
12:      19      terminals  
13:      72      pmos  
14:      72      nmos  
15:  
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
17:    count  
18:      67      nets  
19:      19      terminals  
20:      72      pmos  
21:      72      nmos  
22:  
23:  
24: Terminal correspondence points  
25: N58   N17   clk  
26: N65   N2    d<0>  
27: N63   N3    d<1>  
28: N61   N4    d<2>  
29: N59   N5    d<3>  
30: N56   N6    d<4>  
31: N53   N7    d<5>  
32: N52   N8    d<6>  
33: N50   N9    d<7>  
34: N49   N0    gnd!  
35: N51   N25   q<0>  
36: N48   N24   q<1>  
37: N66   N23   q<2>  
38: N64   N22   q<3>  
39: N62   N21   q<4>  
40: N60   N20   q<5>  
41: N57   N19   q<6>  
42: N54   N18   q<7>  
43: N55   N1    vdd!  
44:  
45: Devices in the rules but not in the netlist:  
46:     cap nfet pfet nmos4 pmos4  
47:  
48: The net-lists match.  
49:  
50:           layout schematic  
51:                   instances  
52:     un-matched      0      0  
53:     rewired        0      0  
54:     size errors     0      0  
55:     pruned         0      0  
56:     active          144    144  
57:     total           144    144  
58:  
59:           nets  
60:     un-matched      0      0  
61:     merged          0      0  
62:     pruned          0      0  
63:     active          67    67  
64:     total           67    67  
65:  
66:           terminals  
67:     un-matched      0      0  
68:     matched but     0      0  
69:     different type   0      0  
70:     total            19    19  
71:  
72:  
73: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
74:  
75: devbad.out:  
76:  
77: netbad.out:  
78:  
79: mergenet.out:  
80:  
81: termbad.out:  
82:  
83: prunenet.out:  
84:  
85: prunedev.out:  
86:  
87: audit.out:  
88:  
89:  
90: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
91:  
92: devbad.out:  
93:  
94: netbad.out:  
95:  
96: mergenet.out:  
97:  
98: termbad.out:  
99:  
100: prunenet.out:  
101:  
102: prunedev.out:  
103:  
104: audit.out:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc  
.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/  
CMPE315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Using terminal names as correspondence points.  
7: Compiling Diva LVS rules...  
8:  
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
10:    count  
11:      117      nets  
12:      21       terminals  
13:      104      pmos  
14:      104      nmos  
15:  
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
17:    count  
18:      117      nets  
19:      21       terminals  
20:      104      pmos  
21:      104      nmos  
22:  
23:  
24: Terminal correspondence points  
25: N107   N2      clk  
26: N114   N18     d<0>  
27: N112   N17     d<1>  
28: N110   N16     d<2>  
29: N108   N15     d<3>  
30: N105   N14     d<4>  
31: N102   N13     d<5>  
32: N100   N12     d<6>  
33: N98    N11     d<7>  
34: N97    N0      gnd!  
35: N99    N20     q<0>  
36: N96    N19     q<1>  
37: N115   N8      q<2>  
38: N113   N7      q<3>  
39: N111   N6      q<4>  
40: N109   N5      q<5>  
41: N106   N4      q<6>  
42: N103   N3      q<7>  
43: N116   N9      rd  
44: N104   N1      vdd!  
45: N101   N10     wr  
46:  
47: Devices in the rules but not in the netlist:  
48:     cap nfet pfet nmos4 pmos4  
49:  
50: The net-lists match.  
51:  
52:           layout schematic  
53:                   instances  
54: un-matched      0      0  
55: rewired         0      0  
56: size errors     0      0  
57: pruned          0      0  
58: active          208    208  
59: total           208    208  
60:  
61:                         nets  
62: un-matched      0      0  
63: merged          0      0  
64: pruned          0      0  
65: active          117    117  
66: total           117    117  
67:  
68:                         terminals  
69: un-matched      0      0  
70: matched but    0      0  
71: different type 0      0  
72: total           21     21  
73:  
74:  
75: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
76:  
77: devbad.out:  
78:  
79: netbad.out:  
80:  
81: mergenet.out:  
82:  
83: termbad.out:  
84:  
85: prunenet.out:  
86:  
87: prunedev.out:  
88:  
89: audit.out:  
90:  
91:  
92: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
93:  
94: devbad.out:  
95:  
96: netbad.out:  
97:  
98: mergenet.out:  
99:  
100: termbad.out:  
101:  
102: prunenet.out:  
103:  
104: prunedev.out:  
105:  
106: audit.out:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/b  
in/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc  
.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/  
CMPE315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Using terminal names as correspondence points.  
7: Compiling Diva LVS rules...  
8:  
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/lay  
out/netlist  
10:    count  
11:      47      nets  
12:      11      terminals  
13:      39      pmos  
14:      39      nmox  
15:  
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/sch  
ematic/netlist  
17:    count  
18:      47      nets  
19:      11      terminals  
20:      39      pmos  
21:      39      nmox  
22:  
23:  
24: Terminal correspondence points  
25: N44   N4    clk  
26: N38   N0    gnd!  
27: N40   N10   new_tag<0>  
28: N37   N9    new_tag<1>  
29: N45   N5    new_tag<2>  
30: N46   N3    rd  
31: N42   N8    tag<0>  
32: N39   N7    tag<1>  
33: N36   N6    tag<2>  
34: N43   N1    vdd!  
35: N41   N2    wr  
36:  
37: Devices in the rules but not in the netlist:  
38:     cap nfet pfet nmos4 pmos4  
39:  
40: The net-lists match.  
41:  
42:           layout schematic  
43:           instances  
44: un-matched      0      0  
45: rewired        0      0  
46: size errors    0      0  
47: pruned         0      0  
48: active          78     78  
49: total           78     78  
50:  
51:           nets  
52: un-matched      0      0  
53: merged          0      0  
54: pruned         0      0  
55: active          47     47  
56: total           47     47  
57:  
58:           terminals  
59: un-matched      0      0  
60: matched but    0      0  
61: different type  0      0  
62: total           11     11  
63:  
64:  
65: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
66:  
67: devbad.out:  
68:  
69: netbad.out:  
70:  
71: mergenet.out:  
72:  
73: termbad.out:  
74:  
75: prunenet.out:  
76:  
77: prunedev.out:  
78:  
79: audit.out:  
80:  
81:  
82: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
83:  
84: devbad.out:  
85:  
86: netbad.out:  
87:  
88: mergenet.out:  
89:  
90: termbad.out:  
91:  
92: prunenet.out:  
93:  
94: prunedev.out:  
95:  
96: audit.out:
```

```
1: @(#)SCDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $  
2:  
3: Command line: /afs/umbc.edu/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS -l -s -t /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
4: Like matching is enabled.  
5: Net swapping is enabled.  
6: Using terminal names as correspondence points.  
7: Compiling Diva LVS rules...  
8:  
9:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout/netlist  
10:    count  
11:      19      nets  
12:      7       terminals  
13:      13      pmos  
14:      13      nmos  
15:  
16:     Net-list summary for /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic/netlist  
17:    count  
18:      19      nets  
19:      7       terminals  
20:      13      pmos  
21:      13      nmos  
22:  
23:  
24:     Terminal correspondence points  
25:   N16   N3      clk  
26:   N13   N2      flag  
27:   N12   N0      gnd!  
28:   N17   N4      new_flag  
29:   N18   N6      rd  
30:   N15   N1      vdd!  
31:   N14   N5      wr  
32:  
33: Devices in the rules but not in the netlist:  
34:     cap nfet pfet nmos4 pmos4  
35:  
36: The net-lists match.  
37:  
38:           layout schematic  
39:             instances  
40:   un-matched      0      0  
41:   rewired        0      0  
42:   size errors    0      0  
43:   pruned         0      0  
44:   active          26     26  
45:   total           26     26  
46:  
47:           nets  
48:   un-matched      0      0  
49:   merged          0      0  
50:   pruned          0      0  
51:   active          19     19  
52:   total           19     19  
53:  
54:           terminals  
55:   un-matched      0      0  
56:   matched but  
57:   different type  0      0  
58:     total          7      7  
59:  
60:  
61: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/schematic  
62:  
63: devbad.out:  
64:  
65: netbad.out:  
66:  
67: mergenet.out:  
68:  
69: termbad.out:  
70:  
71: prunenet.out:  
72:  
73: prunedev.out:  
74:  
75: audit.out:  
76:  
77:  
78: Probe files from /afs/umbc.edu/users/s/a/saressal/home/CMPE315/LVS/layout  
79:  
80: devbad.out:  
81:  
82: netbad.out:  
83:  
84: mergenet.out:  
85:  
86: termbad.out:  
87:  
88: prunenet.out:  
89:  
90: prunedev.out:  
91:  
92: audit.out:
```