

# Robert Samuel Bao

robertsbao@gmail.com | 240-750-7079 | www.linkedin.com/in/robert-bao

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## EDUCATION

### **University of Illinois Urbana-Champaign | GPA: 3.95/4.0**

*Bachelor's of Science in Computer Engineering with Highest Honors, IEEE-HKN*

August 2021 - May 2024

- Computer Architecture, VLSI System Design, Operating Systems, Digital Systems

*MS/PhD in Computer Engineering, Promise of Excellence Fellowship*

August 2024 - May 2026/2029

## SKILLS

Software: C/C++, Python, Assembly, Git

Hardware: Verilog/SystemVerilog, Quartus, Vivado, RISC-V, Synopsys (Verdi, DesignVision), I2C, SPI, Cadence Virtuoso

## EXPERIENCE

### **IBM | Sr. Chip Design Intern**

May 2024 – August 2024

- Working on the pre-silicon performance verification team
- Creating C/Assembly test programs to ensure expected performance of processor

### **IBM | Processor Logic Design Intern**

May 2023 – August 2023

- Contributed to development of future Z CPUs by discovering up to 15% IPC improvements for target workloads
- Developed new branch prediction architectures for future Power and Z-mainframe processors
- Integrated separate Power and Z branch prediction models into one standardized model, allowing for easier data analysis
- Automated simulation runs and data analysis from benchmarks and tuned branch prediction structure parameters to optimize performance

### **ECE Department at UIUC | Course Assistant for ECE 110/210/220/385**

January 2022 – Present

- Taught lab curriculum alongside graduate TAs for Intro to Electronics, Analog Signal Processing, Computer Systems & Programming, and Digital Systems Lab; working ~10hrs/week
- Assisted students in completing projects such as superheterodyne AM receivers and SystemVerilog SoC designs
- Guided students through building circuits and emphasized conceptual understanding of analog circuits, digital logic, signal processing, and C programming

### **Healthcare Engineering Systems Center at UIUC | Research Assistant**

March 2023 – May 2023

- Built clinical breast examination training simulator by using Arduino to collect and send data in real time from a force sensing array to server via MQTT protocol; worked ~10hrs/week
- Created augmented reality app using Vuforia in Unity to fetch and display force data on a virtual phantom

## PROJECTS

### **Basic Macro Devices RISC-V CPU | UIUC (ECE411 - Computer Organization & Design)**

March 2024 - May 2024

- Built a 2-way superscalar Out-Of-Order RISC-V CPU using explicit register renaming supporting RISC-V(IM) ISA
- Features include Dadda multiplier, Synopsys IP divider, BTB & BHT/GShare tournament branch predictor, 4-way set-associative PLRU pipelined caches with next-line prefetcher
- Verified design using random coverage, Synopsys VCS and Verdi, Spike

### **32-bit RISC-V Datapath | UIUC (ECE425 - VLSI System Design)**

March 2024

- Created (from scratch) schematic and layout for a RISC-V CPU Datapath including register file, ALU, barrel shifter
- Used bit sliced design to maximize reusability and minimize area consumption

### **Pipelined RISC-V CPU | UIUC (ECE411 - Computer Organization & Design)**

February 2024

- Built a RISC-V CPU with 5-stage pipeline in SystemVerilog
- Included data forwarding, static branch prediction, and stalling to resolve data/control hazards and improve performance; also accounted for variable memory response delays

### **391OS | UIUC (ECE391 - Computer Systems & Engineering)**

December 2023

- Collaborated with a four person team to build a Linux-like operating system from scratch including global descriptor table, interrupt descriptor table, paging, file system, system calls, interrupts, and several hardware drivers (RTC, keyboard, PIC, PIT, terminal)
- Implemented multiple terminal screens and round-robin scheduling

### **Object-tracking Camera & Sensor Suite | UIUC (ECE437 - Sensors & Instrumentation)**

December 2023

- Programmed I2C and SPI protocols from scratch, implemented in Verilog on OpalKelly XEM7310 development board
- Implemented block-throttled pipe communications to achieve over 20 frames per second from onboard camera while also collecting data from magnetometer and accelerometer
- Interfaced FPGA with Python/OpenCV for image processing and thresholding to control a PWM motor for tracking