Complete IRQ 8-Bit Data Bus 15 0 ADC Multiplexer ADC CTRL and Status ADC Data Register Select (ADMUX) Register (ADCSRA) (ADCH/ADCL) MUX0 ADFR REFS0 MUX2 MUX1 MIX3 ADPS2 ADPS1 ADPS0 ADCF9:01 MUX Decoder Prescaler Selection Conversion Logic AVCC Internal 1.1V Sample and Hold Reference Comparator AREF 10-Bit DAC Temperature Sensor GND Bandgap Reference ADC7 ADC6 Input ADC MUX Multiplexer ADC5 Output ADC4 ADC3 ADC2 ADC1 ADC0

**ADC** Conversion

Figure 23-1. Analog to Digital Converter Block Schematic Operation

The analog input channel is selected by writing to the MUX bits in ADMUX. Any of the ADC input pins, as well as GND and a fixed bandgap voltage reference, can be selected as single ended inputs to the ADC. The ADC is enabled by setting the ADC Enable bit, ADEN in ADCSRA. Voltage reference and input channel selections will not go into effect until ADEN is set. The ADC does not consume power when ADEN is cleared, so it is recommended to switch off the ADC before entering power saving sleep modes.

The ADC generates a 10-bit result which is presented in the ADC data registers, ADCH and ADCL. By default, the result is presented right adjusted, but can optionally be presented left adjusted by setting the ADLAR bit in ADMUX.

If the result is left adjusted and no more than 8-bit precision is required, it is sufficient to read ADCH. Otherwise, ADCL must be read first, then ADCH, to ensure that the content of the data registers belongs to the same conversion. Once ADCL is read, ADC access to data registers is blocked.