Nova Blocking Word Extension (Dusky■Petrel)

This document defines the **Blocking Word** CPU extension for Dusky■Petrel. It provides a cooperative "sleep until event" facility while remaining transparent to legacy Nova software that does not use it. When the CPU accesses a designated memory address and the word is not yet ready, the CPU suspends instruction execution while I/O devices (including the watchdog timer) continue to run. The CPU resumes when an event marks the word ready.

Configuration (Host Side)

```
[cpu.blocking_word]
enabled = true            ; default: false (feature disabled)
address = 0o77776         ; physical word address
wake_on_interrupts = true
```

Guest■Visible Semantics

```
* The blocking word behaves like ordinary memory when <ready>.
* When the CPU executes a memory access (e.g., LDA/STA/ISZ) to the blocking address:
  - If <ready> = false → CPU enters Blocked state; PC does not advance; the access is
    not yet completed; devices continue ticking.
  - If <ready> = true  → access completes normally.
* When an event occurs, a device ORs one or more bits into the blocking word and marks
  it <ready>. If the CPU is blocked, it is resumed and the suspended instruction is
  retried. To the guest, the access appears as a long memory cycle.
```

Event Signaling

```
Devices may OR cause bits into the blocking word:
  bit 0 = keyboard input available
  bit 1 = watchdog fired
  bit n = device■defined event

After handling events, guest code should clear the word (write 0) before blocking again.
```

Waking Rules

```
* Device■driven wake: writing a non■zero value to the blocking word marks it ready
  and wakes the CPU.
* Optional wake■on■interrupts: if enabled, any pending interrupt also wakes the CPU;
  interrupt delivery proceeds as usual.
```

Typical Usage Pattern (Nova Assembly)

```
WAIT_EVENT:
        LDA     0, BLOCKLOC      ; blocks until BLOCKLOC != 0
        ; AC0 now contains event bits
        LDA     1, #0
        STA     1, BLOCKLOC      ; clear events
        JMP     WAIT_EVENT
```

Emulator Behavior (Summary)

* CPU states: Running | BlockedOnMem | Halted
* When BlockedOnMem, the main loop advances devices to the next event deadline and resumes the CPU when the blocking word becomes ready (or an interrupt wakes it).
* The blocked instruction is retried on resume; architectural state is unchanged.

Compatibility Notes

* Feature is disabled by default; legacy programs run unchanged.
* The blocking address is configurable to avoid collisions with existing software.
* This extension is not present on physical Novas and is simulator■specific.