

								memory								
			instruction	r1	r2	r14	r15	...	100	101	102	103	104	105	106	...
code																
					3	3	100									
5	jeqzn	r2 18	5 jeqzn r2 18		3	3	100									
6	addn	r15 1	6 addn r15 1		3	3	101									
7	storer	r2 r15	7 storer r2 r15		3	3	101		3							
8	addn	r15 1	8 addn r15 1		3	3	102		3							
9	storer	r14 r15	9 storer r14 r15		3	3	102		3	3						
10	addn	r2 -1	10 addn r2 -1		2	3	102		3	3						
11	calln	r14 5	11 calln r14 5		2	12	102		3	3						
12	loadr	r14 r15	5 jeqzn r2 18		2	12	102		3	3						
13	addn	r15 -1	6 addn r15 1		2	12	103		3	3						
14	loadr	r2 r15	7 storer r2 r15		2	12	103		3	3	2					
15	addn	r15 -1	8 addn r15 1		2	12	104		3	3	2					
16	mul	r1 r1 r2	9 storer r14 r15		2	12	104		3	3	2	12				
17	jumpr	r14	10 addn r2 -1		1	12	104		3	3	2	12				
			11 calln r14 5		1	12	104		3	3	2	12				
			5 jeqzn r2 18		1	12	104		3	3	2	12				
18	setn	r1 1	6 addn r15 1		1	12	105		3	3	2	12				
19	jumpr	r14	7 storer r2 r15		1	12	105		3	3	2	12	1			
			8 addn r15 1		1	12	106		3	3	2	12	1			
			9 storer r14 r15		1	12	106		3	3	2	12	1	12		
			10 addn r2 -1		0	12	106		3	3	2	12	1	12		
			11 calln r14 5		0	12	106		3	3	2	12	1	12		
			5 jeqzn r2 18		0	12	106		3	3	2	12	1	12		
			18 setn r1 1	1	0	12	106		3	3	2	12	1	12		
			19 jumpr r14	1	0	12	106		3	3	2	12	1	12		
			12 loadr r14 r15	1	0	12	106		3	3	2	12	1	12		
			13 addn r15 -1	1	0	12	105		3	3	2	12	1			
			14 loadr r2 r15	1	1	12	105		3	3	2	12	1			
			15 addn r15 -1	1	1	12	104		3	3	2	12				
			16 mul r1 r1 r2	1	1	12	104		3	3	2	12				
			17 jumpr r14	1	1	12	104		3	3	2	12				
			12 loadr r14 r15	1	1	12	104		3	3	2	12				
			13 addn r15 -1	1	1	12	103		3	3	2					
			14 loadr r2 r15	1	2	12	103		3	3	2					
			15 addn r15 -1	1	2	12	102		3	3						
			16 mul r1 r1 r2	2	2	12	102		3	3						
			17 jumpr r14	2	2	12	102		3	3						
			12 loadr r14 r15	2	2	3	102		3	3						
			13 addn r15 -1	2	2	3	101		3							
			14 loadr r2 r15	2	3	3	101		3							
			15 addn r15 -1	2	3	3	100									
			16 mul r1 r1 r2	6	3	3	100									
			17 jumpr r14	6	3	3	100									