to IWDG LSI RC 32 kHz LSCO to RTC OSC32_OUT LSE OSC /32 32.768 kHz OSC32_IN to PWR LSE LSI to AHB bus, core, memory and DMA HSI MCO AHB PRESC / 1→16 HCLK HSE FCLK Cortex free running clock SYSCLK PLLCLK to Cortex system timer / 8 HSI48 Clock APB1 PRESC PCLK1 source to APB1 peripherals / 1,2,4,8,16 OSC_OUT HSE OSC 4-48 MHz HSE x1 or x2 to TIMx OSC IN Clock x=2..7 SYSCLK detector HSI LSE HSI SYSCLK to USARTx x=2..5 to LPUART1 HSI 16 MHz HSI SYSCLK to I2Cx x=1,2,3,4 HSI48 48MHz to LPTIMx x=1,2]HSI /M HSE QUADSPI clock PLLPCLK vco CRS clock **PLLQCLK** /Q PCLK2 χN APB2 PRESC PLLRCLK to APB2 peripherals /R PLL 1,2,4,8,16 x1 or x2 to TIMx, HRTIM1 x=1,8,20,15,16,17 LSE HSI-USART1 SYSCLK PCLK1 FDCAN clock 48 MHz clock to USB, RNG SYSCLK to ADC HSI to SAI1 Pad I2S_CKIN HSI to I2S23

Figure 17. Clock tree

- For full details about the internal and external clock source characteristics, please refer to the "Electrical characteristics" section in your device datasheet.
- 2. The ADC clock can be derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). When the programmable factor is '1', the AHB prescaler must be equal to '1'.

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