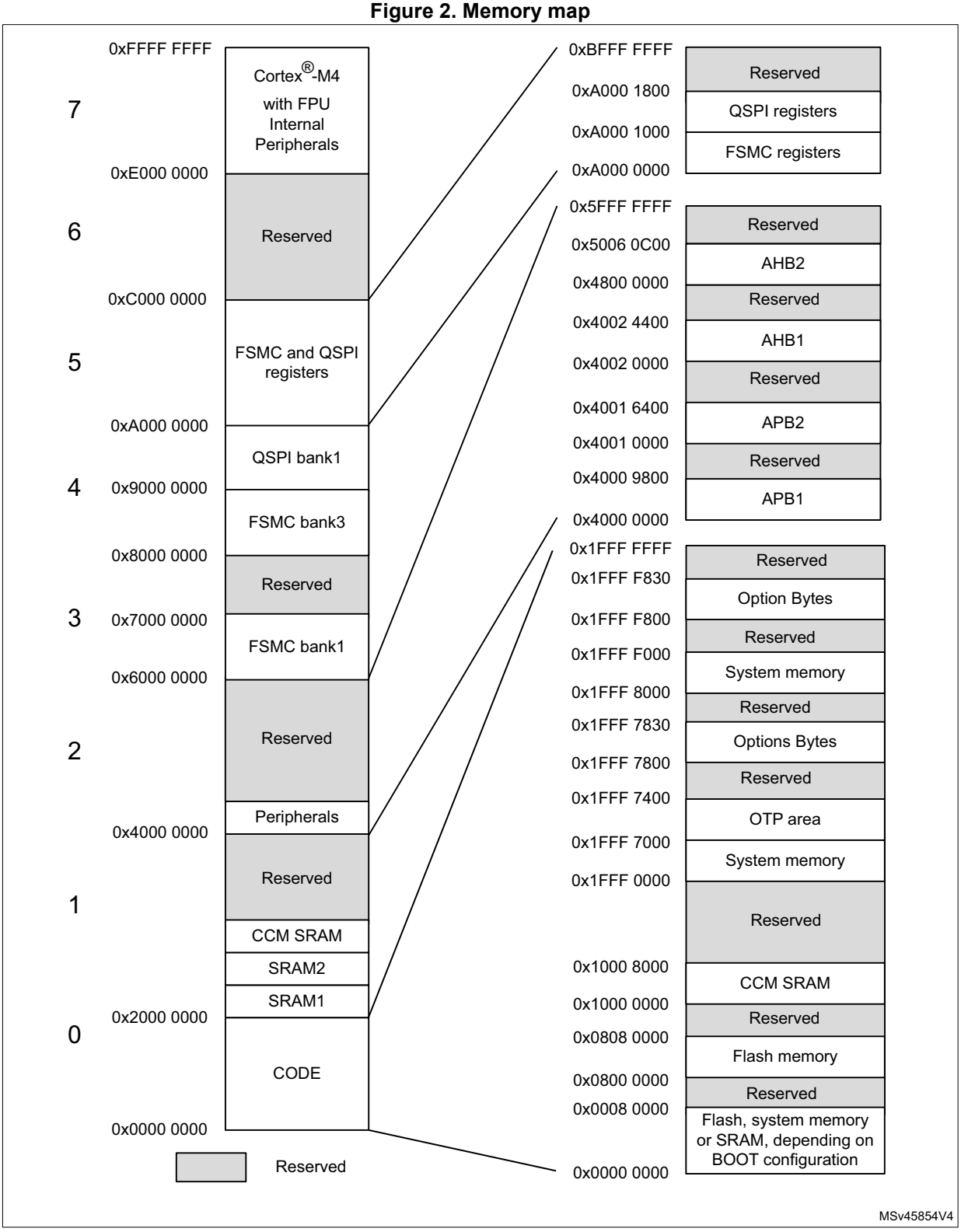
2.2.2 Memory map and register boundary addresses

Figure 2. Memory map



All the memory map areas that are not allocated to on-chip memories and peripherals are considered “Reserved”. For the detailed mapping of available memory and register areas, refer to the following table.

The following table gives the boundary addresses of the peripherals available in the devices.

Table 3. STM32G4 Series memory map and peripheral register boundary addresses(1)

Bus	Boundary address	Size (bytes)	Peripheral	Peripheral register map
-	0xA000 1400 - 0xAFFF FFFF	262 MB	Reserved	-
	0xA000 1000 - 0xA000 13FF	1 KB	QUADSPI control Registers	*Section 20.5.14: QUADSPI register map*
	0xA000 0400 - 0xA000 0FFF	3 KB	Reserved	-
	0xA000 0000 - 0xA000 03FF	1 KB	FSMC	*Section 19.7.8: FMC register map*
AHB2	0x5006 0C00 - 0x5FFF FFFF	256MB	Reserved	-
	0x5006 0800 - 0x5006 0BFF	1 KB	RNG	*Section 26.7.4: RNG register map*
	0x5006 0400 - 0x5006 07FF	1 KB	Reserved	-
	0x5006 0000 - 0x5006 03FF	1 KB	AES	*Section 34.7.18: AES register map*
	0x5000 1800 - 0x5005 FFFF	377 KB	Reserved	-
	0x5000 1400 - 0x5000 17FF	1 KB	DAC4	*Section 22.7.24: DAC register map*
	0x5000 1000 - 0x5000 13FF	1 KB	DAC3	*Section 22.7.24: DAC register map*
	0x5000 0C00 - 0x5000 0FFF	1 KB	DAC2	*Section 22.7.24: DAC register map*
	0x5000 0800 - 0x5000 0BFF	1 KB	DAC1	*Section 22.7.24: DAC register map*
	0x5000 0400 - 0x5000 07FF	1 KB	ADC3 - ADC4 - ADC5	*Section 21.8: ADC register map*
	0x5000 0000 - 0x5000 03FF	1 KB	ADC1 - ADC2	*Section 21.8: ADC register map*
	0x4800 1C00 - 0x4FFF FFFF	127 MB	Reserved	-
	0x4800 1800 - 0x4800 1BFF	1 KB	GPIOG	*Section 9.4.12: GPIO register map*
	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF	*Section 9.4.12: GPIO register map*
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE	*Section 9.4.12: GPIO register map*
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD	*Section 9.4.12: GPIO register map*
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC	*Section 9.4.12: GPIO register map*
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB	*Section 9.4.12: GPIO register map*
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA	*Section 9.4.12: GPIO register map*

Table 3. STM32G4 Series memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral	Peripheral register map
AHB1	0x4002 3400 - 0x47FF FFFF	127 MB	Reserved	-
	0x4002 3000 - 0x4002 33FF	1 KB	CRC	*Section 16.4.6: CRC register map*
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved	-
	0x4002 2000 - 0x4002 23FF	1 KB	Flash interface	*Section 5.7.14: FLASH register map*
	0x4002 1400 - 0x4002 1FFF	3 KB	FMAC	*Section 18.4.9: FMAC register map*
	0X4002 1000 - 0x4002 13FF	1 KB	RCC	*Section 7.4.31: RCC register map*
	0x4002 0C00 - 0x4002 0FFF	1 KB	CORDIC	*Section 17.4.4: CORDIC register map*
	0x4002 0800 - 0x4002 0BFF	1 KB	DMAMUX	*Section 13.6.7: DMAMUX register map*
	0x4002 0400 - 0x4002 07FF	1 KB	DMA 2	*Section 12.6.7: DMA register map*
	0x4002 0000 - 0x4002 03FF	1 KB	DMA 1	*Section 12.6.7: DMA register map*
APB2	0x4001 7800 - 0x4001 FFFF	2 KB	Reserved	-
	0x4001 6800 - 0x4001 77FF	3 KB	HRTIM	*Section 27.5.82: HRTIM register map*
	0x4001 5800 - 0x4001 67FF	4 KB	Reserved	-
	0x4001 5400 - 0x4001 57FF	1 KB	SAI1	*Section 40.6.19: SAI register map*
	0x4001 5000 - 0x4001 53FF	1 KB	TIM20	*Section 28.6.31: TIMx register map*
	0x4001 4C00 - 0x4001 4FFF	1 KB	Reserved	-
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17	*Section 30.8.22: TIM16/TIM17 register map*
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16	*Section 30.8.22: TIM16/TIM17 register map*
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15	*Section 30.7.23: TIM15 register map*
	0x4001 3C00 - 0x4001 3FFF	1 KB	SPI4	*Section 39.9.10: SPI/I2S register map*
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1	*Section 37.8.15: USART register map*
	0x4001 3400 - 0x4001 37FF	1 KB	TIM8	*Section 28.6.31: TIMx register map*
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1	*Section 39.9.10: SPI/I2S register map*
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1	*Section 28.6.31: TIMx register map*
	0x4001 0800 - 0x4001 2BFF	9 KB	Reserved	-
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI	*Section 15.5.13: EXTI register map*
	0x4001 0300 - 0x4001 03FF	1 KB	OPAMP	*Section 25.5.13: OPAMP register map*
	0x4001 0200 - 0x4001 02FF		COMP	*Section 24.6.2: COMP register map*
	0x4001 0030 - 0x4001 01FF		VREFBUF	*Section 23.4.3: VREFBUF register map*
	0x4001 0000 - 0x4001 0029		SYSCFG	*Section 10.2.11: SYSCFG register map*

Table 3. STM32G4 Series memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral	Peripheral register map
APB1	0x4000 AFFE - 0x4000 FFFF	23 KB	Reserved	-
	0x4000 AC00 - 0x4000 AFFF	1 KB	FDCANs Message RAM	*Section 44.4.38: FDCAN register map*
	0x4000 A800 - 0x4000 ABFF	1 KB		
	0x4000 A400 - 0x4000 A7FF	1 KB		
	0x4000 A000 - 0x4000 A3FF	1 KB	UCPD1	*Section 46.7.16: UCPD register map*
	0x4000 8800 - 0x4000 9FFF	6 KB	Reserved	-
	0x4000 8400 - 0x4000 87FF	1 KB	I2C4	*Section 41.7.12: I2C register map*
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1	*Section 38.7.13: LPUART register map*
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1	*Section 32.7.10: LPTIM register map*
	0x4000 7800 - 0x4000 7BFF	1 KB	I2C3	*Section 41.7.12: I2C register map*
	0x4000 7400 - 0x4000 77FF	1 KB	Reserved	-
	0x4000 7000 - 0x4000 73FF	1 KB	PWR	*Section 6.4.23: PWR register map and reset value table*
	0x4000 6C00 - 0x4000 6FFF	1 KB	FDCAN3	*Section 44.4.38: FDCAN register map*
	0x4000 6800 - 0x4000 6BFF	1 KB	FDCAN2	*Section 44.4.38: FDCAN register map*
	0x4000 6400 - 0x4000 67FF	1 KB	FDCAN1	*Section 44.4.38: FDCAN register map*
	0x4000 6000 - 0x4000 63FF	1 KB	USB SRAM 1 Kbyte	-
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB device FS	*Section 45.6.3: USB register map*
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2	*Section 41.7.12: I2C register map*
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1	*Section 41.7.12: I2C register map*
	0x4000 5000 - 0x4000 53FF	1 KB	UART5	*Section 37.8.15: USART register map*
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4	*Section 37.8.15: USART register map*
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3	*Section 37.8.15: USART register map*
	0x4000 4400 - 0x4000 47FF	1 KB	USART2	*Section 37.8.15: USART register map*

Table 3. STM32G4 Series memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral	Peripheral register map
APB1 Cont.	0x4000 4000 - 0x4000 43FF	1 KB	Reserved	-
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3/I2S3	*Section 39.9.10: SPI/I2S register map*
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2	*Section 39.9.10: SPI/I2S register map*
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved	-
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG	*Section 42.4.6: IWDG register map*
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG	*Section 43.5.4: WWDG register map*
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC & BKP Registers	*Section 35.6.21: RTC register map*
	0x4000 2400 - 0x4000 27FF	1 KB	TAMP	*Section 36.6.9: TAMP register map*
	0x4000 2000 - 0x4000 23FF	1 KB	CRS	*Section 8.7.5: CRS register map*
	0x4000 1C00 - 0x4000 1FFF	1 KB	Reserved	-
	0x4000 1800 - 0x4000 1BFF	1 KB	Reserved	-
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7	*Section 29.5.31: TIMx register mapSection 31.4.9: TIMx register map*
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6	*Section 31.4.9: TIMx register map*
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5	*Section 29.5.31: TIMx register map*
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4	*Section 29.5.31: TIMx register map*
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3	*Section 29.5.31: TIMx register map*
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2	*Section 29.5.31: TIMx register map*

1. Refer to *Table 1: STM32G4 Series memory density*, *Table 2: Product specific features* and to the device datasheets for the GPIO ports and peripherals available on your device. the memory area corresponding to unavailable GPIO ports or peripherals are reserved (highlighted in gray).

2.3 Bit banding

The Cortex®-M4 with FPU memory map includes two bit-band regions. These regions map each word in an alias region of memory to a bit in a bit-band region of memory. Writing to a word in the alias region has the same effect as a read-modify-write operation on the targeted bit in the bit-band region.

In the STM32G4 Series devices both the peripheral registers and the SRAM are mapped to a bit-band region, so that single bit-band write and read operations are allowed. The operations are only available for Cortex®-M4 with FPU accesses, and not from other bus masters (e.g. DMA).