Table 12. STM32G431x6/x8/xB pin definition(1)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
-	-	-	-	-	-	-	-	1	PE2	I/O	FT	-	TRACECK, TIM3_CH1, SAI1_CK1, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	-	-	-	-	2	PE3	I/O	FT	-	TRACED0, TIM3_CH2, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	-	-	3	PE4	I/O	FT	-	TRACED1, TIM3_CH3, SAI1_D2, SAI1_FS_A, EVENTOUT	-
-	-	-	-	-	-	-	-	4	PE5	I/O	FT	-	TRACED2, TIM3_CH4, SAI1_CK2, SAI1_SCK_A, EVENTOUT	-
-	-	-	-	-	-	-	-	5	PE6	I/O	FT	-	TRACED3, SAI1_D1, SAI1_SD_A, EVENTOUT	WKUP3, RTC_TAMP3
-	-	1	1	B7	1	C2	1	6	VBAT	S	-	-	-	-
-	-	2	2	C5	2	B1	2	7	PC13	I/O	FT	(2) (3)	TIM1_BKIN, TIM1_CH1N, TIM8_CH4N, EVENTOUT	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT1
-	-	3	3	C7	3	C1	3	8	PC14-OSC32_IN	I/O	FT	(2) (3)	EVENTOUT	OSC32_IN
-	-	4	4	D7	4	D1	4	9	PC15-OSC32_OUT	I/O	FT	(2) (3)	EVENTOUT	OSC32_OUT
-	-	-	-	-	-	-	-	10	PF9	I/O	FT	-	TIM15_CH1, SPI2_SCK, SAI1_FS_B, EVENTOUT	-
-	-	-	-	-	-	-	-	11	PF10	I/O	FT	-	TIM15_CH2, SPI2_SCK, SAI1_D3, EVENTOUT	-
2	2	5	5	E7	5	E1	5	12	PF0-OSC_IN	I	FT_fa	-	I2C2_SDA, SPI2_NSS/ I2S2_WS, TIM1_CH3N, EVENTOUT	ADC1_IN10, OSC_IN
3	3	6	6	E6	6	F1	6	13	PF1-OSC_OUT	O	FT_a	-	SPI2_SCK/ I2S2_CK, EVENTOUT	ADC2_IN10, COMP3_INM, OSC_OUT
4	4	7	7	C6	7	D2	7	14	PG10-NRST	I/O	FT	-	MCO, EVENTOUT	NRST

Table 12. STM32G431x6/x8/xB pin definition(1) (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
-	-	-	-	-	8	E2	8	15	PC0	I/O	FT_a	-	LPTIM1_IN1, TIM1_CH1, LPUART1_RX, EVENTOUT	ADC12_IN6, COMP3_INM
-	-	-	-	-	9	C3	9	16	PC1	I/O	TT_a	-	LPTIM1_OUT, TIM1_CH2, LPUART1_TX, SAI1_SD_A, EVENTOUT	ADC12_IN7, COMP3_INP
-	-	-	-	-	10	D3	10	17	PC2	I/O	FT_a	-	LPTIM1_IN2, TIM1_CH3, COMP3_OUT, EVENTOUT	ADC12_IN8
-	-	-	-	-	11	G1	11	18	PC3	I/O	FT_a	-	LPTIM1_ETR, TIM1_CH4, SAI1_D1, TIM1_BKIN2, SAI1_SD_A, EVENTOUT	ADC12_IN9
-	-	-	-	-	-	-	-	19	PF2	I/O	FT	-	I2C2_SMBA, EVENTOUT	-
5	5	8	8	F7	12	F2	12	20	PA0	I/O	TT_a	-	TIM2_CH1, USART2_CTS, COMP1_OUT, TIM8_BKIN, TIM8_ETR, TIM2_ETR, EVENTOUT	ADC12_IN1, COMP1_INM, COMP3_INP, RTC_TAMP2, WKUP1
6	6	9	9	D6	13	E3	13	21	PA1	I/O	TT_a	-	RTC_REFIN, TIM2_CH2, USART2_RTS_DE, TIM15_CH1N, EVENTOUT	ADC12_IN2, COMP1_INP, OPAMP1_VINP, OPAMP3_VINP
7	7	10	10	F6	14	F3	14	22	PA2	I/O	TT_a	-	TIM2_CH3, USART2_TX, COMP2_OUT, TIM15_CH1, LPUART1_TX, UCPD1_FRSTX, EVENTOUT	ADC1_IN3, COMP2_INM, OPAMP1_VOUT, WKUP4/ LSCO
-	-	-	-	-	15	G2	15	23	VSS_2	S	-	-	-	-
-	-	-	-	-	16	H1	16	24	VDD_2	S	-	-	-	-
8	8	11	11	G7	17	H2	17	25	PA3	I/O	TT_a	-	TIM2_CH4, SAI1_CK1, USART2_RX, TIM15_CH2, LPUART1_RX, SAI1_MCLK_A, EVENTOUT	ADC1_IN4, COMP2_INP, OPAMP1_VINM/ OPAMP1_VINP

Table 12. STM32G431x6/x8/xB pin definition[1] (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
9	9	12	12	E5	18	D4	18	26	PA4	I/O	TT_a	-	TIM3_CH2, SPI1_NSS, SPI3_NSS/ I2S3_WS, USART2_CK, SAI1_FS_B, EVENTOUT	ADC2_IN17, DAC1_OUT1, COMP1_INM
10	10	13	13	F5	19	E4	19	27	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, SPI1_SCK, UCPD1_FRSTX, EVENTOUT	ADC2_IN13, DAC1_OUT2, COMP2_INM, OPAMP2_VINM
11	11	14	14	G6	20	G3	20	28	PA6	I/O	TT_a	-	TIM16_CH1, TIM3_CH1, TIM8_BKIN, SPI1_MISO, TIM1_BKIN, COMP1_OUT, LPUART1_CTS, EVENTOUT	ADC2_IN3, OPAMP2_VOUT
12	12	15	15	D5	21	H3	21	29	PA7	I/O	TT_a	-	TIM17_CH1, TIM3_CH2, TIM8_CH1N, SPI1_MOSI, TIM1_CH1N, COMP2_OUT, UCPD1_FRSTX, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP1_VINP, OPAMP2_VINP
-	-	16	-	D4	22	D5	22	30	PC4	I/O	FT_fa	-	TIM1_ETR, I2C2_SCL, USART1_TX, EVENTOUT	ADC2_IN5
-	-	-	-	-	23	F4	23	31	PC5	I/O	TT_a	-	TIM15_BKIN, SAI1_D3, TIM1_CH4N, USART1_RX, EVENTOUT	ADC2_IN11, OPAMP1_VINM, OPAMP2_VINM, WKUP5
13	13	17	16	G5	24	E5	24	32	PB0	I/O	TT_a	-	TIM3_CH3, TIM8_CH2N, TIM1_CH2N, UCPD1_FRSTX, EVENTOUT	ADC1_IN15, COMP4_INP, OPAMP2_VINP, OPAMP3_VINP
-	-	18	17	E4	25	F5	25	33	PB1	I/O	TT_a	-	TIM3_CH4, TIM8_CH3N, TIM1_CH3N, COMP4_OUT, LPUART1_RTS_DE, EVENTOUT	ADC1_IN12, COMP1_INP, OPAMP3_VOUT
-	-	19	18	F4	26	H4	26	34	PB2	I/O	TT_a	-	RTC_OUT2, LPTIM1_OUT, I2C3_SMBA, EVENTOUT	ADC2_IN12, COMP4_INM, OPAMP3_VINM

Table 12. STM32G431x6/x8/xB pin definition(1) (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
14	14	-	19	G4	27	G4	27	35	VSSA	S	-	-	-	-
-	-	20	20	F3	28	G5	28	36	VREF+	S	-	-	-	VREFBUF_OUT
-	-	21	21	G3	29	H5	29	37	VDDA	S	-	-	-	-
15	15	-	-	-	-	-	-	-	VDDA/VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	-	-	-	-	30	38	PE7	I/O	TT_a	-	TIM1_ETR, SAI1_SD_B, EVENTOUT	COMP4_INP
-	-	-	-	-	-	-	31	39	PE8	I/O	FT_a	-	TIM1_CH1N, SAI1_SCK_B, EVENTOUT	COMP4_INM
-	-	-	-	-	-	-	32	40	PE9	I/O	FT	-	TIM1_CH1, SAI1_FS_B, EVENTOUT	-
-	-	-	-	-	-	-	33	41	PE10	I/O	FT	-	TIM1_CH2N, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	-	-	-	34	42	PE11	I/O	FT	-	TIM1_CH2, EVENTOUT	-
-	-	-	-	-	-	-	35	43	PE12	I/O	FT	-	TIM1_CH3N, EVENTOUT	-
-	-	-	-	-	-	-	36	44	PE13	I/O	FT	-	TIM1_CH3, EVENTOUT	-
-	-	-	-	-	-	-	37	45	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, EVENTOUT	-
-	-	-	-	-	-	-	38	46	PE15	I/O	FT	-	TIM1_BKIN, TIM1_CH4N, USART3_RX, EVENTOUT	-
-	-	22	22	F2	30	H6	39	47	PB10	I/O	TT_a	-	TIM2_CH3, USART3_TX, LPUART1_RX, TIM1_BKIN, SAI1_SCK_A, EVENTOUT	OPAMP3_VINM
16	16	-	23	G2	31	G7	40	48	VSS	S	-	-	-	-
17	17	23	24	G1	32	H8	41	49	VDD	S	-	-	-	-
-	-	24	25	E3	33	H7	42	50	PB11	I/O	FT_a	-	TIM2_CH4, USART3_RX, LPUART1_TX, EVENTOUT	ADC12_IN14

Table 12. STM32G431x6/x8/xB pin definition(1) (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
-	-	25	26	F1	34	G8	43	51	PB12	I/O	FT_a	-	I2C2_SMBA, SPI2_NSS/ I2S2_WS, TIM1_BKIN, USART3_CK, LPUART1_RTS_DE, EVENTOUT	ADC1_IN11
-	-	26	27	E2	35	G6	44	52	PB13	I/O	TT_a	-	SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, LPUART1_CTS, EVENTOUT	OPAMP3_VINP
-	-	27	28	D3	36	F8	45	53	PB14	I/O	TT_a	-	TIM15_CH1, SPI2_MISO, TIM1_CH2N, USART3_RTS_DE, COMP4_OUT, EVENTOUT	ADC1_IN5, OPAMP2_VINP
-	-	28	29	E1	37	F7	46	54	PB15	I/O	FT_a	-	RTC_REFIN, TIM15_CH2, TIM15_CH1N, COMP3_OUT, TIM1_CH3N, SPI2_MOSI/ I2S2_SD, EVENTOUT	ADC2_IN15
-	-	-	-	-	-	-	47	55	PD8	I/O	FT_a	-	USART3_TX, EVENTOUT	-
-	-	-	-	-	-	-	48	56	PD9	I/O	FT	-	USART3_RX, EVENTOUT	-
-	-	-	-	-	-	-	49	57	PD10	I/O	FT	-	USART3_CK, EVENTOUT	-
-	-	-	-	-	-	-	-	58	PD11	I/O	FT_a	-	USART3_CTS, EVENTOUT	-
-	-	-	-	-	-	-	-	59	PD12	I/O	TT	-	TIM4_CH1, USART3_RTS_DE, EVENTOUT	-
-	-	-	-	-	-	-	-	60	PD13	I/O	FT	-	TIM4_CH2, EVENTOUT	-
-	-	-	-	-	-	-	-	61	PD14	I/O	FT_a	-	TIM4_CH3, EVENTOUT	OPAMP2_VINP
-	-	-	-	-	-	-	-	62	PD15	I/O	FT	-	TIM4_CH4, SPI2_NSS, EVENTOUT	-
-	-	-	-	-	-	-	50	63	VSS	S	-	-	-	-
-	-	-	-	-	-	-	51	64	VDD	S	-	-	-	-

Table 12. STM32G431x6/x8/xB pin definition(1) (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
-	-	29	-	D1	38	E8	52	65	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, I2S2_MCK, EVENTOUT	-
-	-	-	-	-	39	E7	53	66	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, I2S3_MCK, EVENTOUT	-
-	-	-	-	-	40	F6	54	67	PC8	I/O	FT_f	-	TIM3_CH3, TIM8_CH3, I2C3_SCL, EVENTOUT	-
-	-	-	-	-	41	D8	55	68	PC9	I/O	FT_f	-	TIM3_CH4, TIM8_CH4, I2SCKIN, TIM8_BKIN2, I2C3_SDA, EVENTOUT	-
18	18	30	30	D2	42	E6	56	69	PA8	I/O	FT_f	-	MCO, I2C3_SCL, I2C2_SDA, I2S2_MCK, TIM1_CH1, USART1_CK, TIM4_ETR, SAI1_CK2, SAI1_SCK_A, EVENTOUT	-
19	19	31	31	C3	43	D7	57	70	PA9	I/O	FT_fd	-	I2C3_SMBA, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, SAI1_FS_A, EVENTOUT	UCPD1_DBCC1
20	20	32	32	C2	44	D6	58	71	PA10	I/O	FT_da	-	TIM17_BKIN, USB_CRS_SYNC, I2C2_SMBA, SPI2_MISO, TIM1_CH3, USART1_RX, TIM2_CH4, TIM8_BKIN, SAI1_D1, SAI1_SD_A, EVENTOUT	UCPD1_DBCC2
21	21	33	33	C1	45	C8	59	72	PA11	I/O	FT_u	-	SPI2_MOSI/ I2S2_SD, TIM1_CH1N, USART1_CTS, COMP1_OUT, FDCAN1_RX, TIM4_CH1, TIM1_CH4, TIM1_BKIN2, EVENTOUT	USB_DM

Table 12. STM32G431x6/x8/xB pin definition[1] (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
22	22	34	34	B1	46	B8	60	73	PA12	I/O	FT_u	-	TIM16_CH1, I2SCKIN, TIM1_CH2N, USART1_RTS_DE, COMP2_OUT, FDCAN1_TX, TIM4_CH2, TIM1_ETR, EVENTOUT	USB_DP
-	-	-	35	-	47	B7	61	74	VSS	S	-	-	-	-
-	-	35	36	-	48	A8	62	75	VDD	S	-	-	-	-
23	23	36	37	B2	49	C7	63	76	PA13	I/O	FT_f	(4)	SWDIO-JTMS, TIM16_CH1N, I2C1_SCL, IR_OUT, USART3_CTS, TIM4_CH3, SAI1_SD_B, EVENTOUT	-
24	24	37	38	B3	50	C6	64	77	PA14	I/O	FT_f	(4)	SWCLK-JTCK, LPTIM1_OUT, I2C1_SDA, TIM8_CH2, TIM1_BKIN, USART2_TX, SAI1_FS_B, EVENTOUT	-
25	25	38	39	A1	51	A7	65	78	PA15	I/O	FT_f	(4)	JTDI, TIM2_CH1, TIM8_CH1, I2C1_SCL, SPI1_NSS, SPI3_NSS/ I2S3_WS, USART2_RX, UART4_RTS_DE, TIM1_BKIN, TIM2_ETR, EVENTOUT	-
-	-	39	-	-	52	C5	66	79	PC10	I/O	FT	-	TIM8_CH1N, UART4_TX, SPI3_SCK/ I2S3_CK, USART3_TX, EVENTOUT	-
-	-	40	-	A2	53	B6	67	80	PC11	I/O	FT_f	-	TIM8_CH2N, UART4_RX, SPI3_MISO, USART3_RX, I2C3_SDA, EVENTOUT	-

Table 12. STM32G431x6/x8/xB pin definition(1) (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
-	-	-	-	-	54	A6	68	81	PC12	I/O	FT	-	TIM8_CH3N, SPI3_MOSI/ I2S3_SD, USART3_CK, UCPD1_FRSTX, EVENTOUT	-
-	-	-	-	-	-	-	69	82	PD0	I/O	FT	-	TIM8_CH4N, FDCAN1_RX, EVENTOUT	-
-	-	-	-	-	-	-	70	83	PD1	I/O	FT	-	TIM8_CH4, TIM8_BKIN2, FDCAN1_TX, EVENTOUT	-
-	-	-	-	-	55	B5	71	84	PD2	I/O	FT	-	TIM3_ETR, TIM8_BKIN, EVENTOUT	-
-	-	-	-	-	-	-	-	85	PD3	I/O	FT	-	TIM2_CH1/ TIM2_ETR, USART2_CTS, EVENTOUT	-
-	-	-	-	-	-	-	-	86	PD4	I/O	FT	-	TIM2_CH2, USART2_RTS_DE, EVENTOUT	-
-	-	-	-	-	-	-	-	87	PD5	I/O	FT	-	USART2_TX, EVENTOUT	-
-	-	-	-	-	-	-	-	88	PD6	I/O	FT	-	TIM2_CH4, SAI1_D1, USART2_RX, SAI1_SD_A, EVENTOUT	-
-	-	-	-	-	-	-	-	89	PD7	I/O	FT	-	TIM2_CH3, USART2_CK, EVENTOUT	-
26	26	41	40	A3	56	A5	72	90	PB3	I/O	FT	(4)	JTDO-TRACESWO, TIM2_CH2, TIM4_ETR, USB_CRS_SYNC, TIM8_CH1N, SPI1_SCK, SPI3_SCK/ I2S3_CK, USART2_TX, TIM3_ETR, SAI1_SCK_B, EVENTOUT	-

Table 12. STM32G431x6/x8/xB pin definition[1] (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
27	27	42	41	B4	57	C4	73	91	PB4	I/O	FT_c	(4)	JTRST, TIM16_CH1, TIM3_CH1, TIM8_CH2N, SPI1_MISO, SPI3_MISO, USART2_RX, TIM17_BKIN, SAI1_MCLK_B, EVENTOUT	UCPD1_CC2
28	28	43	42	A43	58	B4	74	92	PB5	I/O	FT_f	-	TIM16_BKIN, TIM3_CH2, TIM8_CH3N, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI/ I2S3_SD, USART2_CK, I2C3_SDA, TIM17_CH1, LPTIM1_IN1, SAI1_SD_B, EVENTOUT	-
29	29	44	43	C4	59	A4	75	93	PB6	I/O	FT_c	-	TIM16_CH1N, TIM4_CH1, TIM8_CH1, TIM8_ETR, USART1_TX, COMP4_OUT, TIM8_BKIN2, LPTIM1_ETR, SAI1_FS_B, EVENTOUT	UCPD1_CC1
30	30	45	44	A5	60	A3	76	94	PB7	I/O	FT_f	-	TIM17_CH1N, TIM4_CH2, I2C1_SDA, TIM8_BKIN, USART1_RX, COMP3_OUT, TIM3_CH4, LPTIM1_IN2, UART4_CTS, EVENTOUT	PVD_IN
31	31	46	45	B5	61	B3	77	95	PB8-BOOT0	I/O	FT_f	(5)	TIM16_CH1, TIM4_CH3, SAI1_CK1, I2C1_SCL, USART3_RX, COMP1_OUT, FDCAN1_RX, TIM8_CH2, TIM1_BKIN, SAI1_MCLK_A, EVENTOUT	-

Table 12. STM32G431x6/x8/xB pin definition(1) (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate function	Additional functions
UFQFPN32	LQFP32	UFQFPN48	LQFP48	WLCSP49	LQFP64	UFBGA64	LQFP80	LQFP100						
-	-	47	46	B6	62	A2	78	96	PB9	I/O	FT_f	-	TIM17_CH1, TIM4_CH4, SAI1_D2, I2C1_SDA, IR_OUT, USART3_TX, COMP2_OUT, FDCAN1_TX, TIM8_CH3, TIM1_CH3N, SAI1_FS_A, EVENTOUT	-
-	-	-	-	-	-	-	-	97	PE0	I/O	FT	-	TIM4_ETR, TIM16_CH1, USART1_TX, EVENTOUT	-
-	-	-	-	-	-	-	-	98	PE1	I/O	FT	-	TIM17_CH1, USART1_RX, EVENTOUT	-
32	32	-	47	A6	63	B2	79	99	VSS	S	-	-	-	-
1	1	48	48	A7	64	A1	80	100	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
3. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the reference manual RM0440 "STM32G4 Series advanced Arm®-based 32-bit MCUs".
4. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.
5. It is recommended to set PB8 in another mode than analog mode after startup to limit consumption if the pin is left unconnected.