VFAT2 - Operating Manual

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Table 1: Project design engineers

1 Introduction

VFAT2 is a trigger and tracking front-end ASIC designed primarily for the TOTEM experiment. VFAT2 fits into the Totem electronics as in figure 1.

Figure 2 shows a block diagram of the VFAT2 chip.

The VFAT2 chip has been designed in 0.25 μm CMOS has two basic functions. The first (Trigger) is to provide fast regional hit information to aid the creation of a first level trigger (LV1) and the second (Tracking) is for providing precise spatial hit information for a given triggered event.

The VFAT2 chip has 128 identical channels. It is a synchronous chip designed for sampling sensors at the LHC clock frequency of 40MHz. Each channel consists of a preamplifier and shaper followed by a comparator. If a particular channel receives a signal greater than the programmable threshold of the comparator a logic 1 is produced for one clock cycle only by a mono-stable (see section 6). This logic 1 is written into the first of two SRAM memories (SRAM1). All other channels that do not go over threshold record a logic 0 in SRAM1. This occurs in parallel for all 128 channels at 40MHz. At the same time a fast OR function can be used to set a flag which

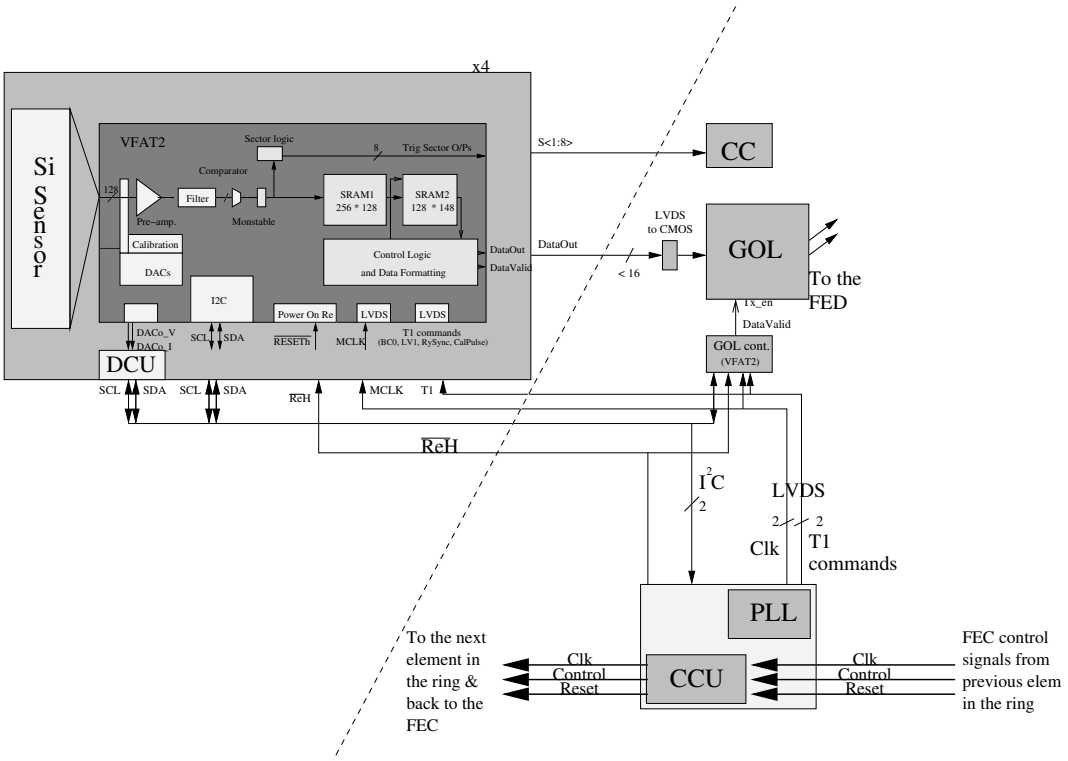

Figure 1: Block diagram of the Totem electronic system.

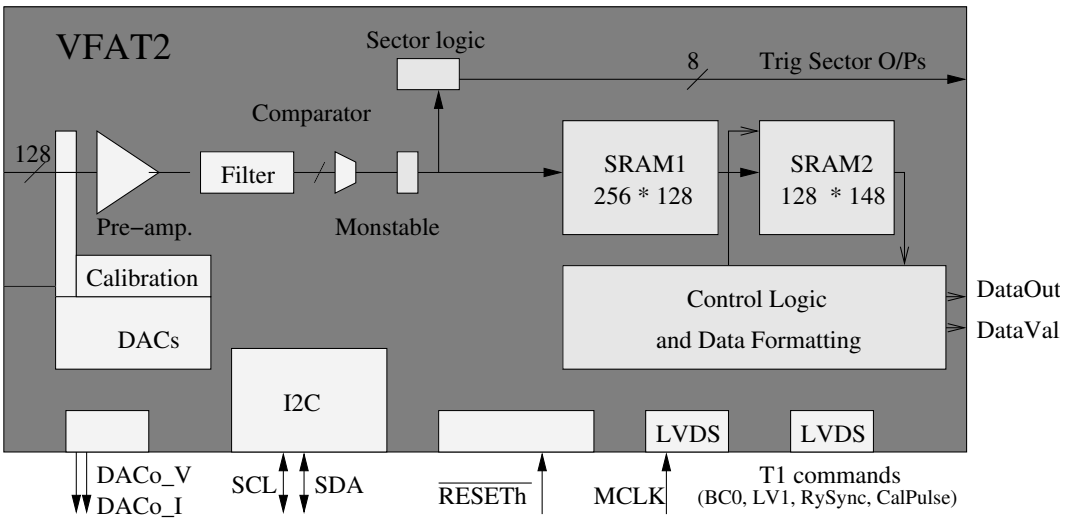

Figure 2: Block diagram of the VFAT2 chip.

can immediately be used for creating a trigger. It is foreseen to have up to eight programmable sectors which can be flagged with the fast OR in this way.

1.1 Triggering functions

Within TOTEM, VFAT2 will provide fast regional hit information to be included within the CMS First Level Trigger.

Channels are grouped together to form sectors. A hit channel in a given sector will set an LVDS output assigned to that sector to a logic "1".

The assignment of channels to sectors is programmable. There are 8 LVDS sector outputs labelled S1 to S8. Not all LVDS outputs need be used and the number sectors used can selected between 1,2,4 and 8. Once the number of sectors have been chosen the channel assignment to the sector can be made with different options. The options are defined by the requirements of the physics needed from VFATs used with the Roman Pots and VFATs used with the GEM detectors. Further details of channel assignment to sectors is given in section 5.1.1.

1.2 Tracking functions

On receiving a LV1A signal, data corresponding to the triggered time slot is transferred to a second SRAM memory (SRAM2). The LV1A latency is not expected to exceed 6.4μs (256 clock periods). Hence, SRAM1 is dimensioned 256 by 128. SRAM2 contains only triggered data. It is dimensioned to be 128 by 148 for data plus headers, hence VFAT2 can store up to 128 triggered events of data for all channels at any one instant in time.

VFAT2 will label the data with 3 headers. These are the Bunch Crossing number (BCN 12 bits), Event number (EN 8 bits), and the chip Identification number (ID 16 bits). The BCN is generated by a 12 bit counter (BC) that increments every clock cycle and is reset to zero on receiving a BC0 T1 command via LVDS. The EN is generated by an 8 bit counter that increments for every LV1. It is also reset by a BC0 command or the $\overline{Clear}$ signal. Both counters are cyclic and return to zero at the end of the counter range.

As soon as SRAM2 contains data the Read cycle begins. During the Read cycle a Data Formatting block streams out a binary data stream to the GOL. The chip operates with a continuous write/read operation without dead time.

1.3 T1 Commands

VFAT2 receives 2 LVDS signals namely the 40MHz master clock "MCLK" and a "T1" signal. The T1 signal is an encoded signal which contains 4 separate commands all synchronous to the MCLK. These 4 commands are decoded within the "Trigger

Decoder" within the chip. The 4 commands are: bunch crossing zero identifier (BC0), the level1 trigger "LV1", a synchronous reset "ReSynch" [1] and a calibration timing pulse "CalPulse".

The coding of the T1 commands is given in table 2.

Pattern	Command Name	Function
100	LV1A (Level 1 Accept)	Trigger
111	CalPulse	Timing of calibration pulse
110	ReSync	Resynchronisation of all state machines
101	BC0	Bunch crossing zero identifier

Table 2: T1 Commands

2 Radiation Hardness and Single Event Upset (SEU) protection

The location of VFAT2 in the experiment means that the chips will be exposed to varying levels of ionising radiation, the design is therefore made to withstand a minimum total dose of 100 MRads(Si). For the digital circuitry a major concern is SEU through charge deposition from particles of high LET.

The logic blocks within VFAT2 essential for the control of the chip have triplicated logic to protect against SEU.

2.1 Triplicated logic, testability through a "scan path" and counting upsets.

The I^2C, programmable registers, control logic and the trigger sequencer are protected from SEU by the use of triplicated flip-flops.

The production testing of the Control Logic flip-flops can be aided by the use of a scan chain.

In the Control Logic each set of triplicated flip-flops contain an output which goes high if there is a discrepancy between them ie. a 2 to 1 vote has taken place. A logic "OR" is made of all of these outputs and the result used to increment an 8 bit

[1] ReSynch : The ReSynch is a synchronous pulse, of 25ns period, that can be applied to VFAT2 to realign logical pointers in the control logic, FIFO and sequencer state machines. All counters need to be reset on a ReSynch. Register contents programmed through the I^2C remain untouched. Application of a ReSynch signal will erase all data stored in VFAT2 awaiting readout. Depending on the state of VFAT2 at the moment of receiving a ReSynch, data corresponding from 0 to 64 LV1A triggers will be lost.

synchronous counter. The result of the counter is stored in an 8 bit register (UpsetReg) which is accessible via the I^2C. The I^2C can then be used to read back the contents of the register.

This is, in fact, a diagnostic tool for understanding the SEU environment in the experiment. It can also be used to detect a "stuck at" fault condition since the "OR" would always be high and the counter clocked to FF.

The counter counts from 0 to FF and stops at FF. It is reset by the "$\overline{Clear}$" signal.

3 The Operation Cycle

Figure 3 shows a flowchart of the operation cycle of VFAT2.

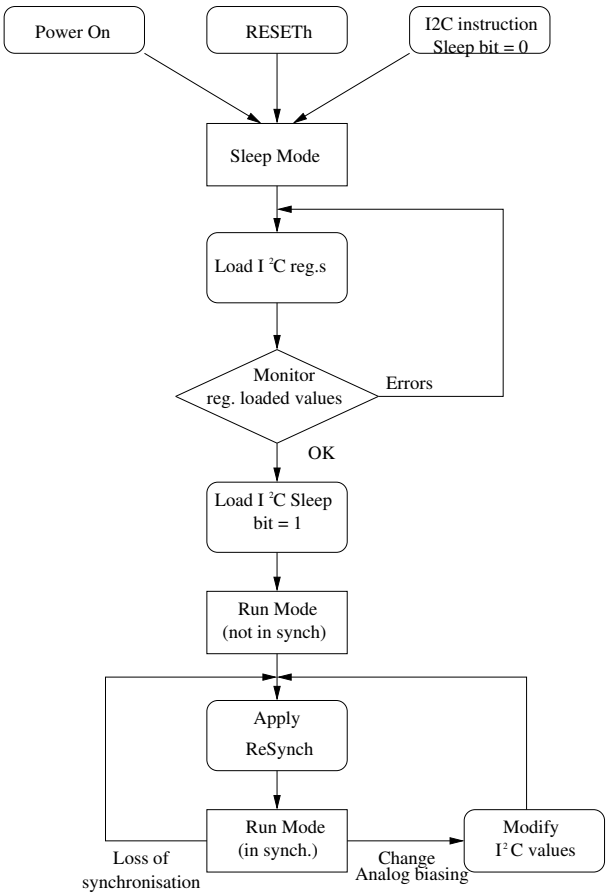

Figure 3: Flowchart of the operation cycle of VFAT2

A key point to the flowchart is direct entry into a "sleep" mode on applying power to the circuit. A power-on reset circuit generates a pulse that sets the internal programmable registers to default conditions. These default conditions mean that the chip is in a non-functional, minimum power consuming condition with only the I^2C circuits remaining responsive.

Figure 4 shows a schematic representation of the circuit configuration. On PowerOn or on the application of a hard reset ($\overline{RESETh}$), an I^2C reset is performed. At the same time multiplexers that switch between the register outputs and the internal functions are set to the default setting. The default setting is hard wired inside the chip.

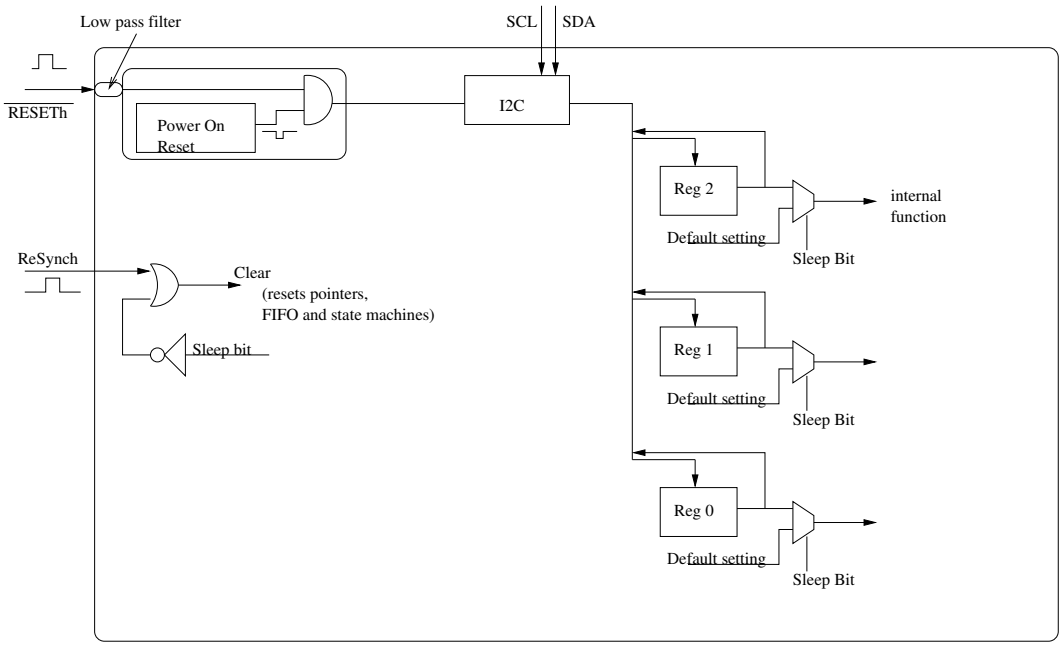

Figure 4: A schematic view of the programmable registers.

4 The I^{2}C interface

4.1 I^{2}C SEU Protection

The function of the I^{2}C is protected against single event upset. Both the main I^{2}C block and the programmable registers are protected against SEU through triplicated logic.

4.2 I^{2}C requirements

A summary of the main requirements of the I^{2}C port is given in table 3

1,	Should work correctly with all functions of the CCU
2,	Triplicated to guard against SEU
3,	The application of a ($\overline{RESETh}$) will reset the I^{2}C and apply sleep values to the registers .
4,	The input pads for the SDA and SDL lines should have hysteresis and rail to rail glitch protection.

Table 3: I2C specifications

5 Programmable registers

There are a number of programmable features in VFAT2 accessible through the I^2C port on each chip. There are 4 control registers, data registers and a chip ID.

5.1 The Control Registers

VFAT2 has four "Control Registers" labelled Cont.Reg. 0, to Cont.Reg. 3 which have bit allocations as shown in tables 4, 5, 6 and 7.

7	6	5	4	3	2	1	0
CalMode $\langle 1 \rangle$	CalMode $\langle 0 \rangle$	CalPolarity	MSPolarity	Trigmode $\langle 2 \rangle$	TrigMode $\langle 1 \rangle$	TrigMode $\langle 0 \rangle$	SleepB Sleep/Run

Table 4: Control Register 0

7	6	5	4	3	2	1	0
ReHitCT $\langle 1 \rangle$	ReHitCT $\langle 0 \rangle$	LVDSPowerSave	ProbeMode	DACsel $\langle 3 \rangle$	DACsel $\langle 2 \rangle$	DACsel $\langle 1 \rangle$	DACsel $\langle 0 \rangle$

Table 5: Control Register 1

7	6	5	4	3	2	1	0
DigInSel	MSPulse-Length $\langle 2 \rangle$	MSPulse-Length $\langle 1 \rangle$	MSPulse-Length $\langle 0 \rangle$	HitCount-Sel $\langle 3 \rangle$	HitCount-Sel $\langle 2 \rangle$	HitCount-Sel $\langle 1 \rangle$	HitCount-Sel $\langle 0 \rangle$

Table 6: Control Register 2

The function of the bits are as shown in table 8.

5.1.1 Trigger Sector Configurations

The selection of the trigger functions through the TrigMode bits are detailed in table 9.

VFAT2 has a number of possible trigger modes (TrigMode) defined by the combination of 3 bits (TrigMode$\langle 2:0 \rangle$) shown in table 9. The trigger functions are different depending on whether VFAT2 is used with the Roman Pots or with the GEM detectors. Bit TrigMode$\langle 2 \rangle$ is used to tell VFAT2 if it is in Roman Pot mode or GEM mode.

7	6	5	4	3	2	1	0
-	-	-	DFTestPattern	PbBG	TrimDAC-range $\langle 2 \rangle$	TrimDAC-range $\langle 1 \rangle$	TrimDAC-range $\langle 0 \rangle$

Table 7: Control Register 3

In Roman Pot mode Trig$\langle 2 \rangle$ is 0 and bits TrigMode$\langle 1 : 0 \rangle$ are used to define 4 sector configurations. There are 8 possible sector outputs within VFAT2. If all 8 are chosen by setting the TrigMode to 011 then the 128 channels are divided into eight equal regions. Sector 1 (S1) contains channels 1 to 16, sector 2 (S2) contains channels 17 to 32 etc. If 4 sectors are chosen by setting the TrigMode to 010 then the 128 channels are divided into four equal regions. Sector 1 (S1) contains channels 1 to 32, sector 2 (S2) contains channels 33 to 64 etc. The unused LVDS output drivers can be shut down to conserve power by setting the LVDPowerSave bit of Control register 1 to a "1".

In GEM mode, bit TrigMode$\langle 2 \rangle$ is 1. The allocation of channel number to sector is given in table 10. Channels 1,2,3 and 134,125,126,127 and 128 are not used and left unbonded.

A 24 bit counter (HitCount) is included which can be read via the I2C. The incrementing of the counter is programmable to either a FastOR of all channels or any of the 8 sectors. This way a diagnostic possibility exists for examining the activity of a particular region. The assignment of how the HitCounter should count is shown in table 11.

5.1.2 Measuring internal DAC response

Each DAC response can be measured periodically in order to apply the correct settings for biasing. VFAT2 will has two outputs labelled "DACo-I" and "DACo-V". These outputs feed to the DCU chip which has an on board ADC. The measured value can then be read back in digital form through the DCU chip I^2C.

A switching mechanism therefore exists in VFAT2 to route (one by one) the output of each current DAC to DACo-I, and each voltage DAC to DACo-V. The selection of the DACs is controlled by bits DACsel $\langle 3 : 0 \rangle$, see table 12.

5.1.3 Calibration functions

VFAT2 includes an internal calibration circuit. This circuit delivers an electronic test pulse to an injection capacitor at the input of a given channel (see section 5.5 for channel selection) therefore applying a charge pulse to the preamplifier. The test pulse switches between two voltages. One voltage is fixed (around 1.067 V) called the

Bit name	Function
Sleep/Run	0 = Sleep (Default), 1 = Run
TrigMode$\langle 1:0 \rangle$	Trigger mode settings : as in table 9
CalMode$\langle 1:0 \rangle$	Calibration settings : as in table 13
MSPolarity	Monostable input polarity - tells the monostable polarity of input signal 0 = positive I/P signal (default), 1 = negative I/P signal
CalPolarity	Calibration pulse polarity - to match with the input signal polarity 0 = positive I/P signal (default), 1 = negative I/P signal
LVDSPowerSave	Enables power saving for unused LVDS sector divers 0 = Enable all Sector LVDS drivers (default) 1 = Enable only Sector LVDS drivers needed (save power)
DACsel$\langle 3:0 \rangle$	Controls DAC selection for DCU monitoring, see table 12
HitCountSel$\langle 3:0 \rangle$	Defines the input for the HitCounter, see table 11
MSPulseLength$\langle 2:0 \rangle$	Defines the length of the monostable pulse, see table 19
ReHitCT$\langle 1:0 \rangle$	The cycle time (or number of bits) for the Hit counter
DigInSel	selects the input via the digital input pads (bypass of the analog frontend), default (0) analog pads
TrimDACrange$\langle 2:0 \rangle$	Adjusts the range of the TrimDACs, default (0)
PbBG	Enables pad access to the bandgap output, default 0 = pad unconnected
DFTestPattern	A predefined data packet is sent to the DataOut without need for an input signal or trigger

Table 8: Bit function of the control registers

baseline. The second voltage is variable (from around 1.074V to 877mV) and is called VCal. The injection pulse amplitude is the difference between the two voltages and the polarity is governed by the "CalPolarity" setting in the ContReg1.

Before applying a calibration pulse the calibration circuit response must be calibrated. For this one must connect the calibration circuit output (CalOut) to the DCU as shown in table 12 with setting 0110 (VCal to DACo-V). Measuring the amplitude of the voltage step is done in two stages. The first step is to measure VCal for all DAC settings (CalMode$\langle 1:0 \rangle = 01$). The second step is to measure the baseline also for each VCal DAC setting (CalMode$\langle 1:0 \rangle = 10$). The difference between the two is the voltage step applied for each VCAL DAC setting.

It is also possible to apply an external voltage pulse to a given channel by setting CalMode$\langle 1:0 \rangle = 11$ for test purposes in the lab. This latter mode will not be used during the running of the experiment.

The selection of calibration functions through the CalMode bits are detailed in table 13.

TrigMode⟨2⟩	TrigMode⟨1⟩	TrigMode⟨0⟩	Function
0	0	0	No Trigger (default)
0	0	1	One sector (S1)
0	1	0	Four sectors (S1 to S4)
0	1	1	Eight sectors (S1 to S8)
1	X	X	GEM mode (S1 to S8 as defined in table 10)

Table 9: TrigMode functions.

5.2 The Chip ID registers

There is a 24 bit chip ID contained within three Chip-ID registers called ChipID3 (ID23(MSB) - ID16), ChipID2 (ID15(MSB) - ID8) and ChipID1 (ID7 - ID0(LSB)). The 24 bits are defined by a set of fuses which are laser blown on wafer. The I^2C interface and register block is therefore presented with a 24 bit ID. However only 12 bits of this ID are used due to limitations in the data packet size on DataOut.

5.3 The latency register (LAT)

There is one 8 bit register used for programming the LV1A latency into the chip. Each bit represents one clock cycle of latency. The latency can be programmed from 1 to 256 clock periods (ie. up to 6.4μs). The default setting is 1000 0000 (=128 clock cycles).

5.3.1 The Upset register (UpsetReg)

The result of the Upset counter (explained in section 2.1) is stored in the Upset register bit for bit as in table 14.

GEM mode channel assignment					
Sector	Channel assignment to sector				
S1	4	28	52	76	100
	5	29	53	77	101
	6	30	54	78	102
S2	7	31	55	79	103
	8	32	56	80	104
	9	33	57	81	105
S3	10	34	58	82	106
	11	35	59	83	107
	12	36	60	84	108
S4	13	37	61	85	109
	14	38	62	86	110
	15	39	63	87	111
S5	16	40	64	88	112
	17	41	65	89	113
	18	42	66	90	114
S6	19	43	67	91	115
	20	44	68	92	116
	21	45	69	93	117
S7	22	46	70	94	118
	23	47	71	95	119
	24	48	72	96	120
S8	25	49	73	97	121
	26	50	74	98	122
	27	51	75	99	123

Table 10: Sector configuration for the GEM mode.

HitCountSel$\langle 3:0 \rangle$	Function
0 0 0 0	HitCounter counts a FastOR of all 128 channels
0 0 0 1	HitCounter counts S1
0 0 1 0	HitCounter counts S2
0 0 1 1	HitCounter counts S3
0 1 0 0	HitCounter counts S4
0 1 0 1	HitCounter counts S5
0 1 1 0	HitCounter counts S6
0 1 1 1	HitCounter counts S7
1 X X X	HitCounter counts S8

Table 11: Input selection for the HitCounter

DACsel⟨3⟩	DACsel⟨2⟩	DACsel⟨1⟩	DACsel⟨0⟩	Function
0	0	0	0	Normal Running (default) (DACo-V "low", DACo-I "Hi Z")
0	0	0	1	IPreampIn to DACo-I (DACo-V "low")
0	0	1	0	IPreampFeed to DACo-I (DACo-V "low")
0	0	1	1	IPreampOut to DACo-I (DACo-V "low")
0	1	0	0	IShaper to DACo-I (DACo-V "low")
0	1	0	1	IShaperFeed to DACo-I (DACo-V "low")
0	1	1	0	IComp to DACo-I (DACo-V "low")
0	1	1	1	IThreshold1 to DACo-I (DACo-V "low")
1	0	0	0	IThreshold2 to DACo-I (DACo-V "low")
1	0	0	1	VCal to DACo-V (DACo-I "hiZ")
1	0	1	1	CalOut to DACo-V (DACo-I "hiZ")
1	1	*	*	Spare

Table 12: VFAT2 DACs to DCU control

CalMode⟨1⟩	CalMode⟨0⟩	Function
0	0	Normal running (default)
0	1	CalOut = VCal (programmable voltage level) (possible to connect to DACo-V)
1	0	CalOut = Baseline (fixed voltage level) (possible to connect to DACo-V)
1	1	CalOut = External calibration pulse (not possible to connect to DACo-V)

Table 13: CalMode functions.

7	6	5	4	3	2	1	0
UpsetCounter⟨7⟩ (MSB)	⟨6⟩	⟨5⟩	⟨4⟩	⟨3⟩	⟨2⟩	⟨1⟩	UpsetCounter⟨0⟩ (LSB)

Table 14: The Upset register (UpsetReg)

5.4 The Channel Registers (ChanReg)

There are 128 active channels in VFAT2. Whilst most programmable settings are common to all channels there are some settings which need to be channel specific. These include the "CalChan" command, "MASK" and "TrimDAC" setting. To accommodate these channel specific commands each channel will be assigned an 8 bit Channel Register. There will hence be 128 Channel registers labelled ChanReg$\langle 2:128 \rangle$ for channels 2 to 128. ChanReg$\langle 1 \rangle$ has a slight variation.

7	6	5	4	3	2	1	0
-	CalChan	Mask	TrimDAC $\langle 4 \rangle$	TrimDAC $\langle 3 \rangle$	TrimDAC $\langle 2 \rangle$	TrimDAC $\langle 1 \rangle$	TrimDAC $\langle 0 \rangle$

Table 15: The Channel Specific register (ChanReg)

7	6	5	4	3	2	1	0
CalChan0	CalChan1	Mask	TrimDAC $\langle 4 \rangle$	TrimDAC $\langle 3 \rangle$	TrimDAC $\langle 2 \rangle$	TrimDAC $\langle 1 \rangle$	TrimDAC $\langle 0 \rangle$

Table 16: Channel Register 1 (ChanReg1)

There is one analog test channel which is numbered channel 0. This channel does not have it's own channel register, instead it uses the Mask and TrimDAC settings of channel 1. The CalChan setting for channel 0 is located in the MSB of ChanReg$\langle 1 \rangle$

5.5 The calibration channel selection

The internal calibration pulse can be delivered to any individual channel and any number of channels simultaneously. Bit CalChan in each channel's ChanReg is devoted to this function. The default setting for each bit is 0 which is for normal running. A logic 1 is for applying the calibration pulse to the specified channel.

5.6 Masking a channel

Each channel has to have the possibility of being masked in order to silence a noisy channel. This requires 1 Mask bit per channel. Bit "5" of the ChanReg is used for this function. The default setting for each bit is 0 which is for normal running (an active channel). A logic 1 is for applying the Mask, effectively switching off that particular channel.

5.7 Fine adjustment of the comparator threshold

The course setting for the threshold of the comparators is made via a DAC labelled ThReg. This is common for all channels.

The VFAT2 sensor has varying levels of input capacitance which can have a small effect on the gain of a given channel. The gain may also be modified by exposure to very high levels of radiation. Some channels may receive more radiation than others resulting in varying levels of gain.

Hence fine adjustment of the threshold on a channel by channel basis could be necessary. To prepare for this each channel is equipped with a 5 bit Trim DAC. Bits ChanReg$\langle 4:0 \rangle$ are allocated for this function.

5.8 The DAC registers

There are a number of DACs controlling the analog variables. These are IPreampIn, IPreampFeed, IPreampOut, IShaper, IShaperFeed, IComp, IThreshold1, IThreshold2 and VCal. Each of these DACs has an 8 bit register associated with it which can be set via the I^2C.

5.8.1 Sleep Settings

The allocation of I^2C registers and their sleep settings are given in tables 17.

Principal Registers :				
Reg. Name	Hardwired Sleep value	Software Default Value	Reg. Add.	Reg. type
Cont.Reg⟨0⟩	0000 0000	0000 0000	0	W/R
Cont.Reg⟨1⟩	0000 0000	0000 0000	1	W/R
IPreampIn	0000 0000	1010 1000	2	W/R
IPreampFeed	0000 0000	0101 0000	3	W/R
IPreampOut	0000 0000	1001 0110	4	W/R
IShaper	0000 0000	1001 0110	5	W/R
IShaperFeed	0000 0000	0110 0100	6	W/R
IComp	0000 0000	0111 1000	7	W/R
ChipID⟨0⟩			8	RO
ChipID⟨1⟩			9	RO
UpsetReg.			10	RO
HitCount0			11	RO
HitCount1			12	RO
HitCount2			13	RO
ExtRegPointer	0000 0000	0000 0000	14	W/R
ExtRegData	0000 0000	0000 0000	15	W/R
Extended Registers :				
Lat	1000 0000	1000 0000	⋆0	W/R
ChanReg⟨1 : 128⟩	0000 0000	0000 0000	⋆1 to ⋆128	W/R
VCal	0000 0000	0110 0100	129	W/R
VThreshold1	0000 0000	0000 0000	⋆130	W/R
VThreshold2	0000 0000	0001 1010	⋆131	W/R
CalPhase	0000 0000	0000 0000	⋆132	W/R
Cont.Reg⟨2⟩	0000 0000	0000 0000	⋆133	W/R
Cont.Reg⟨3⟩	0000 0000	0000 0000	⋆134	W/R
Spare⟨135⟩	0000 0000	-	⋆135	W/R
⋆ → addressed via Principal registers 14 and 15				

Table 17: The VFAT2 Register Sleep settings

6 The Masked Monostable Block

This block basically consists of a clocked monostable.

Figure 5 shows a block diagram for the channel from the shaper output through to SRAM1.

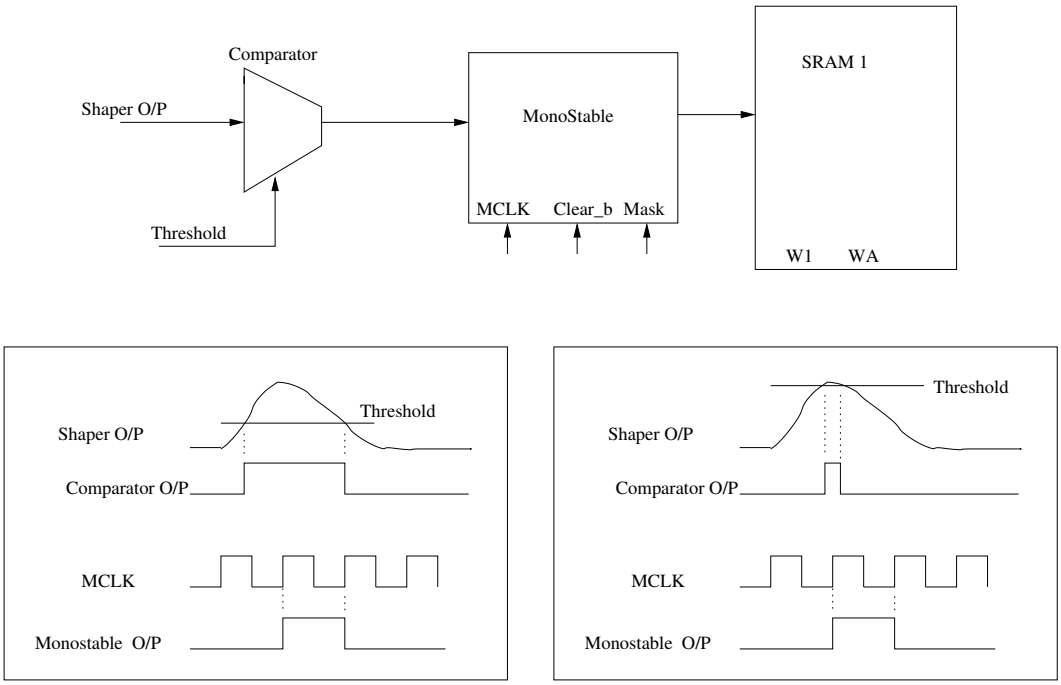

Figure 5: Block diagram of the masked monostable block.

The comparator is an asynchronous comparator without hysteresis. On passing a programmable threshold the comparator output goes high and returns low again when descending back through the threshold. For very large signals the comparator output may remain high for more than one clock cycle. Also if the signal barely passes threshold the comparator output may go high for less than one clock period. Both cases should trigger the monostable which should provide a pulse of one clock period only (in the default mode). It is this pulse which is sampled by SRAM1.

The mask bit can be used to disable the channel and force the monostable output to be always zero as in table 18.

Mask bit	Function
0	Normal operation (default)
1	Masked (Monostable output = 0)

Table 18: Mask bit functions.

The pulse from the monostable can also be stretched over many clock periods. The length is programmable as in table 19. If the monostable pulse is stretched (to say X clock periods) it is possible that the output of the comparator returns below threshold and a second signal makes the comparator go back over threshold. In this case the monostable output pulse remains high until X clock periods after the last over threshold result from the comparator.

MSPulseLength$\langle 2:0 \rangle$	Function
0 0 0	The MonoStable pulse length = 1 clock period (default).
0 0 1	The MonoStable pulse length = 2 clock periods.
0 1 0	The MonoStable pulse length = 3 clock periods.
0 1 1	The MonoStable pulse length = 4 clock periods.
1 0 0	The MonoStable pulse length = 5 clock periods.
1 0 1	The MonoStable pulse length = 6 clock periods.
1 1 0	The MonoStable pulse length = 7 clock periods.
1 1 1	The MonoStable pulse length = 8 clock periods.

Table 19: Stretching the MonoStable pulse length.

7 Logic Blocks

7.1 Command decoder

The Command Decoder receives the "T1" command which contains 4 separate signals encoded within 3 successive bits. The encoded commands are as given in table 2. The Command Decoder separates out these 4 commands into 4 separate pulses synchronous with the 40MHz. These 4 signals are "LV1A", CalPulse", "ReSync" and "BC0". The "LV1A", "ReSync" and "BC0" signals are pulses of one clock period (25ns duration). The "CalPulse" however has a duration of 8 clock periods (200ns).

No two successive T1 commands can arrive closer than 3 clock periods due to their encoded nature.

The Command Decoder has a self reset mechanism which resets when receiving 4 or more successive zeros on the T1 input.

7.2 Control Logic

The Control Logic contains a "Write State Machine" and counters for the BCO, EN and Upset counter. Figure 6 shows in a block diagram format these building blocks. All of these state machines are clocked by the 40MHz master clock and transitions take place on the rising edge.

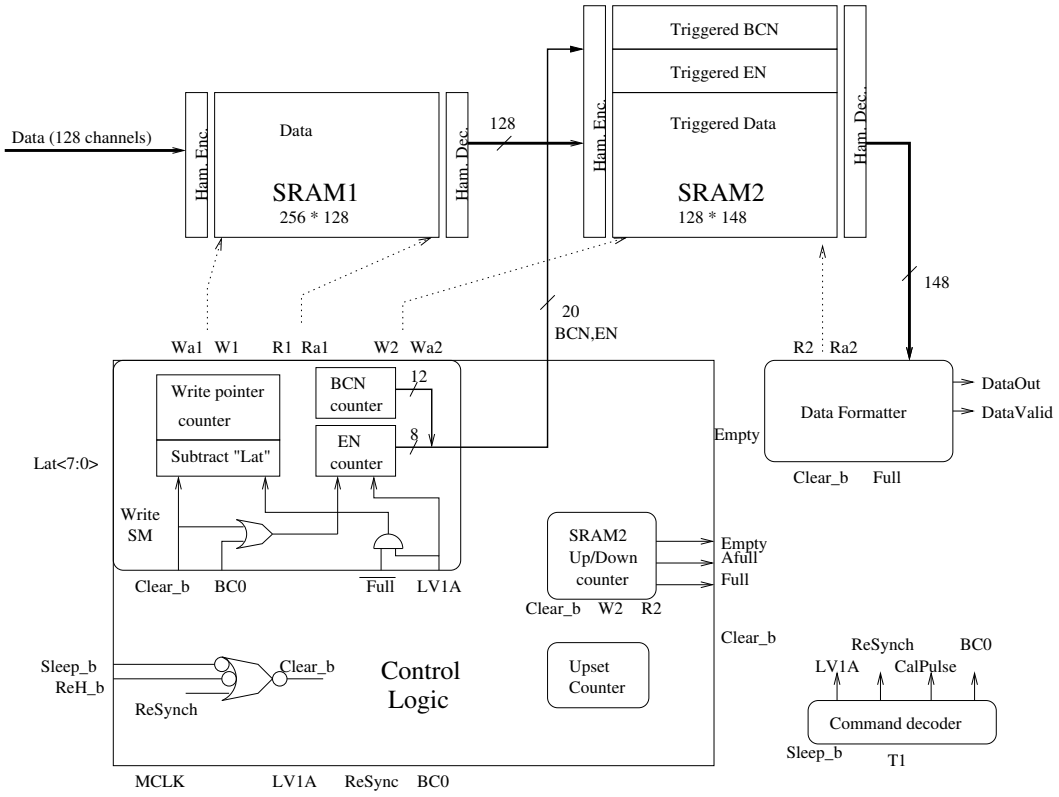

Figure 6: The Control Logic.

VFAT2 contains two SRAM blocks. Each 25ns the comparator outputs are sampled and the results stored in parallel in the first of the SRAM blocks (SRAM1). On receiving a trigger (LV1) the data stored in SRAM1 corresponding to the time slot that initiated the LV1A is transferred to the second SRAM (SRAM2). SRAM2 will therefore contain "hit" information for each channel for triggered events.

7.2.1 The Write State Machine

The "Write SM" controls the timing of the signals used for sampling the outputs of the comparators at 40MHz and for transferring triggered data from SRAM1 to SRAM2. Wa is the write address, W is the write signal, Ra is the read address and R is the read signal.

It contains the Write Pointer, Bunch Crossing Number (BCN) and Event Number (EN) counters.

The Write Pointer counter is a cyclic 8 bit counter that increments every clock period providing the write address "Wa". It is reset to zero on receiving a $\overline{Clear}$ signal.

The BCN counter is a cyclic 12 bit counter that increments for every clock period. It is reset to zero on receiving a $\overline{Clear}$ signal.

The EN counter is a cyclic 8 bit counter that increments for every LV1A. It is also reset to zero on receiving a $\overline{Clear}$ signal.

The function of the Write State machine is as follows: The "write pointer counter" provides "Wa" for SRAM1 incrementing every clock period. On receiving an LV1A the channel data corresponding to the trigger is located by subtracting the Latency (Lat$\langle 7:0\rangle$) number from the "Wa", hence $Ra1 = Wa1 - Lat$. The triggered channel data is then transferred to SRAM2 together with the value of the BCN and EN counter.

Inputs	Outputs
$\overline{Clear}$, MCLK, LV1A, Lat$\langle 7:0\rangle$	Wa, W1, Ra1, R1, Wa2, W2, BCN$\langle 11:0\rangle$, EN$\langle 7:0\rangle$

Table 20: Write state machine I/Os

A timing diagram for the Write SM signal is shown in 7.

7.2.2 The $\overline{Clear}$ Signal

A signal "$\overline{Clear}$" is defined as "$\overline{RESETh}$" OR "ReSynch" OR "$\overline{Sleep}$". On release of the "$\overline{Clear}$" signal the Write state machine starts.

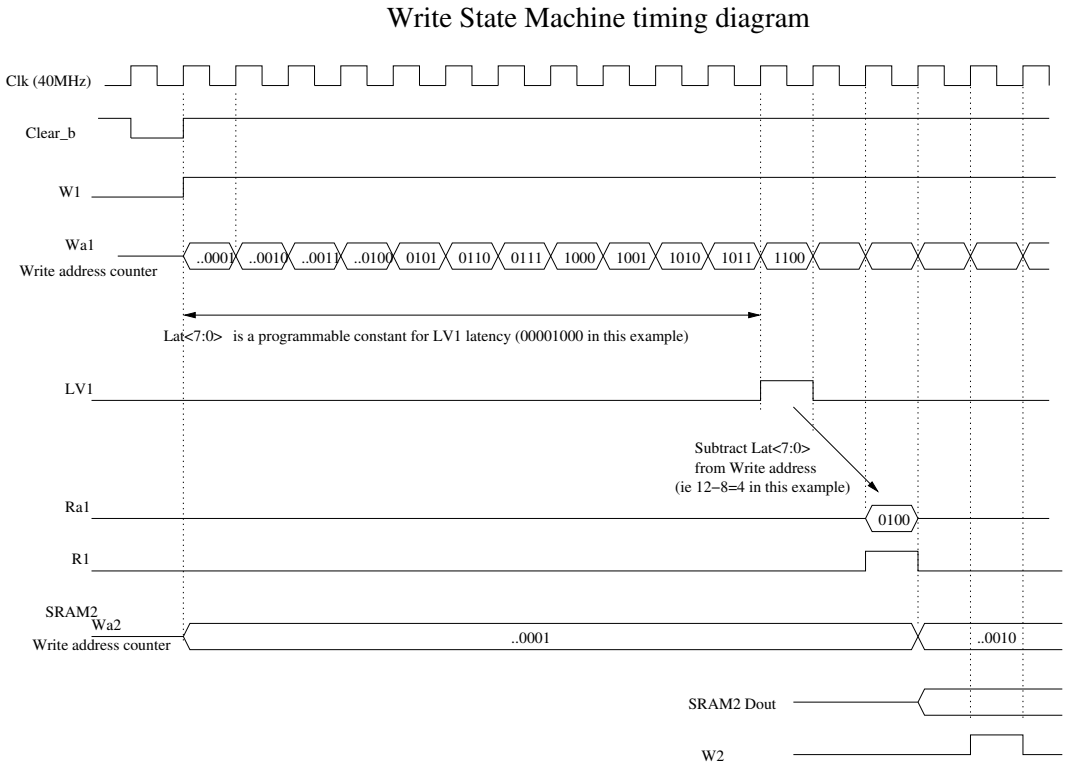

Figure 7: Timing diagram for the Write State Machine.

7.2.3 SRAM2 up/down Counter

The generation of flags is achieved via a 6 bit counter emulating the state of SRAM2. The counter counts up in steps of 1 for every W2 signal received. It counts down in steps of 1 for every R2 signal.

A number of flags are generated to satisfy internal VFAT2, and possible system emulation functions. These are specified in table 21 along with the thresholds for each.

LV1s are also blocked if they are received within the latency period following a ReSynch signal. Logically, an LV1A received during this period would relate to an event before or during the ReSynch and is hence not valid and is rejected.

Flag	Flag generator counter =	Corresponding no. of stored LV1s	Action within VFAT2
EMPTY	0	0	Start the "read" state machine on the "Empty" to "Not empty" transition
AFULL	126	127	No action inside VFAT2 Possible system emulator LV1A throttle
FULL	127	128	Inhibit further reception of LV1s by VFAT2 when this flag is set. The SRAM2 will fill to a maximum depth of 64.

Table 21: Flags used in the VFAT2.

7.3 The Data Formatter

The data format is defined as in figure 8.

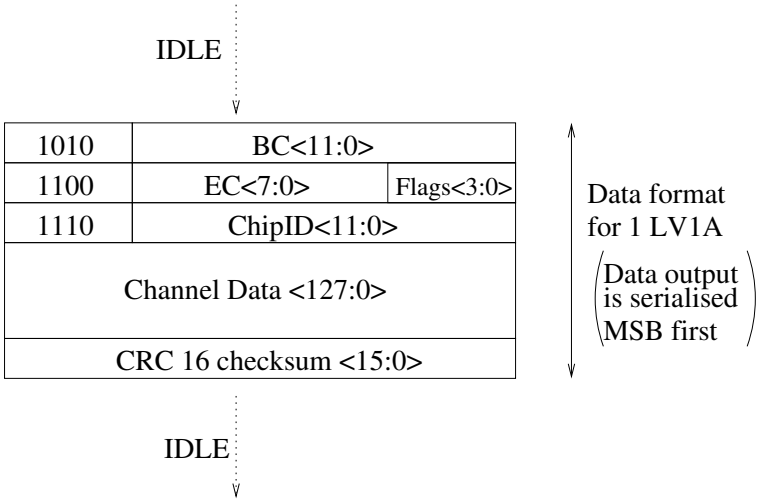

Figure 8: FAT2 data field format

The data exits the VFAT2 chip serially through an LVDS output pad called "DataOut". The data field exits the chip for each LV1A in the form given in figure 8, MSB first. Hence the first bit is the MSB of the BC number and the last bit is the LSB of the checksum. The 4 bits used for flags carry the information : *Hamming Error, AFULL, SEUlogic, SEUI2C.*

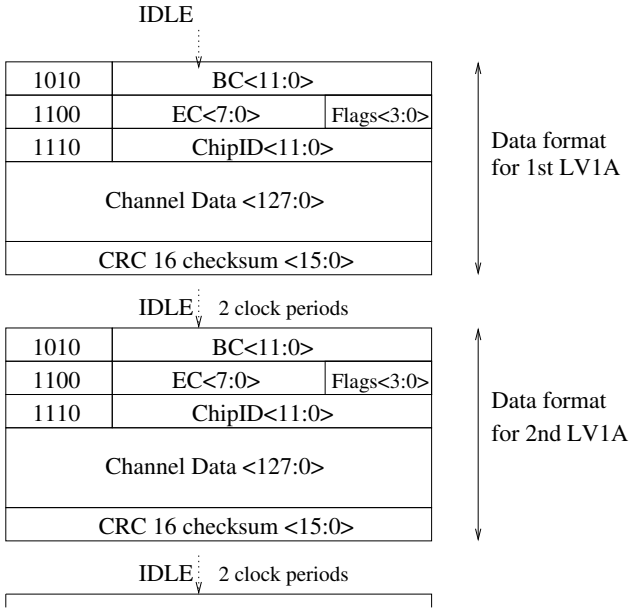

Figure 9: The data format for multiple triggers

If more than one LV1A has been stored in VFAT2 then data fields (corresponding

to each LV1A) exit the chip one after the other following a FIFO order. Each data field is separated by two clock periods which are called "IDLE". This is shown in figure 9. Hence the total time for the readout of 1 LV1A is 192 clocks for the data field plus 2 clocks for the IDLE period, this gives a total of 194 clock periods (4.85 μs).

Another LVDS output "DataValid" goes high for the duration of the data field and returns low to signify an IDLE period. Figure 10 shows the timing of this signal.

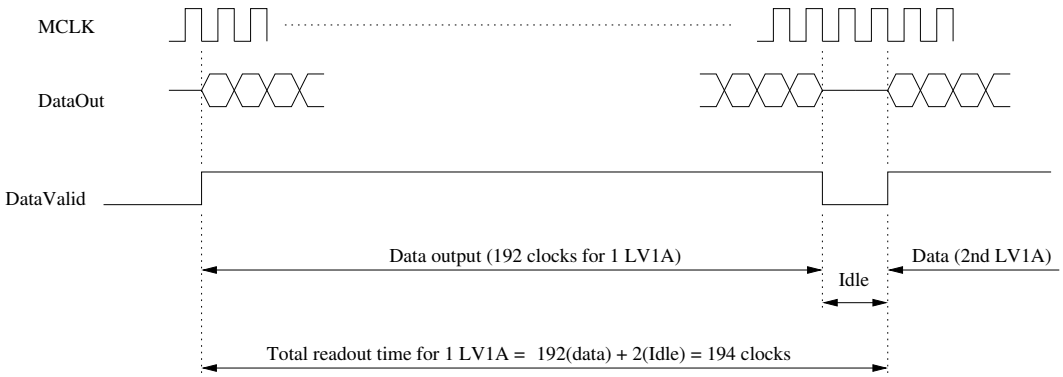

Figure 10: The DataValid signal

For TOTEM, it is foreseen to connect up to 16 VFAT2s to one GOL. Figure 11 shows this in block diagram format. The DataValid signal is connected from one VFAT2 to the "DAV/tx en" pin of the GOL (the CAV/tx er pin of the GOL should be tied low).

All VFAT2s will be synchronous and output their data at the same time. Hence following an LV1A, the "DataValid" signal goes high and the first bit of the data field for each VFAT2 is sent to each VFAT2s DataOut pin. The GOL will multiplex these bits within one clock cycle creating a 800M Bit/s stream. The bit data at the output of VFAT2 changes every 25ns. When the data field has finished, the "DataValid" signal returns low commanding the GOL to generate IDLE patterns.

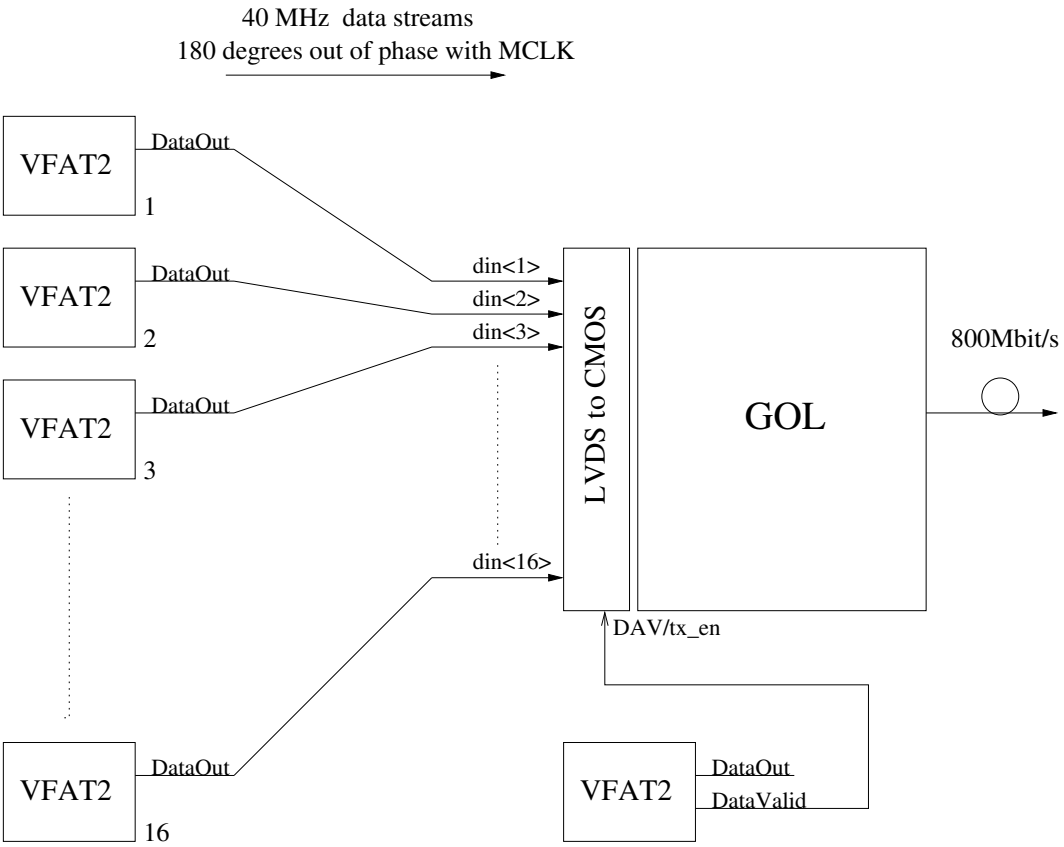

Figure 11: Connection between VFAT2 and GOL

8 Test Modes

VFAT2 has been designed with testability in mind and a number of analog and digital test possibilities have been implemented.

8.1 Scan Chain

The Scan chain enables the testing of all flip flops in the Control Logic to detect fabrication errors. When put into "ScanMode", all flip flops are cascaded. A serial pattern can then be clocked into "ScanIn". This serial pattern will pass through all flip flops and exit the chip through "ScanOut". If all flip flops are operational then the two patterns will match.

This test is useful because a faulty flip flop may not be noticed at the operation level because of the voting mechanism. Hence it would go unnoticed if only functional testing was employed. The Scan Chain however will find a flip flop with a "stuck at 1 or 0" condition.

If a number of VFAT2s are mounted on a board then the Scan chain inputs and outputs can be daisy chained together as in figure 12. All chips may then be tested at the same time.

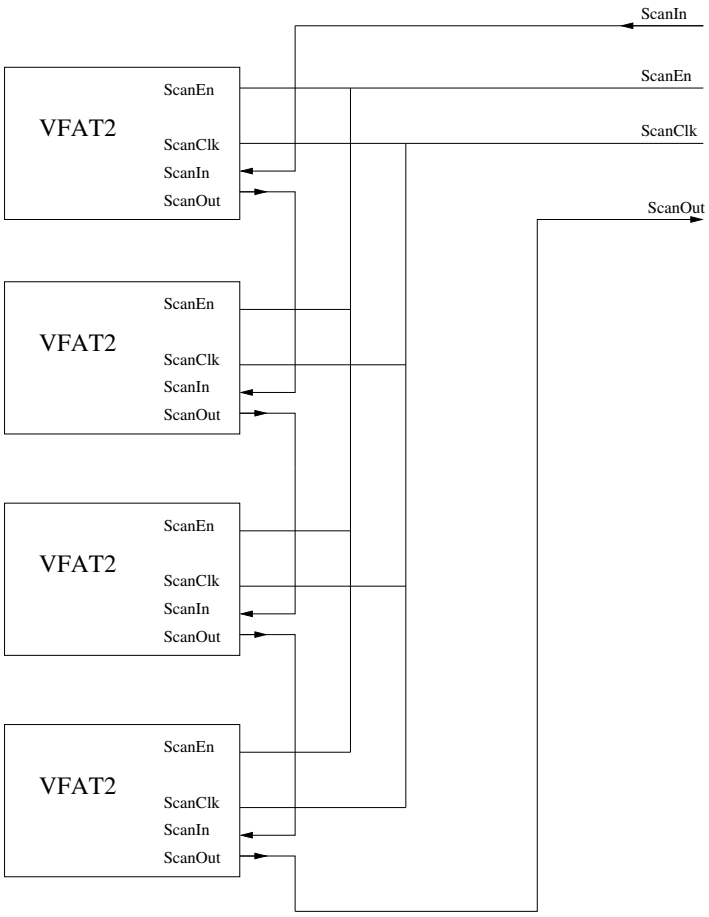

Figure 12: Daisy chaining of chips for Scan Chain testing.

9 Pad list

The floor plan for VFAT2 is given in figure 13 and the layout in 14.

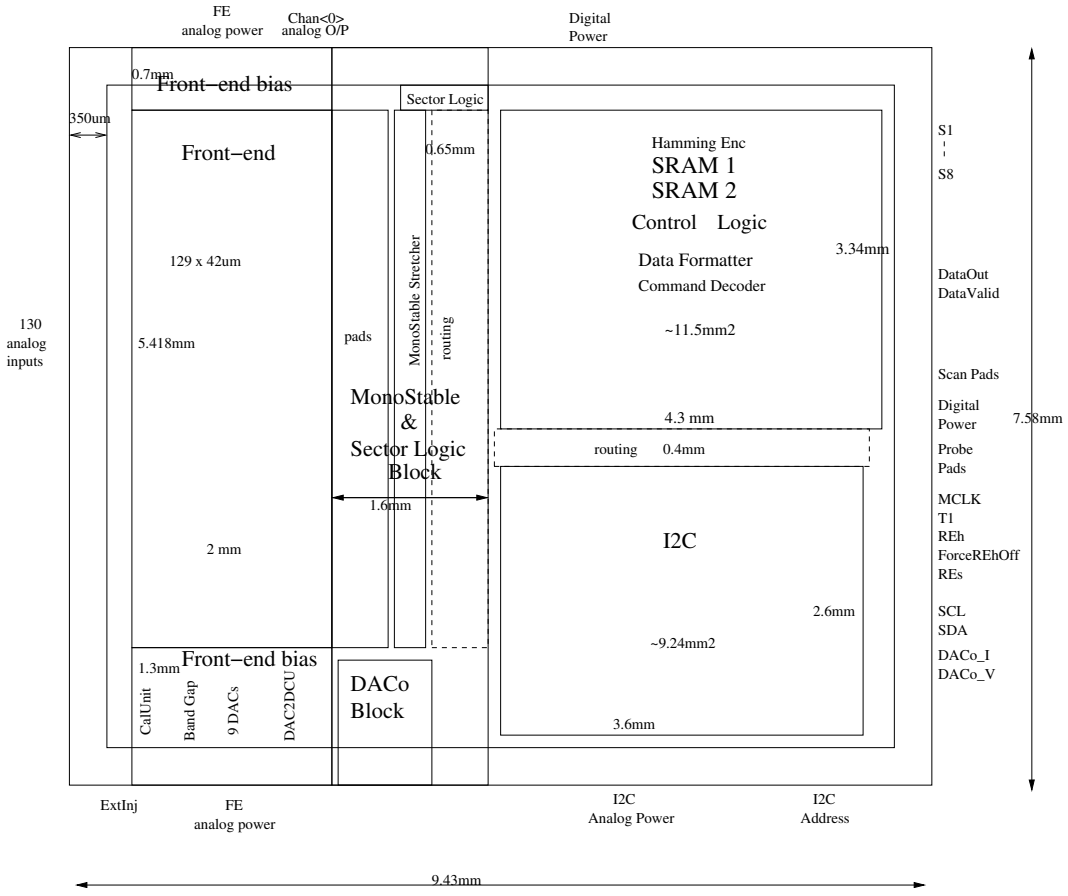

Figure 13: VFAT2 floorplan

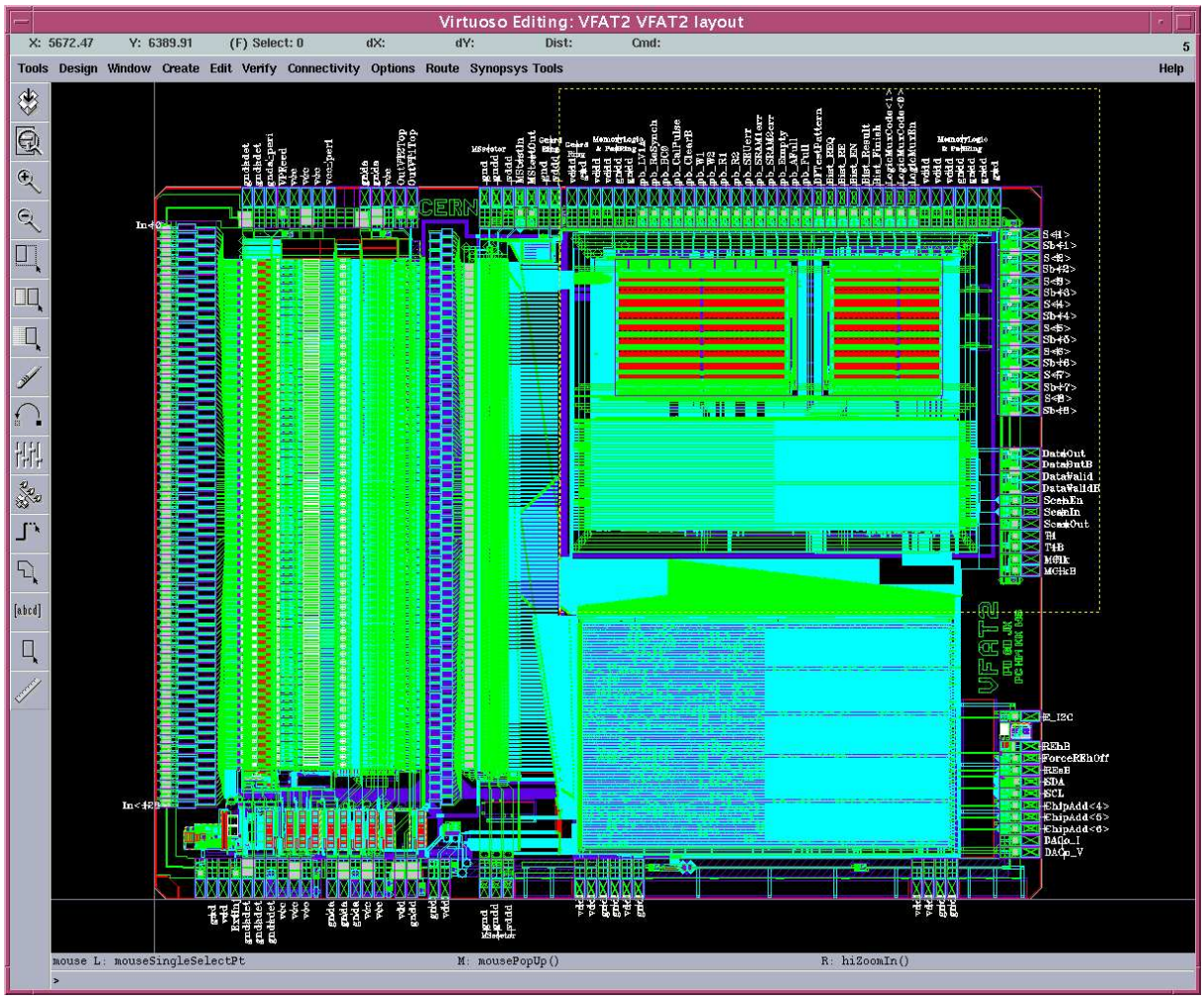

Figure 14: VFAT2 layout

A corresponding pad list is given in tables 22, 23, 24 and 25 for the 4 sides of the chip.

Pin No.	Pin Name	An./Dig., I/O	function	X	Y	Bond
1-129	In$< 0 : 128 >$	A,I	Analog input from sensors (In$< 1 : 128 >$) In$< 0 >$ is for test purposes	?	?	Yes

Table 22: VFAT2 pad list (left hand side, from top to bottom)

Pin No.	Pin Name	An./Dig., I/O	function	X	Y	Bond
130	BGV	A,I/0	BandGap output	?	?	No
131	gnd!	power	FE pad ring	?	?	Yes
132	vdd!	power	FE pad ring	?	?	Yes
133	ExtInj	A,I	test input	?	?	No
134	gnd!	power	Detector gnd	?	?	Yes
135	gnd!	power	Detector gnd	?	?	Yes
136	gnd!	power	Detector gnd	?	?	Yes
137	vdd!	power	FE vdda	?	?	Yes
138	vdd!	power	FE vdda	?	?	Yes
139	vdd!	power	FE vdda	?	?	Yes
140	gnd!	power	FE return	?	?	Yes
141	gnd!	power	FE return	?	?	Yes
142	gnd!	power	FE return	?	?	Yes
143	vdd!	power	FE vdda	?	?	Yes
144	vdd!	power	FE vdda	?	?	Yes
145	vdd!	power	FE vdda	?	?	Yes
146	gnd!	power	FE return	?	?	Yes
147	gnd!	power	DACo return	?	?	Yes
148	vdd!	power	DACo vdda	?	?	Yes
149	gnd!	power	MS Block substrate	?	?	Yes
150	gndd!	power	MS Block return	?	?	Yes
151	vddd!	power	MS Block vddd	?	?	Yes
152	vdd!	power	I2C vdda	?	?	Yes
153	vdd!	power	I2C vdda	?	?	Yes
154	gnd!	power	I2C return	?	?	Yes
155	gnd!	power	I2C return	?	?	Yes
156	vdd!	power	I2C guard ring	?	?	Yes
157	gnd!	power	I2C guard ring	?	?	Yes
158	vdd!	power	I2C vdda	?	?	Yes
159	vdd!	power	I2C vdda	?	?	Yes
160	gnd!	power	I2C return	?	?	Yes
161	gnd!	power	I2C return	?	?	Yes

Table 23: VFAT2 pad list (bottom side, from left to right)

Pin No.	Pin Name	An./Dig., I/O	function	X	Y	Bond
162	DACo-V	A,O	Voltage output	?	?	Yes
163	DACo-I	A,O	Current output	?	?	Yes
164-166	ChipAdd$< 6:4 >$	D,I	Chip address	?	?	Yes
167	SCL	D,I	I2C	?	?	Yes
168	SDA	D,I/O	I2C	?	?	Yes
169	REsB	D,I	Soft Reset	?	?	Yes
170	ForceREhOff	D,I	bond to gnd	?	?	yes
171	REhB	D,I	Hard Reset	?	?	Yes
172	E I2C	D,O	SEU in I2C, request REs	?	?	Yes
173-174	MCLKB, MCLK	D,I	LVDS clock (40MHz)	?	?	Yes
175-176	T1B, T1	D,I	LVDS pair	?	?	Yes
177	ScanOut	D,O	Scan chain	?	?	Yes
178	ScanIn	D,I	Scan chain	?	?	Yes
179	ScanEn	D,I	Scan chain	?	?	Yes
180-181	DataValidB, DataValid	D,O	LVDS pair	?	?	Yes
182-183	DataOutB, DataOut	D,O	LVDS pair	?	?	Yes
184-185	SB8, S8	D,O	LVDS pair	?	?	Yes
186-187	SB7, S7	D,O	LVDS pair	?	?	Yes
188-189	SB6, S6	D,O	LVDS pair	?	?	Yes
190-191	SB5, S5	D,O	LVDS pair	?	?	Yes
192-193	SB4, S4	D,O	LVDS pair	?	?	Yes
194-195	SB3, S3	D,O	LVDS pair	?	?	Yes
196-197	SB2, S2	D,O	LVDS pair	?	?	Yes
198-199	SB1, S1	D,O	LVDS pair	?	?	Yes

Table 24: VFAT2 pad list (right hand side, upwards from the bottom)

Pin No.	Pin Name	An./Dig., I/O	function	X	Y	Bond
200	gnd!	power	Memory Logic substrate	?	?	Yes
201-203	gndd!	power	Memory Logic return	?	?	Yes
204-206	vddd!	power	Memory Logic Power	?	?	Yes
207	LogicMuxEn	D,I	Logic test pin	?	?	Yes
208-209	LogicMuxCode< 0 : 1 >	D,I	Logic test pin	?	?	Yes
210	Bist Finish	D,O	Logic test pin	?	?	No
211	Bist Result	D,O	Logic test pin	?	?	No
212	Bist En	D,I	Logic test pin	?	?	Yes
213	Bist RE	D,I	Logic test pin	?	?	Yes
214	Bist REQ	D,I	Logic test pin	?	?	Yes
215	DFTestPattern	D,I	Logic test pin	?	?	Yes
216	pb Full	D,O	Logic test pin	?	?	No
217	pb AFull	D,O	Logic test pin	?	?	No
218	pb Empty	D,O	Logic test pin	?	?	No
219	pb SRAM2err	D,O	Logic test pin	?	?	No
220	pb SRAM1err	D,O	Logic test pin	?	?	No
221	pb SEUerr	D,O	Logic test pin	?	?	No
222	pb R2	D,O	Logic test pin	?	?	No
223	pb R1	D,O	Logic test pin	?	?	No
224	pb W2	D,O	Logic test pin	?	?	No
225	pb W1	D,O	Logic test pin	?	?	No
226	pb ClearB	D,O	Logic test pin	?	?	No
227	pb CalPulse	D,O	Logic test pin	?	?	No
228	pb BC0	D,O	Logic test pin	?	?	No
229	pb ReSynch	D,O	Logic test pin	?	?	No
230	pb LV1A	D,O	Logic test pin	?	?	No
231-232	gndd!	power	Memory Logic return	?	?	Yes
233-234	vddd!	power	Memory Logic Power	?	?	Yes
235	gnd!	power	Memory Logic guard ring	?	?	Yes
236	vddd!	power	Memory Logic guard ring	?	?	Yes
237	vddd!	power	MS Block guard ring	?	?	Yes
238	gnd!	power	MS Block guard ring	?	?	Yes
239	MStestOut	D,0	test point for Monostable	?	?	No
240	MStestIn	D,I	test point for Monostable	?	?	No
241	vddd!	power	MS Block vddd	?	?	Yes
242	gndd!	power	MS Block return	?	?	Yes
243	gnd!	power	MS Block substrate	?	?	Yes
244	OutVT1Top	A,0	test point for Frontend	?	?	No
245	OutVT2Top	A,0	test point for Frontend	?	?	No
246	vdd!	power	FE vdda	?	?	Yes
247-248	gnd!	power	FE return	?	?	Yes
249	vdd!	power	FE vdda peri	?	?	Yes
250-252	vdd!	power	FE vdda	?	?	Yes
253	VPFeed	A,I	Frontend test bias	?	?	No
254	gnd!	power	FE peri	?	?	Yes
255-256	gnd!	power	FE detector gnd	?	?	Yes

Table 25: VFAT2 padlist (top side, from right to left)

The active signals that are transmitted to and from VFAT2 are shown in table 26. Global signals are shared between more than one chip while "Unique" signals are specific to an individual chip.

Signal No.	Signal Name	An./Dig., I/O	function	Unique or Global
1	REh-B	D,I	Hard Reset	Global
2	REs-B	D,I	Soft Reset	Global
3-4	MCLK(B)	D,I	LVDS clock (40MHz)	Global
5-6	T1	D,I	LVDS pair	Global
7	SCL	D,I	I2C	Global
8	SDA	D,I/O	I2C	Global
9-10	DataOut	D,O	LVDS pair	Unique
11-12	DataValid	D,O	LVDS pair	Unique
13-14	S1	D,O	LVDS pair	Unique
15-16	S2	D,O	LVDS pair	Unique
17-18	S3	D,O	LVDS pair	Unique
19-20	S4	D,O	LVDS pair	Unique

Table 26: The signal list transmitted to and from VFAT2

References

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http://cmsdoc.cern.ch/~aspell/PACE3/design_docs/PACE3DigitalSpecV4.pdf

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