Final Lab Practical Exam (Concept Questions)

Due: Thu, 19 Nov 2020 15:21:13 (approximately 22 days ago)
[Score: 8 / 25 points possible]
Weight = 4.0

Instructions

This is a two-hour exam that you are given four hours to complete. Please pay careful attention to the due date for this exam. Press any of the 'Save' buttons often to make sure your work is saved. (Please do not double-click or click-storm the 'Save' button. That will cause problems for you.) Each time you save, the due date shown above will be updated. The course staff will be watching out for any system or infrastructure problems that might interfere with your progress. If you encounter a system problem, send e-mail to your lab TA. We cannot repair global Internet problems, but it's good for us to know about them.

When you save your work, scan the page to look for **Red warning text** that tells you that you've made some kind of syntax error. In addition, most text boxes where you must enter an answer are given an **orange** background color until you fill in a response and press "Save".

This exam is open-notes, open-book, and open-simulator. Nevertheless, you must not use commercial web sites that are not affiliated with the course and especially do not look at web sites that solve problems for you. You should also not seek help for any of these problems from any other person---including the course staff. You may look at Piazza, but you may not ask questions there. You are expected to be able to solve all of these problems on your own.

Academic Honesty Statement [0 ... -25 points]

The course staff want to make this exam as low stress as possible. In return, we expect that you will not engage in any form of academic dishonesty. Nevertheless, we expect that some students will, and we will be watching out for this. If you have evidence indicating any student is not in full compliance with the statement below, you can let the course staff know, and we will give it our full attention.
By typing my name, below, I hereby certify that the work on this exam is my own and that I have not received assistance from or given assistance to any other person or web site (other than the ECE 362 course web site) while completing it. I understand that if I fail to honor this agreement, I will fail the course and I will be recommended for expulsion from the university.

Raghuram Selvaraj 

Remember: It's all about the STM32F091RCT6

All of the questions and problems on this exam pertain specifically to the STM32F091RCT6 microcontroller that has been described in lecture and that you have been using in lab experiments.

Part 1: Concept Questions

There are 25 questions here. Don't spend too much time on any one. You should plan on spending 30 minutes on this section.

Q1 [1 point]

[1 point]

What value should be written to the ADC_CHSELR to measure an analog voltage on pin PB1 of the STM32F091RCT6? (Express your answer as a C-style hexadecimal integer.)

0x200 

Q2 [1 point]

[1 point]

What value should be ORed with ADC_CFGR1 to produce a left-aligned, 10-bit conversion result? Express your answer as a C-style hexadecimal number rather than the CMSIS symbols.

0x28 

Q3 [1 point]

[1 point]

Given that:

- VSSA is 0 V
- VDDA is 3.5300000000000002 V
- ADC_CFGR1 is set to 0x0

If the voltage applied to a pin configured for ADC input is 2.9240 V, what value will be read from the ADC_DR when ADC conversion completes? Express your answer as a C-style hexadecimal number. (In some cases, depending on how you calculate it, you might arrive at an answer that is 1 higher or 1 lower than what we expect. If so we'll still accept that as correct.)

0xD40 

Q4 [1 point]

[1 point]

Given that

- VSSA is 0 V
- VDDA is 2.5 V
- ADC_CFGR1 is set to 0x28

If the voltage applied to a pin configured for ADC input is 3.0100 V, what value will be read from the ADC_DR when ADC conversion completes? Express your answer as a C-style hexadecimal number. (In some cases, depending on how you calculate it, you might arrive at an answer that is 1 higher or 1 lower than what we expect. If so, we'll still accept that as correct.)

0xD0 

Q5 [1 point]

[1 point]

If the value 0xaf written to the DAC_DHR8R1 register produces a particular analog output voltage after the DAC is triggered, what value should be written to the DAC_DHR12L1 register to produce the same voltage? Express your answer as a C-style hexadecimal number.

0xaf0 

Q6 [1 point]

[1 point]

Given that

- VSSA is 0 V
- VDDA is 3.4699999999999998 V

if the value 0x2fa67c3a is written to the DAC_DHR12L1 register, what voltage will be produced on the analog output pin? (Obviously, some parts of the 32-bit value written to the DHR will be ignored.) Express your answer as a floating-point number with as much precision as you can in terms of Volts. (i.e., if your answer is 53 mV, you should write only "0.053". Do not write a unit.)

1.6833227539 

Q7 [1 point]

[1 point]

Assume the DAC_CR is in its default (reset) state. What value must be written to it to configure **Channel 1** for only the following things:

- Enable DMA trigger for channel 1
- Trigger on Timer 2 TRGO event
- Enable the trigger
- Enable the channel

Express your answer as a C-style hexadecimal number.

0x1025 ✓

Q8 [1 point]

[1 point]

Assume that TIM1_CCMR1 is in its default (reset) state. What values should you write to TIM1_CCMR1 so that:

- Channel 1 is configured for output, PWM mode 1, with preload enable
- Channel 2 is configured for output, toggle mode, without preload enable

(For all channels, do not set OCxFE or OCxCE) Express your answer as a C-style hexadecimal number.

0x3068 ✓

Q9 [1 point]

[1 point]

Given that:

- The system clock is 48 MHz
- TIM1_PSC = 115-1
- TIM1_ARR = 1158-1
- TIM1_CCR1 = 888
- the timer is configured for output PWM mode 1, output is enabled,
- and the output is routed to an external pin,

What will the duty cycle of the resulting output waveform be? Express your answer in terms of percent. 100.0 represents "always on". 50.0 represents a perfect square wave. (Express your answer with as much precision as possible.)

76.61777394 ✗

Q10 [1 point]

[1 point]

Given that:

- Output "high" pin voltage is 3.000 V
- Output "low" pin voltage is 0.0 V
- The system clock is 48 MHz
- TIM1_PSC = 36-1
- TIM1_ARR = 1721-1

and the timer is configured for output PWM mode 1, output is enabled, and the output is routed to an external pin connected to a resistor and capacitor comprising a low-pass filter like the one you connected to the TIM1_CH4 output in lab 7. What value should be written to TIM1_CCR1 to make the average voltage on the pin as near as possible to 0.561302 V? You may express your answer as a **positive decimal integer**. (No need for hexadecimal everywhere.)

967

Q11 [1 point]

[1 point]

Assume that SPI1_CR1 is in its default (reset) state. What value should be ORed with SPI1_CR1 to configure the SPI channel in the following way:

- Enable output in bidirectional mode
- Set the baud rate to 1500.000000 kHz
- Select master mode
- Set the clock polarity to 0 when idle

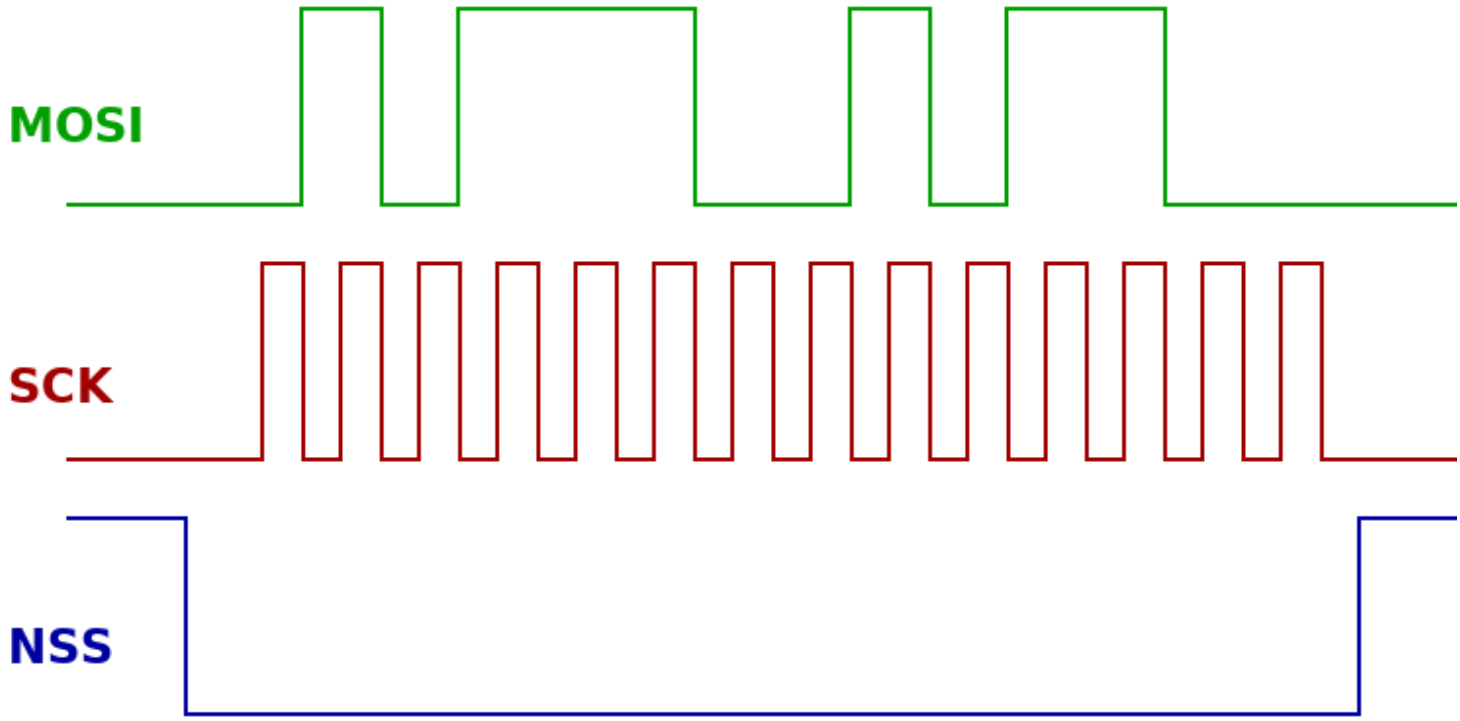
Express your answer as a C-style hexadecimal number.

0x8024

Q12 [1 point]

[1 point]

The following logic analyzer trace of an SPI transaction was made with CPOL=0, and CPHA=0, and automatic NSS assertion. Use this diagram for this and the next question.



What is the word size (in bits) of the SPI channel?

14 ✓

Q13 [1 point]

[1 point]

What value was written to the SPI_DR to produce the previous logic analyzer trace? Express your answer as a C-style hexadecimal number.

0x2E58 ✗

Q14 [1 point]

[1 point]

Consider the following logic analyzer trace of an I2C transaction where the first word is sent by the master device and the second word is either a request or response. Use this diagram for this and the next two questions.

What is the I2C address of the slave device the master device is communicating with? Express your answer as a C-style hexadecimal number.

0x7F

Q15 [1 point]

[1 point]

Is the first word a read or write request?

read

Q16 [1 point]

[1 point]

What value is communicated in the second word? Express your answer as a C-style hexadecimal number.

0x3FF

Q17 [1 point]

[1 point]

Consider the following logic analyzer trace of an asynchronous serial transmitter, just like the ones in the STM32, which is configured for 8-bit word size with no parity bits and one stop bit. The diagram shows the transmission of a single 8-bit character with tick marks to indicate the likely delineation of 1 and 0 bits in the protocol. Use this diagram for this and the next question.

What value must be written to USART_TDR to produce this pattern? Express your answer as a C-style hexadecimal number.

0x1CC

Q18 [1 point]

[1 point]

If generation of even parity would have been enabled, what value should the parity bit be for this transmitted word?

1

Q19 [1 point]

[1 point]

If the baud rate for a serial communication device is 385189 and it is configured for 8 bits, even parity, and 0.5 stop bits, how many useful characters of data are sent per second? Express your answer as a floating-point number with as much precision as you can.

Q20 [1 point]

[1 point]

For the STM32 USART, with a system clock of 48MHz, and a channel configured for 16x oversampling, what should the USART_BR register be set to have a baud rate of 6432? (Find the value that produces the nearest baud rate.) Express your answer as a C-style hexadecimal number.

Q21 [1 point]

[1 point]

If the CxS is in the default configuration for every channel of **both** of the DMA controllers, which DMA channel **of which controller** is triggered for USART3_TX?

DMA1_Channel7 ✓

Q22 [1 point]

[1 point]

If the CxS is in the default configuration for every channel of **both** of the DMA controllers, which DMA channel **of which controller** is triggered for DAC_Channel2?

DMA2_Channel4 ✗

Q23 [1 point]

[1 point]

Assume that DMA1_CCR1 is in the default (reset) configuration. What value should be ORed with it to enable the following things:

- High priority
- 8-bit memory data size
- 8-bit peripheral data size
- Memory increment mode enabled
- Peripheral increment mode disabled
- Circular mode enabled
- Read from peripheral and write to memory
- Transfer error interrupt enabled
- Half Transfer interrupt disabled
- Transfer Complete interrupt enabled
- Enable the channel

Express your answer as a C-style hexadecimal number.

0x20EB ✗

Q24 [1 point]

[1 point]

If a DMA channel is triggered by a timer 937741 times per second, and the DMA channel's CNDTR value is 2034, and the Half-Transfer interrupt of the channel is enabled, how many times per second will the Half-Transfer interrupt be raised? Express your answer as a floating-point number with as much precision as you can.

922.0658800393

Q25 [1 point]

[1 point]

What is the absolute address of the DMA2_CCR3 configuration register? Express your answer as a C-style hexadecimal integer.

0xD28

Yes, there are only 25 concept questions this time.

Part 2: Programming Exercise

This part is reported separately.