Pre-lab Assignment 8

Due: Fri, 30 Oct 2020 23:59:59 (approximately 41 days ago)
[20 points possible] [100 penalties possible] [0 penalties graded so far]

The following questions should prepare you for a lab involving the Serial Peripheral Interface (SPI) hardware found in the STM32.

Academic Integrity Statement [0 ... -100 points]

By typing my name, below, I hereby certify that the work on this prelab is my own and that I have not copied the work of any other student (past or present) while completing it. I understand that if I fail to honor this agreement, I will receive a score of zero for the lab, a one letter drop in my final course grade, and be subject to possible disciplinary action.

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(1) [1 point]

The clock output for an SPI channel is driven by the STM32 at a fraction of the system clock. If the system clock is 48 MHz, what will the SPI clock frequency be if the SPIx_CR1 register's BR (baud rate) field is set to the three-bit binary value '100'? Express your answer in Hz. (e.g., if your answer is 4 kHz, write 4000)

1500000

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(2) [1 point]

What value should be used for the BR field to set up an SPI frequency of approximately 1.5 MHz? Again, assume the STM32 system clock is 48 MHz. Enter your answer as a three-bit binary value.

100

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(3) [1 point]

Consult the STM32 Family Reference Manual's description of the SPIx_CR2 register's DS (data size) field. When setting the field, what happens when you set this field to the binary value '0001'?

The data size field is set to 8-bit mode

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(4) [1 point]

Look at the documentation for the STM32's SPIx_CR1 register. Upon reset or the first time it is enabled, what is the default SPI clock polarity configuration for the STM32's SPI peripheral? (e.g. is it "CK to 0 when idle" or "CK to 1 when idle"?)

CK to 0 when idle

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(5) [1 point]

Look at the documentation for the STM32's SPIx_CR1 register. Upon reset or the first time it is enabled, what is the default SPI clock phase configuration for the STM32's SPI peripheral?

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(6) [1 point]

Look at the documentation for the STM32's SPIx_CR2 register. Upon reset or the first time it is enabled, what is the default SPI transfer data size? (Don't write down the DS bitfield value. Say how many bits the transfer data size is set to.)

8

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(7) [1 point]

Examine the STM32 Family Reference Manual documentation for the SPIx_CR2 NSSP bit. (See page 793 of the FRM as well as the description on page 768.) What must the CPHA bit of the SPI_CR1 register be set to in order for automatic NSS pulse management to occur?

0

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(8) [1 point]

What value should you write to SPIx_CR2 if you want to configure it for a 12-bit word size, NSS pulse management, and SS output enable? Specify this value symbolically by ORing together the CMSIS symbolic names.

SPI_CR2_NSSP | SPI_CR2_DS_DS0 | SPI_CR2_DS_DS1 | SPI_CR2_DS_DS3 | SPI_CR2_SS

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(9) [3 points]

What external pins can each of the following signals be routed to for the STM32F091RCT6? Keep this list handy as you do lab 8. You will need to know these pins when you do the wiring for the lab. Remember that the STM32F091RCT6 has no GPIO Port E, and only a few pins for Ports D and F.

SPI2_NSS: PB12, PB9
SPI2_SCK: PB10, PB13
SPI2_MOSI: PB15, PC3

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(10) [1 point]

Which external pins are used for SPI2 signals when their AFR values are 0101?

PB9. PB10

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(11) [1 point]

Use the CMSIS symbols to write a C statement that will configure the RCC to enable the clock to the SPI2 peripheral.

RCC->APB1ENR |= RCC_APB1ENR_SPI2EN;

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(12) [1 point]

What I/O register and bit indicates that the SPI2 transmitter is empty? (Specify the CMSIS symbolic names.)

GPIOB_ODR_ODR9

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(13) [1 point]

What field must be set in the SPIx_CR2 register to trigger a DMA transfer every time the SPI transmit buffer is empty? (Specify it as a CMSIS symbolic name.)

SPIx_CR2 _LDMA_TX

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(14) [1 point]

Which bit in what I/O register should be set to invoke an interrupt each time the SPI2 transmitter buffer is empty?

GPIOB_ODR_ODR12

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(15) [1 point]

Which DMA channel number must be used with the SPI2 transmitter on the STM32F091RCT6? (Whenever you see a question like this, you should look at Table 31 that starts on page 202 of the STM32 Family Reference Manual. Pay careful attention to the superscript (1) and (2) notes. One of them is the default and the other represents something that can be selected by changing SYSCFG register fields.)

The TAs mentioned the differences between Table 31 (for the STM32F07) and Table 32 (for the STM32F09, which is what we have). I was hoping to just use the **default mapping** for the SPI2_TX. That's the same between the F07 and F09. Differences in SYSCFG_CFGR1 and DMA_CSELR/RMPCR can then be discounted. We don't need to make this painful. There's a DMA channel that's easy to use for SPI2_TX. Decide which one that is.

Channel 7

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(16) [1 point]

Write a C statement to initialize the DMA Channel specified in question 15 to set the peripheral data transfer size to be 16 bits. You may assume that all the bits for the field should set are already initialized to zero. Use CMSIS symbols to write the statement.

```
DMA->CCR7 = DMA_CCR_PSIZE0;
```

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(17) [1 point]

Write a C statement to initialize the DMA channel specified in question 15 so that the direction of transfer is from memory to peripheral. Use CMSIS symbols to write the statement.

```
DMA->CPAR7 = (uint32_t)(&(GPIOB->BSRR[12]));
```

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(18) [1 point]

Write a C statement to configure the appropriate register of the DMA channel specified in question 15 to transfer 42 data elements. Use CMSIS symbols to write the statement.

```
DMA->CNDTR7 |= 42-1;
```