

EAGLE Design Rules

The circuit diagram illustrates a two-stage CMOS differential amplifier. The first stage is a differential pair of NMOS transistors (2N3820) with a tail current source implemented using a PMOS transistor (2N3820) and a 100kΩ resistor connected to a 4.7μF capacitor. The differential outputs of the first stage are connected to the gates of a second differential pair of PMOS transistors (2N3820). The sources of these PMOS transistors are connected to a common source node, which is biased by a current mirror consisting of two NMOS transistors (2N3820) and a 100kΩ resistor connected to a 4.7μF capacitor. The output of the second stage is a single-ended signal, which is then connected to a load resistor (100kΩ) and a coupling capacitor (4.7μF) leading to the final output. The circuit is powered by a 10V supply (Vcc) and grounded (GND).

