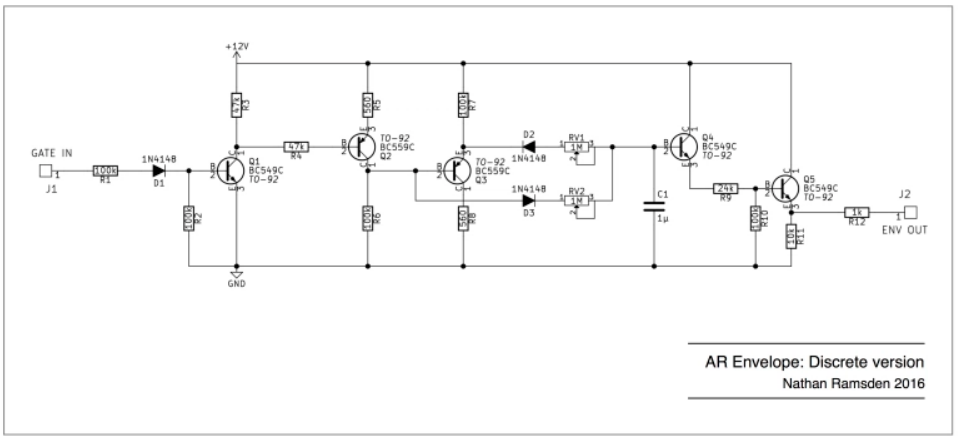
…Envelope Circuits: a simple discrete AR design

As a companion to my simple op-amp AR envelope circuit (https://synthnerd.wordpress.com /2016/04/06/envelope-circuits-a-simple-ar-design-using-op-amps/), here's a discrete version. It has the same basic functionality – gated input, variable attack and release times – but is made with transistors instead of integrated circuits. Power consumption is very low (just a handful of mA), and it runs from a positive supply of your own choosing. Like its op-amp cousin, it could be powered with a battery, or in a Eurorack system, or you could add it into an existing synth like the Moog Werkstatt as a mod (https://synthnerd.wordpress.com/moog-werkstatt-o1/).

The main difference between this and the op-amp circuit, aside from it being discrete, is that I have included a very simple way to set the level of the envelope output (see below for details).

RV1 is Release, RV2 is Attack. The Gate input can be anything over a couple of volts. Negative-going inputs (eg., from a bipolar LFO) will be removed by D1. The output goes to nominally 0V when fully off (closer than the op-amp version, in fact).



(https://synthnerd.files.wordpress.com/2016/06/discrete-ar.jpg)
Discrete AR envelope schematic

Parts List

R1, R2, R6, R7, R10: 100k
R3, R4: 47k
R5, R8: 560 Ohm
R9: 24k
R11: 10k
R12: 1k
RV1, RV2: 1M linear pot
C1: 1µ non-polarized
D1, D2, D3: 1N4148 or equivalent
Q1, Q4, Q5: BC549C or equivalent
Q2, Q3: BC559C or equivalent

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How it works

Compare the first pair of transistors with my discrete gate buffer (https://synthnerd.wordpress.com/2016/03/17/synth-diy-gate-buffer/) circuit. A positive voltage on the input turns on Q1, taking the base of Q2 low. This turns on Q2, taking its collector high. This is how we drive our envelope.

Now compare the diode and potentiometer arrangement with my op-amp AR (https://synthnerd.wordpress.com/2016/04/06/envelope-circuits-a-simple-ar-design-using-op-amps/). Once you're past the transistors, it works in basically the same way.

Q3 inverts the output of Q2, so when Q2 is on, Q3 is off, and vice versa. When the collector of Q2 is high, the capacitor charges through diode D3 and pot RV2 (Attack). When the gate input goes low, the transistors Q1-3 switch off, off, and on, respectively. In this state, the capacitor discharges through RV1 (Release) and D2.

Note the two 560 ohm resistors: one on the emitter of Q2, the other on the collector of Q3. When the gate input is high and the capacitor is charging, current flows through Q2's emitter resistor; when the gate is off and the capacitor is discharging, current flows through Q3's collector resistor. These two resistors put a lid on the current flow and limit the fastest times for Attack and Release. The value is a trade-off between current and snappiness. With the values shown, maximum current through these resistors is around 16mA and the fastest rise and fall times of the envelope are around 2ms.

The final two transistors in the circuit after the capacitor are the output buffer; notice the two resistors between them, forming a potential divider. With the values shown, if you run this circuit on 12V, the envelope output will be around 8V max.

There are better ways to set the peak level of an envelope, but my aim here is to keep things simple as a base for experiment.

Changes

The most obvious things to tweak are the envelope times and the output level.

The values of the two potentiometers affect the attack and release times, but the envelope can be substantially stretched by using a larger capacitor. It would be easy to add a switch that connected, say, a 4.7µF or 10µF capacitor in parallel with the existing one, which would multiply the envelope's times substantially (use perhaps a 25V electrolytic, with its -ve terminal to ground).

The two resistors between the output buffer transistors can be adjusted to suit your requirements. If you want full-scale output (ie., envelope peak closer to the supply voltage), remove R9 and R10, and connect the emitter of Q4 directly to the base of Q5. In fact, this circuit will also work with just a single NPN as a buffer (miss out Q4 and the divider resistors, connect the cap to the base of Q5), but amongst other things the 'zero' value is less close to actual zero; if you want to experiment with a single transistor here, setting the level of the output can be done by replacing the 10k resistor on its emitter with a pair of resistors as a potential divider, or even a 10k trimmer with the output taken from the wiper.

Feel free to experiment with the circuit in Falstad's handy online simulator (http://tinyurl.com /js5vsc8).