VERILOG ASSIGNMENT 3
GROUP 17
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Binary Counter :-
It is a circuit that counts either up or down depending on the circuit. In this assignment, we have to design a 4-bit counter using behavioural and structural design.

For behavioural design, the code is straight forward. We take a register variable and increment it on every rising edge of the clock. We also have to implement an asynchronous reset, which means that whenever the reset signal is high, counter value = 0 irrespective of the clock pulse.

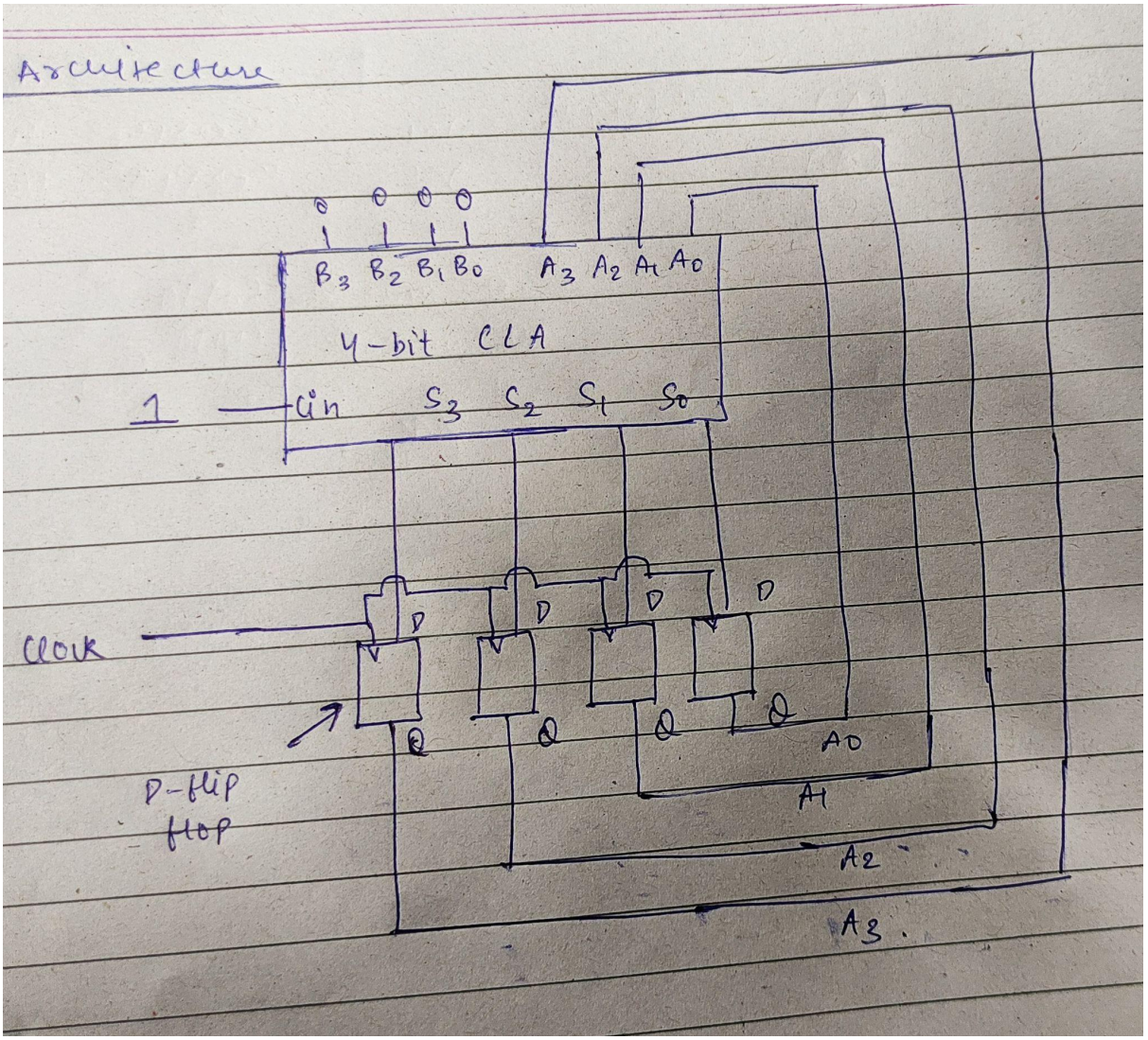
Clock Divider :-
As the system frequency of the FPGA board is very high (100Mhz), we first have to develop a clock divider circuit that divides the clock pulse before inputting it to the counter. The desired clock frequency is 20Hz, hence we need a dividing factor of 100 MHz / 20Hz = 5 Mhz.
For that we have developed a module that toggles the output clock only when the internal counter in the module reaches a certain value. That certain value is the clock dividing number. The internal counter is incremented by the system clock. The value of the dividing factor is 5000000, for the desired frequency of the counter.

Optimised Adder :-
We will be using a 4 bit Carry Look Ahead Adder. With one input as a 4 bit number (A), we only have to increment that number by 1. This can be achieved by assigning another number (B) as 0 and assigning input carry as 1 (cin = 1).
We know :-
Pi = Ai ^ Bi
Gi = Ai & Bi
Ci = Gi + Pi & Ci-1
With all the Bi's as 0, we get Pi = Ai and Gi = 0
Hence the simplified carry equations are :-
C1 = A0
C2 = A0 & A1
C3 = A0 & A1 & A2
C4 = A0 & A1 & A2 & A3

We know the sum equations :-
Si = Pi ^ Ci
=> Si = Ai ^ Ci
The simplified equations are :-
S0 = A0 ^ 1 = ~A0
S1 = A1 ^ A0
S2 = A2 ^ (A0 & A1)
S3 = A3 ^ (A0 & A1 & A2)

Counter Circuit Architecture :-

We use the output of the 4 bit adder as the input to 4 D flip flops. Every bit of sum will be the input of a flip flop. Then the output of the D flip flops would be sent back to the adder as 4 bits of input A. The output of the flip flops is also the output of the counter. If the output of flip flops is X, then the value at the input of the flip flops would be X+1, as this is the value given out by the adder and this value would be the output of the counter on the rising edge of the clock input of the counter.



Submitted Verilog files:

Counter_adder.v
Counter_adder_tb.v
Counter_behav.v
counter_behav_tb.v