Fully-integrated wideband CMOS VCO with improved *f–V* linearity and low tuning sensitivity

C.-W. Kim, K.-H. Koo and S.-W. Yoon

A technique to improve the linearity of the frequency–voltage (f–V) characteristic and to reduce the differential tuning sensitivity, K_{VCO}, of voltage-controlled oscillators (VCOs) is proposed. The VCO designed using the linearisation technique is tunable from 806 to 1113 MHz with a 34% tuning range and exhibits a nearly constant K_{VCO} of 62 MHz/V over the entire frequency range.

Introduction: Voltage-controlled oscillators (VCOs) are the most critical building blocks in phase-locked loop (PLL)-based frequency synthesisers. Using a VCO with a linear f–V characteristic gives the advantage of having the same PLL transfer function with the same loop filter for all frequencies inside the frequency range. If the VCO gain changes owing to the nonlinear f–V relation, the loop gain of the PLL changes for frequencies inside the frequency range. This eventually leads to jitter transfer and generation [1, 2]. Furthermore, the large capacitance ratio of MOS varactors obtained from their steep C–V characteristic gives rise to an excessively nonlinear and high K_{VCO}, which in turn can result in increasing noise and spurious power owing to frequency modulation of the control voltage noise [2–4].

In this Letter, we propose a technique to improve the f–V linearity and to reduce the K_{VCO} of CMOS VCOs. The VCO designed using the proposed technique was implemented in a standard 0.18 μm CMOS process. The overall performance of the VCO is discussed.

VCO design and implementation: The schematic of the proposed VCO is shown in Fig. 1. It is a differential VCO with both PMOS and NMOS cross-coupled pairs, which generate a negative resistance. The dual cross-coupled topology helps to generate a symmetric oscillation waveform at the resonator node. This ensures equal rise and fall times of the oscillation waveform, which suppresses the $1/f$ noise up-conversion. The resonator of the VCO consists of a spiral inductor (L), two MOS varactors (C_1, C_2), and three resistors (R_1, R_2, R_3). R_1 and R_2 are connected in parallel to the C_1 and C_2 nodes to precisely control the varactor voltage. The resistances of R_1, R_2, and R_3 should be high enough not to affect the Q-factor and power consumption of the VCO.

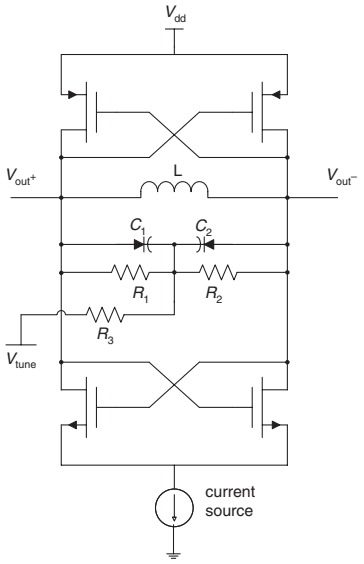

Fig. 1 *Schematic of differential VCO proposed in this work*

To make a comparison between the proposed VCO having additional resistors in the resonator and the conventional VCO without additional resistors, we performed harmonic balance simulations using Agilent's ADS. The simulated results for the oscillation frequency against tuning voltage and phase noise characteristics are shown in Figs 2*a* and *b*.

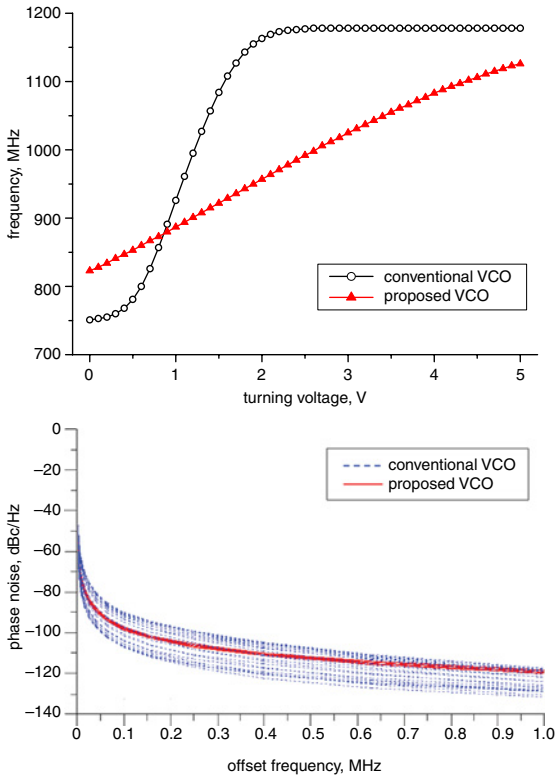

Fig. 2 *Comparison of simulated results between proposed and conventional VCOs*

a Oscillation frequency against tuning voltage V_{tune}
b Phase noise characteristics within entire tuning range (V_{tune}= 0 – 5 V, 0.5 V step)

In Fig. 2*a*, both VCOs show similar oscillating frequency ranges but the shapes of the f–V transfer curves are significantly different. The transfer function of the conventional VCO exhibits a high gain (referred to as K_{VCO}) across a narrow linear range for voltage control and early saturation, in which the frequency was stuck and no longer controllable. On the other hand, the transfer function of the proposed VCO shows a low gain across a wide linear range, in which the VCO is very responsive with a constant slope. In the conventional LC resonator, the tuning voltage, V_{tune}, is applied directly to the MOS-varactors. Thus, the capacitance of the varactors changes steeply with respect to V_{tune}. If additional resistors (R_1, R_2, and R_3 in Fig. 1) are connected, the voltage across them changes very gradually with varying V_{tune} since the voltage becomes $(R_{1(2)}V_{tune})/(R_{1(2)} + R_3)$, which leads to a gradual variation in the capacitance of the MOS varactors. This makes the fine tuning of the VCO to a desired oscillating frequency possible, as the f–V conversion is made with much higher resolution. Furthermore, the gain in the proposed VCO leads to a reduction in noise and spurious powers of PLL-based synthesisers.

Fig. 2*b* shows the simulated phase noise characteristics for both VCOs within the entire tuning range. The minimum phase noise of the conventional VCO (dashed lines) is 4 dB lower than that of the proposed VCO (solid lines), while the maximum phase noise of the proposed VCO is 7 dB lower than that of the conventional one. The deviation of the phase noise with respect to V_{tune} in the proposed VCO is smaller than that in the conventional VCO, which probably results from the more linear tunability and lower K_{VCO} in the proposed VCO.

We fabricated the proposed VCO using TSMC's 180 nm CMOS technology to verify the simulation results. The interconnection lines were designed with a ground-shielded microstrip line (GSML) structure to significantly reduce the dielectric loss of the low resistive silicon substrate [5]. Fig. 3 shows a die photograph of the fabricated VCO chip. The chip size is 0.815 × 0.680 mm.

Experimental results: The VCO chip was wire bonded onto an Au/FR-4 substrate. Single-ended measurements were performed on one of the differential output signals, while the other was terminated by a 50 Ω surface-mounted resistor on the substrate. The spectrum analyser (Agilent E4407B) had noise floors low enough to measure the phase noise of the VCO, corrected the measured spectrum automatically,

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and displayed the phase noise. The losses from cables, connectors and the FR-4 substrate were not calibrated out of the measurements. The VCO operated at a supply voltage of 1.8 V and provided a constant bias current of 27 mA for the core and output buffer amplifiers.

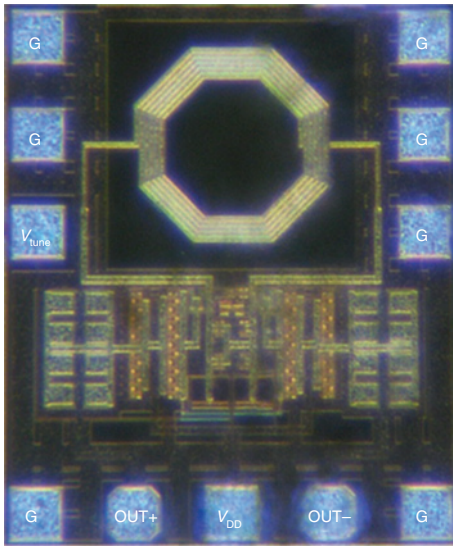

Fig. 3 *Photograph of fabricated VCO*

Fig. 4 shows the oscillating frequency and single-ended output power of the VCO against V_{tune}. The free-running frequency was tuned linearly from 806 to 1113 MHz with a tuning voltage range of 0.0–5.0 V. The tuning range was 307 MHz (34%) with a linear f–V relationship. The differential tuning sensitivity exhibited a low value of 62 MHz/V, which was almost constant over the entire frequency range. The output power varied from −7.5 to −4.3 dBm with increasing V_{tune}. The minimum phase noise was −100.4 dBc/Hz at a 100 kHz offset from a 904 MHz carrier frequency. This phase noise performance was maintained throughout the entire frequency range displaying values between −96 and −100.4 dBc/Hz.

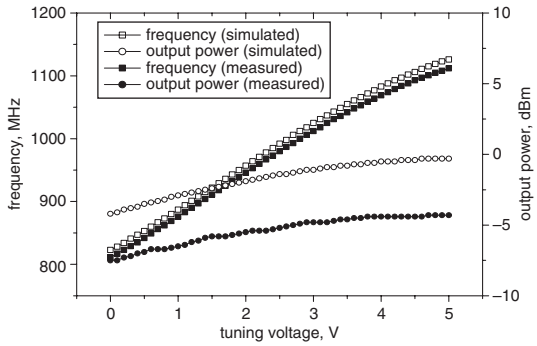

Fig. 4 *Oscillating frequency and single-ended output power against tuning voltage V_{tune}*

Conclusions: We propose a technique to improve the f–V linearity and to reduce the K_{VCO} of CMOS VCOs. The VCO designed using the proposed technique is linearly tunable from 806 to 1113 MHz with a low and constant $KVCO$ of 62 MHz/V and with −100.4 dBc/Hz phase noise at a 100 kHz offset frequency. Consequently, the proposed technique provides linear frequency tuning, low fluctuation of the output power and phase noise and can easily be used as a quality PLL design without any correction circuits for the nonlinear f–V characteristic of the VCOs.

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One or more of the Figures in this Letter are available in colour online.

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