Structured LNA design

Ernst H. Nordholt
Catena.
Elektronicaweg 40
2628 XG Delft, Netherlands

Abstract

A qualitative structured approach to the design of low-noise amplifiers is presented. Emphasis is on design methodology rather than on specific specification issues. The LNA configuration is synthesized based on the requirements of the source and the load. Some examples will support the design methodology.

1. Introduction.

LNA design is traditionally approached as a copy and modify action of proven concepts known from literature or recommended by colleague designers. Usually it requires a lot of iterations to realize the required specifications if at all achievable with the chosen concept. There is another way to approach the design. It is based on qualitative reasoning supported by a proper set of generic models, by error reduction techniques as well as by a good understanding of the influences of various design measures. This method leads to a quick decision with respect to the choice of a good amplifier configuration. For this purpose we first have to study the properties of the signal source in terms of its modeling and its signal spectrum. This will lead to criteria for the input port of the LNA. Criteria for the output port will have to be derived from the properties of the load which is usually a mixer or a set of mixers. Dependent on these properties we may have very different requirements for different source and load conditions, which means that we have to investigate various amplifier configurations. The transfer properties of the source quantity (voltage, current or power) to the load quantity in terms of noise, linearity and speed are related to these criteria.

M. Steyaert et al. (eds.), Analog Circuit Design, 47–76.

Due to the biasing elements there will usually be more input ports, which receive unwanted signals. The sensitivity of these ports should be made sufficiently low so as to have sufficiently low interfering signals at the output port. Especially in system on chip applications this plays an extremely important role. Techniques for desensitizing these parasitic input ports will be discussed separately.

To cover all aspects of LNA design in one article will be impossible. Therefore we will restrict ourselves to qualitative aspects and some examples without providing a full background. The interested reader is referred to [1] for this purpose

2. Properties of the signal source; LNA requirements.

We will assume that the LNA is used as the first block in a radio system and therefore it has to process the signals generated by an antenna. These signals normally cover a very wide spectrum. It contains many channels from which we wish to make a selection. As an example we consider the European FM broadcast band, which ranges from $87.5MHz$ to $108MHz$. The radio channels in this band are on a $100kHz$ raster. A nearby transmitter might generate a signal in the antenna of $2V$. For remote transmitters or with poor reception conditions we still wish to receive signals in the order of a few microvolts. So we need to cover a dynamic range of signals in the order of $120dB$. It may be clear that it is not possible to linearly handle such a large dynamic range in a fixed-gain amplifier operating at a supply voltage of for example $3V$. Moreover, outside the FM band we have a lot of other radio and TV signals that can be very strong and could easily overdrive the LNA if no proper measures were taken such as prefiltering and automatic gain control.

It is frequently assumed without further discussion that the impedance of the source for the LNA is 50Ω (or 75Ω). The antenna may have a fixed and real impedance in the frequency band of interest under ideal conditions. In the proximity of other objects, the impedance may become different and frequency dependent. Also the received signal levels depend on the

environment. Though it may be convenient from a measurement point of view to standardize on characteristic impedances, there is no fundamental reason why an antenna should be terminated for optimum power transfer. The required termination is much more determined by the way of connecting the antenna to the LNA input. Frequently we need a cable or a stripline when the antenna is not extremely close to the LNA input port. Moreover, we need filtering between the antenna and the input of the LNA. The filter will have to prevent the receiver from becoming sensitive to all kinds of unwanted channels due to nonlinearities in the front-end signal path, and - in the case of heterodyning - to image channels or channels related to local-oscillator harmonics. The cable will need a real termination in order to avoid power reflections and thereby (strong) fluctuations in the sensitivity. A filter, when implemented with lossless elements (LC), will need at least at one port a real impedance termination in order to bring the poles in their required positions. Sometimes real terminations at both ports are needed in order to apply practical inductor and capacitor values. Due to the losses in these components, the insertion loss of the filter will be sometimes sufficiently high to obtain the required filter characteristic without real terminations. The conclusion is that we do not always need or wish to have an optimum power transfer. Sometimes it is more convenient to have either a high or a low impedance termination.

At the output of the LNA, we also may have different requirements. The most common situation is that we have to drive one or more mixers that convert the input frequency band to another band (heterodyning), centered about the so-called IF frequency. Dependent on the type of mixers, we may need a voltage source character or a current-source character of the LNA output port. In some cases it may be necessary to have additional band-pass filtering, which again may require real-impedance terminations at their input or output port or at both ports. In the case where we have more than one mixer, the output signal of the LNA has to be distributed to all of them. This all means that only in certain cases, a definition of the power gain of an LNA can be meaningful. Frequently we will have to define the gain in terms of voltage or current gain or in terms of a transimpedance or a transconductance. On top of that, we may have special

requirements on the input or on the output impedance. From this perspective it is useful to define ideal amplifier types before we start designing an LNA.

3. Ideal amplifiers and basic implementations.

In the introduction it has been made plausible that different amplifier types may be needed as LNAs. We can characterize all of these by means of a transmission-parameter representation:

$$V_i = AV_o + BI_o,$$
$$I_i = CV_o + DI_o,$$

where we use associated directions for voltages and currents. The ideal amplifiers with only one transmission parameter different from zero are characterized as follows:

Voltage amplifier	$A_v = 1/A$	$Z_i = \infty$	$Z_o = 0$
Transconductance amplifier	$G = 1/B$	$Z_i = 0$	$Z_o = \infty$
Transimpedance amplifier	$Z = 1/C$	$Z_i = \infty$	$Z_o = 0$
Current amplifier	$A_i = 1/D$	$Z_i = 0$	$Z_o = \infty$

As can be seen from this table, the input and output impedances are either zero or infinity. As a matter of fact these amplifier types define the ideal controlled sources (transactors). They are perfectly linear, produce no noise and have an infinite available power gain. They sense either the source voltage or the current in an ideal way and deliver a voltage or a current to the load. Approximations of these transactors can be realized as single-loop negative-feedback configurations. The other useful amplifier types have an input impedance and/or an output impedance different from 0 or ∞.

Parameters ≠ 0	Z_i	Z_o
A and B	∞	B/A
A and C	A/C	0
A and D	AZ_l/D	DZ_s/A
B and C	B/CZ_l	B/CZ_s
B and D	B/D	∞
C and D	0	D/C

From this table it is not yet completely clear how we can realize them. For the first and last two configurations the starting point could be one of the transactors of the first table, where we use series or shunt impedances at their input or output ports in order to fix the input or output impedance. In cases where these impedances are intended as dissipative matching terminations for the source or the load, they will, however, seriously affect the noise performance (at the input) or the power dissipation (at the output). The only good way to realize these properties in an LNA is by using negative feedback, where we use two feedback loops instead of one. It is important that the feedback networks are chosen in such a way that they minimally affect the noise performance or the power consumption. We can distinguish various types of feedback. Setting up a ranking order in terms of increasing effects on noise, distortion and dissipation, we have:

1. *Non-energic feedback to be realized by using elements which are lossless and without memory (transformer, gyrator, short-circuit, open-circuit)*
2. *Lossless feedback using lossless components with memory (L,C).*
3. *Resistive feedback using resistors*
4. *Active feedback with one or more active devices in the feedback network*
5. *Indirect feedback using copies of input or output stages (example: current mirror)*

Non-energic feedback is not a very realistic concept except for realizations with short and open circuits. To classify negative feedback amplifiers, however, it is a good starting point. Figure 1 shows an example of a feedback configuration around a gain block

(ideally a nullor) with four feedback loops, fixing all four transmission parameters, from which all other configurations can be derived.

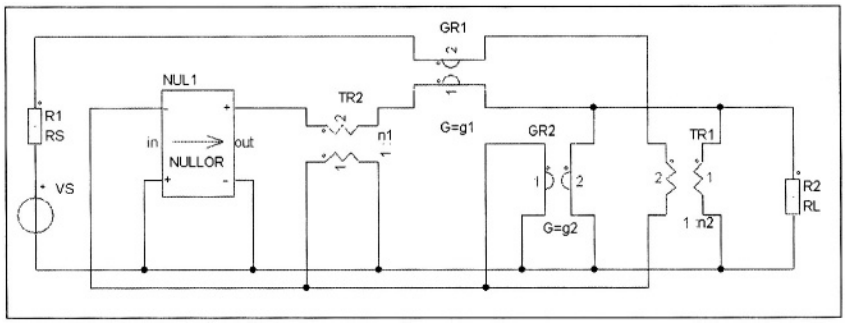

Fig. 1. Feedback configuration with 4 non-energic feedback loops

It can easily be proven that the equivalent input noise sources of the gain block (provided that all its transmission parameters have a value very close to zero) have very nearly the same values as the equivalent noise sources of the amplifier in the case of one or two feedback loops. This means that the feedback networks don't have any influence on the noise figure. Since there is no power dissipation in the feedback elements, any influence on the power dissipation is also absent. Single loop feedback configurations using short and open circuits in their feedback network are known as the voltage follower and the current follower with unity voltage and current gain, respectively. They are shown in figure 2.

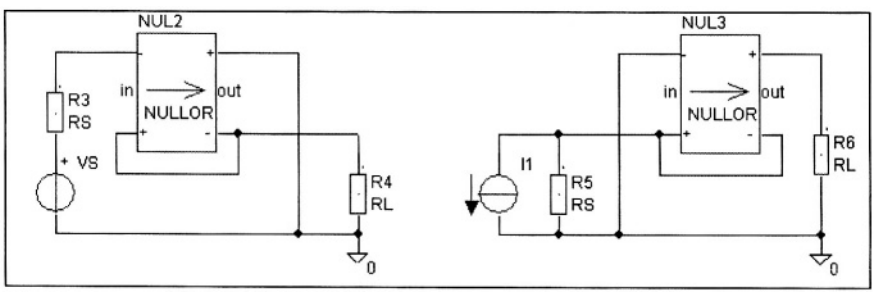

Fig. 2. Voltage follower and current follower

The use of transformers for a limited frequency range may be a possibility on silicon. However the insertion loss will normally be unacceptably high so that no advantage over resistive feedback

would be obtained.

Lossless feedback is a more realistic concept since it makes use of capacitors and/or inductors. Transconductances and transimpedances will become frequency dependent using these elements. In voltage and current amplifiers it is still possible to realize wide-band amplifiers since the transfer function will be determined by impedance ratios. This type of feedback has an influence on the noise figure and on the power dissipation although the elements do not generate noise themselves or dissipate power.

Resistive feedback is the most commonly used type of feedback in wide-band amplifiers. Due to their thermal noise generation and power dissipation the resistors will contribute to an increase of the noise figure and the power dissipation. These influences can, however, be much less than those of shunt or series resistors at the input or output port of the amplifier.

Active feedback configurations use active devices in their feedback network(s) which may introduce unacceptable non-linearity or noise.

Indirect feedback normally has a large influence both on the noise and the power dissipation and is therefore the least attractive feedback technique. It should be avoided in LNAs as much as possible.

For quantitative aspects of these types of feedback we refer to [1].

Before we will discuss the design of some basic LNA examples, we will briefly address some modeling considerations.

4. Device modeling considerations.

For the purpose of a systematic approach, we need different device models at different stages in the design. In order to find design strategies, we need generic device models that allow us to investigate the influence of error reduction techniques such as negative feedback, compensation, isolation and error feedforward.

Once we understand these influences, their benefits and their drawbacks, we can develop a suitable circuit topology and design and verify in more detail with specific device models with

increasing complexity. The proposed *generic* models are:

1. *A non-linear two-port model using generalized non-linear (voltage-controlled) i – v relations will be used for investigating the influence of error-reduction techniques on non-linear behavior:*

$$i_i = \hat{\imath}_i(v_i, v_o),$$
$$i_o = \hat{\imath}_o(v_i, v_o),$$

where we use associated directions for voltages and currents.

The fact that we have to supply DC power to the actual device in order to obtain power amplification, can be made explicit by defining an operating point characterized by: $V_{iQ}, V_{oQ}, I_{iQ}, I_{oQ}$.

For excursions from this operating point, to be marked by a tilde (~), a power amplification in these devices is possible, provided that we have chosen the correct operating conditions. We separate the excursions from the operating-point quantities and the equations can thus be written as:

$$I_{iQ} + \tilde{\imath}_i = \hat{\imath}_i(V_{iQ} + \tilde{v}_i, V_{oQ} + \tilde{v}_o),$$
$$I_{oQ} + \tilde{\imath}_o = \hat{\imath}_o(V_{iQ} + \tilde{v}_i, V_{oQ} + \tilde{v}_o),$$

Based on these equations, we can then build a new two-port, where the operating point is translated to the origin by adding the operating-point sources to the input and the output, respectively, as shown in figure 3.

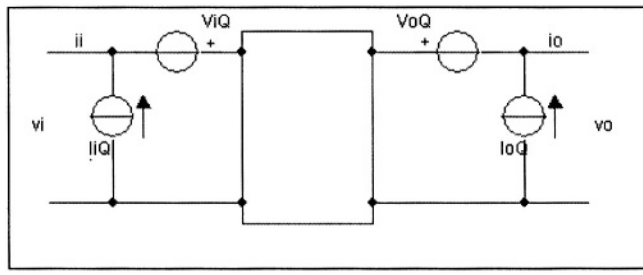

Fig. 3.*Non-linear two-port with operating point translated to the origin.*

The new two-port has equations can then be written as:

$$\tilde{\imath}_i = \hat{\imath}_{iQ}(\tilde{v}_i, \tilde{v}_o),$$
$$\tilde{\imath}_o = \hat{\imath}_{oQ}(\tilde{v}_i, \tilde{v}_o),$$

where $\hat{i}_{iQ}$ and $\hat{i}_{oQ}$ can formally be found from the equations of the original device.

The advantage of the generic modelling is that it fits to all three-terminal devices, whether it is a bipolar transistor, a field-effect device or even a vacuum tube. It is particularly useful for studying the influence of compensation techniques (e.g. balancing).

2. *As for the ideal amplifier types discussed in section* 3, *a linear two-port model using transmission parameters will be used for investigating the influence of error-reduction techniques on small-signal and noise behavior:*

$$V_i = AV_o + BI_o,$$
$$I_i = CV_o + DI_o,$$

where A, B, C, and D are in general complex quantities representing the transmission parameters. The reason why we use these is because we frequently wish to approximate the behavior of an ideal transactor in the sense that the behavior is as much as possible determined by well fixed and linear transmission parameters. One other reason is that they greatly simplify noise calculations [1].

The specific design models are as a matter of course based on the complete device models (such a Gummel Poon, BSIM, etc.). In RF processes, the models can be even more complicated than these, thereby resulting in subcircuits. These models are completely useless for initial design purposes. Therefore, we need additional simplified models. The following *device specific* models are proposed:

3. *Derive a simplified non-linear model, not dealing with memory effects, from the complete model. Together with a graphical representation of the device characteristics, this model can be used for discussing biasing techniques and evaluating behavioral aspects relating to operating point and low-frequency non-linearity.*

4. *From this simplified model, we derive a linearized (small-signal) model to which we add small-signal capacitances resulting in the hybrid π equivalent circuit for the bipolar transistor and in similar equivalent circuits for the other devices. This model allows us to study the small-signal dynamic behavior in*

terms of gain, immittances, poles and zeros, impulse response, etc.

5. *In order to obtain a noise model, we add (stationary) noise sources to the small-signal model. In general these noise sources will depend on the biasing conditions, so that this model allows us to optimize the noise performance for a certain source impedance.*

The small-signal models for the different device types have the same topology. The bipolar transistor has the most complicated model, called the hybrid π model and is shown in figure 4.

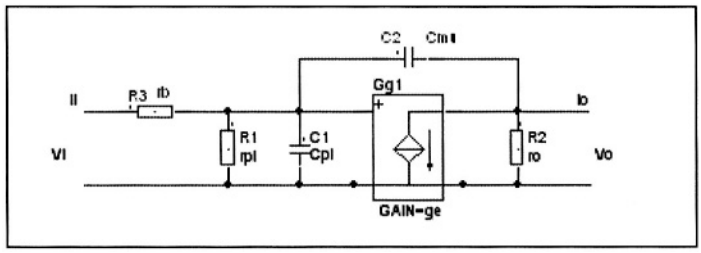

Fig. 4. Hybrid π model of the bipolar transistor.

In the FET model $r_\pi = \infty$. The noise models for these two types of devices are given in figures 5 and 6, respectively.

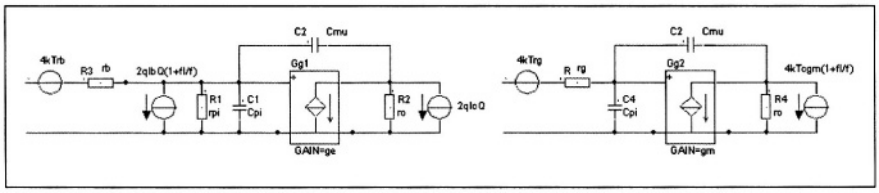

Fig. 5,6. Noise models for the bipolar transistor and the FET

Note that the 1/*f* noise in the bipolar transistor occurs in the input current noise source whereas in the FET it occurs in the output current source. The influence of these 1/*f* noise sources is therefore distinctly different for different source impedance conditions.

5. Single stage LNA examples.

5.1.Introduction.

Although the design methodology as advocated here is

illustrated by LNA topology examples with bipolar transistors, it is a general methodology that can equally well be applied to MOS transistors, junction transistors or even vacuum tubes. As a matter of course, the models of these other devices are different in terms of their static, dynamic and noise performance. It may be clear that we will have specific process technology requirements dependent on frequency and dynamic range. Moreover, some topologies are more suited to be used at lower supply voltages than others. It is not the purpose of this text to discuss all these aspects but rather illustrate the way of reasoning, the use of generic models and error-reduction techniques. In order to keep it simple we will even ignore the dynamic behavior in our examples.

We will discuss in this section some examples of single-stage amplifiers based on an idealized bipolar transistor biased in its normal operating region. It is characterized by its exponential relation between base-emitter voltage and collector current and a fixed relation between base current and collector current:

$$I_{BQ} = I_{CQ}/\beta,$$
$$I_{CQ} = I_S\left(e^{\frac{V_{BEQ}}{V_T}} - 1\right).$$

Although this is a highly simplified model for the device, it serves our purpose of showing trends in performance improvement due to different design measures.

Ignoring the influence of I_s with respect to I_{CQ}, the *generic* non-linear voltage-controlled model leads to the following equations for excursions from the operating point.

$$\tilde{\imath}_b = \tilde{\imath}_c/\beta,$$
$$\tilde{\imath}_c = I_{CQ}\left(e^{\frac{\tilde{v}_{be}}{V_T}} - 1\right).$$

Alternatively we can write these equations in a current-controlled form as:

$$\tilde{v}_{be} = V_T \ln(1 + \tfrac{\beta\tilde{\imath}_b}{I_{CQ}}), \text{ or}$$
$$\tilde{v}_{be} = V_T \ln(1 + \tfrac{\tilde{\imath}_c}{I_{CQ}}).$$

The small-signal model (without memory effects and the base resistance) is given in figure 7, where

$$r_\pi = \frac{d\tilde{v}_{be}}{d\tilde{\imath}_b} = \frac{\beta V_T}{I_{CQ}} \text{ and } g_e = \frac{d\tilde{\imath}_c}{d\tilde{v}_{be}} = \frac{I_{CQ}}{V_T}.$$

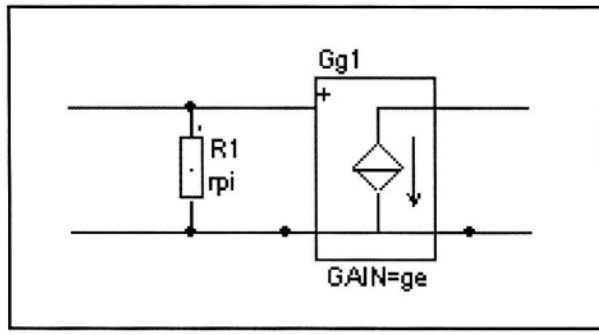

Fig. 7. Simplified small-signal model of the bipolar transistor.

In figure 8, we have added the shot-noise sources

$$S(i_{bn}) = 2qI_{BQ} \text{ and } S(i_{cn}) = 2qI_{CQ}.$$

With $g_e = \frac{I_{CQ}}{V_T} = \frac{qI_{CQ}}{kT}$, these can alternatively be written as equivalent thermal noise sources:

$$S(i_{bn}) = 4kTg_e/2\beta \text{ and } S(i_{cn}) = 4kTg_e/2.$$

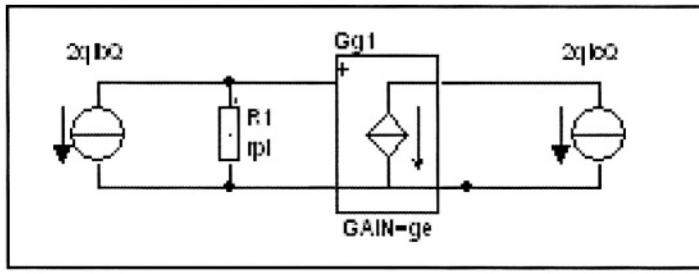

Fig. 8. Bipolar transistor model with noise sources.

Note that we have left out the base resistance r_b and its associated noise source $S(r_b) = 4kTr_b$, a simplification that is only allowed when $r_b < 1/2g_e$. In many cases, however r_b contributes significantly to the noise (as the gate resistance r_g does in a MOSFET).

5.2 CE stage.

As an example, we will now consider a single stage amplifier implemented as a common-emitter stage intended as an LNA for a 50Ω source. The load is modeled as a noise-free resistor. The noise contribution of the load can then be modelled by two equivalent noise sources representing the noise of the block that is driven by the amplifier. This amplifier is shown in figure 9, where we have added the four biasing sources to the transistor in order to translate the operating point to the origin.

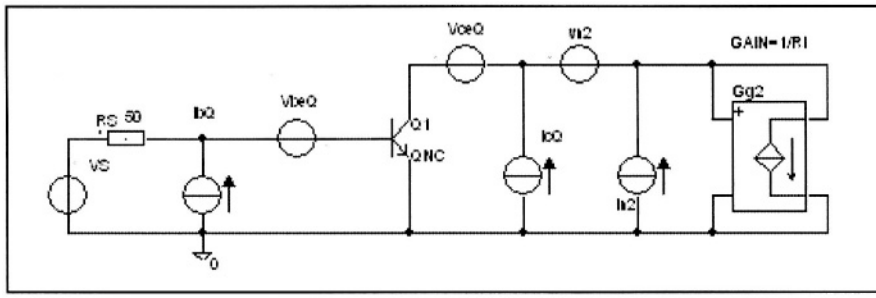

Fig. 9. Basic CE stage amplifier with second-stage noise sources v_{n2} and i_{n2}.

Although this is not a realistic way of biasing, it serves our purpose of highlighting the amplifier properties without any effect of the biasing components.

Due to the (over)simplified modeling of the transistor ($A = 0, C = 0$), only the noise-current source at the output will contribute to the total equivalent noise of the amplifier. This noise will be transformed to the input into two equivalent sources:

$$v_{oeq} = Bi_{n2},$$
$$i_{oeq} = Di_{n2},$$

where $B = 1/g_e$ and $D = 1/\beta$.

Note that we cannot define a noise figure for the block behind the amplifier in a situation like this since the amplifier has an infinite output impedance.

Assuming that we can ignore the contributions of this block with respect to the noise production of the transistor itself, we find (with a Norton-Thevenin transformation) for the total equivalent

input noise:

$$S(v_{ntot}) = 4kT(R_s + \frac{1}{2g_e} + \frac{g_e R_s^2}{2\beta}).$$

This noise can be minimized by making the two contributions of the transistor equal, which leads to

$$1/g_{eopt} = \frac{R_s^2}{\sqrt{\beta}}.$$

With $\beta = 100$ in the present example, the optimum value of g_e amounts to

$g_{eopt} = 200mA/V$. This requires a collector bias current of $5mA$. The noise figure is then given by

$F = 1 + 1/g_e R_s = 1.1$ and $NF = 0.41dB$.

The input impedance of the amplifier has a value of $R_i = B/D = \beta/g_e = 500\Omega$. This means that we don't have an input power match. If we need a 50Ω termination, we would need a bias current of $50mA$ or we would have to use a shunt resistance. The first option would lead to $NF = 1.76dB$, but is quite unrealistic in view of its current consumption. The second option would lead to a noise figure of at least $3dB$. A combination of noise optimization and power matching in one *CE* stage appears to be impossible without using other techniques. Before we consider these possibilities, we will briefly look at linearity issues.

First, we assume that the input impedance of the stage is much higher than the source impedance. The source voltage then appears entirely on the base-emitter junction. In this situation we can evaluate the compression and intercept points. Here, we consider the third-order intercept point (*IP*3) exclusively. For this purpose we apply two voltage sources at two different frequencies at the input, each with an *rms* value of for example $1mV$ ($60dB\mu V$).

Note that we present the IP3 figures in relation to the open source voltage, which is not conventional!

The intermodulation component at the output is then $68dB$ below the required signal components and the third-order intercept point is found at about $50mV$ ($94dB\mu V$). As the bias current is made larger, the linearity will improve, however not very significantly. For example at $5mA$, where the noise optimum occurs, we still have about 90% of the signal on the base-emitter junction and the *IP*3 will increase by about $2dB$. At $50mA$, where

we obtain a 50Ω termination, the *IP*3 will further increase to about $200mV\ (106dB\mu V)$.

5.3 CE stage with matching network.

The combination of noise optimization and power matching is not possible for a *CE* stage. When we use a matching network at the input, we can, however, manipulate the dynamic range. A wide-band match would require a transformer. A narrow-band match can be obtained by means of an *LC* network. In figure 10 we show two examples, where a 50Ω termination of the source is supposed to be realized.

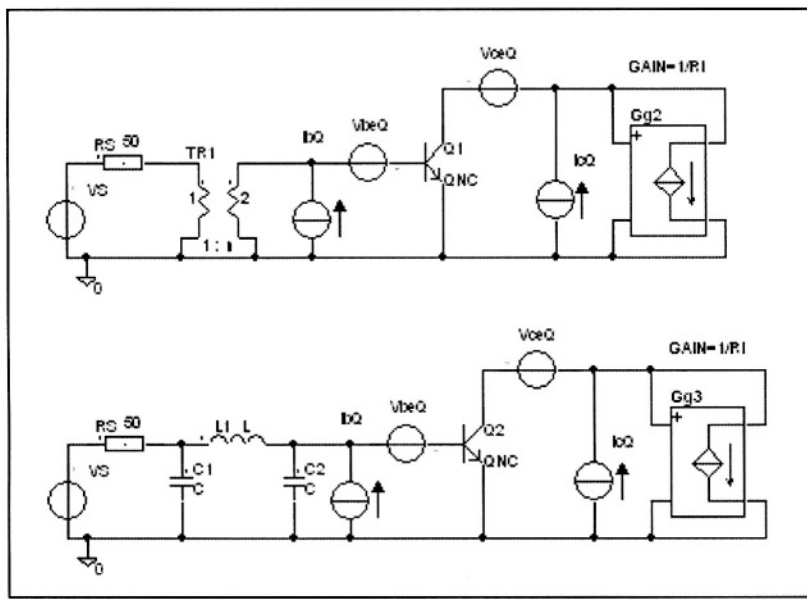

Fig. 10. CE stages with matching networks

Assuming that we have no insertion loss, the source impedance of 50Ω is ideally transformed by a factor n^2, where n is the turns ratio of the transformer. Let n^2 be 10, so that we need to realize an input impedance of 500Ω in the *CE* stage. This will require a bias current of about $5mA$ (as opposed to $50mA$ in the previous section). We will find that in this case $NF = 1.76dB$ (as in the $50mA$ case without matching network). Because the base-emitter voltage is about $\sqrt{10}$ times larger than in the $50mA$ case, the *IP*3 will be about $10dB$ lower $(96dB\mu V)$.

A noise figure of $1.76dB$ can also be obtained when we take $n^2 = 1/10$. In that case we need a bias current of $500mA$ to obtain a 50Ω termination. Since the base-emitter voltage is now much lower, the $IP3$ will be higher ($116dB\mu V$).

5.4 Single stage with non-energic feedback.

From section 5.2 it is clear that we create some more degrees of freedom by using a matching network in combination with a *CE* stage. In this section we will show that the application of negative feedback can do the same, however at a much lower current consumption. For this purpose we consider a single stage configuration where the current gain is made close to unity by means of non-energic shunt feedback at the input in combination with series feedback at the output. This results in a common-base (*CB*) stage. All transmission parameters remain virtually the same as in the *CE* stage, except the parameter *D* which obtains a value close to unity. The non-energic feedback will lead to virtually the same values for the equivalent input noise sources as in the *CE* stage.

The input impedance (with *A* and *C* still equal to zero) is given by: $Z_i = B/D \cong 1/g_e$.

If we wish to terminate the source in a 50Ω impedance, we have to bias the stage at about $0.5mA$. In this operating point, the noise voltage source is dominant and the noise figure will given by

$F \cong 1 + 1/2g_eR_s = 1.5$ ($NF \cong 1.76dB$).

The base-emitter voltage now equals half the open source voltage and therefore we can expect a better linearity than in the *CE* stage in the same operating point. The $IP3$ now has a value of $106dB\mu V$, the same as was obtained for the *CE* stage at a bias current of $50mA$!

Also in this case, we cannot combine a noise optimization with a power match. The optimum noise figure would be obtained at a collector bias current of $5mA$, same as in the *CE* stage. The input impedance will then be about 5Ω. When the antenna is very close to the LNA input, this could be a proper termination. The source current is sensed in this way and it allows band-pass filtering with a series *LC* tank as shown in figure 11.

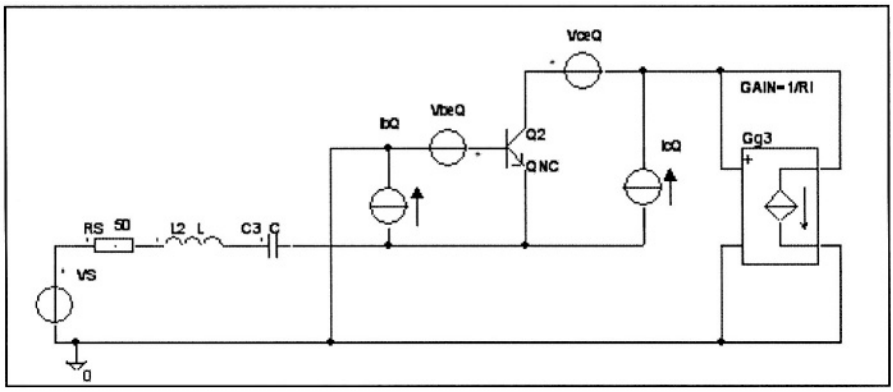

Fig. 11. *Band-pass filtering at the input of a basic CB-stage amplifier*

In this case we find that the exponential $i - v$ relation of the base-emitter junction has much less influence on the non-linearity. We find: $NF = 0.45dB$ and $IP3 = 123dB\mu V$. This leaves us with the question how to realize such a high dynamic range while simultaneously meeting the power match and the noise optimum. For this purpose we need dual-loop negative feedback.

5.5 Non-energic dual-loop feedback.

The *CB* stage uses a single negative feedback loop. It uses series feedback at its output port, giving it a current source character at the output and shunt feedback at the input port resulting in a low input impedance, thereby making it suitable for current sensing. In the operating point that optimizes the noise performance for a 50Ω source impedance, the input impedance is much too low for obtaining a power match. By applying an additional feedback loop that realizes series feedback at the input, we can increase the input impedance to the required value of 50Ω. Preferably, this second feedback loop would also use a non-energic element. Looking now at the table of useful amplifier types, this element should either increase the transmission parameter B or A. In the first case we would have $Z_i = B/D$ and in the second case $Z_i = AZ_l/D$. Increase of the parameter B requires output series feedback (current sensing) together with a conversion into a voltage to be applied in series with the input. It would

therefore need a gyrator as a non-energic negative feedback element and this cannot be considered as a realistic option. The second case leads to an influence of the load impedance on the input impedance. For Z_i to be equal to 50Ω, we need AZ_l to be equal to 50Ω as well. In order to linearize the $v - i$ relation of the input port, we would also require the load to have a linear $v - i$ relation (assuming that the feedback element is linear). If Z_l is the input impedance of a block behind the LNA this is not very likely. Therefore, we have no other good option than to use a linear resistor as a load for the stage and make sure that this load is not significantly influenced by the load of the block behind the LNA. For this purpose we could use a voltage follower when the load has to be driven by a voltage or a transconductance stage delivering a current. We will present one of these options as an example.

The first step is to bias a *CB* stage for optimum noise performance ($5mA$ for a 50Ω source) and provide this stage with a linear resistive load. Note that this load resistance affects the noise figure as if it were in parallel with the input since $D \cong 1$. Therefore, it should be much larger than 50Ω, let's say $1k\Omega$. The parameter A should then have a value of $A = 0.05$. For this purpose we can use a transformer as a non-energic element with a turns ratio of 20. The circuit could look like figure 12.

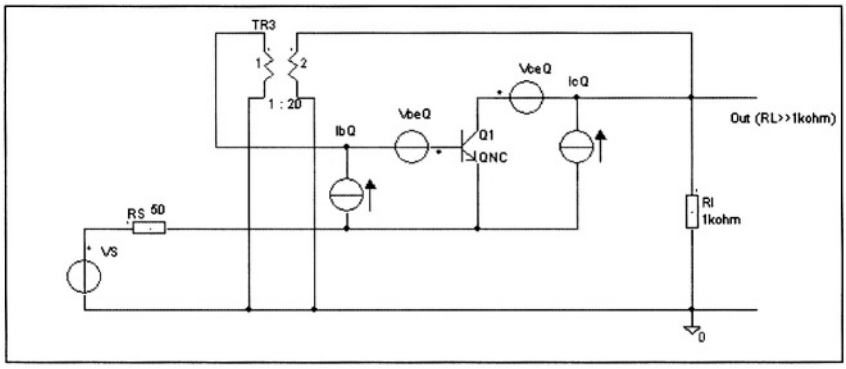

Fig. 12. CB stage with two non-energic feedback loops.

Due to the load resistor, the noise figure is somewhat higher than the absolute minimum at $NF \cong 0.67dB$. The $IP3$ increases to $131dB\mu V$. Much better figures cannot be achieved in a single idealized stage. With a real transformer, the primary inductance

should be large enough not to form an additional load for the *CB* stage at the frequencies of interest. This is usually an unrealistic requirement.

5.6 Single stage lossless and resistive feedback.

An alternative for the transformer is a lossless or a resistive 20 : 1 voltage divider. Lossless feedback would affect the load impedance so that the wide-band character is lost, whereas resistive feedback leads to a resistor in the base lead of 50Ω. This would result in a noise figure of more than $3dB$. Using an additional voltage (emitter) follower solves this problem in the way shown in figure 13.

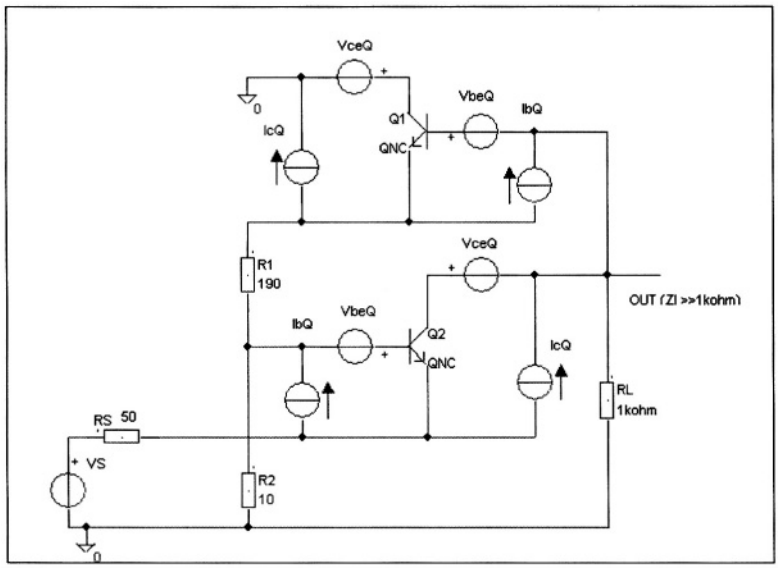

Fig. 13. Dual loop resistive feedback around a CB stage

Due to noise of this stage and its resistive load, noise and linearity performance will degrade with respect to non-energic feedback. We find: $NF = 1.6dB$ and $IP3 = 123dB\mu V$.

We can alternatively base the design on the fourth type of amplifier in the table with dual-loop configurations. The input

impedance is then given by $Z_i = B/CZ_l$. Obviously, we have to fix both the transconductance and the transimpedance of the stage and we need a resistive linear load Z_l at the output port. We can base such a design on a *CE* stage, where the transconductance is chosen for optimum noise performance: $g_e = 200mA/V$ for a 50Ω source impedance. Then $B = 5\Omega$ and consequently $CZ_l = 0.1$. As an example we take $C = 5.10^{-4}A/V$ and $Z_l = 200\Omega$. The transmission parameter C is determined by shunt feedback both at the input and at the output, resulting in the circuit of figure 14.

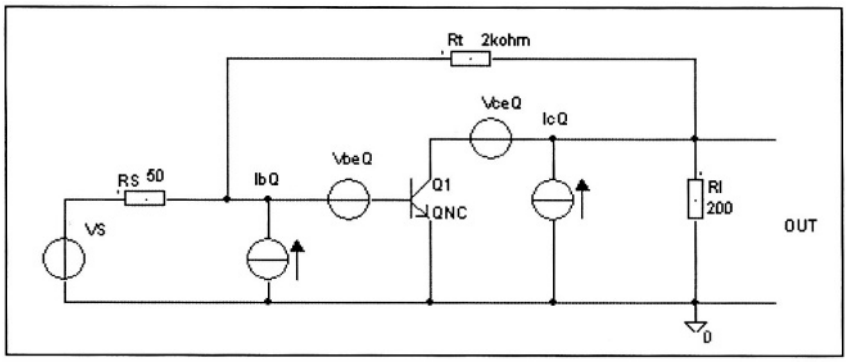

Fig. 14 Amplifier stage with fixed transconductance (g_e) and transimpedance (R_t).

For this circuit we achieve a power match to 50Ω at $NF = 0.6dB$ and $IP3 = 107dB\mu V$. Also here a voltage follower or a transconductance amplifier would be needed when the load has to be driven by a voltage or a current, respectively. If we do so, we might as well include the second stage in the transimpedance feedback loop as shown in figure 15. This doesn't affect the previous figures significantly but we can now load the output stage with much less effect on the input impedance.

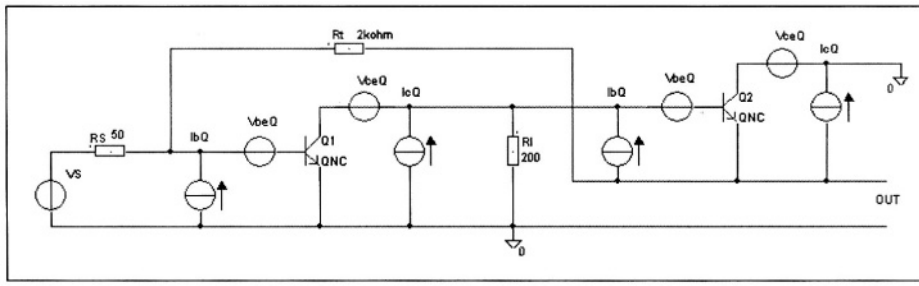

Fig. 15. Two stage amplifier with 50Ω input impedance and low output impedance

5.7 Conclusions on single stage configurations.

We have demonstrated in this section how we can manipulate the dynamic range of single-stage low-noise amplifiers. In order to avoid the use of transformers , the *CB* stage, being a non-energic feedback configuration, is a good starting point for obtaining a high-dynamic range LNA. Especially in cases where we wish to sense the source current, the *CB* stage will be a good option as demonstrated in section 5.4. A power match can be obtained at a low bias current, which results in a relatively high dynamic range. When the range has to be extended, we need an additional stage as argued in section 5.5. We didn't discuss the realization of a high input impedance which would be needed for sensing a source voltage. It goes without saying that the emitter follower and the transconductance stage (sometimes labeled as emitter degeneration) are the best single-stage options in that situation.

As was mentioned in the introduction, LNAs may have more ports where interfering signals from other sources than the desired one can enter into the amplifier. In discrete designs, we can normally take proper measures to avoid this. For example, we can have a good ground plane as well as proper decoupling of the supply voltage. In an integrated circuit, the bondwires make the internal ground and supply connections to relatively high

impedance nodes at high frequencies. Common supply and ground rails can therefore act as serious sources of interference. Moreover, coupling between bondwires and package pins may introduce other sources. Finally, substrate coupling will be an important issue especially in systems where digital processing is done on the same chip. The design strategy in such cases tries to desensitize all parasitic input ports of sensitive parts in the system by using balancing and isolation techniques. Simultaneously it has to lower the production of interfering signals by using similar techniques (for example current-mode logic in extreme cases). In the next section we will discuss a design approach.

6. Balanced configurations.

6.1. Introduction.

Besides the technique of negative feedback some other techniques are required especially to prevent interfering signals from entering into the LNA through unintended input ports. The most powerful technique uses a combination of balancing and isolation. The result of this technique for single devices is the well-known differential pair. Under ideal drive and load conditions, a differential source signal and a differential load, we obtain favorable properties with respect to the sensitivity to interfering signals. Frequently it is difficult to meet these conditions since the source signal is normally not available in differential mode. The load is normally on chip and can therefore be made differential. In this section we will briefly present a general approach to the synthesis of balanced configurations.

6.2 Odd function synthesis.

A differential pair has odd $v - i$ characteristics as opposed to a single stage where both even and odd terms describe the Taylor expansion of these characteristics. In a structured design approach it is useful to develop a synthesis technique for odd functions in general and investigate the behavioral modifications that it brings about. A starting point for this technique is the use of generic

non-linear two-port equations as introduced in section 4. We can write these generic equations in six different forms (like the equations of linear two-ports). To illustrate the approach, we will only use voltage and current controlled representations of the biased two-ports.

Voltage controlled representation:

$$\tilde{\imath}_i = \hat{\imath}_{iQ}(\tilde{v}_i, \tilde{v}_o),$$
$$\tilde{\imath}_o = \hat{\imath}_{oQ}(\tilde{v}_i, \tilde{v}_o).$$

Current controlled representation:

$$\tilde{v}_i = \hat{v}_{iQ}(\tilde{\imath}_i, \tilde{\imath}_o),$$
$$\tilde{v}_o = \hat{v}_{oQ}(\tilde{\imath}_i, \tilde{\imath}_o).$$

Taking the voltage-controlled representation as an example and reversing the orientation of the non-linearities as shown in figure 16, the equations change into:

$$\tilde{\imath}'_i = -\hat{\imath}_{iQ}(-\tilde{v}_i, -\tilde{v}_o),$$
$$\tilde{\imath}'_o = -\hat{\imath}_{oQ}(-\tilde{v}_i, -\tilde{v}_o).$$

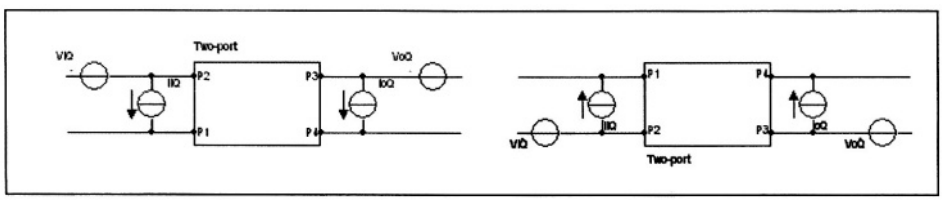

Fig. 16. Two-ports with normal and reversed orientation, respectively

These equations do not only represent the reversed two-port but also the two-port where complementary devices replace the original devices. In other words when the original two-port contains *NPN* devices, the other contains *PNP* devices with the same values of the model parameters. Moreover, all two-terminal devices in that two-port are reversely connected.

A new two-port, described by a set of odd functions is obtained when we add the input currents as well as the output currents of the original two-port and the reversed or complementary two-port as shown in figure 17.

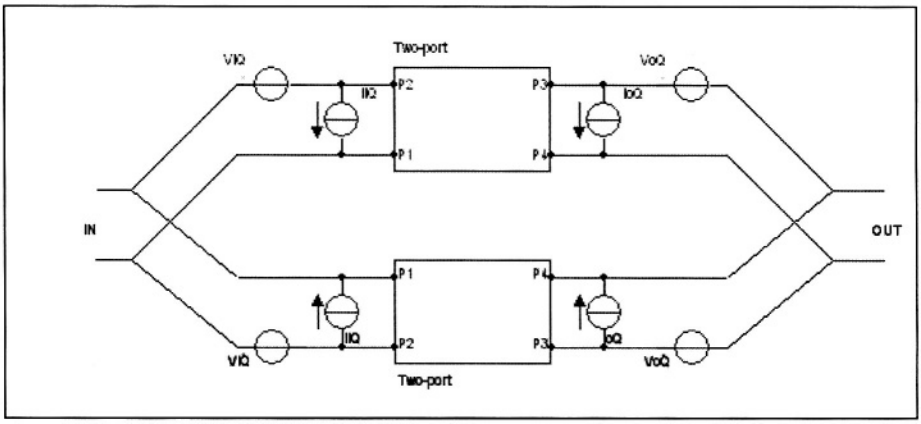

Fig. 17 Anti-parallel connected biased two-ports

Provided that we do not violate the two-port constraints of the individual two-ports, we can write the equations describing the combination as

$$\tilde{\imath}_{ii} = \tilde{\imath}_i + \tilde{\imath}'_i = \hat{\imath}_{iQ}(\tilde{v}_i, \tilde{v}_o) - \hat{\imath}_{iQ}(-\tilde{v}_i, -\tilde{v}_o),$$
$$\tilde{\imath}_{oo} = \tilde{\imath}_o + \tilde{\imath}'_o = \hat{\imath}_{oQ}(\tilde{v}_i, \tilde{v}_o) - \hat{\imath}_{oQ}(-\tilde{v}_i, -\tilde{v}_o).$$

We label this combination as an anti-parallel connection of two identical two-ports or as a parallel connection of two complementary two-ports. In the case where the two-port contains a three-terminal device like a bipolar transistor, the two-port constraints will be violated in an anti parallel connection. The result is still an odd function but the two-port will behave as the anti-parallel connection of two diodes. The equations will not be valid for this configuration. In the parallel connection of two complementary three-terminal devices, however, the equations are valid. As an illustration, consider the configuration of figure 18, where we have two biased complementary transistors in parallel.

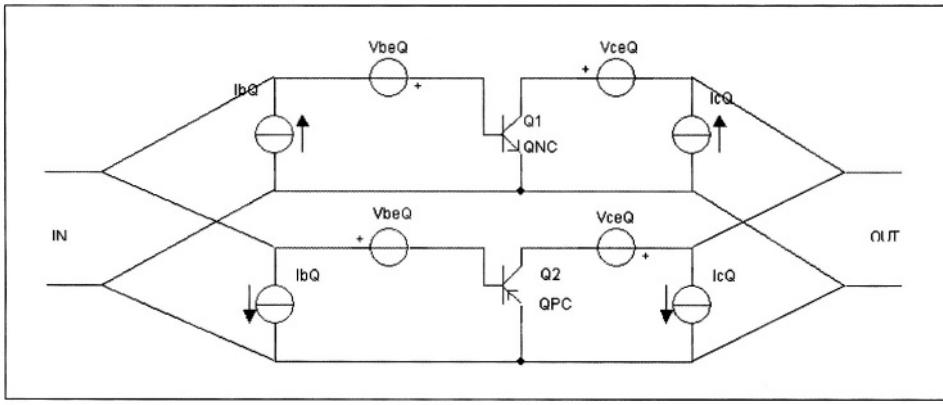

Fig. 18. *Anti-parallel connected complementary devices.*

It is immediately clear that the biasing current sources can be omitted since they cancel in pairs. Using the simplified device equations for the bipolar transistor of section 5, we find

$$\tilde{\imath}_{in} = I_{CQ}\left(e^{\frac{\tilde{v}_{be1}}{V_T}} - 1\right)/\beta - I_{CQ}\left(e^{\frac{-\tilde{v}_{be2}}{V_T}} - 1\right)/\beta = 2I_{CQ}\sinh\left(\frac{v_i}{V_T}\right)/\beta,$$

$$\tilde{\imath}_{out} = I_{CQ}\left(e^{\frac{\tilde{v}_{be1}}{V_T}} - 1\right) - I_{CQ}\left(e^{\frac{-\tilde{v}_{be2}}{V_T}} - 1\right) = 2I_{CQ}\sinh\left(\frac{v_i}{V_T}\right).$$

Note that these characteristics show no compression. They are expanding up to the level where the signal is limited by the supply voltage (or current). This illustrates that the frequently assumed relation between the $1dB$ compression point and $IP3$ does not always exist. Due to the odd characteristics, we find ideally no even-order distortion or intermodulation products.

It is interesting to see what happens to the transmission parameters and the equivalent noise sources of such a stage. Without proof (easy to verify) we will find that the transmission parameter B is halved (twice the transconductance of a single device) and that the transimpedance ($1/C$) is halved. For the noise sources, we find that the spectrum of the equivalent noise voltage source at the input has half the value of each single two-port, whereas the spectrum of the equivalent input current source is doubled. This means for example that we can obtain the same noise figure as in a single two-port at half the bias current.

This example has a limited practical value since normally we

have no good *PNP* transistors in a process. For *MOS* devices it may be more useful. Furthermore, since the configuration will be biased by voltage sources, there is normally not a good isolation from the supply and ground rails. We can much better isolate by using anti-series connections both at the input and at the output port. These follow from the current controlled representation.

To synthesize these, we take both the original two-port and the reversed (or complementary) two-port and connect them as shown in figure 19.

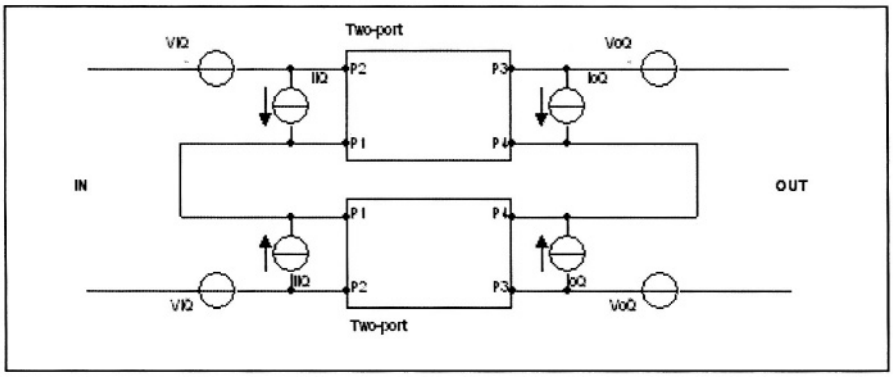

Fig. 19. Identical two-ports connected in anti-series.

Obviously, we can now omit the bias voltage sources, since these cancel in pairs. This leads in practice to much better isolation possibilities. The resulting equations now become:

$$\tilde{v}_{in} = \tilde{v}_i + \tilde{v}_i' = \hat{v}_{iQ}(\tilde{\imath}_i, \tilde{\imath}_o) - \hat{v}_{iQ}(-\tilde{\imath}_i, -\tilde{\imath}_o),$$
$$\tilde{v}_{out} = \tilde{v}_o + \tilde{v}_o' = \hat{v}_{oQ}(\tilde{\imath}_i, \tilde{\imath}_o) - \hat{v}_{oQ}(-\tilde{\imath}_i, -\tilde{\imath}_o).$$

For the bipolar transistor with the simple model this leads to:

$$\tilde{v}_{in} = V_T \ln\left(1 + \frac{\tilde{\imath}_{c1}}{I_{CQ}}\right) - V_T \ln\left(1 - \frac{\tilde{\imath}_{c2}}{I_{CQ}}\right) = 2V_T . \tanh^{-1}\left(\frac{\tilde{\imath}_{out}}{I_{CQ}}\right).$$

When converted to a voltage controlled representation, we find:

$$i_{out} = I_{CQ} \tanh\left(\frac{\tilde{v}_i}{2V_T}\right),$$

and with $I_{CQ} = \beta I_{BQ}$:

$$i_{in} = I_{BQ} \tanh\left(\frac{\tilde{v}_i}{2V_T}\right).$$

The characteristics of the anti-series connection of two bipolar transistors are obviously compressing. Again, we will have no

even-order distortion and intermodulation products.

For the transmission parameters of general anti-series connected two-ports, we now find that B has been doubled, whereas C will be halved. The input voltage noise spectrum doubles and the current noise spectrum is halved. The anti-series connection of two single devices obviously yields a differential pair.

6.3 Balanced LNAs.

In order to fully profit from the properties of a anti-series balanced configuration, we need to drive it from a balanced source and make sure that also the load is balanced. This normally requires that we use a balun (**bal**anced to **un**balanced network) at the input of the amplifier. Ideally this would be a transformer with a floating output port. However, from an application point of view this is usually not highly appreciated. Since transformers on the chip are not very realistic, neither are on-chip inductances because of their low Q and consequently high insertion loss, we have to find a solution outside the chip. This requires of course two pins. However, also in an unbalanced case it will be wise to spend two pins for the input of the LNA. One of these can then be connected to the external ground plane so that interfering signals have less chance of entering into the LNA. In this section we present only one configuration of a balanced LNA, which is based on the example in figure 13.

Since the noise voltage source of an anti-series connection is $3dB$ larger than in a single stage and the noise current source is $3dB$ smaller, the noise optimum for a given source impedance occurs at four times the total current consumption. For a 50Ω source this would lead to a current of $10mA$ per transistor. In order to achieve a lower current consumption, the use of a balun that converts the 50Ω impedance in for example 200Ω is recommended. The biasing current for minimum noise can then be reduced to a total of $5mA$. The noise figure can then again be as low as $0.45dB$, provided that we use no feedback or non-energic feedback. In the first case, we have an anti-series connection of two CE stages (a conventional differential pair). The following table gives NF and $IP3$ values for different operating currents.

$2I_{CQ}$	NF	$IP3$
$0.5mA$	$1.78dB$	$97dB\mu V$
$5mA$	$0.45dB$	$99dB\mu V$
$50mA$	$1.78dB$	$106dB\mu V$

At $50mA$ total bias current we obtain a power match at the input. The NF and $IP3$ values are the same as for a single stage as could be expected.

Next we look at the anti-series connection of two CB stages. Now, a power match is obtained at a total current of $0.5mA$, whereas the optimum noise figure is again found at $5mA$. The results are given below:

$2I_{CQ}$	NF	$IP3$
$0.5mA$	$1.86dB$	$106dB\mu V$
$5mA$	$0.45dB$	$128dB\mu V$

We assume now that we wish to have a power match in combination with a very low noise figure and use the same technique with an additional emitter follower as before. Figure 20 shows this configuration where $NF = 1.45dB$ and $IP3 \cong 118dB\mu V$ with a current of $2.5mA$ per emitter follower. A larger current in the follower will yield a higher noise figure as well as a higher $IP3$. At $5mA$, we find $NF = 1.62dB$ and $IP3 = 127dB\mu V$.

Assuming that the supply voltage is sufficiently high, this topology is capable of directly driving a double balanced mixer when using the collector currents of $Q18$ and $Q20$. Furthermore, the topology is also suitable for driving two of such mixers by doubling the output stages. The noise currents at the outputs, being mainly determined by the input stage, are almost fully correlated so that the noise in the image channel can be optimally rejected. Since we have a power match, it makes sense to express the $IP3$ in terms of dBm and find $IP3 = +8dBm$. *Note that this figure is related to the power entering into the amplifier and not to the open source voltage as before.*

In such an amplifier with real transistors, we can expect the noise figure to be about $1dB$ higher, mainly because of the non-zero base resistors. At frequencies below f_T/β the $IP3$ will be

close to +8*dBm* at higher frequencies it drops because of decreasing loop gain. An LNA configuration like this would be capable of meeting the very high dynamic-range requirements in a high-end FM receiver.

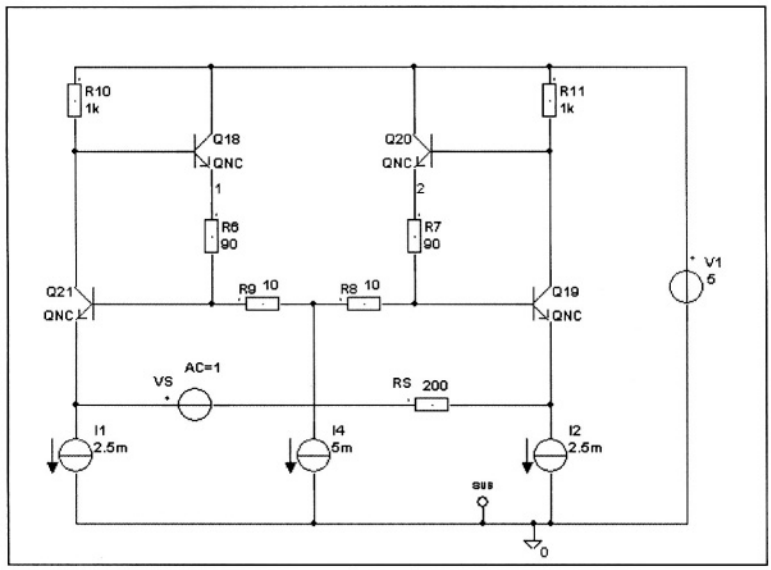

Fig. 20. Balanced two stage amplifier with dual-loop feedback

In most receivers for mobile communication, the dynamic range requirements are much lower, even so that in some applications no negative feedback has to be applied. If so required, an impedance match can then be obtained by virtue of the base resistance and the input capacitance, resulting however in a noise figure larger than 3dB. The application of inductive series feedback is another popular way to fix the input impedance. Its use is limited to narrow-band applications and requires a fair amount of silicon area. The dynamic range will significantly benefit from this type of feedback.

7. Conclusions.

This text has briefly dealt with a structured design approach for low-noise amplifiers. Although we could not provide a full background and justification for the way of reasoning, we believe that the examples sufficiently illustrate how this approach can be

used. In order not to complicate things too much, we deliberately ignored the effects of reactive elements and bulk resistances in the devices. Moreover, we didn't discuss the effects of biasing elements. It goes without saying, that these effects need careful attention in a real design. However, their presence doesn't affect the way of reasoning as far as the choice for an LNA concept is concerned. Presently, LNAs are designed in silicon or silicon-germanium technology for frequencies ranging from 100kHz up to several GHz. It depends highly on the system specifications which technology is most suited to the integration of these circuits. It is save to say that bipolar silicon and silicon-germanium are the preferred technologies for high performance LNAs. The topologies discussed in this text are useful up to at least one tenth of the transit frequency. For other parts of the system, such as active IF filters, CMOS may be a very welcome addition. The use of RFCMOS processes is still limited to lower performance requirements, not in the first place because the noise and speed properties would be insufficient, but mainly due to inadequate modeling and characterization.

Reference.

[1] "Design of High-Performance Negative Feedback Amplifiers", E.H. Nordholt, Delft University Press, Delft, 2000, ISBN 90-407-1247-6.