Admittance Matrix Models for the Nullor Using Limit Variables and Their Application to Circuit Design

David G. Haigh, *Fellow, IEEE*, and Paul M. Radmore

***Abstract*—A framework for symbolic analysis and synthesis of linear active circuits has previously been proposed which is based on the use of admittance matrices and infinity-variables. The notation has the important advantage that it can describe both ideal circuit elements, for which an infinite limit is implied, and nonideal circuit elements for which matrix elements are considered finite. The nullor is a very important circuit element because it can represent the ideal operational amplifier and the ideal transistor. For the nonideal case, the use of finite matrix elements implies that the operational amplifier and transistor are both modelled as a voltage-controlled current source, which is fine if the transistor is a field effect transistor or if the operational amplifier is of the transconductance type, but not otherwise. The purpose of this paper is to apply the ∞-variable framework in order to derive alternative models for the nullor that can be used to model voltage, current and transresistance operational amplifiers and bipolar junction transistors. We also show that the ∞-variable description of an ideal transistor can include a factor to represent transistor geometry.**

***Index Terms*—Active circuits, admittance matrix, circuit modelling, nullor, operational amplifier, transistor.**

I. Introduction

A SYMBOLIC framework for working with linear active circuits using the admittance matrix has been presented in [1]. The framework is based on the concept of matrix port-equivalence and the description of some circuit elements using infinity-variables (∞-variables). The elements so described are those that do not (in the conventional sense) possess an admittance matrix description and include the nullor, which can represent the ideal operational amplifier (op-amp) and transistor, the dependent sources and the impedance converter [2]. A theorem for matrices containing ∞-variables dictates how matrix elements may be scaled and moved within the admittance matrix while maintaining port equivalence, thus providing a basis for symbolic circuit analysis and the synthesis of circuits from symbolic transfer functions [1]. An important feature of the ∞-variable method is that the same notation can describe nonideal elements as well as ideal ones; nonideal elements are represented by replacing ∞-variables in the admittance matrix with finite values [1]. As a consequence, the method provides a systematic basis for circuit and element modelling. In [1], for example, three circuit models are derived for the current-controlled voltage source that are distinct in the nonideal case although they have identical behavior in the ideal case (i.e., at the limit). Since the nullor element has the key role of representing ideal transistors and op-amps (and other elements [2]), deriving models for it using the ∞-variable approach is an attractive possibility and that is the aim of the present paper.

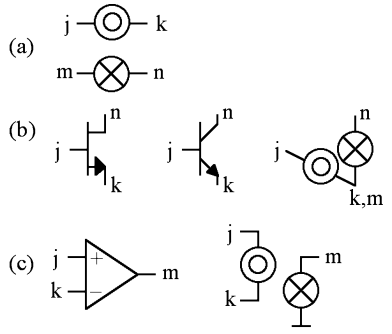


Fig. 1. (a) Nullor element; nullator symbol (top) and norator symbol. (b) Transistor-nullor equivalence. (c) Op-amp-nullor equivalence.

The nullor consists of a pair of elements called the nullator and norator, whose symbols are shown in Fig. 1(a), [2]–[7]. For the nullator, voltage and current are both zero; for the norator, they are both unconstrained. The nullor provides a small-signal circuit representation for the ideal transistor and the ideal op-amp, as shown in Figs. 1(b) and (c). The admittance matrix description for a nullor, with nullator connected between nodes j and k and norator between nodes m and n, as in Fig. 1(a), has the form [1]

$$\begin{array}{c} \\ m \\ n \end{array} \begin{array}{c} \begin{array}{cc} j & k \end{array} \\ \begin{bmatrix} \infty_i & -\infty_i \\ -\infty_i & \infty_i \end{bmatrix} \end{array}. \tag{1}$$

Subscript i refers to a particular nullor, e.g., nullor i, and the ∞-variables themselves, ∞_i, imply a limit to infinity in the corresponding elements of the admittance matrix. This limit is meaningful when viewed as a limit of the admittance matrix defining equation $\mathbf{I} = \mathbf{YV}$ [1]. Hence, a limit on the matrix elements actually applies to the admittance matrix equation. The ∞-variables are fully compatible with the usual operations of algebra, including Gaussian elimination and pivotal expansion [1]. Higher level circuit functions that traditionally do not possess admittance matrices, including the dependent sources of the voltage-controlled voltage, current-controlled voltage and current-controlled current types and the impedance converter [2], can also be described by admittance matrices containing ∞-variables [1]. Hence, ∞-variables, in addition to describing the elements of a circuit, can describe also the function that the

Manuscript received April 21, 2005; revised November 30, 2005. This paper was recommended by Associate Editor P. K. Rajan.

D. G. Haigh is with the Department of Electrical and Electronic Engineering, Imperial College, London, SW7 2BT, U.K. (e-mail: dhaigh@ee.ic.ac.uk).

P. M. Radmore is with the Department of Electronic and Electrical Engineering, University College, London, WC1E 7JE, U.K. (e-mail: pradmore@ee.ucl.ac.uk).

Digital Object Identifier 10.1109/TCSI.2006.882809

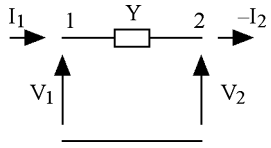


Fig. 2. Series-connected admittance Y.

circuit implements and the analysis and synthesis operations that link them [1], [8], [9].

In the case where a transistor or op-amp in a circuit is nonideal, circuit behavior can be assessed by replacing each ∞-variable ∞_i representing the ideal element in the admittance matrix in (1) by a finite parameter G_{mi}

$$\begin{matrix} & j & k \\ m \\ n \end{matrix} \begin{bmatrix} G_{mi} & -G_{mi} \\ -G_{mi} & G_{mi} \end{bmatrix}. \tag{2}$$

Making such a replacement is tantamount to replacing each ideal active element by a finite gain voltage-controlled current source (VCCS). This may be appropriate if the active element is a field-effect transistor (FET) or a transconductance op-amp. However, if the device is a voltage, current or transresistance op-amp or a bipolar junction transistor (BJT), then a voltage-controlled voltage, current-controlled current or current controlled voltage source model would be more appropriate.

In this paper, we present alternative admittance matrix models for the nullor that meet this requirement and we illustrate their use by means of examples. We also show that for circuits whose behavior depends on the geometry of ideal transistors, it is possible to include a transistor geometry factor in the corresponding nullor description. We will then illustrate these methods of circuit modelling using the V-mirror circuit [10]. We begin by deriving admittance matrix descriptions for the nullor from circuit models; the same descriptions are then derived using the theorem for matrices containing ∞-variables of [1]. The present paper is an expanded version of [11].

II. Admittance Matrix Description of Nullor

A. Sufficiency of Conditions for Dependent Source—Nullor Equivalence

Consider the 2-port network consisting of the series-connected admittance Y shown in Fig. 2 and its transmission matrix

$$\begin{bmatrix} 1 & Y^{-1} \\ 0 & 1 \end{bmatrix}. \tag{3}$$

Using this transmission matrix and the null transmission matrix for the nullor, we can write the identities

$$\begin{aligned} \begin{bmatrix} 1 & Y^{-1} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} &\equiv \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} 1 & Y^{-1} \\ 0 & 1 \end{bmatrix} \\ &\equiv \begin{bmatrix} 1 & Y_1^{-1} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} 1 & Y_2^{-1} \\ 0 & 1 \end{bmatrix} \\ &\equiv \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \end{aligned} \tag{4}$$

where $Y, Y_1, Y_2 \neq 0$. These identities imply that a nullor connected in cascade with a series-connected nonzero admittance, either at its input port, at its output port or at both input and output ports, is indistinguishable from the nullor itself.

A dependent source of any of the four possible types (voltage-controlled current, current-controlled voltage, voltage-controlled voltage, current-controlled current) becomes equivalent to a nullor if its gain tends to infinity, as shown by their transmission matrices

$$\begin{aligned} \left.\begin{bmatrix} 0 & G_m^{-1} \\ 0 & 0 \end{bmatrix}\right|_{G_m \to \infty} &\equiv \left.\begin{bmatrix} 0 & 0 \\ R_T^{-1} & 0 \end{bmatrix}\right|_{R_T \to \infty} \\ &\equiv \left.\begin{bmatrix} \mu^{-1} & 0 \\ 0 & 0 \end{bmatrix}\right|_{\mu \to \infty} \\ &\equiv \left.\begin{bmatrix} 0 & 0 \\ 0 & \beta^{-1} \end{bmatrix}\right|_{\beta \to \infty} \\ &\equiv \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}. \end{aligned} \tag{5}$$

Equation (5) implies that as well as the gains of the dependent sources tending to infinity their input and output admittances are ideal, e.g., for the VCVS, the input admittance and the output impedance are zero.

The expressions in (4) correspond to ideal dependent sources with gain tending to infinity, as in (5), with the addition of a series-connected admittance at the input, the output or both. Such admittances can be interpreted as finite input or output admittances of dependent sources that are otherwise ideal in that their gain still tends to infinity. This suggests that, for equivalence to a nullor, the gains of dependent sources must be infinite, but their input and output admittances are unrestricted provided they are not zero. Hence, although (5) is a sufficient condition for equivalence to a nullor, it is over-restrictive, since a weaker sufficient condition [based on (4)] exists. We now derive admittance matrix descriptions for the nullor based on (4). We assume initially that the nullator and norator are connected to the reference node; the general case will be considered later.

B. Nullor Descriptions Based on Dependent Sources

We show, in the first column of the first row of Table I, the admittance matrix for the voltage-controlled current source (VCCS), where node 1 is the input node and node 2 is the output node.[1] The transconductance G_m in Table I has a negative sign so that, with $G_m > 0$, a positive input voltage causes a positive current to flow out of node 2; the reference directions for the port currents adopted are positive directed towards the 2-port circuit. The remaining entries in row 1 of Table I are admittance matrices for the current-controlled voltage source (CCVS), voltage-controlled voltage source (VCVS) and current-controlled current source (CCCS) using ∞-variables, as derived in [1]. If the ∞-variables in these admittance matrices are replaced by finite variables, then the admittance matrices take the forms in the second row of Table I which now describe nonideal dependent sources. The nonideal sources have the

[1]Unlabeled rows and columns in admittance matrices are assumed to be labeled in numerical order $(1, 2, \ldots)$ and correspond to the node numbers in the circuit.

TABLE I
DERIVATION OF ADMITTANCE MATRICES FOR THE NULLOR VIA DEPENDENT SOURCES

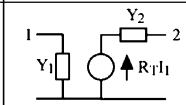
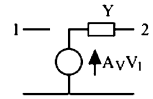
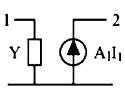
	VCCS	CCVS	VCVS	CCCS
$\mathbf{Y}_{\text{source}}$	$\begin{bmatrix} 0 & 0 \\ -G_m & 0 \end{bmatrix}$	$\begin{bmatrix} \infty_1 & 0 \\ -\infty_1\infty_2 R_T & \infty_2 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ -A_v\infty_1 & \infty_1 \end{bmatrix}$	$\begin{bmatrix} \infty_1 & 0 \\ -A_I\infty_1 & 0 \end{bmatrix}$
$\mathbf{Y}_{\text{non-ideal source}}$	$\begin{bmatrix} 0 & 0 \\ -G_m & 0 \end{bmatrix}$	$\begin{bmatrix} Y_1 & 0 \\ -Y_1Y_2R_T & Y_2 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ -A_vY & Y \end{bmatrix}$	$\begin{bmatrix} Y & 0 \\ -A_IY & 0 \end{bmatrix}$
Equivalent Circuit				
$\mathbf{Y}_{\text{nullor}}$	$\begin{bmatrix} 0 & 0 \\ -\infty_G & 0 \end{bmatrix}$	$\begin{bmatrix} Y_1 & 0 \\ -Y_1Y_2\infty_R & Y_2 \end{bmatrix}$	$\begin{bmatrix} 0 & 0 \\ -\infty_vY & Y \end{bmatrix}$	$\begin{bmatrix} Y & 0 \\ -\infty_iY & 0 \end{bmatrix}$

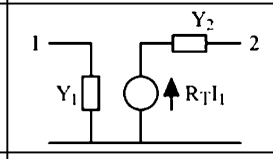
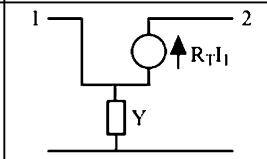
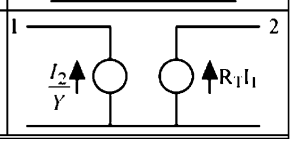
TABLE II
CONSTRAINTS IMPOSED BY ALTERNATIVE NULLOR DESCRIPTIONS

$\mathbf{Y}_{\text{nullor}}$	Constraints
$\begin{bmatrix} 0 & 0 \\ -\infty_G & 0 \end{bmatrix}$	$I_1 = 0$ $I_2 = -\infty_G V_1$ and $I_2 = \text{finite} \Rightarrow V_1 \to 0$
$\begin{bmatrix} Y_1 & 0 \\ -Y_1Y_2\infty_R & Y_2 \end{bmatrix}$	$I_2 = Y_2(V_2 - \infty_R Y_1 V_1)$ and $I_2, V_2 = \text{finite} \Rightarrow V_1 \to 0$ $I_1 = Y_1 V_1$ and $V_1 \to 0 \Rightarrow I_1 \to 0$
$\begin{bmatrix} 0 & 0 \\ -\infty_vY & Y \end{bmatrix}$	$I_1 = 0$ $I_2 = Y(V_2 - \infty_V V_1)$ and $I_2, V_2 = \text{finite} \Rightarrow V_1 \to 0$
$\begin{bmatrix} Y & 0 \\ -\infty_iY & 0 \end{bmatrix}$	$I_2 = -\infty_i Y V_1$ and $I_2 = \text{finite} \Rightarrow V_1 \to 0$ $I_1 = YV_1$ and $V_1 \to 0 \Rightarrow I_1 \to 0$

equivalent circuit models shown in the third row of Table I. Admittances Y_1, Y_2 and Y in the equivalent circuits in Table I can be interpreted as series-connected admittances, as in Fig. 2, in cascade with the input and/or output port of an ideal dependent source. If the gain of the ideal dependent source tends to infinity but the input and output admittance parameters remain finite nonzero, then our discussion arising from (4) proves that each circuit becomes equivalent to a nullor. This leads to the four admittance matrices for the nullor in the bottom row of Table I.[2] The way in which the four matrices impose conditions on the port voltages and currents is stated in Table II.

The admittance matrix for the CCVS given in the first row of Table I is one of three alternative representations derived in [1] and the complete set is shown in Table III. Table III also shows their equivalent circuits for the nonideal case. In the case of the type 2 and 3 descriptions, the parameter Y which tends to infinity cannot be interpreted as the admittance of a series-connected element at the input or output port of an ideal source

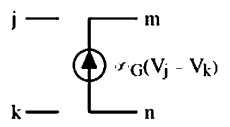
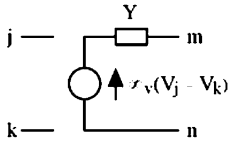
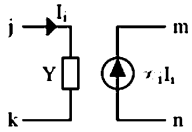
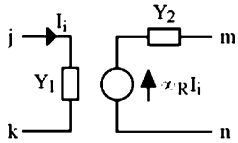
TABLE III
ADMITTANCE MATRICES AND CIRCUIT MODELS FOR THE CCVS

Type	Admittance matrix	Equivalent circuit
1	$\begin{bmatrix} \infty_1 & 0 \\ -\infty_1\infty_2 R_T & \infty_2 \end{bmatrix}$	
2	$\begin{bmatrix} -R_T^{-1} & R_T^{-1} \\ \infty_1 + R_T^{-1} & -R_T^{-1} \end{bmatrix}$	
3	$\begin{bmatrix} 0 & R_T^{-1} \\ \infty_1 & 0 \end{bmatrix}$	

and therefore we have to assume that, for equivalence to a nullor, both Y and R_T must tend to infinity. Under this condition, both admittance matrices become identical with that for the nullor derived from the VCCS shown in column 1 of Table I. Hence,

[2]The admittance matrices in the top and bottom row of Table I, for the ideal source and for the nullor, respectively, can be considered to be the result of taking the admittance matrices in the second row to different limits. It is possible to take all of the parameters to a limit of infinity and this leads to a set of equivalent admittance matrices for the nullor which have been presented in [11] but are unnecessarily over-restrictive relative to the ones we present here.

TABLE IV
ADMITTANCE MATRIX DESCRIPTIONS FOR THE NONGROUNDED NULLOR WITH CIRCUIT MODELS

Basis	Y_{nullor}	Equivalent Circuit
VCCS	$\begin{matrix} & j & k \\ m & -\infty_G & \infty_G \\ n & \infty_G & -\infty_G \end{matrix}$	
VCVS	$\begin{matrix} & j & k & m & n \\ m & -\infty_v Y & \infty_v Y & Y & -Y \\ n & \infty_v Y & -\infty_v Y & -Y & Y \end{matrix}$	
CCCS	$\begin{matrix} & j & k \\ j & Y & -Y \\ k & -Y & Y \\ m & -\infty_i Y & \infty_i Y \\ n & \infty_i Y & -\infty_i Y \end{matrix}$	
CCVS	$\begin{matrix} & j & k & m & n \\ j & Y_1 & -Y_1 & 0 & 0 \\ k & -Y_1 & Y_1 & 0 & 0 \\ m & -Y_1Y_2\infty_R & Y_1Y_2\infty_R & Y_2 & -Y_2 \\ n & Y_1Y_2\infty_R & -Y_1Y_2\infty_R & -Y_2 & Y_2 \end{matrix}$	

only the type 1 CCVS description in Table III, which we have used in Table I, leads to a distinctive nullor description.[3]

The matrix equivalences in Table I have been derived by making use of equivalent circuits for dependent sources. We now carry out the derivation using the theorem for matrices with ∞-variables [1].

C. Systematic Derivation of Equivalent Admittance Matrices for the Nullor

We start from the admittance matrix for the nullor derived from the VCCS in column 1 of Table I, which we show again in (6)-LH.[4] The matrix is not changed if we scale the ∞-variable by a unity factor Y/Y, where arbitrary parameter Y has the dimensions of admittance

$$\begin{bmatrix} 0 & 0 \\ -\infty_G & 0 \end{bmatrix} \rightarrow \begin{bmatrix} 0 & 0 \\ -\infty_G \frac{Y}{Y} & 0 \end{bmatrix}. \tag{6}$$

The next step is to perform a pivotal expansion [8]. This can be done in two ways.

[3]The fact that the CCVS descriptions of type 2 and 3 behave similarly in this respect is interesting because, as shown in [1], they are mathematically related through the theorem for matrices with ∞-variables.

[4]LH and RH denote left-hand and right-hand matrices, respectively.

Case 1) :We expand (6) so that ∞_G lies in the 3,1 position

$$\begin{bmatrix} 0 & 0 \\ -\infty_G \frac{Y}{Y} & 0 \end{bmatrix} \rightarrow \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & Y \\ \infty_G & 0 & Y \end{bmatrix} \rightarrow \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & Y \\ \infty_G & -Y & Y \end{bmatrix} \rightarrow \begin{bmatrix} 0 & 0 \\ -Y\frac{\infty_G}{Y} & Y \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 \\ -Y\infty_v & Y \end{bmatrix}. \tag{7}$$

In the third matrix, we have used the arbitrary element theorem of [1] in order to introduce into the 3,2 position a finite element $-Y$ by virtue of the ∞-variable ∞_G; then we have used Gaussian elimination to get back to a 2×2 matrix [8]. The final matrix is identical with the VCVS nullor description in column 3 of Table I where ∞_G/Y becomes the dimensionless parameter ∞_v.

Case 2) :We now expand (6) so that ∞_G lies in the 2,3 position

$$\begin{bmatrix} 0 & 0 \\ -\infty_G \frac{Y}{Y} & 0 \end{bmatrix} \rightarrow \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \infty_G \\ Y & 0 & Y \end{bmatrix} \rightarrow \begin{bmatrix} 0 & 0 & -Y \\ 0 & 0 & \infty_G \\ Y & 0 & Y \end{bmatrix} \rightarrow \begin{bmatrix} Y & 0 \\ -Y\frac{\infty_G}{Y} & 0 \end{bmatrix} \equiv \begin{bmatrix} Y & 0 \\ -Y\infty_i & 0 \end{bmatrix}. \tag{8}$$

In the third matrix, we have used the arbitrary element theorem in order to introduce element $-Y$ into position 1,3. Gaussian elimination leads to the final 2×2 matrix which is identical with the CCCS nullor description in column 4 of Table I with ∞_G/Y replaced by the dimensionless parameter ∞_i.

We now combine the approaches in case 1) and case 2).

Case 3) :We can use the VCVS-based nullor description derived in (7) as a starting point for the operations carried out in (6) and (8)

$$\begin{aligned}\begin{bmatrix} 0 & 0 \\ -Y_2\infty_v & Y_2 \end{bmatrix} &\rightarrow \begin{bmatrix} 0 & 0 \\ -(Y_2\infty_v)\frac{Y_1}{Y_1} & Y_2 \end{bmatrix} \\ &\rightarrow \begin{bmatrix} 0 & 0 & 0 \\ 0 & Y_2 & (Y_2\infty_v) \\ Y_1 & 0 & Y_1 \end{bmatrix} \\ &\rightarrow \begin{bmatrix} 0 & 0 & -Y_1 \\ 0 & Y_2 & (Y_2\infty_v) \\ Y_1 & 0 & Y_1 \end{bmatrix} \\ &\rightarrow \begin{bmatrix} Y_1 & 0 \\ -Y_1\frac{(Y_2\infty_v)}{Y_1} & Y_2 \end{bmatrix} \\ &\equiv \begin{bmatrix} Y_1 & 0 \\ -Y_1Y_2\infty_R & Y_2 \end{bmatrix}. \end{aligned} \tag{9}$$

The final matrix is identical with the CCVS nullor description in column 2 of Table I with ∞_v/Y_1 replaced by ∞_R, which has the dimensions of impedance as required.

D. Descriptions for the Nongrounded Nullor

The equivalent admittance matrix descriptions for the nullor in Table I apply to a nullor for which both nullator and norator are connected to the reference node. Matrices describing a nongrounded nullor with nullator connected between nodes j and k and norator connected between nodes m and n, as in Fig. 1(a), are shown in Table IV.[5] The nodes in Table IV that correspond with nodes 1 and 2 in Table I are j and m. Table IV also shows circuit models that correspond to the nongrounded nullor models.

There is a simple method for obtaining the element stamps in Table IV. For the VCVS, elements $\pm Y$ are inserted in rows and columns corresponding to the output nodes; these elements are duplicated, multiplied by $-\infty_v$ and shifted to the columns corresponding to the input nodes. For the CCCS, elements $\pm Y$ are inserted in rows and columns corresponding to the input nodes; these elements are duplicated, multiplied by $-\infty_i$ and shifted to the rows corresponding to the output nodes. Similar statements apply for the CCVS description. The nullor descriptions in Table IV will now be used to derive admittance matrices for devices.

[5]Each element $y_{pq} = y$ in an admittance matrix describing a grounded circuit element can be considered to have corresponding elements in row 0 and column 0 of its indefinite admittance matrix given by $y_{p0} = y_{0q} = -y, y_{00} = y$. The matrix for the corresponding nongrounded circuit element may be formed simply by moving these elements in row 0 and column 0 to appropriate rows and columns.

TABLE V
ADMITTANCE MATRIX STAMPS FOR THE IDEAL AND NONIDEAL FET AND BJT

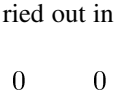
VCCS-based	CCCS-based
$\begin{matrix} & j & k \\ k & -\infty_G & \infty_G \\ n & \infty_G & -\infty_G \end{matrix}$	$\begin{matrix} & j & k \\ j & Y & -Y \\ k & -Y-\infty_i Y & Y+\infty_i Y \\ n & \infty_i Y & -\infty_i Y \end{matrix}$
$\infty_G \rightarrow G_m$	$\infty_i \rightarrow \beta$ $Y = r_\pi^{-1} = g_\pi$
 FET	 BJT

TABLE VI
ALTERNATIVE ADMITTANCE MATRIX STAMPS FOR IDEAL AND NONIDEAL OP-AMPS

Basis	Y-matrix	Conditions	Op-amp type
VCCS	$\begin{matrix} & j & k \\ m & -\infty_G & \infty_G \end{matrix}$	$\infty_G \rightarrow G_m$	Transconductance op-amp
VCVS	$\begin{matrix} & j & k & m \\ m & -\infty_v Y & \infty_v Y & Y \end{matrix}$	$\infty_v \rightarrow \mu$ $Y = r_{out}^{-1} = g_0$	Voltage op-amp
CCCS	$\begin{matrix} & j & k \\ j & Y & -Y \\ k & -Y & Y \\ m & -\infty_i Y & \infty_i Y \end{matrix}$	$\infty_i \rightarrow \beta$ $Y = r_{in}^{-1} = g_i$	Current op-amp
CCVS	$\begin{matrix} & j & k & m \\ j & Y_1 & -Y_1 & 0 \\ k & -Y_1 & Y_1 & 0 \\ m & -Y_1Y_2\infty_R & Y_1Y_2\infty_R & Y_2 \end{matrix}$	$\infty_R \rightarrow R_T$ $Y_1 = r_{in}^{-1} = g_i$ $Y_2 = r_{out}^{-1} = g_0$	Transresistance op-amp

III. ADMITTANCE MATRIX REPRESENTATIONS FOR DEVICES

The ideal transistor can be viewed as a nullor with a nullator node and a norator node co-incident, as shown in Fig. 1(b). Equivalent admittance descriptions for the ideal transistor derived from the VCCS- and CCCS-based descriptions in Table IV are given in Table V. The nullator and norator nodes in Table IV that have merged are k and m, respectively. This choice ensures that when the ∞-variables are replaced by finite variables, the transconductance y_{nj} for both transistor types is positive, i.e., positive gate (base) voltage causes current to flow into the drain (collector) terminal. The node created by merging nodes k and m is denoted node k. Note that when two nodes merge, corresponding rows and columns of the corresponding matrix from Table IV are added. Table V shows also the introduction of finite parameter values to replace the ∞-variables for nonideal analysis. G_m is the transconductance of the FET using the VCCS model; β is the current gain of the BJT using the CCCS model. Parameter g_π is the input admittance of the BJT.

The ideal op-amp can be viewed as a nullor where one of the norator nodes is connected to the reference node, as shown in Fig. 1(c). Admittance matrix descriptions for the ideal op-amp derived from all four nullor descriptions in Table IV are given in Table VI, where for all cases node n has been connected to the reference node. This choice ensures that when the ∞-variables

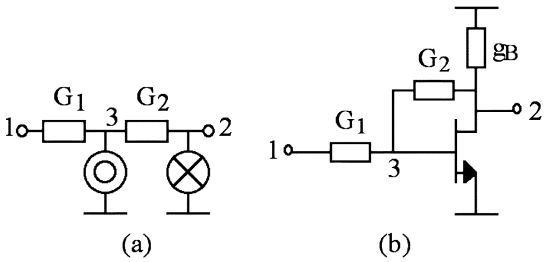


Fig. 3. Inverting amplifier. (a) Nullor equivalent. (b) Actual circuit.

are replaced by finite variables, the transconductance $I_m/(V_j - V_k)$ for all types of op-amp is negative, as is the case for real op-amps, i.e., positive differential input voltage causes current to flow out of the output terminal. The ∞-variables in Table VI may be replaced by finite parameters: G_m is the transconductance gain of the transconductance op-amp based on the VCCS model, μ is the voltage gain of the voltage op-amp based on the VCVS model, β is the current gain of the current op-amp based on the CCCS model and R_T is the transresistance gain of the transresistance op-amp based on the CCVS model. Other parameters are as follows: for the voltage op-amp, g_0 is the output admittance; for the current op-amp, g_ι is the input admittance; for the transresistance op-amp, g_0 is the output admittance and g_ι is the input admittance.

IV. Examples Illustrating Alternative Nullor Descriptions

A. Inverting Amplifier Using a Transistor

In [8], the synthesis of a voltage amplifier with voltage gain $A_v = -G_1/G_2$ leads to the nodal admittance matrix[6]

$$\left[\begin{array}{cc|c} G_1 & 0 & -G_1 \\ 0 & G_2 & \infty_1 - G_2 \\ \hline -G_1 & -G_2 & G_1 + G_2 \end{array}\right]. \tag{10}$$

he equivalence (11) in This matrix describes a circuit comprising two resistors and a grounded nullor, as shown in Fig. 3(a). The nullor may be replaced by an ideal transistor as shown in Fig. 3(b). Resistor g_B has been introduced for biasing and it may be represented by an extra term g_B in y_{22} in (10). Replacement of the ∞-variable ∞_1 in (10) by a finite parameter G_m models the transistor as a finite gain VCCS, which is appropriate if the transistor is a FET. For the case where the transistor is a BJT, then a CCCS model would be more appropriate and we now replace the VCCS-based nullor description in (10) with the CCCS-based one. The source of the transistor in the circuit in Fig. 3 is grounded. This is tantamount to node k in Table V being connected to the reference node, in which case row and column k in the two equivalent matrices may be deleted to yield the equivalence

$$\begin{matrix} j \\ n \end{matrix}\left[\infty_G\right]_{\mathrm{VCCS}} \equiv \begin{matrix} j \\ n \end{matrix}\left[\begin{matrix} Y & j \\ \infty_i Y & \end{matrix}\right]_{\mathrm{CCCS}}. \tag{11}$$

[6]The partition lines serve to denote that the circuit is a 2-port circuit, i.e., rows and columns beyond the partition lines refer to internal, or nonport, nodes (node 3 in this case) [1].

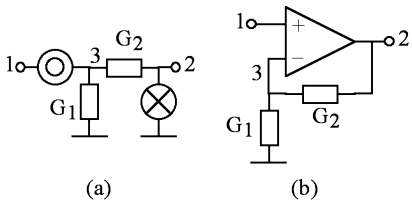


Fig. 4. Noninverting amplifier (a) Nullor equivalent (b) Actual circuit.

From Fig. 3, drain and gate nodes n and j in (11) are given by $n = 2$ and $j = 3$. Substitution of t(10) leads to the matrix

$$\left[\begin{array}{cc|c} G_1 & 0 & -G_1 \\ 0 & G_2 & \infty_i Y - G_2 \\ \hline -G_1 & -G_2 & Y + G_1 + G_2 \end{array}\right] \rightarrow \left[\begin{array}{cc|c} G_1 & 0 & -G_1 \\ 0 & G_2 & \beta g_\pi - G_2 \\ \hline -G_1 & -G_2 & g_\pi + G_1 + G_2 \end{array}\right]. \tag{12}$$

In (12)-RH, we have the represented the case of a nonideal BJT, by replacing the element ∞_i by the finite parameter β and Y by g_π, as in Table V. Reduction of the nonideal matrix in (12)-RH to a 2×2 port matrix allows us to determine the open-circuit voltage gain $(A_v = -y_{21}/y_{22})$ of the BJT amplifier, which we compare with that for the FET amplifier obtained from (10) with ∞_1 replaced by the finite parameter G_m

$$A_{v(\mathrm{BJT})} = -\frac{G_1}{G_2}\frac{1 - \frac{G_2}{\beta g_\pi}}{1 + \frac{1}{\beta} + \frac{G_1}{\beta g_\pi}}$$
$$A_{v(\mathrm{FET})} = -\frac{G_1}{G_2}\frac{1 - \frac{G_2}{G_m}}{1 + \frac{G_1}{G_m}}. \tag{13}$$

In principle, such an approach can be used to determine specifications on parameters needed for alternative types of device and hence make a choice as to which device type is most appropriate. For a circuit with more than one nullor, Gaussian elimination is valid for a combination of ideal and nonideal devices and therefore the replacement of nullors by nonideal transistors may be carried out one by one.

B. Noninverting Amplifier Using an Op-amp

In [8], the synthesis of a voltage amplifier with voltage gain $A_v = (G_1 + G_2)/G_2$ leads to the nodal admittance matrix

$$\left[\begin{array}{cc|c} 0 & 0 & 0 \\ -\infty_1 & G_2 & \infty_1 - G_2 \\ \hline 0 & -G_2 & G_1 + G_2 \end{array}\right]. \tag{14}$$

This matrix describes a circuit comprising two resistors and a nullor, as shown in Fig. 4(a). The norator is grounded and therefore the nullor may be replaced by an ideal op-amp as shown in Fig. 4(b). Replacement of the ∞-variable ∞_1 in (14) by a finite parameter G_m models the op-amp as a finite gain transconductance op-amp, but it is more likely that a voltage or current op-amp will be used. We first use the matrix equivalence in

Table VI to replace the VCCS-based op-amp description within (14) with the VCVS-based description[7]

$$\left[\begin{array}{cc|c} 0 & 0 & 0 \\ -\infty_v Y & Y+G_2 & \infty_v Y - G_2 \\ \hline 0 & -G_2 & G_1+G_2 \end{array}\right] \rightarrow \left[\begin{array}{cc|c} 0 & 0 & 0 \\ -\mu g_0 & g_0+G_2 & -\mu g_0 - G_2 \\ \hline 0 & -G_2 & G_1+G_2 \end{array}\right]. \quad (15)$$

We have then replaced the ideal VCVS gain ∞_v by the finite voltage gain μ and finite parameter Y by output admittance g_0, as in Table VI.

Now replacing the VCCS-based op-amp description in (14) with the CCCS-based description in Table VI, we have

$$\left[\begin{array}{cc|c} Y & 0 & -Y \\ -\infty_v Y & G_2 & \infty_v Y - G_2 \\ \hline -Y & -G_2 & Y+G_1+G_2 \end{array}\right] \rightarrow \left[\begin{array}{cc|c} g_i & 0 & -g_i \\ -\beta g_i & G_2 & \beta g_i - G_2 \\ \hline -g_i & -G_2 & g_i+G_1+G_2 \end{array}\right]. \quad (16)$$

We have then replaced the ideal CCCS ∞-variable ∞_i by the finite current gain β and finite parameter Y by g_i, as in Table VI. Reduction of the nonideal matrices in (15) and (16) to 2×2 port matrices allows us to determine the open-circuit voltage gain of the circuit using nonideal voltage and current op-amps

$$A_{v(V-\mathrm{op-amp})} = \frac{G_1+G_2}{G_2+\frac{1}{\mu}(G_1+G_2)+\frac{G_1G_2}{\mu g_0}}$$
$$A_{v(I-\mathrm{op-amp})} = \frac{G_1+G_2(1+1/\beta)}{G_2\left[1+\frac{1}{\beta}\left(1+\frac{G_1}{g_i}\right)\right]}. \quad (17)$$

Again, we see that this approach can be used to make an informed choice of device type and to specify device parameters. Additional parasitic admittances may be introduced into the circuit nodal admittance matrix and included in the analysis if required.

V. Description of Ideal Transistors With Specified Device Geometry

An ideal transistor can be represented in a circuit by a nullor, which can be described in the admittance matrix using ∞-variables, as in (1). When an ideal transistor occurs in a circuit which realises a network function, then two cases can be distinguished, depending on whether the network function is independent of or dependent on the transistor gain in the limit. An example of the first case is the circuit in Fig. 3 where we are interested in the open-circuit voltage gain. The voltage gain of this circuit is given by (13), and we can see that, in the ideal case, for $G_m \rightarrow \infty$, the voltage gain becomes independent of G_m. However, there exists a second class of circuits for which a network function is dependent on the gain of one or more transistors in the limit [12]. We now show that in such cases, the admittance matrix representation using ∞-variables may be extended to include geometry parameters of individual transistors.

[7]The correspondence between nodes in Table VI and nodes in Fig. 4 and (14), (15) and (16), is: $j = 1, k = 3, m = 2$.

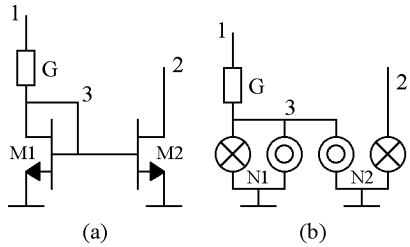


Fig. 5. (a) Example circuit. (b) Nullor equivalent.

When a circuit is implemented in integrated circuit form, the transconductance of each transistor depends partly on semiglobal parameters that affect a whole group of transistors on the integrated circuit, such as the N-FETs or the P-FETs, and partly on individual transistor parameters. In the case of MOSFETs, a key global parameter is oxide thickness; key individual parameters would be gate width-to-length ratio ($k_i = W_i/L_i$), where i refers to a particular device M_i, and gate–source bias voltage. The ∞-variable notation can accommodate global and individual transistor parameters by letting the transconductance gain for the ith ideal transistor be defined according to

$$\infty_i = k_i \infty_n \quad (18)$$

where k_i is a geometry-dependent parameter for transistor i and ∞_n is the global parameter which affects the gain of a group of transistors on the integrated circuit of which the transistor is a member. Note that whereas the dimensions of ∞_i in (18) are Siemens, the dimensions of k_i and ∞_n depend on the choice of individual and global parameters.

Consider as an example the circuit shown in Fig. 5 with its nullor equivalent circuit. Initially, the two FETs are considered ideal. Using the ∞-variable notation, the nodal admittance matrix may be written

$$\left[\begin{array}{cc|c} G & 0 & -G \\ 0 & 0 & \infty_2 \\ \hline -G & 0 & G+\infty_1 \end{array}\right] \rightarrow \left[\begin{array}{cc|c} G & 0 & -G \\ 0 & 0 & k_2\infty_n \\ \hline -G & 0 & G+k_1\infty_n \end{array}\right]. \quad (19)$$

In (19)-RH, we have introduced the notation of (18) where $k_i = (W/L)_i$ is the gate width-to-length ratio for transistor i and ∞_n is the transconductance parameter for N-MOSFETs. Gaussian elimination leads to the 2×2 port matrix

$$\left[\begin{array}{cc} \frac{Gk_1\infty_n}{G+k_1\infty_n} & 0 \\ \frac{Gk_2\infty_n}{G+k_1\infty_n} & 0 \end{array}\right] \rightarrow \left[\begin{array}{cc} G & 0 \\ G\frac{k_2}{k_1} & 0 \end{array}\right] = \left[\begin{array}{cc} G & 0 \\ G\frac{W_2L_1}{W_1L_2} & 0 \end{array}\right] \quad (20)$$

where we have taken the limit. From the final matrix, the short-circuit input admittance, transconductance and current gain of the circuit can be determined

$$\begin{aligned} Y_{\text{in}} &= \left.\frac{I_1}{V_1}\right|_{V_2=0} = y_{11} = G \\ G_m &= \left.\frac{I_2}{V_1}\right|_{V_2=0} = y_{21} = G\frac{W_2L_1}{W_1L_2} \\ \beta &= \left.\frac{I_2}{I_1}\right|_{V_2=0} = \frac{y_{21}}{y_{11}} = \frac{W_2L_1}{W_1L_2}. \end{aligned} \tag{21}$$

These expressions and their dependence on the FET dimensions are clearly correct.

In the case where the conductance G in Fig. 5 is replaced by a short-circuit, then the circuit becomes a current mirror [7]. The circuit obtained can be described by letting parameter G in the 2-port admittance matrix in (20)-LH become an ∞-variable ∞_G

$$\begin{bmatrix} \dfrac{\infty_G k_1 \infty_n}{\infty_G + k_1\infty_n} & 0 \\ \dfrac{\infty_G k_2 \infty_n}{\infty_G + k_1\infty_n} & 0 \end{bmatrix} \rightarrow \begin{bmatrix} k_1\infty_n & 0 \\ k_2\infty_n & 0 \end{bmatrix} \tag{22}$$

where we have taken a limit assuming that $\infty_G \gg k_1\infty_n$. Equation (22)-RH contains ∞-variables and comparison with the CCCS model in Table I shows that it describes a CCCS of gain and input admittance given by

$$\begin{aligned} A_I &= -\frac{I_2}{I_1} = -\frac{y_{21}}{y_{11}} = -\frac{k_2}{k_1} = -\frac{W_2L_1}{W_1L_2} \\ Y_{\text{in}} &= y_{11} = k_1\infty_n = \frac{W_1}{L_1}\infty_n \rightarrow \frac{W_1}{L_1}G_n \end{aligned} \tag{23}$$

where ∞_n has been set to the finite transconductance factor for the N-MOSFETs. The predicted gain and input admittance of the current mirror, and their dependence on the geometry parameters of the two FETs, are correct.

Thus the description of ideal transistors using ∞-variables in an admittance matrix can be extended to include transistor geometry parameters. As a further example of the use of alternative nullor descriptions, we next consider the example of the V-mirror (or Gilbert current mirror) discussed in [10].

VI. V-Mirror Circuit Example

A. General

The V-mirror 2-port circuit and its nullor representation are shown in Fig. 6. We will use the ∞-variable notation in order to achieve a number of aims.

1) To identify the type of the circuit as a classical 2-port.
2) To provide a quick and simple explanation of the observation in [10] that when port 1 is excited by an ideal independent current source, the current at port 2 is remarkably independent of the port 2 voltage (in one implementation it is still within 1% of its nominal value when V_2 is as low as 36 mV).
3) To explore the option of using FETs or BJTs for M_1 and M_2 and the option of using a transconductance, voltage or current type of op-amp.

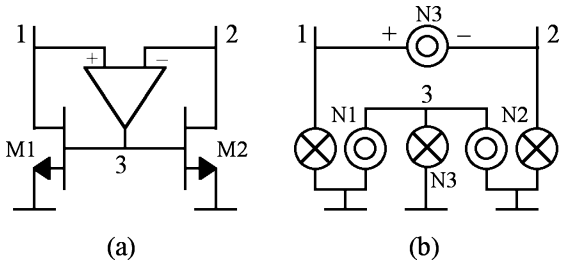


Fig. 6. (a) V-mirror circuit. (b) Nullor equivalent.

The second implementation of the V-mirror proposed in [10] uses N-MOSFETs for M_1 and M_2 and the op-amp is a single-stage design with P-MOSFET differential pair and NPN BJT current mirror. Since the input impedance and output impedance of the op-amp are both very high, we can model it as a transconductance op-amp.

B. Use of FETs and a Transconductance Op-amp

For the ideal case, M_1, M_2 and the op-amp in Fig. 6(a) can be modelled as nullors, as shown in Fig. 6(b). Using simple VCCS nullor models with transconductances ∞_1, ∞_2 and ∞_3, respectively, the nodal admittance matrix of the circuit is

$$\left[\begin{array}{cc|c} 0 & 0 & 0 \\ 0 & 0 & \infty_2 \\ \hline -\infty_3 & \infty_3 & 0_{33} \end{array}\right]. \tag{24}$$

The element 0_{33} is a form of limit variable called a zero-variable (0-variable) that can represent an element with a limit value of zero [1]. In practice, no matrix element can be zero because it will always have a lower bound governed by the net parasitic capacitance of the devices connected to the corresponding node. Since the element 0_{33} in (24) is in a pivot position, we recognise that its precise value will become critical in the nonideal case.

We next reduce the nodal admittance matrix in (24) to a port admittance matrix by Gaussian elimination

$$\begin{bmatrix} \dfrac{\infty_1\infty_3}{0_{33}} & -\dfrac{\infty_1\infty_3}{0_{33}} \\ \dfrac{\infty_2\infty_3}{0_{33}} & -\dfrac{\infty_2\infty_3}{0_{33}} \end{bmatrix}. \tag{25}$$

We can then write (25) in the form of the admittance matrix stamp for an impedance converter [1] with voltage gain A_v and reverse current gain A_i

$$\begin{bmatrix} A_V A_I \infty_y & -A_I\infty_y \\ -A_V\infty_y & \infty_y \end{bmatrix}. \tag{26}$$

Comparing (25) and (26), we have

$$A_V = 1 \quad A_I = -\frac{\infty_1}{\infty_2} \quad \infty_y = -\frac{\infty_2\infty_3}{0_{33}}. \tag{27}$$

A circuit model for an impedance converter which corresponds to (26) is shown in Fig. 7(a)[1]. From the expressions in (27) the voltage gain is positive and the current gain is negative.[8] We can thus classify the circuit of Fig. 6 as a *negative impedance converter*. It is clear from the expression for A_I in (27) that the

[8]The negative sign of the model parameter ∞_y does not necessarily imply instability because the nature of the limit admittance 0_{33} and the circuit embedding are important critical factors.

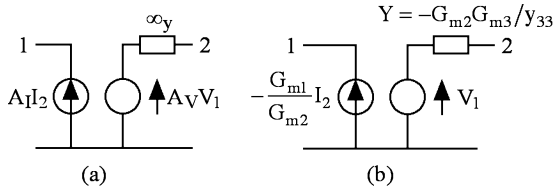


Fig. 7. (a) Ideal impedance converter circuit model. (b) Nonideal model.

current gain is governed by ratios of the dimensions of the two transistors.

We can now replace the ∞-variables in (27) by representations for nonideal devices. Replacing ∞_1, ∞_2 and ∞_3 by G_{m1}, G_{m2}, and G_{m3} and 0_{33} by the actual parasitic admittance y_{33} at node 3 of the circuit, the circuit model of Fig. 7(a) becomes as in Fig. 7(b). The admittance Y is the only nonideal element in the model and its form can be used to explain much about the behavior of the circuit. At low frequencies, the parasitic admittance y_{33} has a very small value, and therefore even if G_{m1} and G_{m2} are allowed to fall significantly (e.g., due to low output voltage) the parasitic admittance Y can still remain high and the circuit behavior is close to the ideal.

It is clear from the circuit model in Fig. 7(b) that the input and output voltages are approximately equal and therefore the constant current observed at node 2 for this circuit in [10] is obtained only when port 1 is driven by a perfect current source with no parasitic admittance. Thus, this impedance converter behaves quite differently from the current mirror, which approximates a CCCS, for which the output current can be relatively independent of output voltage even with nonzero source admittance. At high frequencies, the parasitic admittance y_{33} at node 3 in the V-mirror circuit will increase significantly, making the circuit much less ideal. In fact, the circuit in [10] has a compensation capacitor connected between nodes 1 and 3 in Fig. 6(a) and this will serve to control y_{33} and the high frequency behavior of the circuit. Terms representing the compensation capacitor may be added into the nodal admittance matrix in (24) and its effect included in the analysis. We now consider alternative choices of device for the V-mirror circuit.

C. Use of Alternative Types of Op-amp

We let M_1 and M_2 in the circuit of Fig. 6(a) remain as MOSFETs, but the op-amp now becomes a voltage or current op-amp. Then, from the circuit admittance matrix in (24) and the op-amp models in Table VI, we obtain the nodal admittance matrices[9]

$$Y_{V-\mathrm{op-amp}} = \left[\begin{array}{cc|c} 0 & 0 & \infty_1 \\ 0 & 0 & \infty_2 \\ \hline -\infty_v Y & \infty_v Y & Y \end{array}\right].$$

$$Y_{I-\mathrm{op-amp}} = \left[\begin{array}{cc|c} Y & -Y & \infty_1 \\ -Y & Y & \infty_2 \\ \hline -\infty_i Y & \infty_i Y & 0_{33} \end{array}\right]. \quad (28)$$

For the voltage op-amp, ∞_v represents the voltage gain and Y the output admittance; for the current op-amp, ∞_i represents the current gain and Y represents the input admittance. Finite parameters may be introduced to describe nonideal elements as in Table VI and the matrices reduced in order to obtain the properties of the impedance converter realisations. Notice that the matrices in (28) confirm the expected property that when a voltage op-amp is used the parasitic admittance at node 3 becomes relatively insignificant. We now consider in more detail the other case considered in [10] where an alternative choice of elements for M_1, M_2, and the op-amp in Fig. 6 is made.

[9]The correspondence between nodes in Table VI and nodes in Fig. 6, (24), and (28) is $j = 1, k = 2, m = 3$.

D. Use of BJTs With a Voltage Op-amp

Using BJTs for M_1 and M_2 and a voltage op-amp, the nodal admittance matrix of the V-mirror circuit in (24) now becomes

$$\left[\begin{array}{cc|c} 0 & 0 & \infty_{i1} Y_1 \\ 0 & 0 & \infty_{i2} Y_2 \\ \hline -\infty_{v3} Y_3 & \infty_{v3} Y_3 & Y_1 + Y_2 + Y_3 \end{array}\right]. \quad (29)$$

Variables ∞_{i1}, ∞_{i2} represent the current gains of the BJTs and Y_1, Y_2 represent their input admittances; ∞_{v3} represents the voltage gain of the op-amp and Y_3 its output admittance. Hence, (29) may be written

$$\left[\begin{array}{cc|c} 0 & 0 & \beta_1 g_{\pi 1} \\ 0 & 0 & \beta_2 g_{\pi 2} \\ \hline -\mu g_0 & \mu g_0 & g_{\pi 1} + g_{\pi 2} + g_0 \end{array}\right]. \quad (30)$$

We can reduce this matrix to obtain the port admittance matrix

$$\left[\begin{array}{cc} \dfrac{\beta_1 g_{\pi 1} \mu g_0}{g_{\pi 1} + g_{\pi 2} + g_0} & -\dfrac{\beta_1 g_{\pi 1} \mu g_0}{g_{\pi 1} + g_{\pi 2} + g_0} \\ \dfrac{\beta_2 g_{\pi 2} \mu g_0}{g_{\pi 1} + g_{\pi 2} + g_0} & -\dfrac{\beta_2 g_{\pi 2} \mu g_0}{g_{\pi 1} + g_{\pi 2} + g_0} \end{array}\right]. \quad (31)$$

Comparison with the impedance converter model of (26) gives the parameters in the circuit model of Fig. 7

$$A_v = 1 \quad A_i = -\frac{\beta_1 g_{\pi 1}}{\beta_2 g_{\pi 2}} = -\frac{\beta_1 r_{\pi 2}}{\beta_2 r_{\pi 1}}$$
$$Y = -\frac{\beta_2 g_{\pi 2} \mu g_0}{g_{\pi 1} + g_{\pi 2} + g_0} = -\frac{\beta_2 \mu}{r_{\pi 2} + r_0 \left(1 + \frac{r_{\pi 2}}{r_{\pi 1}}\right)}. \quad (32)$$

The form of this expression for Y is quite different from that for the circuit with MOSFETs and the transconductance op-amp. This leads to circuit performance being very much less dominated by parasitic admittance. For the performance to be optimised, the device gains β and μ should be maximised and the device impedances r_π and r_0 minimised. Device geometry factors, device capacitances and op-amp finite bandwidth can be included in the analysis if required.

VII. Conclusion

The ∞-variable notation of [1] has been used to derive new admittance matrix descriptions for the nullor. Whereas the existing admittance matrix description for the nullor degrades in the nonideal case always to a voltage-controlled current source, which is fine for modelling FETs and transconductance op-amps, the new descriptions can degrade to the voltage-controlled voltage, current-controlled voltage and current-controlled current sources. This permits accurate modelling for op-amps of the voltage, current and transresistance

types and for bipolar transistors, allowing a circuit to be optimised in terms of choice of device type and specification of device parameters. We have also shown that ∞-variables may be used with an associated scaling factor to represent the geometry factors of transistors.

The nullor models we derived in Section II are just representatives of an almost unlimited set of descriptions for the nullor that can be obtained by applying the theorem of [1] to any admittance matrix description for the nullor containing ∞-variables. Many of these matrix descriptions will not correspond with attractive circuit models but some may and could be worth exploring. Compared with the finite nullor description using the transmission matrix in (5), descriptions using ∞-variables seem to offer a rich potential for modelling and design. The technique can be used in principle to model any linear active circuit that is of interest and seems to be able to bridge the gap between circuit synthesis, where ideal active elements are assumed, and practical circuit design with real elements.

ACKNOWLEDGMENT

The authors would like to thank the anonymous reviewers for their very helpful comments and Dr. T. J. W. Clarke of Imperial College, London, U.K., for very helpful discussions.

REFERENCES

[1] D. G. Haigh, T. J. W. Clarke, and P. M. Radmore, "Symbolic framework for linear active circuits based on port equivalence using limit variables," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 9, pp. 2011–2024, Sep 2006.

[2] G. S. Moschytz, *Linear Integrated Networks—Fundamentals*. New York: Van Nostrand, 1974.

[3] H. Schmid, "Approximating the universal active element," *IEEE Trans Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 11, pp. 1160–1169, Nov. 2000.

[4] J. A. Svoboda, "Current conveyors operational amplifiers and nullors," in *Proc. Inst. Elect. Eng.*, Dec. 1989, vol. 136, no. 6, pp. 317–322, Pt. G.

[5] P. Kumar and R. Senani, "Bibliography on nullors and their applications in circuit analysis, synthesis and design," *Anal. Integr. Circuits Signal Process.*, vol. 33, no. 1, pp. 65–76, Oct. 2002.

[6] A. C. Davies, "The significance of nullators norators and nullors in active network theory," *Radio Electron. Eng.*, vol. 34, pp. 259–267, Jul.—Dec. 1967.

[7] *The Circuits and Filters Handbook* W.-K. Chen, Ed. Boca Raton, FL: CRC, 2002.

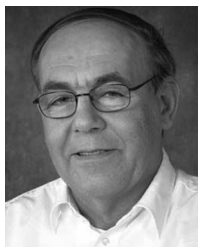
[8] D. G. Haigh, F. Q. Tan, and C. Papavassiliou, "Systematic synthesis of active-*RC* circuit building-blocks," *Anal. Integr. Circuits Signal Process.*, vol. 43, no. 3, pp. 297–315, Jun. 2005.

[9] D. G. Haigh, "Symbolic active-RC circuit synthesis by admittance matrix expansion," in *Proc. 2005 IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 248–251.

[10] B. Gilbert, "Current mode voltage mode or free mode—A few sage suggestions," *Anal. Integr. Circuits Signal Process.*, vol. 38, no. 2/3, pp. 83–101, 2004.

[11] D. G. Haigh and P. M. Radmore, "New admittance matrix descriptions for the nullor with application to circuit design," in *Proc. Eur. Conf. Circuit Theory and Design*, Sep. 2005, vol. III, pp. 43–46.

[12] E. A. M. Klumperink, F. Bruccoleri, and B. Nauta, "Finding all elementary circuits exploiting transconductance," *IEEE Trans Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 11, pp. 1039–1053, Nov. 2001.



David G. Haigh (M'70–SM'90–F'99) was born in Middlesex, U.K., in 1946. He received the B.Sc. degree in electrical engineering from Bristol University, Bristol, U.K., in 1968, and the Ph.D. degree from the University of London, London, U.K., in 1976.

From 1968 to 1972, he was with the GEC (U.K.) Hirst Research Centre, Wembley, U.K., and in 1972, he joined Imperial College London, London, U.K. In 1987, he moved to the Electronic and Electrical Engineering Department, University College London, London, U.K., and then returned to Imperial College in 2003. His fields of interest are RF circuits, mixed-signal circuits, and computer-aided circuit design.

Dr Haigh is a Fellow of the Institution of Electrical Engineers (U.K.) (IEE). He is the European Editor-in-Chief of the *Analog Integrated Circuits and Signal Processing Journal* and a former Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. He was co-recipient of the 1973 J. J. Thomson Premium of the IEE and co-recipient of the 1979 Darlington Award of the IEEE Circuits Syst. Society. The book *Analogue IC Design: The Current-Mode Approach* (IEE, 1990), which he co-edited, was a joint winner of the 1991 IEE Rayleigh Book Award and he was the recipient of the 1996 IEE Marconi Premium.

Paul M. Radmore was born in London, U.K., in 1955. He received the B.Sc. degree in mathematics and the Ph.D., from Imperial College London, London, U.K., in 1977 and 1980, respectively.

He is with the Department of Electronic and Electrical Engineering, University College London, London, U.K. His Ph.D. thesis was in the area of differential equations underlying quantum mechanics and general relativity. His fields of interest are quantum optics, communications, circuits and systems and several other areas where mathematical techniques play a key role in solving research problems in electronic engineering. He is the co-author of *Methods in Theoretical Quantum Optics* (Clarendon Press, 2002) and *Advanced Mathematical Methods for Engineering and Science Students* (Cambridge University Press, 1990). In addition, he has published many technical papers in several fields.