A CMOS Fully Balanced Four-Terminal Floating Nullor

Hussain Alzaher and Mohammed Ismail, *Fellow, IEEE*

***Abstract*—This paper presents design and implementation of a CMOS fully balanced realization of the four-terminal floating nullor (FTFN). The proposed fully balanced FTFN (FBFTFN) is an essential building block for implementing fully balanced architectures of both voltage and current-mode analog CMOS integrated circuits (ICs). A low-power class AB CMOS realization of the proposed circuit is fabricated in a 1.2-μm technology. The proposed circuit has numerous applications. Several applications including fully balanced amplifiers, filters, and sinusoidal oscillators are presented. All proposed design techniques and circuits are experimentally verified.**

***Index Terms*—Amplifiers, current-mode circuits, filters, four-terminal floating nullor, mixed-mode analog integrated circuits, sinusoidal oscillators.**

I. Introduction

THE four-terminal floating nullor (FTFN) combining both voltage and current mode capabilities is a more versatile analog building block than the operational amplifier (opamp) or the second-generation current conveyor (CCII) [1]–[5]. It was demonstrated in [1] that any active circuit can be realized by FTFN. Recently, it has been used in several applications ranging from current amplifiers, voltage to current converters, gyrators, floating immittances to active-RC filters and sinusoidal oscillators; see, for example, [6]–[15]. At present, FTFN is not yet commercially available. Practically, FTFN can mainly be implemented using current sensing technique [3], [5] or two CCIIs [7].

In modern systems, analog and digital circuits are implemented in the same integrated circuit (IC) chip. Therefore, it is required to implement the analog part using fully balanced architecture. Fully balanced systems are more immune to digital noise. In addition, fully balanced architectures are used in high performance analog applications to enhance the dynamic range, reduce harmonic distortion, and minimize the effect of coupling between various blocks [16]. The single single-ended FTFN is, therefore, not suitable for mixed analog and digital circuits.

Researchers' attention has mainly been devoted to FTFN applications using single-ended realizations. However, no effort was made to extend its operation to fully balanced architectures.

Manuscript received October 19, 2000; revised October 15, 2001. This paper was recommended by Associate Editor R. Gharpurey.

H. Alzaher was with The Ohio State University, Columbus, OH 43210-1272 USA. He is now with the King Fahd University of Petroleum and Minerals, Dhahran 31261, Saudi Arabia.

M. Ismail is with the Analog VLSI Laboratory, Department of Electrical Engineering, The Ohio State University, Columbus, OH 43210 USA.

Publisher Item Identifier S 1057-7122(02)03124-0.

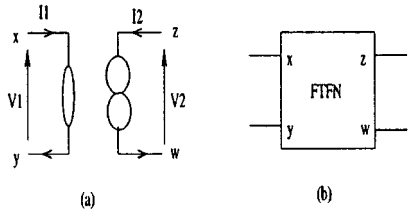

Fig. 1. FTFN: (a) Nullor model. (b) Single-ended symbol.

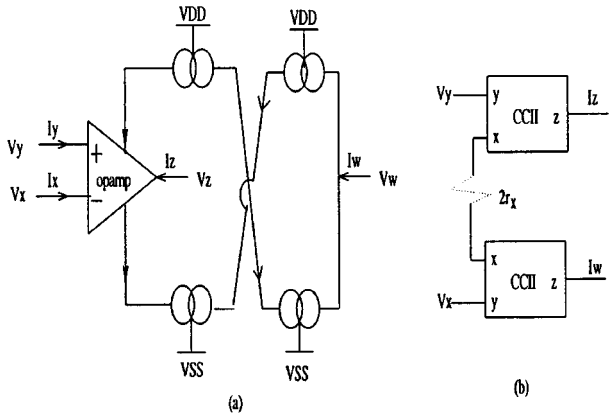

Fig. 2. Practical realization of FTFN. (a) Opamp based. (b) CCII based.

This paper presents the design and implementation of fully balanced FTFN (FBFTFN). Using the proposed circuit, any single-ended FTFN based circuit can be converted to its fully balanced architecture. This paves the way for FTFN-based circuits to be used in IC applications. A low-power class AB CMOS realization of the proposed FBFTFN is fabricated in a 1.2-μm chip. We show that the FBFTFN provides solutions for fully balanced realizations of both voltage and current-mode circuits. For example, it will be demonstrated that countless op-amp based circuits requires the use of FBFTFN for their FB realizations. Also, it is shown that unlike the op-amp, the FBFTFN can be configured as an inverting voltage-controlled voltage source (VCVS) with an infinite input impedance. Hence, it can be used to realize the fully balanced version of the minimum-component Sallen–Key bandpass filter [17]. In addition, new current and voltage-mode universal fully balanced filters are given. A novel application of the FBFTFN in designing controlled phase shift sinusoidal oscillators is also presented. The design and the implementation of the proposed low-power class AB FBFTFN are described in Section II. Section III demonstrates the use of the proposed FBFTFN in designing fundamental voltage and current-mode analog signal processing integrated circuits. Designs

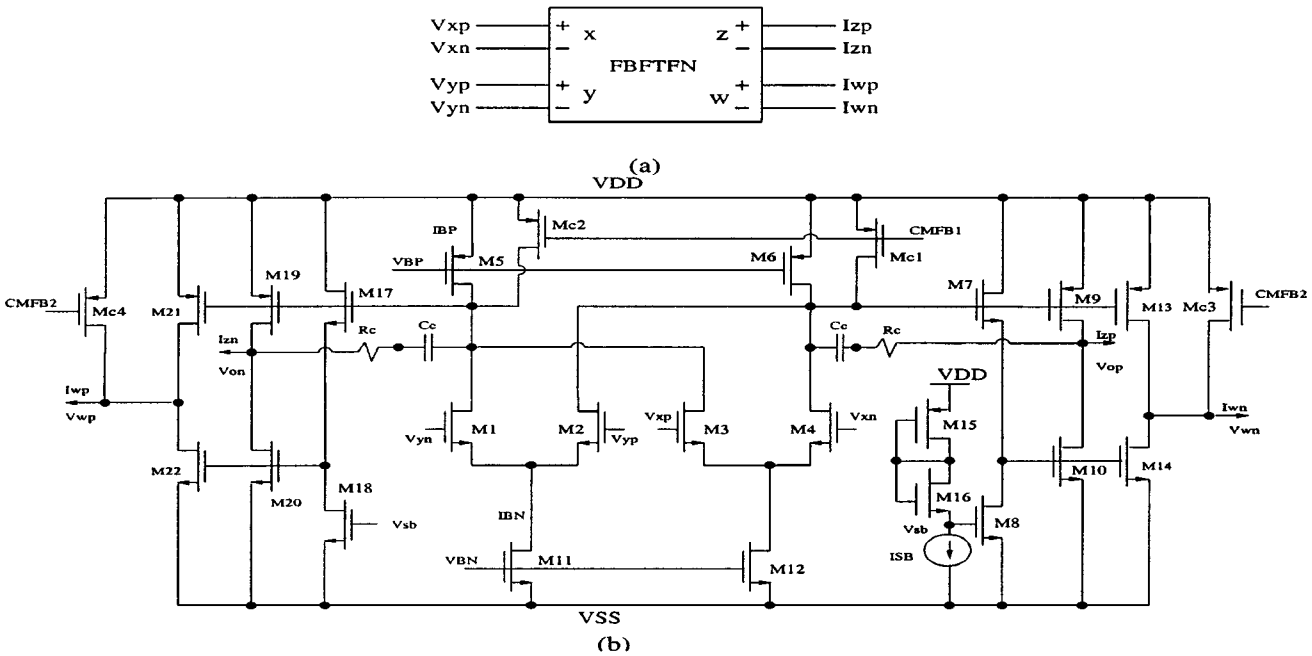

Fig. 3. Proposed class AB fully balanced FTFN. (a) Symbol. (b) CMOS implementation.

of fully balanced current and voltage-mode universal filters as well as a novel sinusoidal oscillator are given in Section IV.

II. Proposed Design and Monolithic Implementation

FTFN comprises a nullator $(V_1 = 0, I_1 = 0)$ at one port and a norator at the other port with arbitrary (V_2 and I_2) as illustrated in Fig. 1(a). According to the definition of FTFN, an ideal FTFN symbolically shown in Fig. 1(b), exhibits these terminal characteristics: $I_x = I_y = 0, V_x = V_y$ and $I_z = -I_w$. Fig. 2(a) shows the FTFN realization based on the current sensing technique [5]. Since this particular realization is based on a single active element, it generally exhibits better performance in terms of noise and linearity and voltage tracking error over the two CCII realization shown in Fig. 2(b). In fact, careful observation shows that the two ports of the circuit of Fig. 2(b) are not isolated, hence, violating the FTFN definition. Actually, due to the small internal resistance of the X terminal (r_x) of the two current conveyors, the voltage at the nullator port (V_1) produces a current at the norator port (I_2) given by $(I_2 = V_1/2r_x)$. As the parasitic resistant r_x increases, the voltage tracking error of nullator port increases and the current of the norator becomes no longer arbitrary. This means that if (r_x) is not very small, the circuit function simulates the operation of a dual-output transconductance amplifier rather than FTFN. Moreover, unlike the realization based on two CCIIs, the circuit of Fig. 2(a) exhibits high and low impedances at the norator port allowing its usage in both voltage and current mode applications. That is, if the output signal is desired to be in voltage mode, it can be obtained directly from the low impedance terminal whereas if the output signal is current it can be provided by the high impedance terminal. In fact, based on this realization both the opamp and the negative type second generation current conveyor (CCII-) become special cases of FTFN.

According to the FTFN definition, its fully balanced version (we give it the symbol in Fig. 3(a)) is an eight terminal device that can be characterized by the following equations:

$$I_{xp} = I_{xn} = I_{yp} = I_{yn} = 0 \tag{1}$$

$$V_{dx} = V_{xp} - V_{xn} = V_{dy} = V_{yp} - V_{yn} \tag{2}$$

$$I_{dz} = I_{zp} - I_{zn} = -I_{dw} = -(I_{wp} - I_{wn}). \tag{3}$$

We can extend the circuit of Fig. 2(a) to fully balanced operation by implementing the following modifications.

1) Two differential input ports, (V_{yp}, V_{yn}) and (V_{xp}, V_{xn}) are required rather than two single-ended inputs as is the case in the conventional opamp.
2) Two fully balanced outputs from the op-amp are needed instead of single-ended.
3) The current of the new output of the opamp has to be sensed and transferred to an additional current port.
4) There is no need to invert the current using cross coupled current mirrors because in fully balanced system the input or the output terminals (I_{zp}, I_{zn} and I_{wp}, I_{wn}) can be exchanged to change the transfer function polarity.

The proposed low-power CMOS realization is shown in Fig. 3(b). It has been fabricated in a 1.2-μm N-well CMOS process with the device sizes shown in Table I. Like the op amp, the circuit consists mainly of two stages: a differential-input single ended output transconductance stage (differential pair with active loads) and a second gain stage. Class AB output stages are used to achieve well determined low standby power consumption with good output current driving capability instead of the conventional class A (common-source amplifier) counterparts. Two similar rail-to-rail output stages are incorporated. The first consists of transistors M7–M10, and the second formed by transistors M17–M20. Transistors M15 and

TABLE I
DEVICE SIZES OF THE FBFTFN

Device Names	W/L (μm/μm)
M_1, M_2, M_3, M_4	198/3.0
M_5, M_6	99/3.0
M_7, M_8, M_{17}, M_{18}	9/4.8
M_9, M_{13}, M_{15}, M_{19}, M_{21}	180/2.4
M_{10}, M_{14}, M_{16}, M_{20}, M_{22}	72/2.4
M_{11}, M_{12}	150/2.4
M_{c1}, M_{c2}	99/3.0
M_{c3}, M_{c4}	180/2.4

M16 are used to properly bias both stages. Considering the first output stage, its operation can be described by the following two translinear loop equations:

$$V_{\mathrm{SG9}} + V_{\mathrm{GS7}} + V_{\mathrm{GS10}} = V_{\mathrm{DD}} - V_{\mathrm{SS}} \tag{4}$$

$$V_{\mathrm{SG15}} + V_{\mathrm{GS16}} + V_{\mathrm{GS8}} = V_{\mathrm{DD}} - V_{\mathrm{SS}}. \tag{5}$$

Since transistors M7 and M8 have the same size and carry the same current, they have the same gate source voltages (i.e., $V_{\mathrm{GS7}} = V_{\mathrm{GS8}}$).

$$V_{\mathrm{SG15}} + V_{\mathrm{GS16}} = V_{\mathrm{SG9}} + V_{\mathrm{GS10}} = \text{constant}. \tag{6}$$

During standby mode, no current is withdrawn from the output terminal and the currents of M9 and M10 are equal. Therefore, the current of the output transistors is equal to the standby current

$$I_{M9} = I_{M10} = I_{M15} = I_{M16} = I_{\mathrm{SB}}. \tag{7}$$

However, when the circuit is supplying, current M9 will be fully conducting while M10 will be almost off. Similarly, when the circuit is sinking current, the transconductance of M10 is dominant and that of M9 is negligible.

The two differential pairs convert the two differential voltages into two currents that are subtracted, converted into a voltage by the active load and amplified by the second stage. The fully balanced architecture of the output ports is designed in much the same way as the conventional op-amp. The outputs of the circuit can be expressed as

$$V_{\mathrm{op}} = -V_{\mathrm{on}} = A_o[(V_{yp} - V_{yn}) - (V_{xp} - V_{xn})] \tag{8}$$

where A_o is the open-loop gain given by

$$A_o = g_{m1}(r_{ds1}//r_{ds3}//r_{ds5}//r_{dsc1}) \times (g_{m9} + g_{m10})(r_{ds9}//r_{ds10}) \tag{9}$$

where g_m and r_{ds} are the small signal transconductance and the output resistance of MOS transistors. Analogous to the traditional op-amp, when a negative feedback is applied the differential voltages of the two input ports become equal

$$V_{yp} - V_{yn} = V_{xp} - V_{xn} \quad \text{as} \quad A_o \to \infty. \tag{10}$$

As the finite open-loop gain A_o decreases, the difference between the two differential voltages increases. Therefore, the open-loop gain is required to be as large as possible in order to improve the performance. Equation (8) is obtained assuming

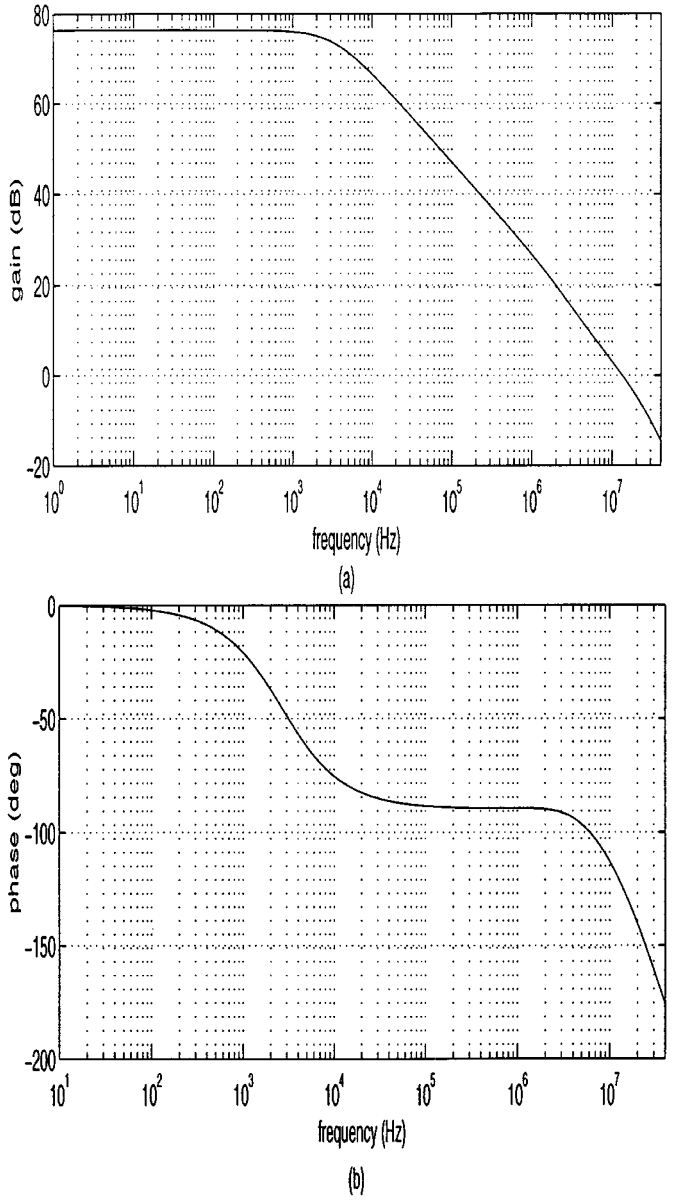

Fig. 4. Open-loop transfer characteristics of the FBFTFN. (a) Amplitude response. (b) Phase response.

that the two differential pairs M1–M2 and M3–M4 are matched and their tail currents are equal. It can be shown that matching errors between the two differential pairs produce a degraded common-mode rejection, an offset voltage, and nonlinearity. But reduced common-mode rejection ratio caused by mismatch turns to be independent of the input voltages. Thus, it will usually result in a constant closed-loop gain error. Similar effects are observed when considering mismatch between the two tail current sources. Matching between transistors is improved by following special layout techniques such as interdigitized and common centroid formations. The open loop voltage transfer characteristics of the proposed FBFTFN are shown in Fig. 4. It is obtained by measuring the differential output voltage $V_{zp} - V_{zn}$ in response to the differential input $V_{xp} - V_{yp}$ and with V_{xn} and V_{yn} grounded. It can be seen that the proposed circuit exhibits a differential gain of 75 dB and unity gain frequency of 14 MHz using a 3-V supply and a 400

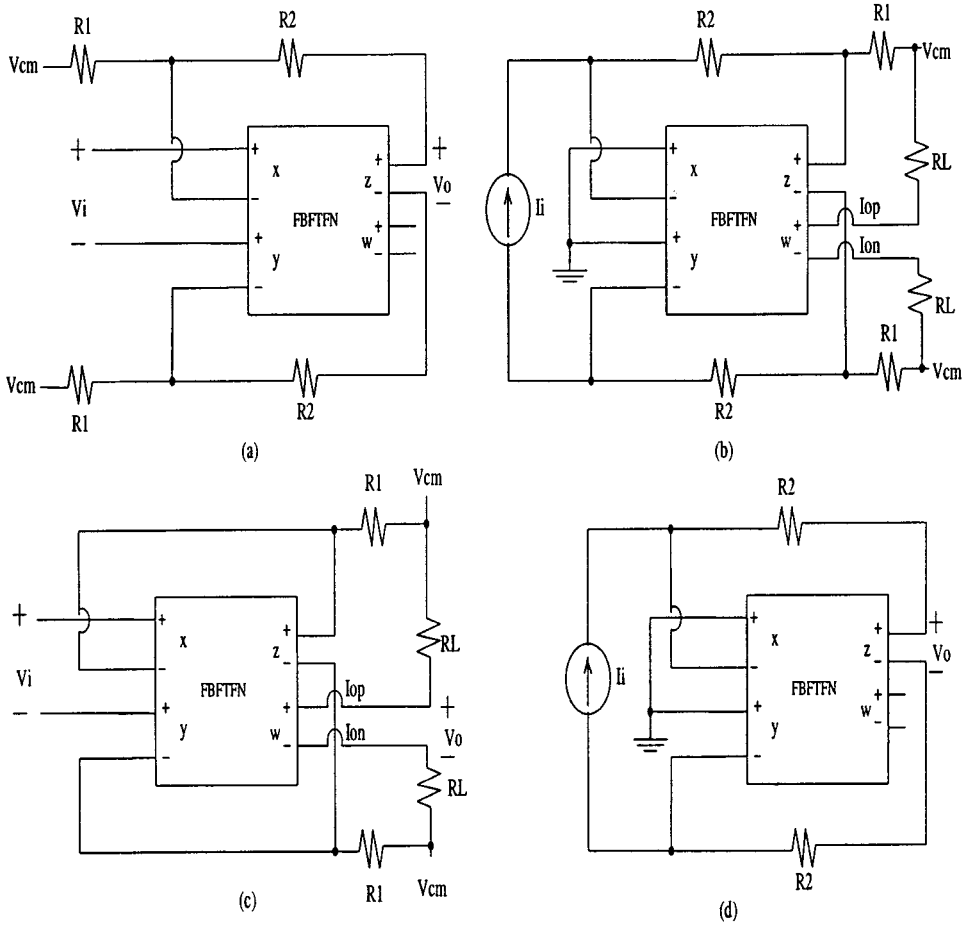

Fig. 5. Fully balanced amplifiers. (a) Voltage amplifier $(A_v = 1 + R_2/R_1)$. (b) Current amplifier $(A_i = 1 + R_2/R_1)$. (c) Transconductance amplifier, $(G_T = 1/R_1)$. (d) Transresistance amplifier $(R_T = R_2)$.

μA total standby current. Compensating capacitor (C_c) and resistor (R_c) are employed to ensure stability.

The currents through the two Z terminals are copied to two new additional current ports (I_{wp} and I_{wn}). Transistors M13–M14 and M21–M22 sense the currents of the Z terminals and copy them to two new current W terminals. Proper operation of the circuit require the use of the Z terminals to achieve negative feedbacks. This ensures stability since the Z terminals are involved in the circuit compensation. Applying negative feedback develops a low impedance at port Z which can be used for distributing voltage-mode signals (cascading, output port) without affecting the operation of the circuit. On the other hand, the W terminals associated with high output impedance is suitable for providing output current signals. Two traditional CMFB circuits (not shown in details for simplicity) [11] are employed to adjust the common mode signals at both norator ports $(V_{\rm op}, V_{\rm on})$ and (V_{wp}, V_{wn}). A CMFB circuit is needed to establish the common-mode output voltage and without it the common-mode voltage output would drift. It determines the output common-mode voltage and controls it such that it is equal to some specified voltage (usually mid-rail V_{cm}) even with the presence of large differential signals.

One major design factor that determines the performance of active devices is noise. Noise is usually calculated in terms of the input referred spectral density. MOS transistors typically generate two types of noise: flicker (the $1/f$) and thermal. It can be shown that the thermal and the flicker input referred noise of proposed FBFTFN are given by

$$V^2_{\rm thermal}(f) = \frac{32}{3}kT\left(\frac{1}{g_{mn}}\right) + \frac{32}{3}kT\left(\frac{g_{mp}}{g_{mn}}\right)^2\left(\frac{1}{g_{mp}}\right) \tag{11}$$

$$V^2_{\rm flicker}(f) = \frac{4}{C_{\rm ox}f}\left[\frac{K_n}{W_nL_n} + \left(\frac{\mu_p}{\mu_n}\right)\left(\frac{K_pL_n}{W_nL_p^2}\right)\right] \tag{12}$$

where k is the Boltzmann's constant $(1.38 \times 10^{-23}\text{JK}^{-1})$, T is the temperature in kelvin, $g_{mn} = g_{mi}$ $(i = 1$ to $4)$, $g_{mp} = g_{m5} = g_{m6} = g_{mc1} = g_{mc2}$ are the small-signal transconductance of MOS transistors, K_n and K_p are the flicker noise constant for NMOS and PMOS transistors, W and L are the width and the length of the transistors, μ_n and μ_p are the carrier mobilities, $C_{\rm ox}$ is the gate-oxide capacitance per unit area, and f is the frequency. It is clear that the transconductance (g_{mn}) of the differential pairs should be made as large as possible to minimize the thermal noise. Also, increasing the width of the differential-pair transistors clearly minimizes the $1/f$ noise. Moreover, it can be shown that the flicker noise exhibits a minimum for an optimum L_n. This is because L_n appears in the numerator and

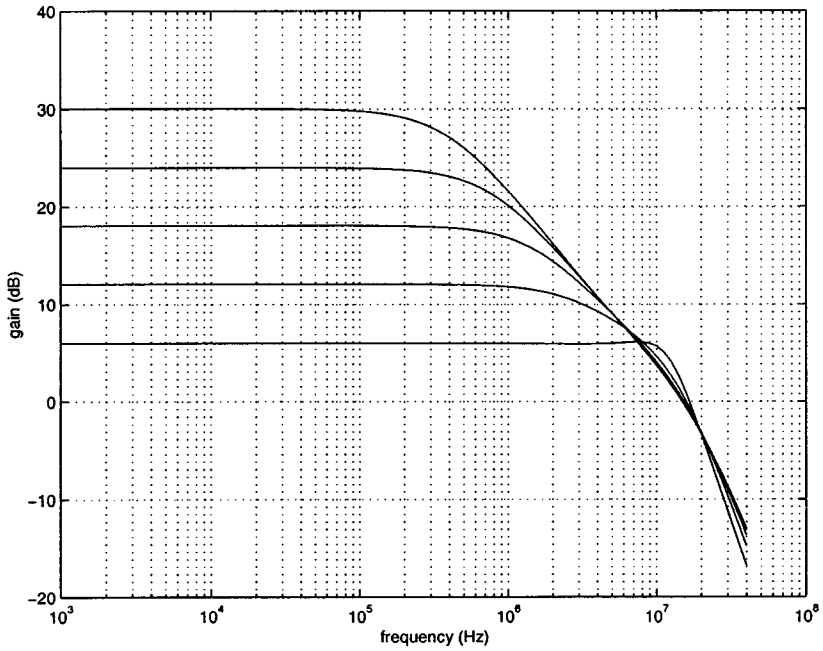

Fig. 6. The measured response of the voltage amplifier.

the denominator of the flicker noise equation. The optimum L_n is given by

$$L_n = \sqrt{\frac{\mu_n K_n}{\mu_p K_p}} L_p. \tag{13}$$

III. Design Examples

This section demonstrate the designs of several fundamental applications based on the proposed FBFTFN. First, four different types of amplifiers are given. Second, the use of FBFTFN in realizing fully balanced versions of several fundamental op-amp circuits is described. Third, a novel realization of the Sallen–Key bandpass filter based on FBFTFN is developed.

A. Fully Balanced Amplifiers

On of the most important features of the FTFN is that it can be configured as any type of the four basic amplifiers. Fully balanced architectures of voltage amplifier, current amplifier, transconductance amplifier and transresistance amplifier based on a single FBFTFN are shown in Fig. 5. It can be seen that the input and output impedances of the FBFTFN are adapted to comply with the type of input and output impedance required by each amplifier type. For example, the input impedance of the voltage amplifier is infinity and the output impedance is small. Whereas, the input and output impedances of the current amplifier are ideally zero, because of the virtual ground and infinity, respectively. All of these amplifiers were implemented and tested experimentally. Using a 3-V supply and a 400-μA total standby current, experimental results of the voltage amplifier of Fig. 5(a) are shown in Fig. 6. It can be seen that as the gain is increased, the bandwidth of the amplifier decreases due to the finite-gain bandwidth product of the FBFTFN.

One solution is to increase the biasing current for each gain step to maintain a constant bandwidth. However, this is not suitable for low-power applications. However, the transconductance amplifier of Fig. 5(c) can be used as a voltage amplifier to circumvent this problem. Fig. 7 shows the photomicrograph of the transconductance amplifier occupying an area of 0.2 mm^2 in a MOSIS test chip. The voltage gain is ideally determined by the resistor ratio R_L/R_1. Note that in this case, the FBFTFN is configured in unity gain feedback topology. Therefore, the bandwidth of the amplifier is constant and maximum. Resistor arrays (R_L) are used to digitally program the gain. Fig. 8 shows the frequency response of the amplifier of Fig. 5(c) under the same testing conditions of the amplifier of Fig. 5(a). Obviously, it exhibits constant bandwidth at the different gain

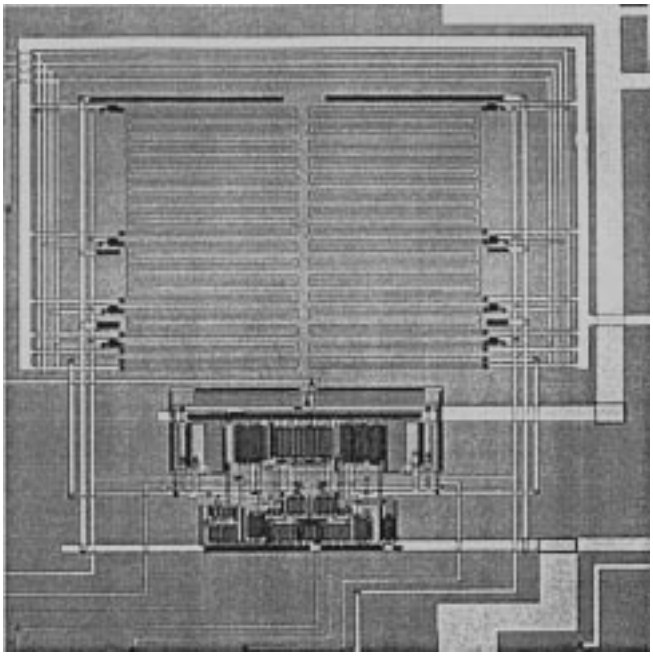

Fig. 7. Die photo of transconductance amplifier.

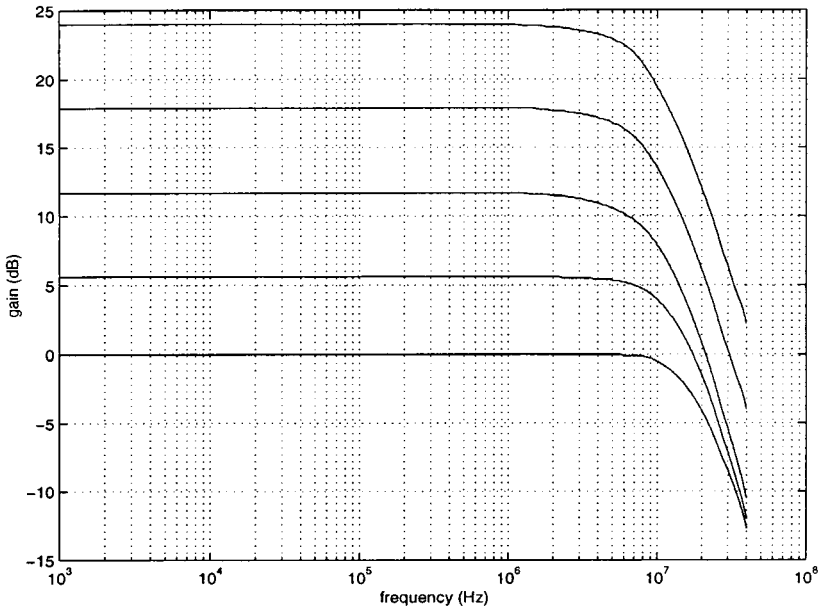

Fig. 8. The measured ac response of transconductance amplifier.

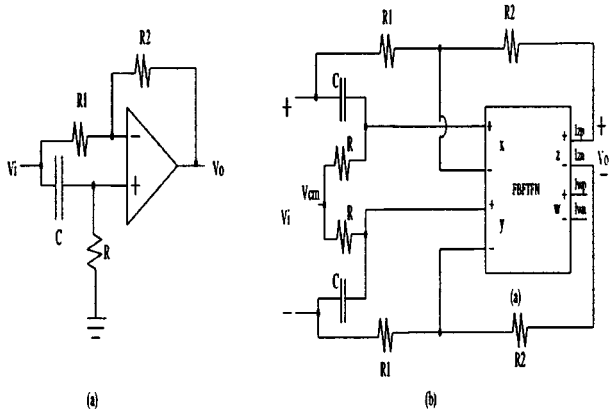

Fig. 9. Allpass filter. (a) Single-ended based on op-amp. (b) Fully balanced based on FBFTFN.

settings while keeping the power consumption at the same level. The input referred flicker noise of the amplifier was measured to be $40(\mathrm{nv}/\sqrt{\mathrm{Hz}})$ at 1 kHz and the thermal noise was $4(\mathrm{nv}/\sqrt{\mathrm{Hz}})$ at the maximum gain setting. Whereas, they were $61(\mathrm{nv}/\sqrt{\mathrm{Hz}})$ and $16(\mathrm{nv}/\sqrt{\mathrm{Hz}})$, respectively, at the minimum gain setting.

B. Opamp Based Circuits

It is well known that circuits based on op-amps can be directly transferred to a fully balanced realization using fully differential opamps. However, this is possible only if each of the opamps in the original circuit has the property that one of its input terminals is grounded. Here, we show that without this property, fully-differential implementations of such circuits can be accomplished using the FBFTFN. This is demonstrated by designing the fully balanced version of the first order allpass filter. The first-order allpass filter based on a single-ended opamp is shown in Fig. 9(a), whereas a fully balanced architecture based on the FBFTFN is shown in Fig. 9(b). The measured response of the filter is shown in Fig. 10. Other applications include the implementation of fully balanced versions of the state-variable filter, instrumentation amplifier, the balanced time constant integrator, the difference amplifier, the noninverting integrator or any other single ended op-amp circuit with floating op-amp inputs.

C. Sallen–Key Bandpass Filter

Sallen–Key (SK) well-known family of filters [17] requires only one op-amp per biquad. Hence, they are simple and attractive for low-power applications. Moreover, since these filters are based on one active element, they are optimum in terms of noise and linearity performance. It is possible to design SK lowpass and highpass filters based on a single opamp. However, SK bandpass filter which uses a single op-amp and seven passive elements [18] suffers from sensitivity problem since it has a negative term in the denominator of its transfer characteristics. On the other hand, the SK minimum-component bandpass filter shown in Fig. 11(a) exhibits low sensitivities. But its implementation requires a practical inverting voltage controlled voltage source (VCVS) with infinite input impedance that cannot be built using a single opamp.

Here, we show that the FBFTFN provides the solution for its implementation. A fully balanced version of the filter based on a single FBFTFN is shown in Fig. 11(b). The FBFTFN and the four resistors (R_3) and (R_4) realize the required fully balanced inverting VCVS with gain (k) given by

$$\frac{V_o}{V_{in}} = -k = -\left(1 + \frac{R_3}{R_4}\right). \tag{14}$$

The transfer function of the filter can be expressed as

$$\frac{V_o}{V_i} = \frac{-skC_2R_2}{s^2C_1C_2R_1R_2(1+k) + s(C_1R_1 + C_2R_2 + C_2R_1) + 1}. \tag{15}$$

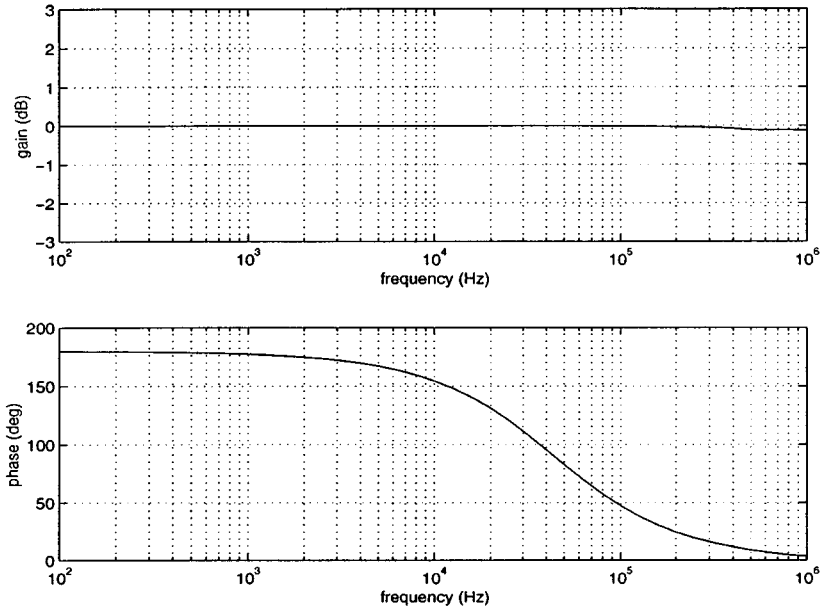

Fig. 10. The measured response of the first-order fully balanced allpass filter.

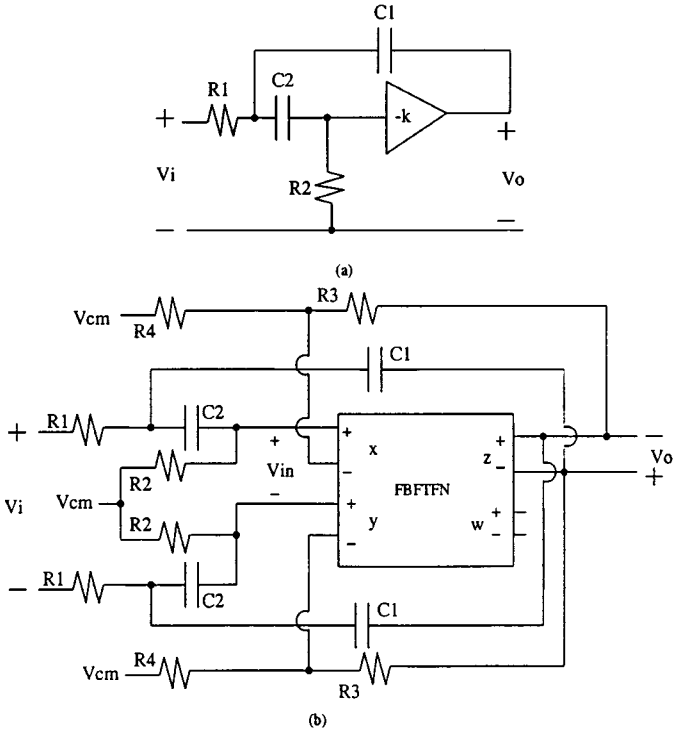

Fig. 11. SK bandpass filter. (a) Based on VCVS. (b) Fully balanced realization.

Hence, the natural center frequency (ω_o) and quality factor (Q) are given by

$$\omega_o = \sqrt{\frac{1}{C_1C_2R_1R_2(1+k)}} \tag{16}$$

$$Q = \frac{\sqrt{C_1C_2R_1R_2(1+k)}}{C_1R_1 + C_2R_2 + C_2R_1}. \tag{17}$$

It can be shown that the passive sensitivities of the parameters (ω_o) and (Q) are given by

$$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = S_{R_1}^{\omega_o} = S_{R_2}^{\omega_o} = -1/2 \tag{18}$$

$$S_{C_1}^{Q} = \frac{1}{2} - \frac{C_1R_1}{C_1R_1 + C_2R_2 + C_2R_1} \tag{19}$$

$$S_{C_2}^{Q} = \frac{1}{2} - \frac{C_2R_2 + C_2R_1}{C_1R_1 + C_2R_2 + C_2R_1} \tag{20}$$

$$S_{R_1}^{Q} = \frac{1}{2} - \frac{C_1R_1 + C_2R_1}{C_1R_1 + C_2R_2 + C_2R_1} \tag{21}$$

$$S_{R_2}^{Q} = \frac{1}{2} - \frac{C_2R_2}{C_1R_1 + C_2R_2 + C_2R_1} \tag{22}$$

$$S_{k}^{\omega_o} = -S_{k}^{Q} = -\frac{1}{2}\frac{k}{1+k}. \tag{23}$$

All of which are less than unity. The filter of Fig. 11(b) was implemented and tested experimentally. Its measured frequency response is shown in Fig. 12.

IV. Applications—Tuned Frequency Selective Circuits

This section presents the design of fully balanced current and voltage-mode universal filters based on the proposed FBFTFN. Active biquad circuits based on multiple amplifiers are generally less sensitive than single amplifier biquads. In addition, post adjustment and tuning can be done easily since the filter parameters can be controlled independently. Moreover, such circuits can be designed to provide all different types of filtering functions. Multifunction filters are commercially desirable as they lend themselves to integration. Mass-production reducing their cost compensates for the large number of active components required in their realizations.

Moreover, sinusoidal oscillators are useful in many communication and measurement systems. RC oscillators are preferred particularly at low and medium frequencies where they are more suitable for integration and physically more compact than other realizations [19]. The design of sinusoidal oscillators based on

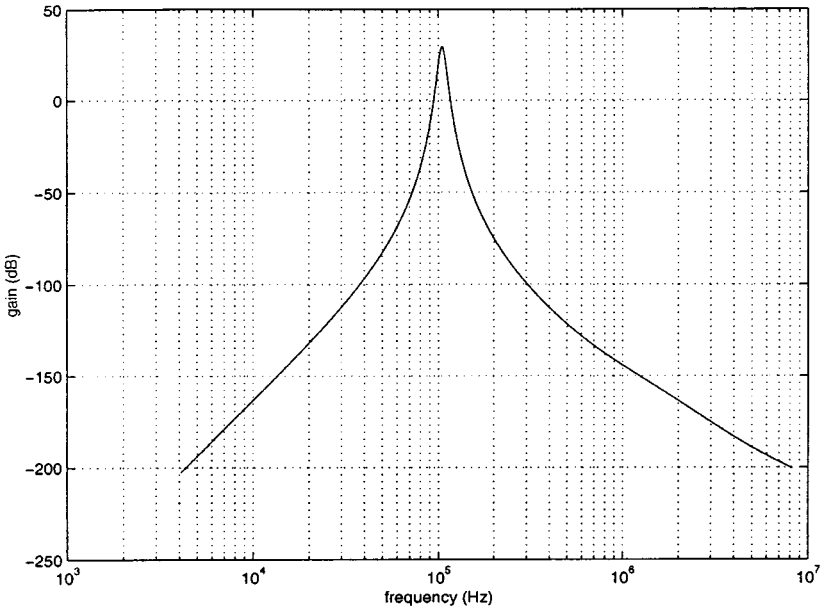

Fig. 12. The measured response of the fully balanced bandpass filter.

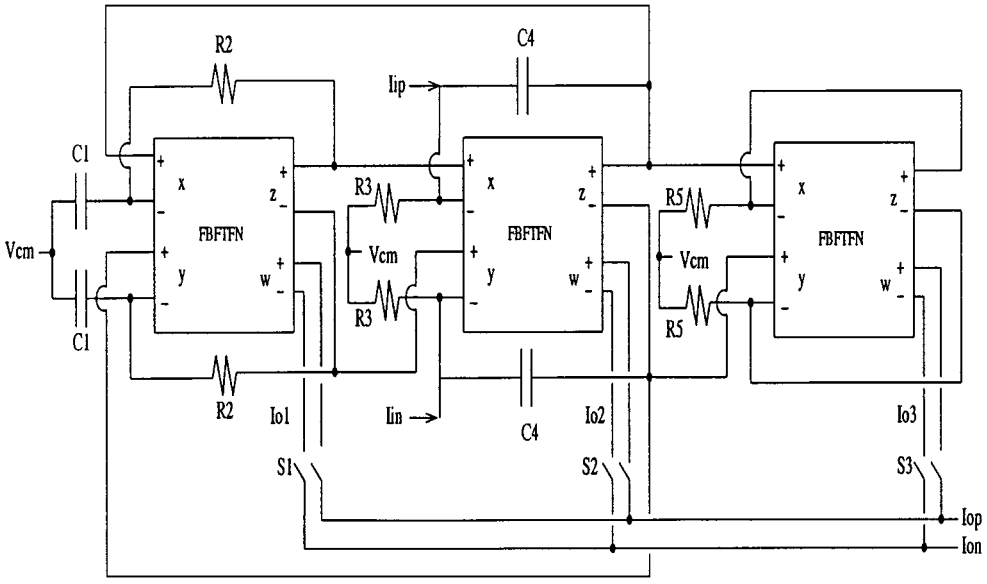

Fig. 13. Proposed fully balanced current-mode universal filter.

TABLE II
SELECTING THE DESIRED CURRENT-MODE FILTER FUNCTION DIGITALLY

S_1	S_2	S_3	Filter
0	0	1	Lowpass
0	1	0	Highpass
1	0	0	Bandpass
0	1	1	Notch
1	1	1	Allpass

a single FTFN has been extensively investigated [12]–[15]. In this section, we present a novel application of oscillator designs based on two FBFTFNs. It is shown that FBFTFN can be used to realize sinusoidal oscillators with controlled phase shift current-mode signals.

A. Current Mode Universal Filter

A new universal fully balanced current-mode filter based on the proposed FBFTFN is presented. The circuit realizes all the basic biquad filter functions, namely, lowpass, highpass, bandpass, notch, and allpass without changing the circuit topology. Therefore, it is suitable for integrated-circuit implementation. Generally, there are two architecture methods to realize current-mode universal filter: multiple input single output (MISO) and single input multiple output (SIMO). Usually, MISO architectures use three inputs that can properly applied individually or simultaneously to provide the desired filter function. In the case of the notch and allpass functions, additional circuits are needed to produce two or three equal currents from the input signal. On the other hand, SIMO architectures employ one input

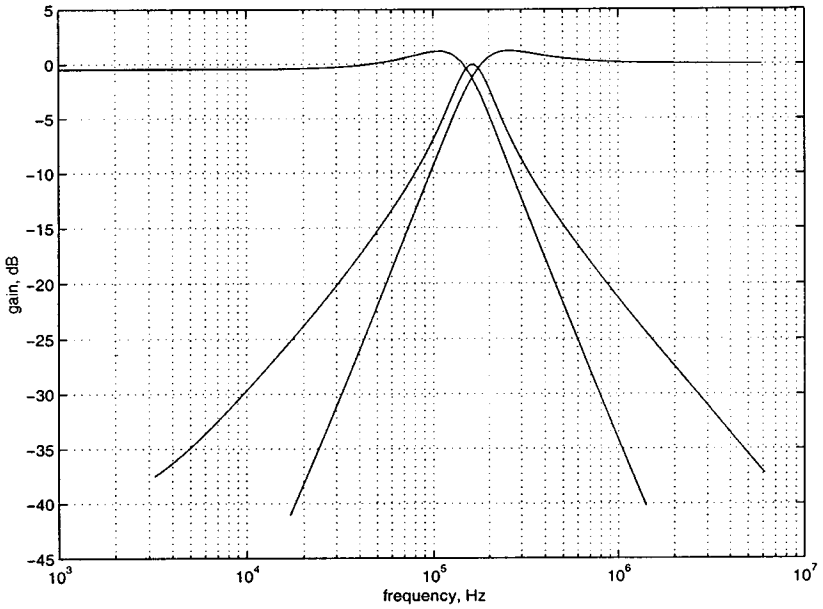

Fig. 14. Measured lowpass, bandpass, and highpass responses of the fully balanced current-mode filter.

to provide three different filter function outputs usually lowpass, bandpass and highpass. SIMO is more suitable for current-mode signal processing, since summing the lowpass, bandpass and highpass output currents to obtain the notch and the allpass requires no further use of active elements. The proposed SIMO filter using three FBFTFN and ten passive element (five element for single-ended topology) is shown in Fig. 13. Routine analysis of the circuit, shows that the proposed circuit offers the following transfer functions:

$$\frac{I_{o1}}{I_i} = \frac{-sC_1R_3}{s^2C_1C_4R_2R_3 + sC_1R_2 + 1} \tag{24}$$

$$\frac{I_{o2}}{I_i} = \frac{s^2C_1C_4R_2R_3}{s^2C_1C_4R_2R_3 + sC_1R_2 + 1} \tag{25}$$

$$\frac{I_{o3}}{I_i} = \frac{R_3/R_5}{s^2C_1C_4R_2R_3 + sC_1R_2 + 1}. \tag{26}$$

Since the lowpass, bandpass, and highpass currents are associated with high output impedances, they can be properly added to generate the desired filter function. The required filter function can be selected digitally by using the three switches of Fig. 13 as summarized in Table II with these additional conditions for the allpass response $R_2 = R_3 = R_5$. These switches are implemented using two CMOS transistors connected as transmission gates. The three controlling terminals of these switches are made available externally for desired selections. The parameters $(\omega_o), (Q)$ and the gains of the filter can be expressed as

$$\omega_o = \sqrt{\frac{1}{C_1C_4R_2R_3}} \tag{27}$$

$$Q = \sqrt{\frac{C_4R_3}{C_1R_2}} \tag{28}$$

$$G_{LP} = R_3/R_5 \tag{29}$$

$$G_{HP} = 1 \tag{30}$$

$$G_{BP} = R_3/R_2. \tag{31}$$

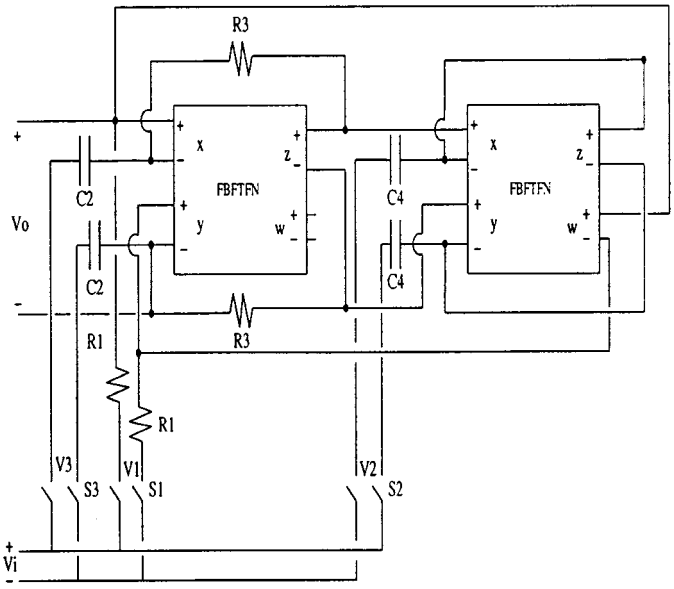

Fig. 15. Proposed fully balanced voltage-mode universal filter.

Since Q is determined by ratios of capacitors and resistors, it can be set quite accurately in an integrated circuit. However, the parameter w_o relies on inaccurate RC time constants. Tuning properties of w_o are essential for analog integrated filters to compensate for both component and temperature variations as integrated RC time constants can vary by as much as 50% [20]. Therefore, the parameter ω_o can be tuned without disturbing Q and the gains by simultaneously programming R_2, R_3 and R_5 using resistor arrays and/or C_1 and C_4 using capacitor arrays. Moreover, since the circuit exhibits high output impedance, it can be cascaded to realize high order filters. Furthermore, it can be shown that the passive sensitivities of the parameters (ω_o) and (Q) are given by

$$S_{C_1}^{\omega_o} = S_{C_4}^{\omega_o} = S_{R_2}^{\omega_o} = S_{R_3}^{\omega_o} = -1/2 \tag{32}$$

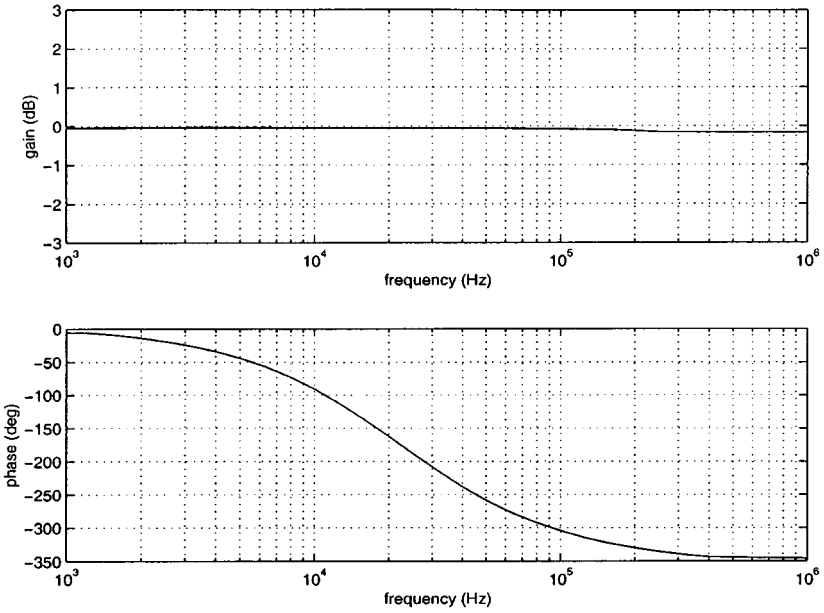

Fig. 16. Measured allpass responses of the fully balanced voltage-mode filter.

$$S_{C_1}^{Q} = -S_{C_4}^{Q} = S_{R_2}^{Q} = -S_{R_3}^{Q} = -1/2 \tag{33}$$

$$S_{R_5}^{\omega_o} = S_{R_5}^{Q} = 0. \tag{34}$$

All of which are small. Experimental results of the lowpass, bandpass, and highpass magnitude responses are shown in Fig. 14.

B. Voltage-Mode Universal Filter

In contrast to the case of current-mode, MISO universal voltage-mode topologies are more efficient than SIMO structures. This is because the input signal can directly be applied at the different input nodes. However, in the case of SIMO voltage mode structures a voltage adder and/or subtracter is required to obtain the notch and the allpass functions. A new fully balanced MISO voltage mode universal filter is shown in Fig. 15. It can be shown that the filter output exhibits the following function:

$$V_o = \frac{s^2 C_2 C_4 R_1 R_3 V_3 - s C_4 R_1 V_2 + V_1}{s^2 C_2 C_4 R_1 R_3 + s C_4 R_1 + 1}. \tag{35}$$

Therefore, the required filter function can be selected digitally by using the three switches to properly apply the input signal. The circuit is particularly attractive for realizing the allpass function since no matching conditions are required.

The parameters $(\omega_o), (Q)$ and the gains of the filter can be expressed as

$$\omega_o = \sqrt{\frac{1}{C_2 C_4 R_1 R_3}} \tag{36}$$

$$Q = \sqrt{\frac{C_2 R_3}{C_4 R_1}} \tag{37}$$

$$G_{LP} = G_{HP} = G_{BP} = 1. \tag{38}$$

The parameter ω_o can be tuned independently programming $R_1 = R_3$ and/or $C_2 = C_4$. In addition, it can be shown that the parameter's sensitivities are small. The measured results of the allpass frequency response are shown in Fig. 16.

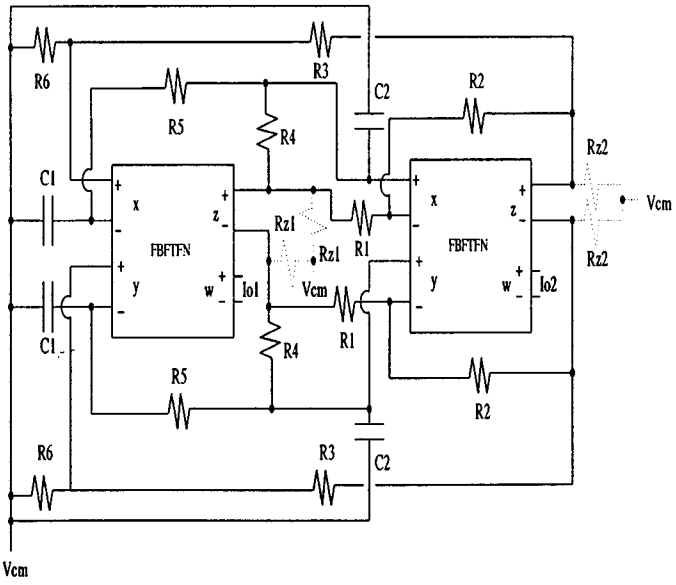

Fig. 17. Proposed fully balanced controlled phase shift sinusoidal oscillator.

C. Controlled Phase Shift Oscillator

A novel application of the FBFTFN in sinusoidal oscillator design is presented. It is shown that the FBFTFN exhibits a special feature that allows the design of controllable phase shift current-mode oscillator. This feature can be used in implementing phase modulated signals for communication systems. The proposed circuit is shown in Fig. 17. Routine analysis of the circuit yields the following characteristic equation:

$$s^2 \frac{C_1 C_2}{R_1 R_3} + s\left(\frac{C_1 + C_2}{R_1 R_3 R_5}\right) - s\frac{C_1}{R_2 R_3 R_4} + \frac{1}{R_2 R_4 R_5 R_6} = 0. \tag{39}$$

$$\frac{I_{o1}}{I_{o2}} = \frac{\frac{1}{Rz1} - \frac{R_1R_3}{R_2R_6}\left(\frac{1}{R_1}+\frac{1}{R_{z1}}+\frac{1}{R_4}\right) + sC_1\left[\frac{R_5}{R_{z1}} + \frac{R_1R_5}{R_2}\left(\frac{1}{R_1}+\frac{1}{R_{z1}}+\frac{1}{R_4}\right)\right]}{\frac{1}{R_{z2}} + \frac{R_3}{R_6}\left(\frac{1}{R_{z2}}+\frac{1}{R_2}+\frac{1}{R_3}\right) - sC_1\frac{R_5}{R_2}} \tag{42}$$

The natural frequency of oscillation (ω_o) and the condition of oscillation can be expressed as

$$\omega_o = \sqrt{\frac{R_1R_3}{C_1C_2R_2R_4R_5R_6}} \tag{40}$$

$$\frac{C_2}{C_1} = \frac{R_1R_5}{R_2R_4} - 1. \tag{41}$$

Thus, the frequency of oscillation is controlled by adjusting the grounded resistor (R_6) without disturbing the condition of oscillation. Also, the floating resistor (R_3) can be pre-selected to set the desired range of frequency of oscillation. In other words, R_6 and R_3 can be used for fine and coarse tuning of the oscillation frequencies, respectively. For example, R_3 can be preset to a small value to allow low frequency of oscillation without requiring large capacitors. Moreover, the condition of oscillation can independently be changed by simultaneously varying resistors R_1 and R_5.

Note that the Z terminals of the FBFTFNs of Fig. 17 are not involved in the calculation of the characteristic equation. Therefore, adding resistors (R_{z1}) and (R_{z2}) to these nodes does not change the characteristic equation and they can be used to control the output current amplitudes and their phase difference. It can be shown that changing R_{z1} varies the amplitude and the phase of the output current (I_{o1}). Similarly, R_{z2} can be used to adjust the amplitude and the phase of the output current (I_{o2}). The phase shift between the two output currents can be obtained from relation (42) shown at the top of the page. The oscillator circuit was tested using these passive components: $R_1 = 2$ k$\Omega, R_2 = R_3 = R_4 = R_5 = 10$ k$\Omega, C_1 = C_2 = 1$ nF. Experimental results show that the frequency of oscillation can be tuned from 170 kHz down to 30 kHz by varying R_6 from 5 to 50 kΩ. The results agree very well with the theoretical analysis with maximum error of 2%. Phase shifts between the two output currents as a function of R_{z1} and R_{z2}, with $f_o = 75$ kHz were measured. Using $R_{z2} = 0.1$ kΩ, phase shift in the range of 62° to 95° is obtained by varying R_{z1} from 0.1 to 5 kΩ. Note that quadrature oscillation or 90° phase shift can precisely be obtained using this circuit. Moreover, the phase shift is further varied from 95° to 142° by changing R_{z2} from 0.1 to 5 kΩ while $R_{z1} = 5$ kΩ is fixed. Furthermore, by changing the polarity of one of the output currents the above phase shift results can be "offseted" by 180°. The experimental results are in good agreement with the theory presented except for small deviation that does not exceed 4.5% due to ideal model used in the calculation.

V. Conclusion

In this paper, the design and implementation of a low-power FBFTFN has been presented. The proposed circuit has been fabricated in a 1.2-μm CMOS technology. This contribution extends the use of FTFN based circuits from discrete to integrated circuit applications. Design examples including amplifiers and frequency selective circuits are given. Fully balanced versions of the four basic amplifier types, namely, voltage amplifier, current amplifier, transconductance amplifier and transresistance amplifier are successfully implemented using the proposed FBFTFN. Also, we showed that the FBFTFN provides the solution for systematically developing fully balanced versions of any single-ended op-amp based circuit. New universal fully balanced current and voltage-mode second order filter suitable for integrated circuit applications have been presented. A novel sinusoidal oscillator providing two current-mode output signals with controllable phase shifts is also described. Experimental results verifying the operation of all proposed circuits are provided.

References

[1] H. Carlin, "Singular network element," *IRE Trans. Circuit Theory*, vol. CT-11, pp. 67–72, Mar. 1964.

[2] J. Huijsing and J. De Korte, "Monolithic nullor—A universal active network element," *IEEE J. Solid-State Circuits*, vol. 12, pp. 59–64, Feb. 1977.

[3] E. H. Nordholt, "Extending op amp capabilities by using a current-source power supply," *IEEE Trans. Circuits Syst.*, vol. CAS-29, pp. 411–414, June 1982.

[4] M. Higagimura, "Realization of current-mode transfer function using four-terminal floating nullor," *Electron. Lett.*, vol. 27, pp. 170–171, Jan. 1991.

[5] C. Toumazou, F. Lidgey, and C. Makris, "Extending voltage-mode op amps to current-mode performance," in *Proc. Inst. Elect. Eng. Circuits Devices Syst.*, vol. 137, 1990, pp. 116–130.

[6] J. Huijsing, "Operational floating amplifier," in *Proc. Inst. Elect. Eng. Circuits Devices Syst.*, vol. 137, 1990, pp. 131–136.

[7] R. Senani, "A novel application of four-terminal floating nullors," *Proc. IEEE*, vol. 75, pp. 1544–1546, Nov. 1987.

[8] M. Higashimura, "Current-mode allpass filter using FTFN with grounded capacitor," *Electron. Lett.*, vol. 27, no. 6, pp. 1182–1183, 1991.

[9] S.-I. Liu, "Cascadable current-mode filters using single FTFN," *Electron. Lett.*, vol. 31, no. 11, pp. 1965–1966, 1995.

[10] S.-I. Liu and J.-L. Lee, "Insensitive current/voltage-mode filters using FTFNs," *Electron. Lett.*, vol. 32, no. 6, pp. 1079–1080, 1996.

[11] M. Abuelma'atti, "Cascadable current-mode filters using single FTFN," *Electron. Lett.*, vol. 32, no. 8, pp. 1457–1458, 1996.

[12] R. Senani, "On equivalent forms of single op-amp sinusoidal RC oscillators," *IEEE Trans. Circuits Syst.*, vol. 41, pp. 617–624, Oct. 1994.

[13] C.-L. Hou, R. Yean, and C.-K. Chang, "Single-element controlled oscillators using single FTFN," *Electron. Lett.*, vol. 32, no. 10, pp. 2032–2033, 1996.

[14] H. Alzaher, "The Four-Terminal Floating Nullor (FTFN) and Its Applications," M.Sc. Thesis, KFUPM, Dhahran, Saudi Arabia, May 1997.

[15] M. Abuelma'atti and H. Alzaher, "Current mode sinusoidal oscillators using single FTFN," *IEEE Trans. Circuits Syst.*, vol. CAS-46, pp. 69–74, Jan. 1999.

[16] D. Johns and K. Martin, *Analog integrated circuit design*. New York: Wiley, 1997, ch. 6.

[17] R. Sallen and E. Key, "A practical method of designing RC active filters," *IRE Trans. Circuits Theory*, vol. CT-2, no. 3, pp. 74–85, 1955.

[18] W.-K. Chen, *Passive and Active Filters Theory and Implementations*. New York: Wiley, 1996, ch. 7.

[19] M. T. Darkani and B. B. Bhattacharyya, "Generation and design of canonic grounded-capacitor variable-frequency RC-active oscillators," *Proc. Inst. Elect. Eng.*, vol. 132, pp. 153–160, Aug. 1985.

[20] A. Durham, W. Redman-White, and J. Hughes, "High-linearity continuous-time filter in 5-V VLSI CMOS," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1270–1276, Sept. 1992.

Hussain A. Alzaher was born in Qatif-Alawamia, Saudi Arabia, in 1972. He received the B.S. and M.S. degrees (with honors) in electrical engineering from King Fahd University of Petroleum and Minerals (KFUPM), Dhahran, Saudi Arabia, in 1994 and 1997, respectively, and the Ph.D. degree from the Ohio State University (OSU), Columbus, in 2001.

He was with the Analog VLSI Laboratory of OSU from 1998 to 2001. He has also been, since 1994, a faculty member in the electrical engineering department of the KFUPM. His current work is in the field of analog baseband IC design for wireless receivers.

Dr. Alzaher is the recipient of the 1994/1995 Prince Muhammed bin Fahd bin Abdulaziz Award for Excellence in Scientific Achievement.

Mohammed Ismail (S'80-M'82-SM'84-F'97) received the B.S. and M.S. degrees in electronics and telecommunications engineering from Cairo University, Cairo, Egypt, in 1974 and 1978, respectively, and the Ph.D. degree in electrical engineering from the University of Manitoba in 1983.

He is a Professor with the Department of Electrical Engineering, The Ohio State University, and is the founder and director of the Analog VLSI Lab. He has held several positions previously in both industry and academia and has served as a corporate consultant to nearly 30 companies in the U. S. and abroad. He held visiting appointments at the Norwegian Institute of Technology, University of Oslo, University of Twente, Tokyo Institute of Technology, Helsinki University of Technology and the Swedish Royal Institute of Technology. He has authored many publications on VLSI circuit design and signal processing and has been awarded several patents in the area of analog VLSI. He has coedited and coauthored several books including a text on Analog VLSI Signal and Information Processing, (New York: McGraw Hill, 1994). He advised the work of 24 Ph.D. students, 70 M.S. students, and 17 visiting scholars. His current interests include low-voltage/low-power VLSI circuits, RF and mixed signal VLSI circuits for wireless communications, statistical computer-aided design and optimization, integrated circuits for image,video and multimedia applications and VLSI information processing systems. He gives intensive courses to industry in these areas. He has cofounded ANACAD-Egypt (now a part of Mentor Graphics) and SPIREA AB, Stockholm, Sweden.

Dr. Ismail has been the recipient of several awards including the IEEE 1984 Outstanding Teacher Award, the NSF Presidential Young Investigator Award in 1985, the OSU Lumley Research Award in 1993, 1997, and 2002, the SRC Inventor Recognition Awards in 1992 and 1993, and a Fulbright/Nokia fellowship Award in 1995. He is the founder of the International Journal of Analog Integrated Circuits and Signal Processing and serves as the Journal's Editor-In-Chief (North America). He has served the IEEE in many editorial and administrative capacities, including General Chair of the 29th Midwest Symposium CAS, member of the CAS Society Board of Governors, chair of the CAS Analog Signal Processing Technical Committee, the Circuits and Systems (CAS) Society's editor of the *IEEE Circuits and Devices Magazine*, founder and co-editor of The Chip, a column in the magazine, and associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON NEURAL NETWORKS, IEEE TRANSACTIONS ON VLSI SYSTEMS, and IEEE TRANSACTIONS ON MULTIMEDIA. He cofounded Micrys, Inc. (formerly ChipWorks, Inc.), a commercial VLSI design company specialized in analog and mixed-signal ASICs.