Homotopy Applied to Analogic Circuit Testing

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Abstract: The increase of complexity on integrated circuits has also raised the demand for new testing methodologies capable to detect functioning failures, in circuits before they reach the market. This work proposes the use homotopy as a tool for testing analogic circuits. On one hand, homotopy paths tend to be attracted by the traces formed by the intersection of equations that belongs to a system of non linear equations from the circuit; on the other hand, failures affect directly the non-linearities of the equilibrium equation. Therefore, the homotopy path is influenced by non linearities from the equilibrium equation of the circuit; this situation can be used to infer failures by detecting changes on the non linearities of the homotopy path.

*Introduction*: The vertiginous increase in the number of circuits by integrated circuit and the high number of non-linearities, present in the circuit, due to the decrease in the physical dimensions of the transistors, makes the integrated circuit testing area a huge challenge whether it is scientific as well as technological. The cost of testing an integrated circuit can represent, in average, the 50% for the total production cost, or even in some cases (specific circuits) represents up to 70% [1-4]. The development of strategies for integrated circuits testing, especially analogic circuits or mixed signal, is an open problem, nowadays, to the scientific community. These kinds of tests must assure complete functionality, quality and performance criterion, for each functional block, and the correct operation for the complete system, as well. Analogic circuits normally are non linear, include noise and has a wide variety of parameters. Besides, the relationship between input and output signals in analogic circuits is difficult to model. All of this becomes a constraint when developing failure simulators and testing algorithms capable to be reliable and broad.

*The homotopy*: Such methods [5, 6] consist on the continuous deformation of non-linear algebraic equation system, from a base state where the system is simplified, until a final state where the system recuperates its original state of high non-linearity. Equilibrium equation *f(x)* for the circuit is established according to the modified nodal analysis (MNA) method [10] becoming:

|  |  |
| --- | --- |
|  | (1) |

where*x* represents the unknown voltages and currents vector of the circuit (nodal voltages and non-NA compatible current elements [10]).

To obtain the homotopy curve, an additional parameter (homotopy parameter) is added into the original equations system, this allows finding the following augmented equation:

|  |  |
| --- | --- |
|  | (2) |

where*H* represents the homotopy function, is the homotopy parameter, *x* represents the electrical variables in the circuit, and is the non-linear equation system that represents the complete behaviour of the circuit.

The homotopy path is the group or solutions family for starting from where the solution is trivial, until where the solution is the desired (for ). Such process can continue as long as more solutions exist or operating points exist in the path.

*Testing and homotopy*: A failure or fabrication defect can beideally modelled as the unexpected existence of spurious resistors between nodes in the circuit. It may happen, as an example, the appearance of a spurious resistor between the *i*-th node and ground. This will affect directly the equilibrium equation, in particular the nodal equation . As smooth as this change appears, it could unchain a series of trastornos in the shape of the homotopy path. This way, it is possible to correlate an alteration in the homotopy path with the presence of failures, or even provide clues to the region where the failure might be located. It is common that some failures are not so soft, that is, no notorious effect can be perceived in the operating point; nevertheless, given the nature for the homotopy paths of being attracted by the crossing folds of the equilibrium equations, these paths could provide the evidence of failures that could make it hard to visualize by other means. The importance to locate these kind of failures is that if not change in a rather evident manner the operating point, they could alter the behaviour of circuits in aspects like: frequency, noise, limit voltages and currents, and other analogic circuit parameters.

*Case of study*: The use of the homotopy shown in equation 2 is proposed, which includes initial and final points within the bounding region. The formulation is provided as follows:

|  |  |
| --- | --- |
|  | (6) |

where is the homotopy parameter, is the equilibrium equation for the circuit, is a constant named solution line, represents the initial point, the final point of the path just at (symmetry axis), and is another constant.

The circuit in Figure 1 was reported and solved using fixed point homotopy [12]. The system of nodal equations (MNA) is formulated, it is chosen as initial point the value of 13V, for nodal values, and 13A for current *IVCC*of voltage source *VCC*. The initial point *xi* is shown in Table 1, just marking the corresponding sign (plus sign means +13, while minus sign means -13; volts or amperes whether is voltage or current respectively).

Now, a failure (*Rf*) is placed between node 8 and ground. This failure is represented as a resistor (*Rf=11kΩ*), which acts as a current leak to ground. There are three aspects of the results to be noticed:

1. The initial point for both simulations (with and without failure) is equal for both cases. Nevertheless, the final point *xf1* for the circuit without failure differs greatly from the final point *xf2* for the circuit with failure (see Table 1). That is, the failure modified the final point of the path; this situation can be used as criteria to detect failures. It is interesting to watch how the final nodal voltage did not change where the failure is located, but it modified the final meaning or voltage value at the nearer nodes (6 and 9).
2. In the circuit without failure, three operating points were located (*p1*, *p2*, and *p3*), while in the circuit simulation with failure only two operating points (*p1* and *p2*) were located. Besides, *p2* remained practically identical, while *p1* and *p3* modified their values drastically. Therefore, there are some changes in , just in the region surrounding *p2*.
3. The aspect of the homotopy path for the circuit without failure (see Figure 2(a)), differs with respect to the homotopy path for the circuit failure (see Figure 2(b)). The change with respect to the homotopy path is not simple to be quantified; nevertheless, the number of steps for the numerical continuation and the number of turning points can be monitored. The number of steps for the numerical continuation, in the case of the circuit without failure, was of 3367 steps, while for the circuit with failure the number of steps was 3555; this indicates that the path for the circuit with failure is longer. The former is proved by the fact that in the circuit without failure there was 19 turning points, while for the circuit with failure the number was 29 turning points. That is, the non-linearity degree increased for the homotopy path of the circuit with failure.

It has been shown how the homotopy path was employed in the analogic circuit test field, this leads to a future research line, the use of non linear analogic functions construction techniques, like the ones shown in [7, 8, 9], in order to implement at transistor level an internally built homotopy function for auto-testing [3] (BIST) of analogic circuits.

*Conclusion:* This work dealt with the application of homotopy to the analogic circuit testing area, leaving demonstrated the feasibility to detect the presence of failures using the homotopy path analysis, involving non linearities, length, and final point of the path. In this work has been introduced a novel area within testing, full of new and interesting research opportunities, also promising a new practical use for the homotopy.

### **References**

1 International Technology Roadmap for Semiconductors (ITRS),‘Test and Test Equipment’, (2001 Edition and 2002 Updated Edition), <http://public.itrs.net>

2 M. SACHDEV, ‘A Realistic Defect Oriented Testability Methodology for Analog Circuits’, Journal of Electronic Testing: Theory and Applications, Vol. 6, 1995, pp. 265-276.

3 V. N. YARMOLIK, A. M. SHMIDMAN, ‘Universal Module for BIST of mixed signal circuits’, 2nd International Mixed-signal Testing Workshop, 1996, pp. 104-108.

4L. MILOR, A. SANGIOVANNI, ‘Optional Test Set Design for Analog Circuts’, IEEE International Conference on Computer Aided Design, 1990, pp. 294-197.

5 R. C. MELVILLE AND L. TRAJKOVI´C, ‘Artificial parameter homotopy methods for the dc operating point problem’, IEEE transactions on computer-aided design of integrated circuits and systems, 1997, vol. 12, no. 6, pp. 861–877.

6 J. LEE AND C. HSIAO-D, ‘Constructive homotopy methods for finding all or multiple dc operating points of nonlinear circuits and systems’, IEEE Transactions on Circuits and Systems I-Fundamental Theory and Applications, 2001, vol. 48, no. 1, pp. 51–66.

7 K. TANNO, O. ISHIZUKA, AND Z. TANG, ‘Four-quadrant cmos current-mode multiplier independent of device parameters’, ieee transactions on circuits and systems—ii: analog and digital signal processing, 2000, vol. 47, no. 5, pp. 473-477.

8 M. T. ABUELMA’ATTI, ‘Universal cmos current-mode analog function synthesizer’, IEEE transactions on circuits and systems—i: fundamental theory and applications, 2002, vol. 49, no. 10, pp. 1468-1474.

9A. P. DIMOKRITOS, W. N. ROBERT, AND K. S. SANJEEV, ‘A current-Mode Exponential Amplifier’, IEEE Transactions on circuits and systems-II: analog and digital signal processing, 2000, Vol. 47, No. 6, pp. 548-552.

10 C. W. HO, A. E. RUEHLI, AND P. A. BRENNAN, ‘The modified nodal approach to network analysis’, IEEE transactions on circuits and systems, 1975, vol. 22, pp. 504–509.

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**Figure and table captions:**

Table 1. Initial and final points for the homotopy paths.

Figure 1. Benchmark circuit without failure (shows three operating points).

Figure 2.Homotopy paths v8 – λ for the circuit without failure and with failure.

1. Circuit without failure.
2. Circuit with failure.

Table 1

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| *x* | *v1* | *v2* | *v3* | *v4* | *v5* | *v6* | *v7* | *v8* | *v9* | *v10* | *v11* | *v12* | *v13* | *IVcc* |
| *xi* | + | - | - | - | - | - | - | - | - | - | - | - | - | - |
| *xf1* | + | - | - | - | + | + | + | + | - | + | - | - | - | + |
| *xf2* | + | - | + | - | - | - | + | + | + | + | + | - | - | - |

Figure 1

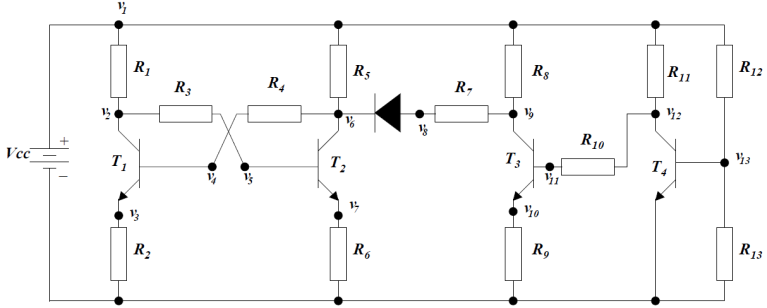
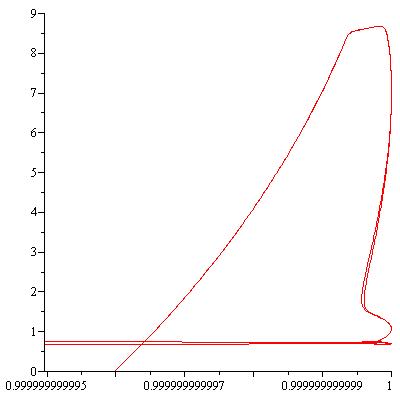
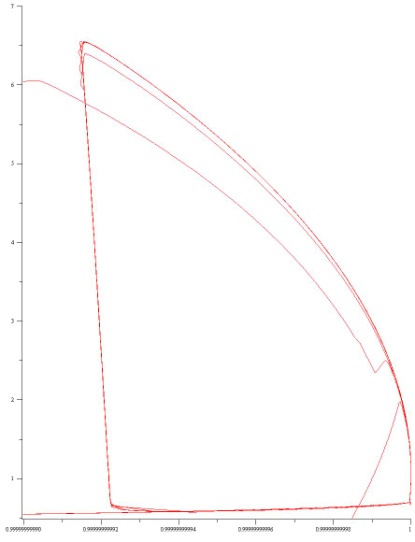


Figure 2



a)



b)