# Practical integrator using operational amplifier

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# 1 Aim

To design, implement and test a $\mu$A741-based voltage integrator.

# Components required

- $\mu$A741 OpAmp
- Resistors R = 120k$\Omega$, 3.3k$\Omega$, 4.7k$\Omega$
- Capacitor C = 0.01 $\mu$F
- Signal generator
- Digital Storage Oscilloscope
- Breadboard
- Jumper wires

## 2 Circuit diagram

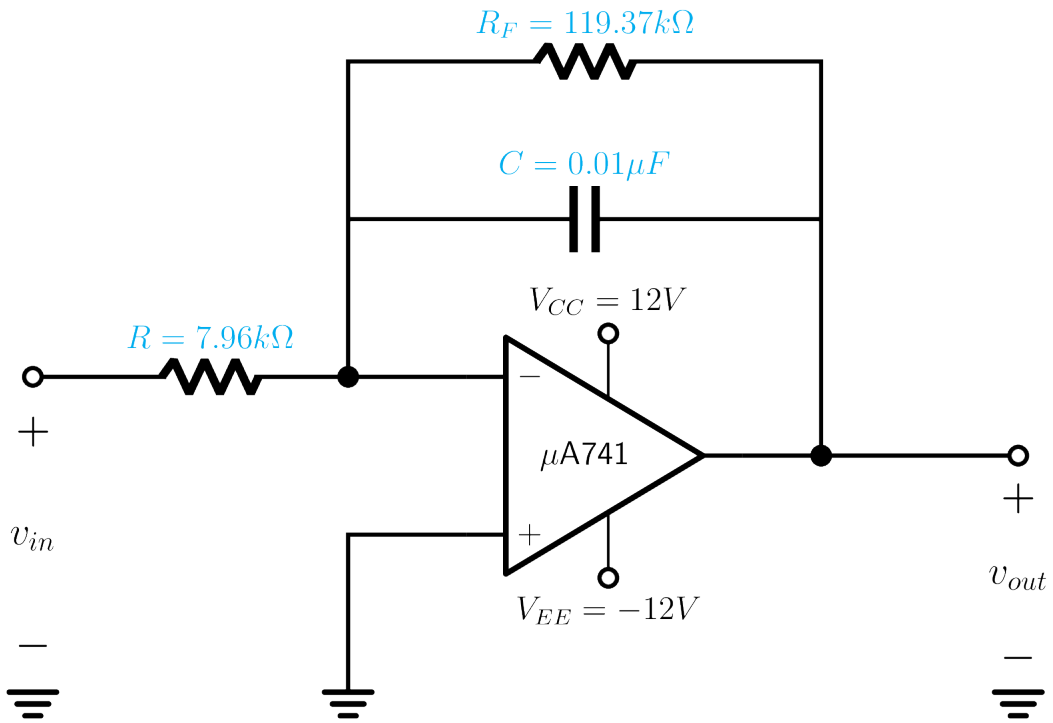



Figure 1: Circuit diagram

# 3 Theory

The operational amplifier based integrator performs the mathematical operation of integration with respect to time, i.e. its output is proportional to the input voltage integrated over time. The integrator circuit is mostly used in analog computers, analog-to-digital converters and wave-shaping circuits such as charge amplifiers.

The response of an opamp circuit with feedback reflects the characteristics of the feedback elements. Thus, in order to achieve integration, the feedback network is constructed using a capacitor.

An operational amplifier based integrator can ideally be constructed as shown in figure 2.

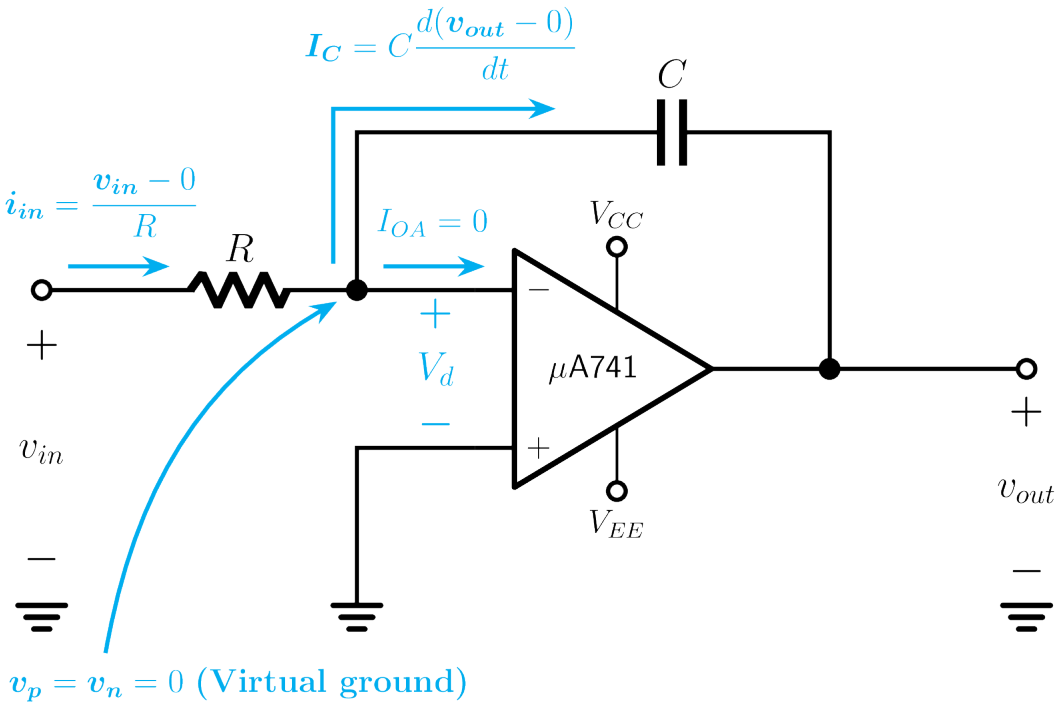



Figure 2: Ideal opamp based integrator

The circuit can be analysed by applying Kirchhoff's current law at the node $V_n$, keeping ideal op-amp behaviour in mind.

$$i_{in} = I_C = \frac{V_{in}}{R} \tag{1}$$

The relationship between between the capacitor's voltage and current is modelled as:

$$I_C = C\frac{dV_C}{dt} \tag{2}$$

Substituting eq. 1 in eq. 2:

$$\frac{v_{in} - 0}{R} = C\frac{d(0 - v_{out})}{dt} \implies \frac{v_{in}}{R} = -C\frac{dv_{out}}{dt}$$

Integrating both sides with respect to time:

$$\int_0^t \frac{v_{in}}{R} = -\int_0^t \frac{dv_{out}}{dt}dt$$

$$v_{out} = -\frac{1}{RC}\int_0^t \frac{dv_{out}}{dt}$$

Thus the output of the circuit shown in figure 2 is the inverted, integrated input with a gain of $\frac{1}{RC}$.

One can overcome the limitations of an ideal integrator by adding a resistor $R_f$ in parallel with capacitor $C$ as shown in figure 3. $R_f$ prevents the opamp from going into open loop configuration at low frequencies.

The resulting circuit is an inverting amplifier with $R_F||\frac{1}{Cs}$ acting as the feedback resistance. The gain of such an amplifier is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{R_F||\frac{1}{Cs}}{R}$$

$$= -\frac{R_F}{R}\frac{1}{(1 + R_F Cs)}$$

Thus, the frequency response of the practical integrator is given by,

$$H(s) = \frac{-R_F||\frac{1}{Cs}}{R} \tag{3}$$

$$H(j\omega) = \frac{-R_F}{R}\left[\frac{1}{1 + R_F Cj\omega}\right] \tag{4}$$

The magnitude and phase response are given by,

$$|H(j\omega)| = \frac{R_F}{R}\frac{1}{\sqrt{1 + \omega^2 R_F^2 C^2}}$$

$$\angle H(j\omega) = \pi - tan^{-1}(\omega R_F C)$$

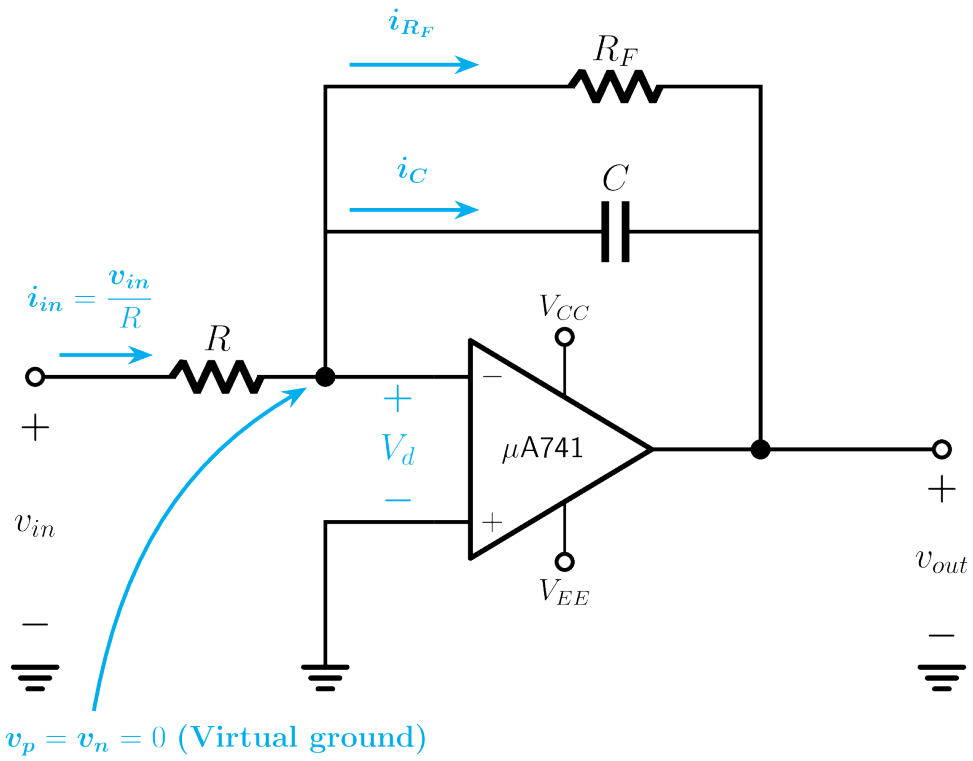



Figure 3: Practical integrator circuit

DC gain is obtained by putting $\omega = 0$ in equation 4.

$$\text{DC gain} = H(j0) = -\frac{R_f}{R} \equiv -20\log_{10}(\frac{R_F}{R}) \text{ dB} \tag{5}$$

Phase shift is given by

$$\phi = \pi - \tan^{-1}(\omega R_F C) \tag{6}$$

$f_{-3dB}$ or cutoff-frequency is given by

$$f_{-3dB} = \frac{1}{2\pi R_F C} \tag{7}$$

$\omega_u$ or unity gain bandwidth is obtained from $|H(j\omega)| = 1$ giving,

$$\omega_u = \frac{1}{RC} \tag{8}$$

Roll-off rate of the frequency response is theoretically -20 dB/decade.

# 4 Design

Q. Design a $\mu$A741 based voltage integrator with unity gain and $f_{-3dB} = f_{in}/15$ for a sinusoidal input $v_{in} = 2sin(4000\pi t)$, keeping the phase error below 5%.

$$\text{Let C} = 0.01\mu F,$$

$$f_{in} = 2000Hz$$

$$f_{-3dB} = \frac{f_{in}}{15} = 133.33Hz$$

$$\frac{1}{2\pi R_F C} = 133.33$$

$$\frac{1}{2\pi RC} = 2000$$

$$R = 7.96k\Omega$$

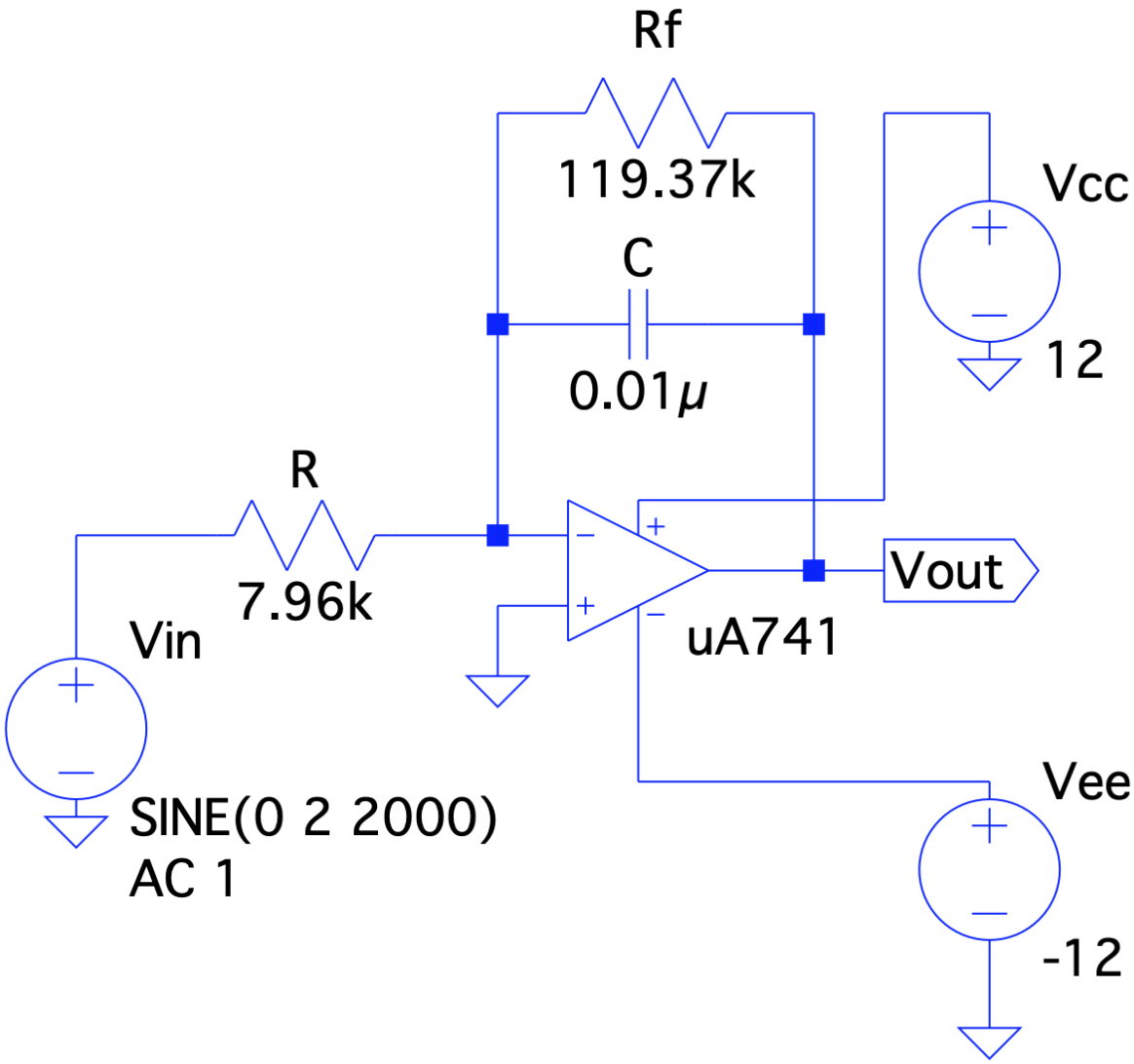
$$R_F = 119.37k\Omega$$

# 5 Calculations

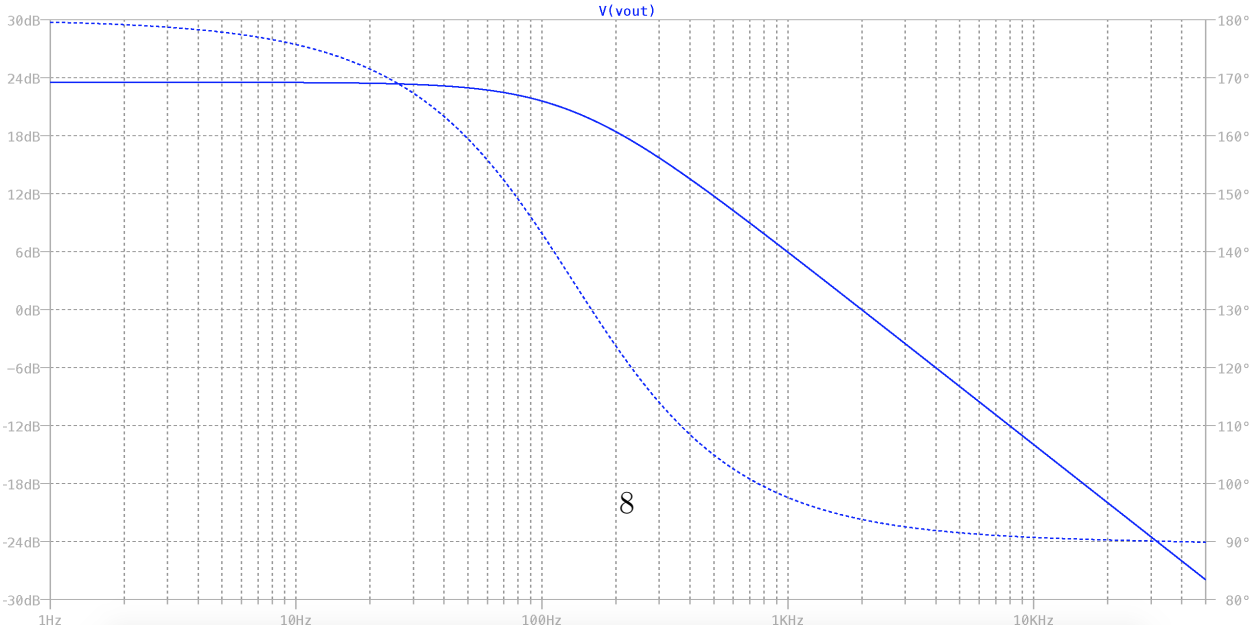
$$\text{Expected DC gain} = \frac{R_f}{R} = 15.25$$

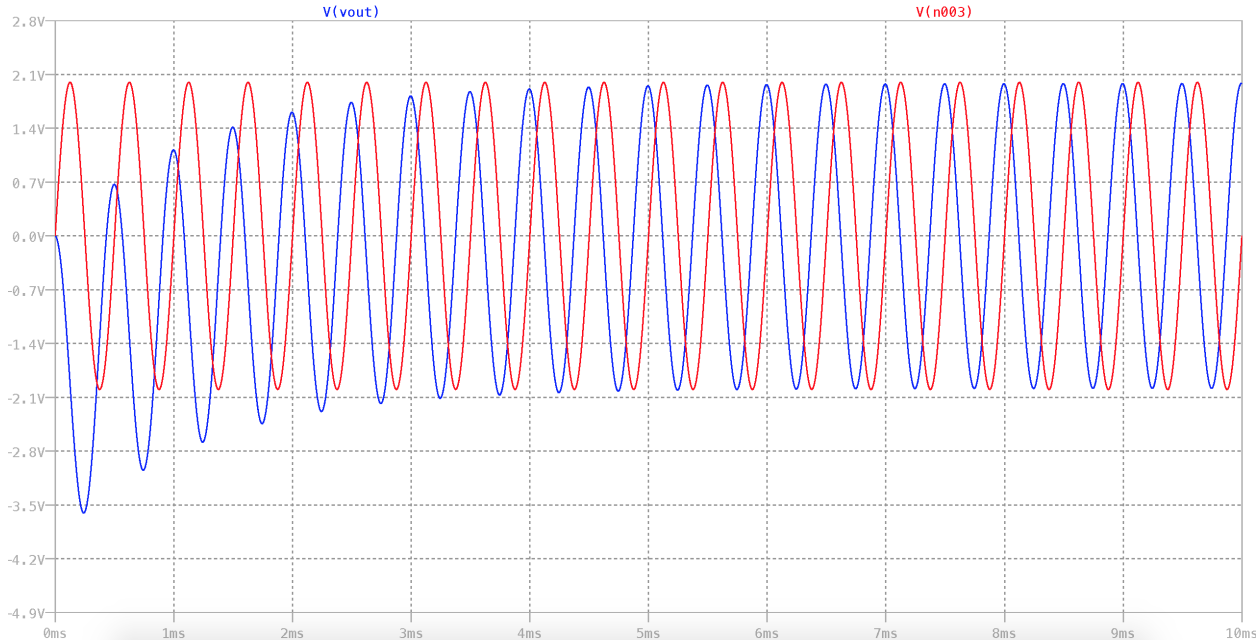
$$\text{Expected phase shift} = \frac{\pi}{2} = 1.57rad$$

# 6 Simulation

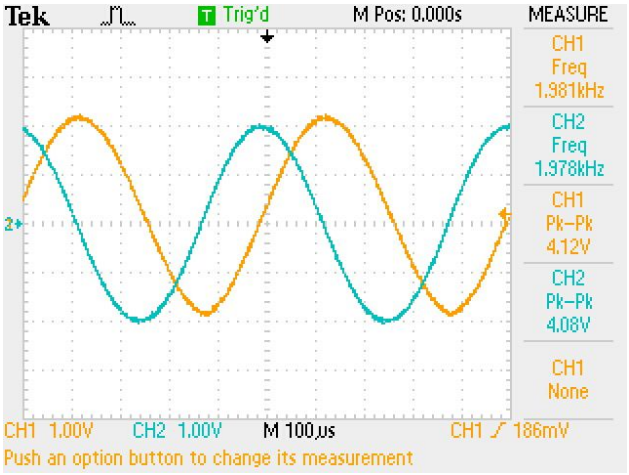


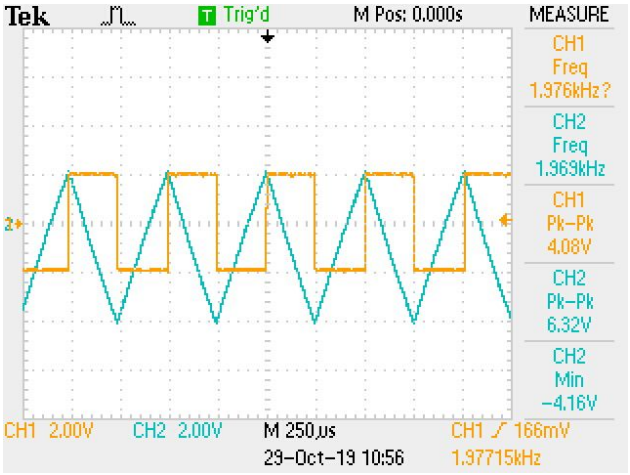

.tran 0.01

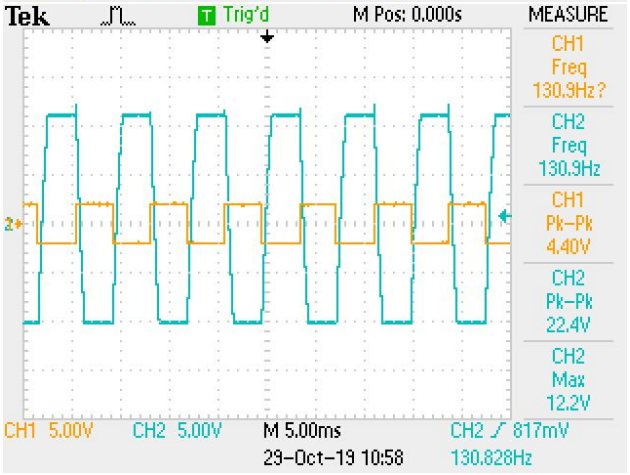



V(vout)
V(n003)
2.8V
2.1V
1.4V
0.7V
0.0V
-0.7V
-1.4V
-2.1V
-2.8V
-3.5V
-4.2V
-4.9V
0ms
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms

# 7 Waveforms


Tek
Trig'd
M Pos: 0.000s
MEASURE
CH1
Freq
1.981kHz
CH2
Freq
1.978kHz
CH1
Pk-Pk
4.12V
CH2
Pk-Pk
4.08V
CH1
None
CH1 1.00V
CH2 1.00V
M 100µs
CH1 ∕ 186mV
Push an option button to change its measurement


Tek
Trig'd
M Pos: 0.000s
MEASURE
CH1
Freq
1.976kHz?
CH2
Freq
1.969kHz
CH1
Pk-Pk
4.08V
CH2
Pk-Pk
6.32V
CH2
Min
-4.16V
CH1 2.00V
CH2 2.00V
M 250µs
CH1 ∕ 166mV
29-Oct-19 10:56
1.97715kHz


Tek
Trig'd
M Pos: 0.000s
MEASURE
CH1
Freq
130.9Hz?
CH2
Freq
130.9Hz
CH1
Pk-Pk
4.40V
CH2
Pk-Pk
22.4V
CH2
Max
12.2V
CH1 5.00V
CH2 5.00V
M 5.00ms
CH2 ∕ 817mV
29-Oct-19 10:58
130.828Hz

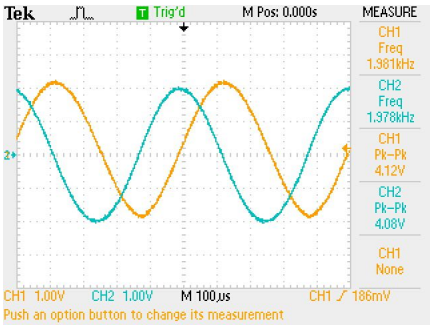



Figure 4: Result of passing a sinusoidal input through the integrator

# 8 Observations

**A**. The practical integrator is first designed based on the following constraints: Unity gain, $f_{-3dB} = f_{in}/15$ for a sinusoidal input $v_{in} = 2sin(4000\pi t)$ and a phase error below 5%.

A leading phase sinusoidal wave appears at the output of the integrator as shown in figure 4. The DC gain, -3dB frequency $f_{3dB}$, unity gain frequency $f_u$, roll-off rate and phase shift are noted from the waveforms obtained on the DSO and the phase error is verified to be below 5%.

DC gain = 14.89

-3dB frequency $f_{-3dB}$ = 132 Hz

Unity gain frequency $f_u$ = 2.07 kHz

Roll-off rate = -18.35 dB/decade

Phase shift $\phi = 1.608^c$ or 92.13°, an error of 2.4%

**B**. The feedback resistor $R_F$ is then removed and the effect on the opamp integrator configuration is observed.

The output is given by $V_{out} = \pm V_{sat}$ due to the capacitor acting as an open circuit at low frequencies as shown in figure 5.This sends the opamp into an open loop configuraton.

**C**. The sinusoidal input is replaced by a square wave of $4V_{pk-pk}$ amplitude and a frequency of 2kHz to observe the integration operation of the configuration more clearly.

A triangular waveform is obtained as a result of the square wave being integrated, as shown in figure 6.

$C\Delta V = I\Delta t$
Substituting $C = 0.01\mu F$, $I = \frac{2}{8k}$, $\Delta t = \frac{0.5}{2000}$,

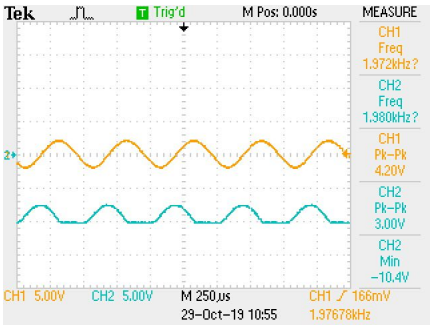



Figure 5: The output of the integrator circuit without $R_F$

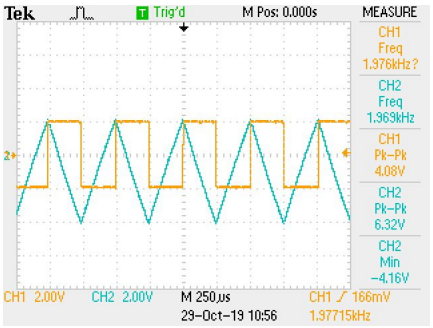



Figure 6: Result of integrating a square wave

$\Delta V = 6.25V$
The output triangular waveform has a peak to peak voltage of around 6.25 V.

D. The frequency of the input is lowered to 130Hz and the output is observed again on the DSO.

$C\Delta V = I\Delta t$
Substituting $C = 0.01\mu F$, $I = \frac{2}{8k}$, $\Delta t = \frac{0.5}{130}$,
$\Delta V = 96.15V$
Since $\Delta V > 2V_{sat}$, $V_{out}$ gets clipped as shown in figure 7.

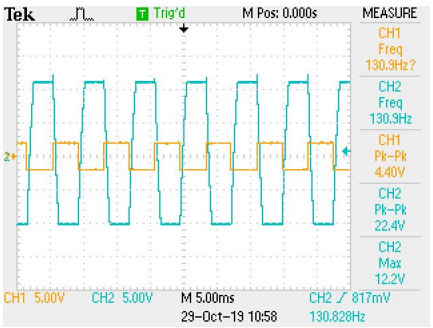



Figure 7: Effect of lowering the input frequency on the output

# 9 Results & Conclusions

The $\mu$A741 based voltage integrator was designed and implemented successfully.