Practical integrator using operational amplifier

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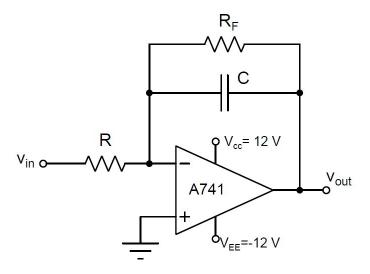


Figure 1: Circuit diagram

1 Aim

To design, implement and test a μ A741-based voltage integrator.

Components required

- μ A741 OpAmp
- Resistors $R = 120k\Omega$, $3.3k\Omega$, $4.7k\Omega$
- Capacitor C = 0.01 μ F
- Signal generator
- Digital Storage Oscilloscope
- Breadboard
- Jumper wires

Circuit diagram

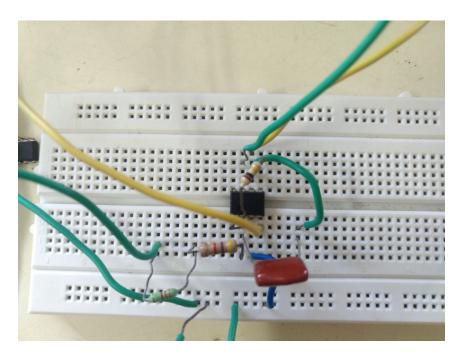


Figure 2: Designed circuit implemented on a breadboard

2 Theory

In an integrator, the output voltage is proportional to the integral of the input. The response of an opamp circuit with feedback will reflect the characteristics of the feedback elements. In order to achieve integration, the feedback network is constructed using a capacitor.

In a practical integrator, one can overcome the limitations of an ideal integrator by adding resistor R_f in parallel with capacitor C. R_f prevents the opamp from going into open loop configuration at low frequencies.

Frequency response of a practical integrator is given by,

$$H(s) = \frac{-R_F || \frac{1}{Cs}}{R} \tag{1}$$

$$H(j\omega) = \frac{-R_F}{R} \left[\frac{1}{1 + R_F C j\omega} \right] \tag{2}$$

The magnitude and phase response are given by,

$$|H(j\omega)| = \frac{R_F}{R} \frac{1}{\sqrt{1 + \omega^2 R_F^2 C^2}}$$
$$\angle H(j\omega) = \pi - \tan^{-1}(\omega R_F C)$$

DC gain is obtained by putting $\omega = 0$ in equation 1.

$$DCgain = H(j0) = -\frac{R_f}{R}$$
(3)

Phase shift is given by

$$\phi = \pi - \tan^{-1}(\omega R_F C) \tag{4}$$

 $\underline{f_{-3dB}}$ or cutoff-frequency is given by

$$f_{-3dB} = \frac{1}{2\pi R_F C} \tag{5}$$

 $\underline{\omega_u}$ or unity gain bandwidth is obtained from $|H(j\omega)|=1$ giving,

$$\omega_u = \frac{1}{RC} \tag{6}$$

Roll-off rate for the frequency response of the practical integrator is theoretically -20 $\frac{dB}{decade}$.

3 Design

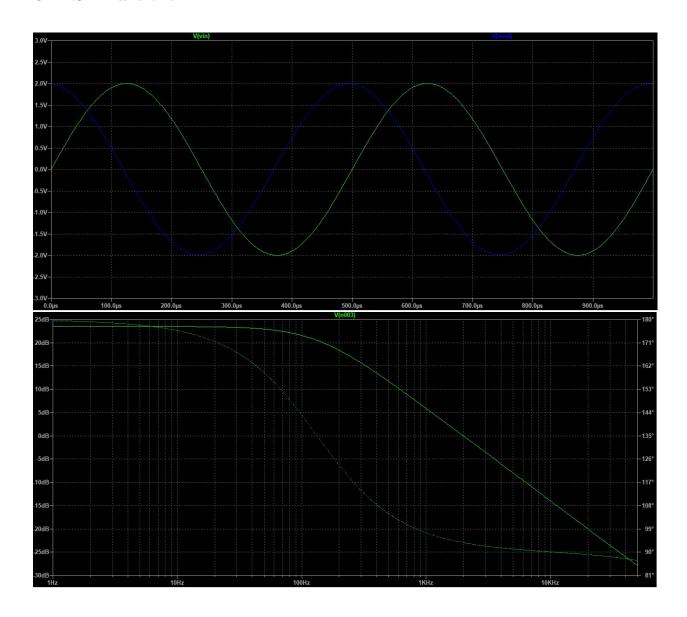
Q. Design a μ A741 based voltage integrator with unity gain and $f_{-3dB} = f_{in}/15$ for a sinusoidal input $v_{in} = 2sin(4000\pi t)$, keeping the phase error below 5%.

Let
$$C = 0.01 \mu F$$
,
 $f_{in} = 2000 Hz$
 $f_{-3dB} = \frac{f_{in}}{15} = 133.33 Hz$
 $\frac{1}{2\pi R_F C} = 133.33$
 $\frac{1}{2\pi RC} = 2000$
 $R = 7.96k\Omega$
 $R_F = 119.37k\Omega$

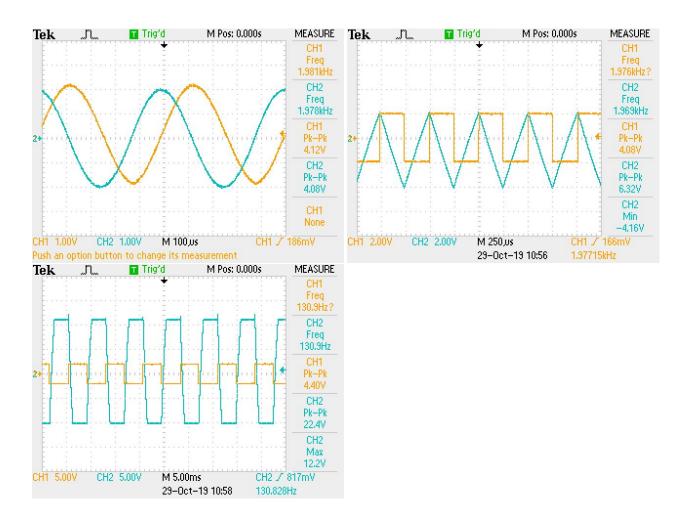
4 Calculations

Expected DC gain =
$$\frac{R_f}{R}$$
 = 15.25
Expected phase shift = $\frac{\pi}{2}$ = 1.57 rad

5 Simulation



6 Waveforms



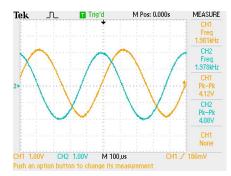


Figure 3: Result of passing a sinusoidal input through the integrator

7 Observations

A. The practical integrator is first designed based on the following constraints: Unity gain, $f_{-3dB} = f_{in}/15$ for a sinusoidal input $v_{in} = 2sin(4000\pi t)$ and phase error below 5%.

A leading phase sinusoidal wave appears at the output of the integrator as shown in figure 3. The DC gain, -3dB frequency f_{3dB} , unity gain frequency f_u , roll-off rate and phase shift are noted from the waveforms obtained on the DSO and the phase error is verified to be below 5%.

DC gain = 14.89-3dB frequency = 132 Hz Unity gain frequency = 2.07 kHz Roll-off rate = -18.35 dB/decade Phase shift = 1.608 rad or 92.13° , an error of 2.4%

B. The feedback resistor R_F is then removed and the effect on the opamp integrator configuration is observed.

The output is given by $V_{out} = \pm V_{sat}$ due to the capacitor acting as an open circuit at low frequencies as shown in figure 4. This sends the opamp into an open loop configuration.

C. The sinusoidal input is replaced by a square wave of $4V_{pk-pk}$ amplitude and a frequency of 2kHz to observe the integration operation of the configuration more clearly.

A triangular waveform is obtained as a result of the square wave being integrated, as shown in figure 5.

$$C\Delta V=I\Delta t$$
 Substituting $C=0.01\mu F,~I=\frac{2}{8k},~\Delta t=\frac{0.5}{2000},$

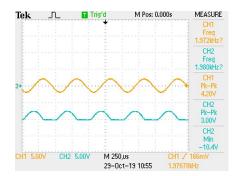


Figure 4: The output of the integrator circuit without R_F

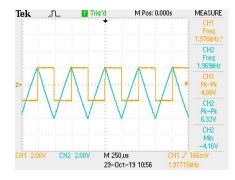


Figure 5: Result of integrating a square wave

$$\Delta V = 6.25V$$

The output triangular waveform has a peak to peak voltage of around 6.25 V.

D. The frequency of the input is lowered to 130Hz and the output is observed again on the DSO.

$$C\Delta V=I\Delta t$$
 Substituting $C=0.01\mu F,\,I=\frac{2}{8k},\,\Delta t=\frac{0.5}{130},\,\Delta V=96.15V$

Since $\Delta V > 2V_{sat}$, V_{out} gets clipped as shown in figure 6.

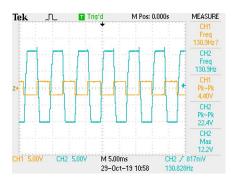


Figure 6: Effect of lowering the input frequency on the output

8 Results & Conclusions

The μ A741 based voltage integrator was designed and implemented successfully.