A Report on
Practical integrators using operational amplifiers

Russel Shawn Dsouza
171EC143

Sathvik S. Prabhu
171EC146

Contents

1   Aim

To design, implement and test a μA741-based voltage integrator.

Components required

- μA741 op-amp
- Resistors R = 120kΩ, 3.3kΩ, 4.7kΩ
- Capacitor C = 0.01 μF
- Signal generator
- Digital Storage Oscilloscope
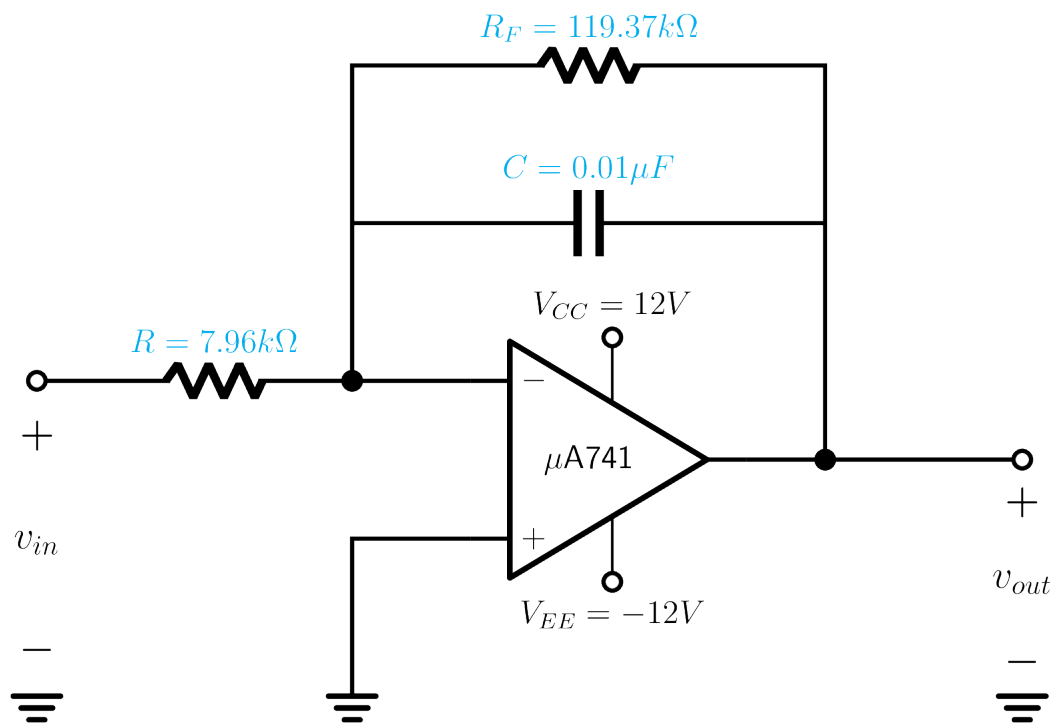- Breadboard
- Jumper wires

2 Circuit diagram

Figure 1: Circuit showing the final design

3   Theory

The operational amplifier based integrator performs the mathematical operation of integration with respect to time, i.e. its output is proportional to the input voltage integrated over time. The integrator circuit is mostly used in analog computers, analog-to-digital converters and wave-shaping circuits such as charge amplifiers.

The response of an op-amp circuit with feedback reflects the characteristics of the feedback elements. Thus, in order to achieve integration, the feedback network is constructed using a capacitor.

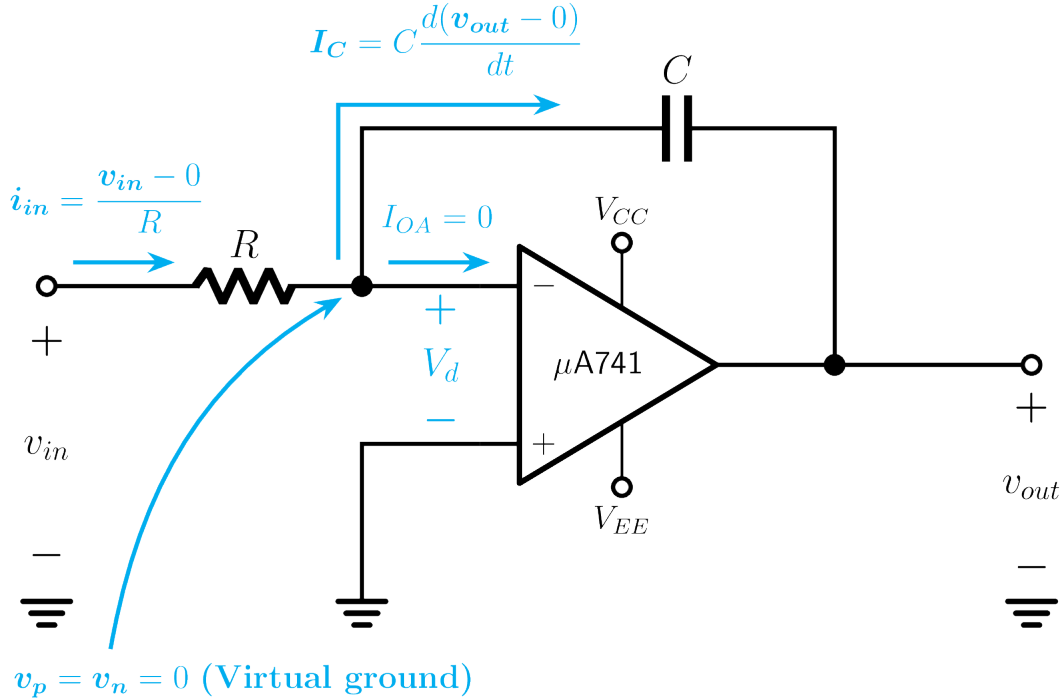An operational amplifier based integrator can ideally be constructed as shown in figure 2.

Figure 2: Ideal op-amp based integrator

The circuit can be analysed by applying Kirchhoff's current law at the node V_n, keeping ideal op-amp behaviour in mind.

$$i_{in} = I_C = \frac{V_{in}}{R} \tag{1}$$

The relationship between between the capacitor's voltage and current is modelled as:

$$I_C = C \frac{dV_C}{dt} \tag{2}$$

Substituting eq. 1 in eq. 2:

$$\frac{v_{in} - 0}{R} = C \frac{d(0 - v_{out})}{dt} \implies \frac{v_{in}}{R} = -C \frac{dv_{out}}{dt}$$

Integrating both sides with respect to time:

$$\int_0^t \frac{v_{in}}{R} = -\int_0^t \frac{dv_{out}}{dt} dt$$

$$v_{out} = -\frac{1}{RC} \int_0^t \frac{dv_{out}}{dt}$$

Thus the output of the circuit shown in figure 2 is the inverted, integrated input with a gain of $\frac{1}{RC}$.

The ideal integrator suffers from two main limitations. One comes from the fact that the output volatage of the op-amp cannot exceed the supply voltage. The output of the integrator is inversely proportional to the time constant $\tau = RC$. The larger the time constant τ, the longer it takes to saturate the integrator. The second limitation is a consequence of the offset voltage present even for zero input. It may be only a few milivolts, but this gets integrated over time and it eventually drives the op-amp to saturation.

One can overcome the limitations of an ideal integrator by adding a resistor R_f in parallel with capacitor C as shown in figure 3. R_f prevents the op-amp from going into open loop configuration at low frequencies.

The resulting circuit is an inverting amplifier with $R_F || \frac{1}{Cs}$ acting as the feedback resistance. The gain of such an amplifier is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{R_F || \frac{1}{Cs}}{R}$$
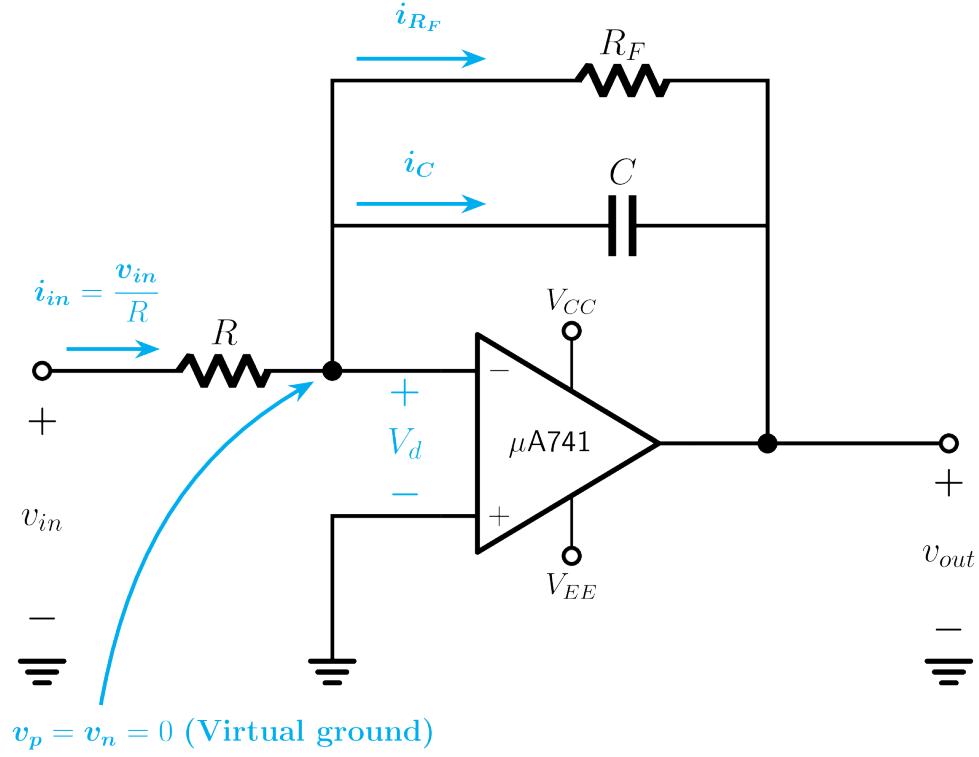
$$= -\frac{R_F}{R} \frac{1}{(1 + R_F C s)}$$

Figure 3: Practical integrator circuit

Thus, the frequency response of the practical integrator is given by,

$$H(s) = \frac{-R_F||\frac{1}{Cs}}{R} \tag{3}$$

$$H(j\omega) = \frac{-R_F}{R}\left[\frac{1}{1 + R_F C j\omega}\right] \tag{4}$$

The magnitude and phase response are given by,

$$|H(j\omega)| = \frac{R_F}{R}\frac{1}{\sqrt{1 + \omega^2 R_F^2 C^2}}$$

$$\angle H(j\omega) = \pi - tan^{-1}(\omega R_F C)$$

DC gain is obtained by putting $\omega = 0$ in equation 4.

$$\text{DC gain} = H(j0) = -\frac{R_f}{R} \equiv -20\log_{10}(\frac{R_F}{R}) \text{ dB} \tag{5}$$

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Phase shift $\Delta\phi$ between the input and output signals is given by

$$\Delta\phi = \pi - \tan^{-1}(\omega R_F C) \tag{6}$$

The practical integrator acts as a first order filter with corner frequency (also cut-off or pole frequency) at $f = -1/R_F C$. Thus, f_{-3dB} or cutoff-frequency is given by

$$f_{-3dB} = \frac{1}{2\pi R_F C} \tag{7}$$

Unity gain bandwidth ω_u is obtained from $|H(j\omega)| = 1$:

$$H(j\omega) = 1 = \frac{R_F}{R} \frac{1}{\sqrt{1 + \omega^2 R_F^2 C^2}}$$

$$\left(\frac{R_F}{R}\right)^2 = 1 + (\omega R_F C)^2$$

$$\left(\frac{R_F}{R}\right)^2 \approx (\omega R_F C)^2 \qquad\qquad \left(\text{for } \frac{R_F}{R} \gg 1\right)$$

$$\implies \omega_u = \frac{1}{RC} \text{ or } f_u = \frac{1}{2\pi RC} \tag{8}$$

Roll-off rate of the frequency response is theoretically -20 dB/decade.

4 Design

The practical integrator is designed for the following constraints

(a) Unity gain

(b) $v_{in} = 2sin(4000\pi t)$

(c) $f_{-3dB} = \dfrac{f_{in}}{15}$

(d) Phase error tolerance of 5%

The provided input is $v_{in} = 2sin(4000\pi t)$ which can be compared with the general equation for sinusoidal waveforms $Asin(2\pi ft)$ to obtain $f_{in} = 2000\text{Hz}$.

From the constraint list the value of f_{-3dB} is obtained as:

$$f_{-3dB} = \frac{f_{in}}{15} \implies f_{-3dB} = 133.33\text{Hz}$$

Using equation 7, and assuming $C = 0.01\mu F$, the value of R_F comes out to be:

$$f_{-3dB} = \frac{1}{2\pi R_F C}$$

$$R_F = \frac{1}{2\pi f_{-3dB} C}$$

$$= \frac{1}{2\pi \times 133.33 \times 0.01 \times 10^{-6}}$$

$$= 119.37k\Omega \approx 120k\Omega$$

From the unity gain constraint, the output has to have the same amplitude as the input at $f_in = 2000\text{Hz}$. Using equation 8, the value of R comes out to be:

$$f_u = \frac{1}{2\pi RC}$$

$$R = \frac{1}{2\pi f_u C}$$

$$= \frac{1}{2\pi \times 2000 \times 0.01 \times 10^{-6}}$$

$$= 7.96k\Omega \approx 8k\Omega$$

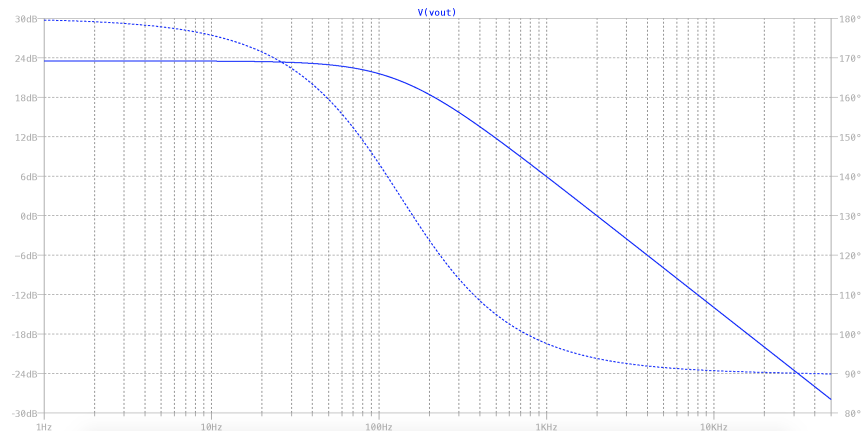# 5   LTSpice simulation and results[1]

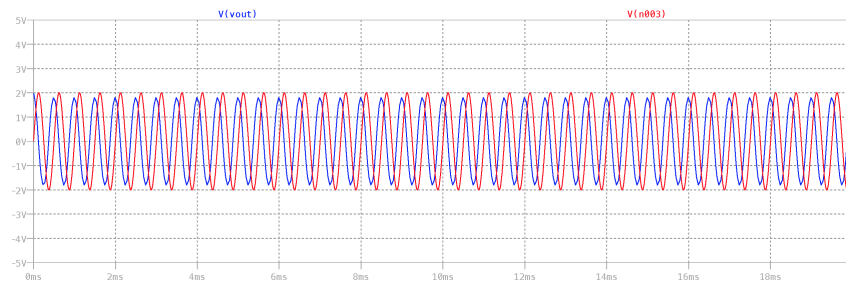Figure 4: Phase and magnitude response of the practical integrator output

Figure 5: V_{out} and V_{in} in time domain

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[1]The .asc file containing the LTSpice schematic can be found at github.com/rshwndsz/aic-report.

6 Observations

A. The practical integrator is first designed based on the following constraints: Unity gain, $f_{-3dB} = f_{in}/15$ for a sinusoidal input $v_{in} = 2sin(4000\pi t)$ and a phase error below 5%.

A leading phase sinusoidal wave appears at the output of the integrator as shown in figure 6. The DC gain, -3dB frequency f_{3dB}, unity gain frequency f_u, roll-off rate and phase shift are noted from the waveforms obtained on the DSO and the phase error is verified to be below 5%.
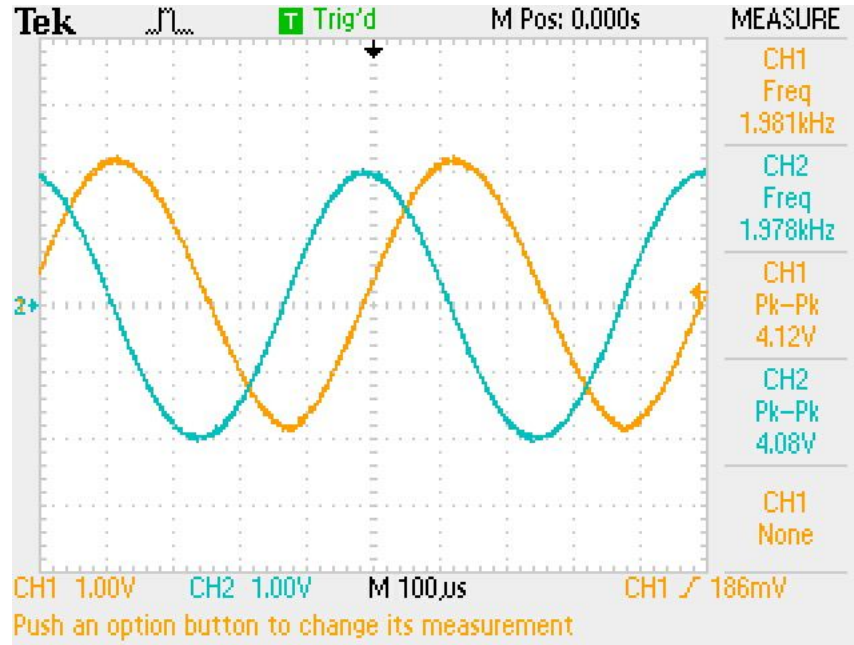

Figure 6: Result V_{out} of passing a sinusoidal input V_{in} through the integrator.

The observed parameters are listed below.

DC gain $= 14.89$

-3dB frequency $f_{-3dB} = 132$ Hz

Unity gain frequency $f_u = 2.07$ kHz

Roll-off rate $= -18.35$ dB/decade

Phase shift $\phi = 1.608^c$ or $92.13°$, an error of 2.4%

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B. The feedback resistor R_F is then removed and the effect on the op-amp integrator configuration is observed.
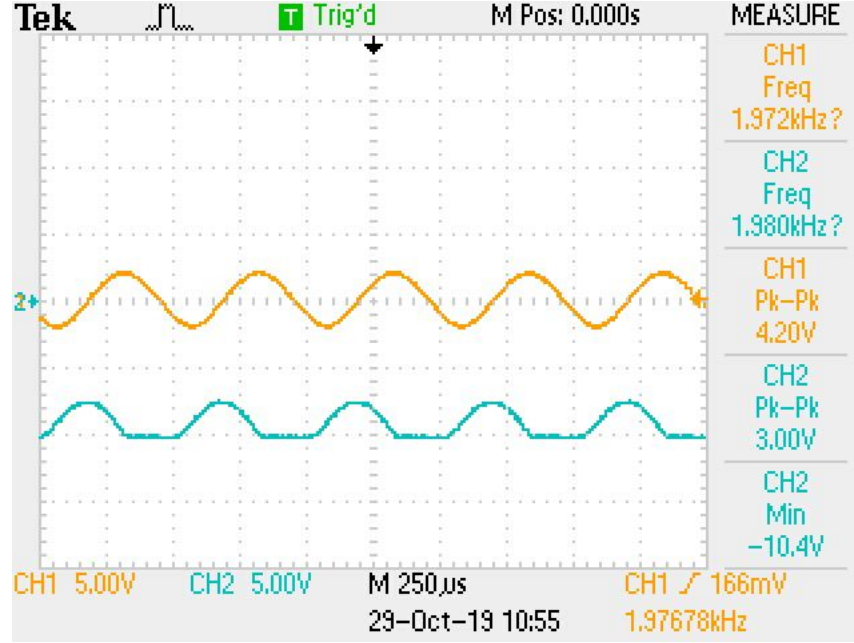

Figure 7: The output V_{out} of the integrator circuit without R_F

The output is given by $V_{out} = \pm V_{sat}$ as the capacitor acts as an open circuit at low frequencies as shown in figure 7. This sends the op-amp into an open loop configuraton.

C. The sinusoidal input is replaced by a square wave of $4V_{pk-pk}$ amplitude and a frequency of 2kHz to observe the integration operation of the configuration more clearly.

A triangular waveform is obtained as a result of the square wave being integrated, as shown in figure 8.

The peak-to-peak amplitude of the output can be obtained by using the relation

$$C\Delta V = I\Delta t$$

Substituting $C = 0.01\mu F$, $I = \dfrac{2}{8 \times 10^3}$, $\Delta t = \dfrac{0.5}{2000}$,

$$\Delta V = 6.25V$$

The output triangular waveform has a peak to peak voltage of around 6.25 V.

D. The frequency of the input is lowered to 130Hz and the output is observed again.

Using, $C\Delta V = I\Delta t$ and substituting $C = 0.01\mu F$, $I = \dfrac{2}{8 \times 10^3}$, $\Delta t = \dfrac{0.5}{130}$, we get:

$$\Delta V = 96.15V$$

Since $\Delta V > 2V_{sat}$, V_{out} gets clipped as shown in figure 9.
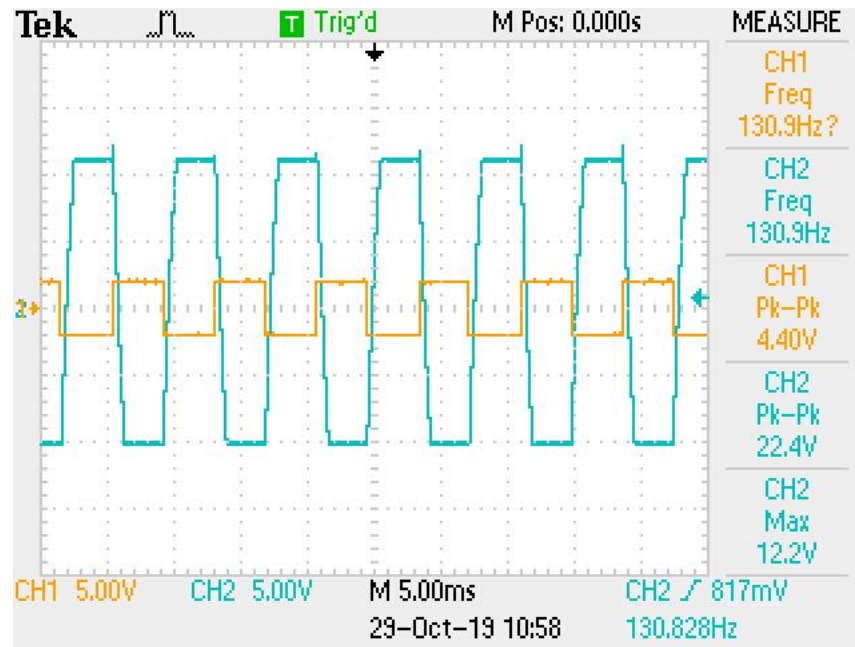
Figure 8: Effect of lowering the input frequency on the output V_{out} & V_{in}
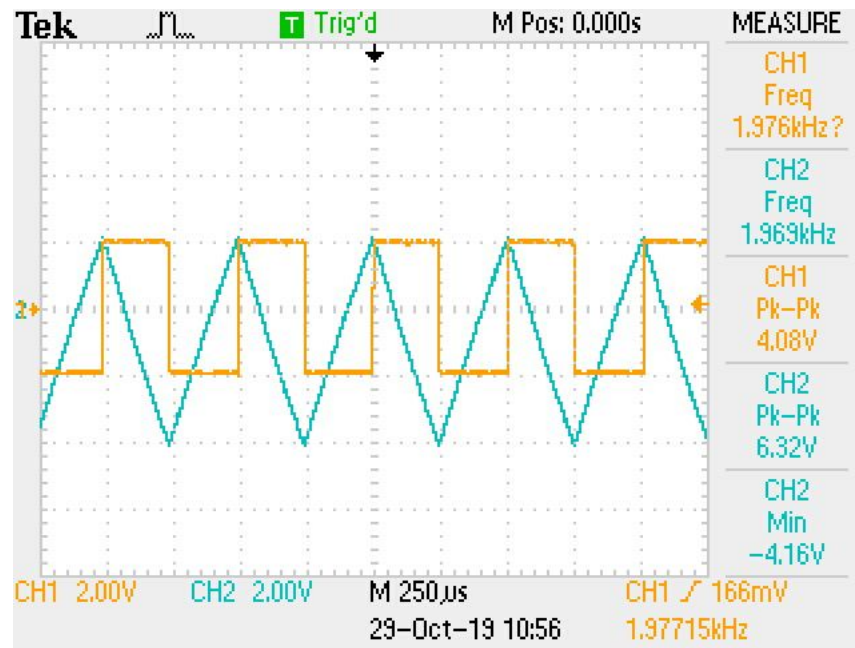

Figure 9: Result of integrating a square wave V_{out} & V_{in}

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7   Results & Conclusions

The μA741 based voltage integrator was designed and implemented successfully.