GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO. 609
TO BE ANSWERED ON: 06.02.2019

WAFER FABRICATION FACILITY

609. SHRI ALOK SANJAR:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be please to state:-
(a) whether the Government proposes to set up semiconductor wafer fabrication manufacturing facilities in the country;
(b) if so, the details thereof;
(c) whether the Government has taken any step to promote manufacturing of semiconductor wafer in the country; and
(c) if so, the details thereof?

ANSWER
MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI S.S. AHLUWALIA)

(a): No, Sir.
(b): Does not arise.

(c) and (d): Based on the recommendations of the Empowered Committed (EC) constituted for the purpose of setting up of Semiconductor Wafer Fabrication (FAB) manufacturing facilities in the country, Government had approved two proposals for setting up of Semiconductor Wafer Fabrication (FAB) facility in India - one from the consortium led by M/s. HSMC Technologies India Pvt. Ltd. and the other from consortium led by M/s. Jaiprakash Associates Ltd. Letter of Intent (LoI) dated 19.03.2014 were issued to both the consortia. As per the LoI, both the consortia were required to submit the documents for demonstration of commitment. The consortium led by M/s. Jaiprakash Associates Ltd., withdrew the proposal on 02.03.2016, whereas the consortium led by M/s. HSMC Technologies India Pvt. Ltd. could not submit the requisite documents as per the LoI, despite being provided extension of time on multiple occasions. Therefore, LoI issued to the consortium led by M/s. HSMC Technologies India Pvt. Ltd. was cancelled on 20.04.2018.

Besides the above, in order to attract investment for setting up semiconductor FAB facilities in the country, capital subsidy of 25% of Capex for units set up in Domestic Tariff Area (DTA) and 20% of Capex for units set up in Special Economic Zones (SEZs) was available under the Modified Special Incentive Package Scheme (M-SIPS). The scheme was open to receive applications till 31.12.2018. However, no proposal has been received for setting up semiconductor FAB facilities in the country under M-SIPS.

Following benefits continue to be available for promoting investment in setting up semiconductor FAB facilities in the country:
(i) Machinery, electrical equipment, other instruments and their parts except populated Printed Circuit Boards for use in fabrication of semiconductor wafer are exempted

from Basic Customs Duty (BCD) vide S.No.422 of Notification No.50/2017-Customs dated 30.06.2017, as amended from time to time.

(ii) Investment linked deduction under Section 35AD of the Income-tax Act has been extended to semiconductor wafer fab manufacturing unit.

(iii) Deduction of expenditure on research and development as admissible under Section 35(2AB) of the Income-tax Act.

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