GOVERNMENT OF INDIA
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
LOK SABHA
UNSTARRED QUESTION NO. 1803
TO BE ANSWERED ON: 13.02.2019

CHIP MANUFACTURING

1803. SHRI L.R. SHIVARAME GOWDA:
SHRIMATI ANJU BALA:
SHRI TEJ PRATAP SINGH YADAV:

Will the Minister of ELECTRONICS AND INFORMATION TECHNOLOGY be please to state:-
(a) whether the Government is planning to invest in the chip manufacturing facilities to be set up in States and if so, the details thereof;
(b) whether consortium of manufacturing firms have withdrawn to set up Semiconductor Wafer Fabrication units and if so, the reasons therefor;
(c) whether the Government has received chip design manufacturing proposals from various global companies and if so, the details thereof; and
(d) the steps taken by the Government to boost the chip manufacturing in the country and cut down the imports?

ANSWER
MINISTER OF STATE FOR ELECTRONICS AND INFORMATION TECHNOLOGY
(SHRI S.S. AHLUWALIA)

(a): No, Sir.

(b): Based on the recommendations of the Empowered Committed (EC) constituted for the purpose of setting up of Semiconductor Wafer Fabrication (FAB) manufacturing facilities in the country, Government had approved two proposals for setting up of Semiconductor Wafer Fabrication (FAB) facility in India - one from the consortium led by M/s. HSMC Technologies India Pvt. Ltd. and the other from consortium led by M/s. Jaiprakash Associates Ltd. Letter of Intent (LoI) dated 19.03.2014 were issued to both the consortia. As per the LoI, both the consortia were required to submit the documents for demonstration of commitment. The consortium led by M/s. Jaiprakash Associates Ltd., withdrew the proposal on 02.03.2016, *inter-alia* conveying that the exchange rates in US $ / ₹ term has gone up by about 12% already over the last two years, even before the commencement of physical implementation, adversely affecting the total capital outlay for the project. Additionally, M/s. Jaiprakash Associates Ltd. conveyed that the viability of the project became questionable due to prevailing conditions in the country and the global scenario which indicated that the trend was likely to continue in the same pattern.

As regards the consortium led by M/s. HSMC Technologies India Pvt. Ltd., they could not submit the requisite documents for demonstration of commitment, as per the LoI, despite being provided extension of time on multiple occasions. Therefore, LoI issued to the consortium led by M/s. HSMC Technologies India Pvt. Ltd. was cancelled on 20.04.2018.

(c): In order to attract investment for setting up semiconductor FAB facilities in the country, capital subsidy of 25% of Capex for units set up in Domestic Tariff Area (DTA) and 20% of Capex for units set up in Special Economic Zones (SEZs) was available under the Modified Special Incentive Package Scheme (M-SIPS). The scheme was open to receive applications till 31.12.2018. However, no proposal has been received for setting up semiconductor FAB facilities in the country under M-SIPS.

(d): Following steps have been taken by the Government to boost the chip manufacturing in the country:

(i) Machinery, electrical equipment, other instruments and their parts except populated Printed Circuit Boards for use in fabrication of semiconductor wafer are exempted from Basic Customs Duty (BCD) vide S.No.422 of Notification No.50/2017-Customs dated 30.06.2017, as amended from time to time.

(ii) Investment linked deduction under Section 35AD of the Income-tax Act has been extended to semiconductor wafer fab manufacturing unit.

(iii) Deduction of expenditure on research and development as admissible under Section 35(2AB) of the Income-tax Act.

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