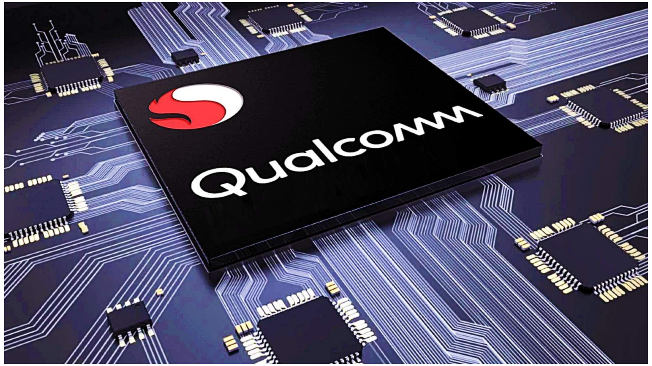
UC San Diego

Qualcomm Capstone

Contents

Qualcomm Background

- Founded in 1985 and headquartered in San Diego, California
- World leader in the development and commercialization of foundational technologies for the wireless industry, specifically semiconductors
- Helped shape modern smartphone era and driving advancements in areas like Internet of Things, automotive technology, and AI



Project Overview

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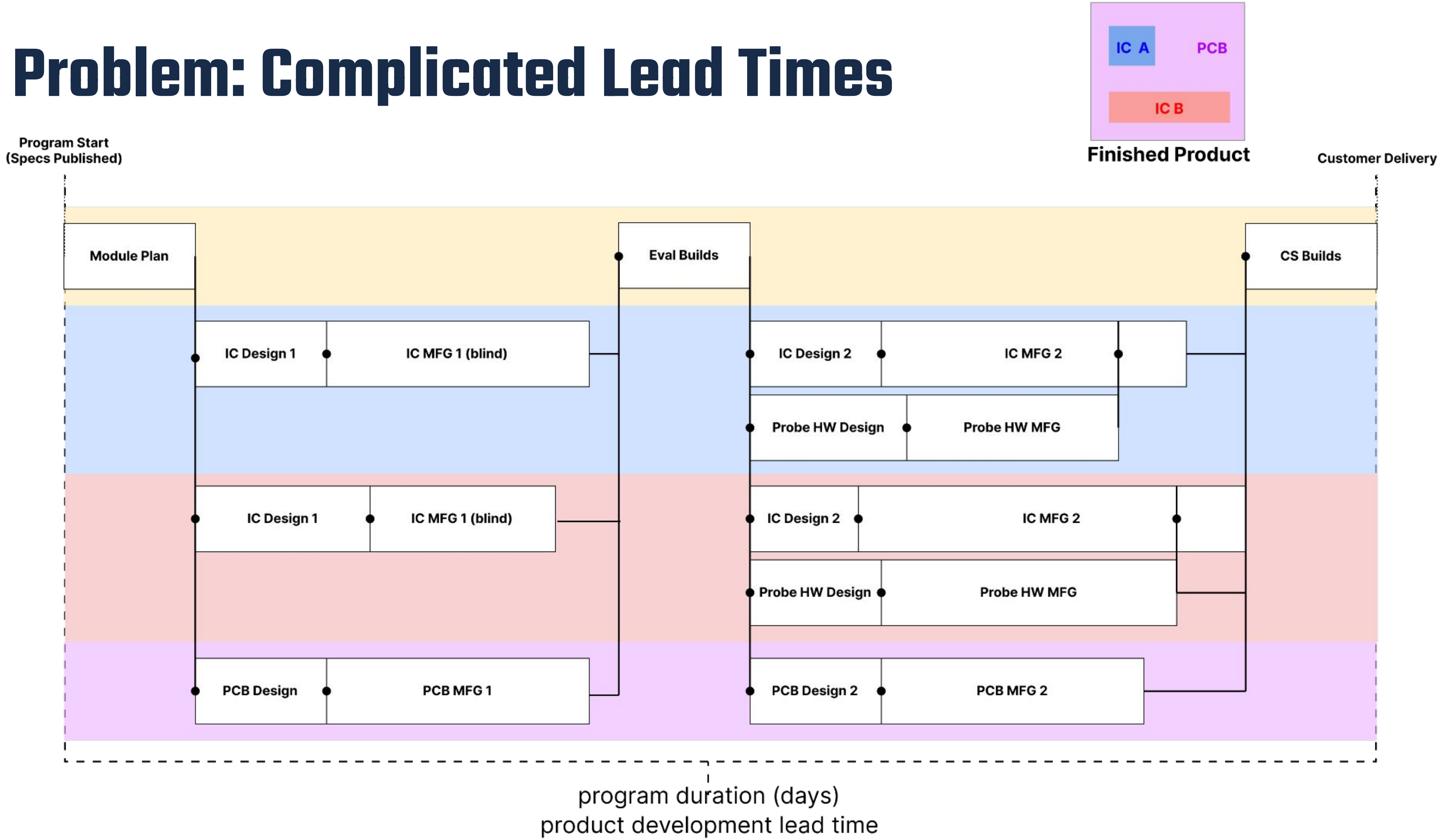
Problem Statement

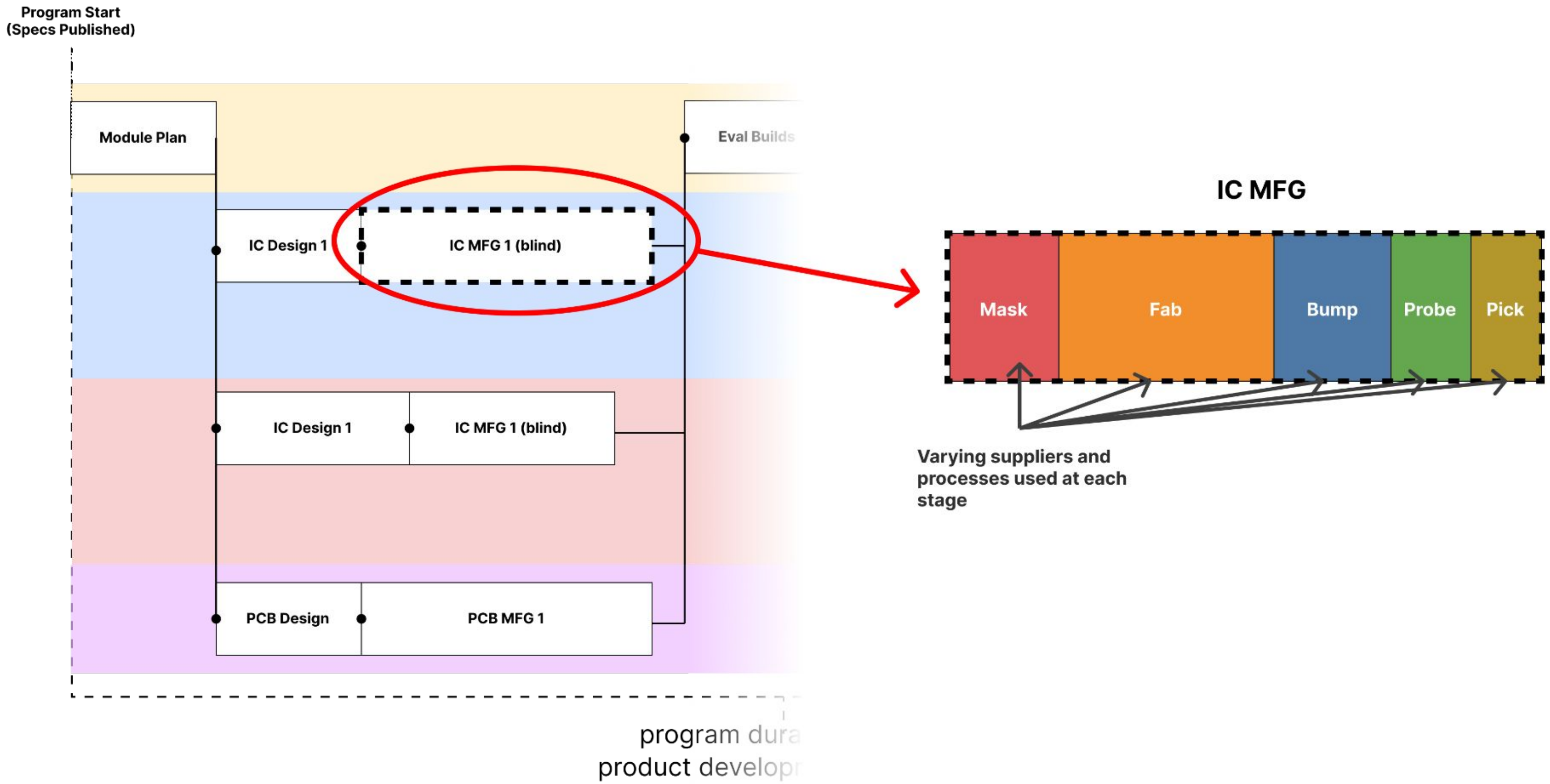
Qualcomm's product development teams currently rely heavily on intuition-based planning, leading to potential inaccuracies in timeline estimates and and inefficient resource allocation.

The goal is to create a data-driven model that predicts development cycle times with greater accuracy, enabling proactive decision-making and improving time-to-market for new semiconductor products.

Problem: Complicated Lead Times

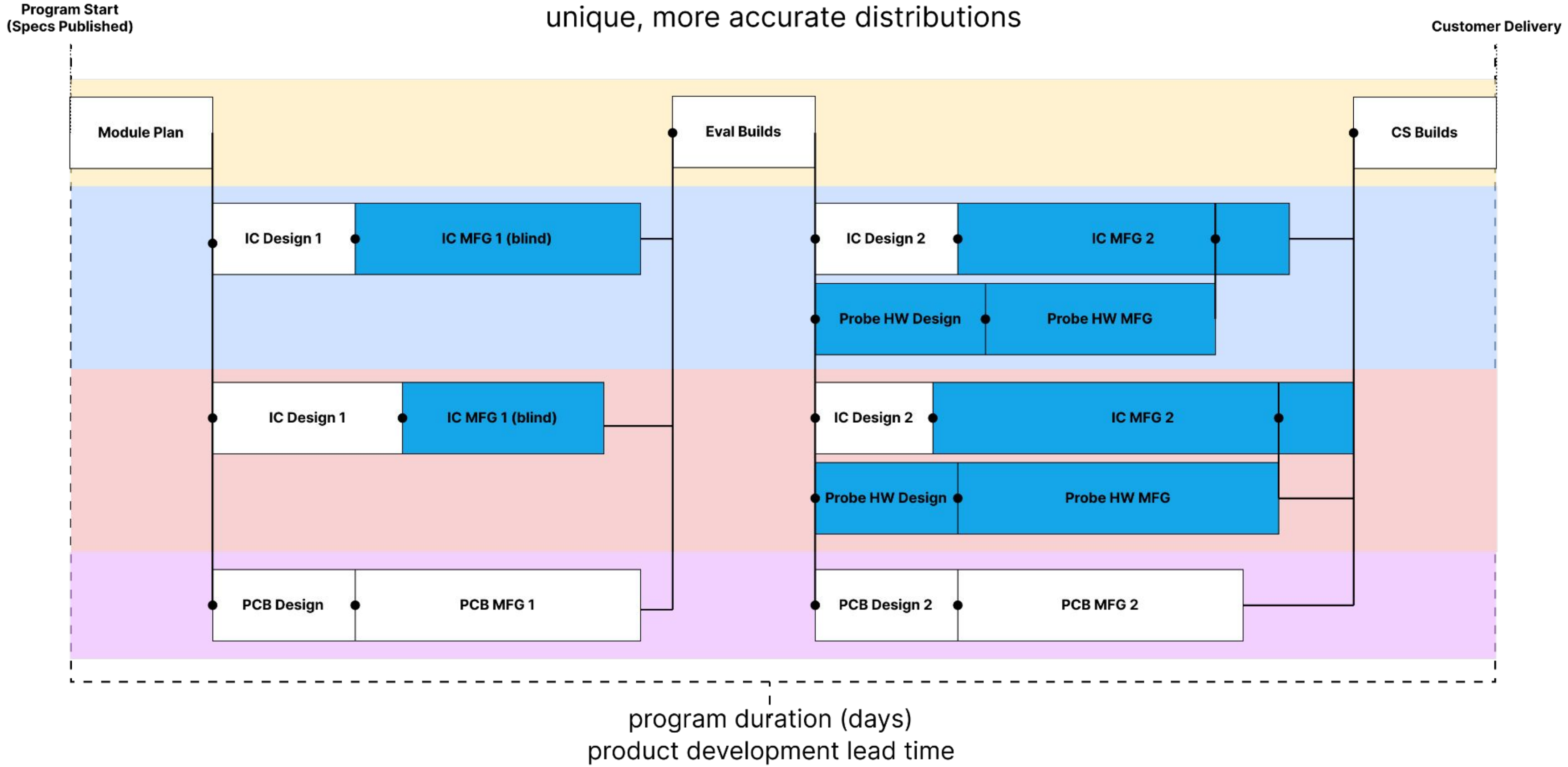


Challenge: Lots of Subcycles and Variation

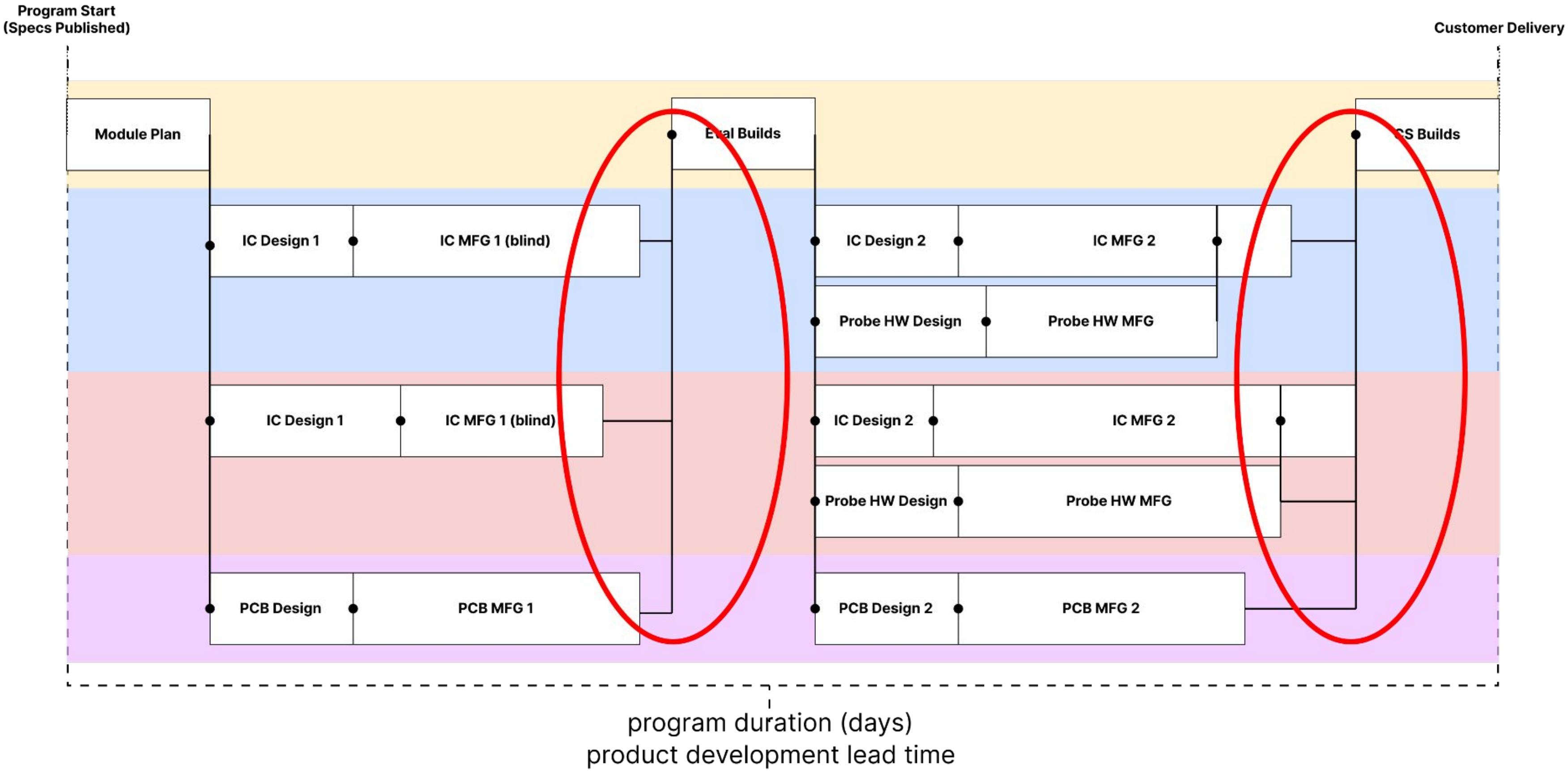


Challenge: Dynamic Simulation

Pass through changing device and supplier parameters to pick from unique, more accurate distributions



Challenge: Changing Critical Paths



Solution Design Overview

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Objective:

- Estimate development lead time for semiconductor module products using a Python-based simulation model.

Key Solution Features:

- Simulate lead time using stacked probabilities from various cycle times.
- Output: Probability distribution of development duration and sensitivity analysis.

Benefits:

- Provides accurate estimates for lead times.
- Highlights bottlenecks and high-risk areas.
- Informs better decisions to optimize product development.

Methodology & Workflow

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Data Preparation

- Clean historical datasets for tasks, lead times, and dependencies
- Exploratory analysis, familiarity with the data

Simulation Framework:

- Test different predictive models
- Tasks modeled with probabilistic distributions
- Directed Acyclic Graphs (DAG) for dependencies that show a defined direction for the procedures

User Interaction:

- GUIs where created to allow the user to input desired deadlines and measure the probabilities of meeting them

Exploratory Data Analysis

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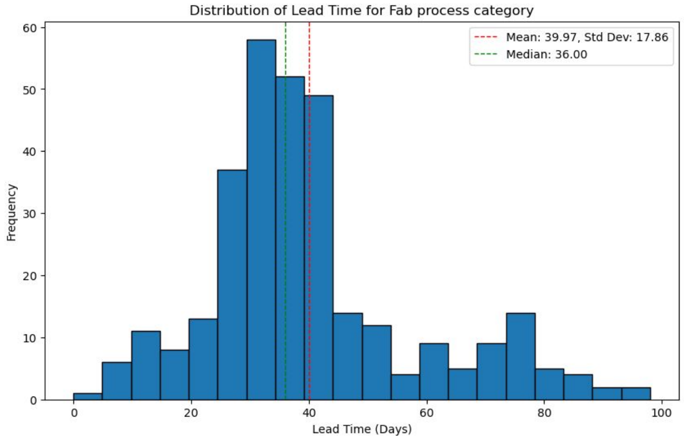
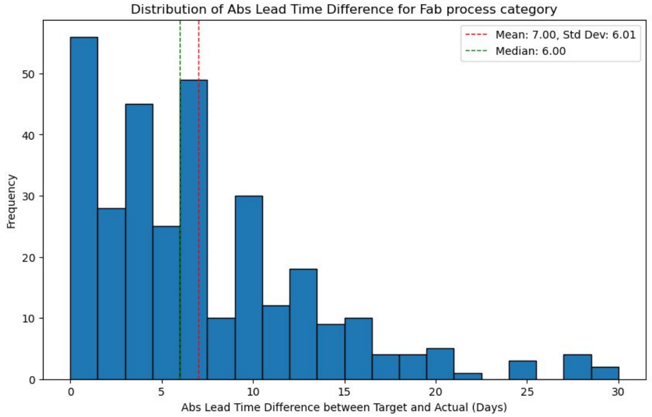
- Visualized Lead time (dependent variable) and lead time difference (Target vs Actual) against features
  - Lead time difference absolute value also reviewed

- 4 Process Categories:
  - Maskset
  - Fabrication
  - Bump
  - DPS

- Fabrication process had largest mean and standard deviation for lead time and lead time difference





Predictive Model

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Goal: Simulation to recommend timelines and determine feasibility

- Bayesian Ridge selected: output includes mean and SD

End State
- Predictive model not used due to inaccuracy compared to historical grouping distributions

Model Type	R^2
Linear	0.80
Random Forest	0.86
Bayesian Ridge	0.80

$$\text{Simulated Cycle Time} \sim \mathcal{N}(\hat{y}_{\text{mean}}, \hat{y}^2_{\text{std}})$$

Historical Data (mean, std) — Predictive Model (pred_mean, pred_std_dev)

	site	platform	stage	expedite	wafertype	mean	std	count	pred_mean	pred_std_dev
0	site_2	platform_1	maskset	nl	spw	12.625000	2.714021	56	17.192267	6.287239
1	site_2	platform_1	fab	shl	spw	37.878049	4.411321	41	17.192267	6.287239
2	site_3	platform_1	dps	shl	spw	5.600000	2.206573	30	16.941030	6.416689
3	site_1	platform_1	bump	nl	spw	10.758621	5.110599	29	15.634206	6.333009
4	site_16	platform_8	maskset	nl	mpw >10 variants	8.272727	2.271601	22	9.335825	6.297020

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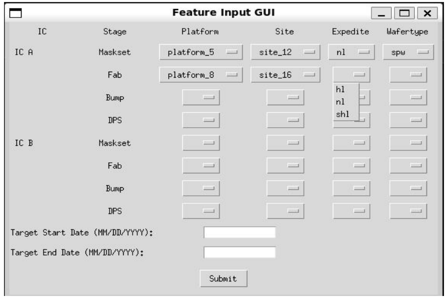
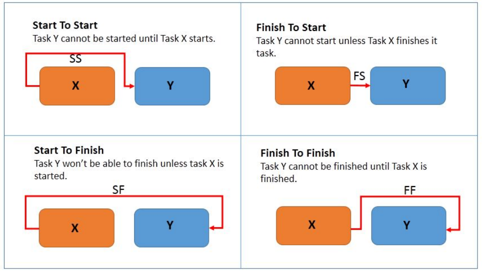
Deliverables and Progress

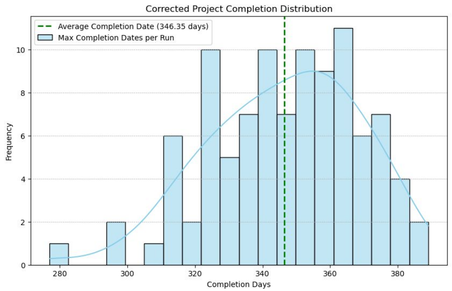
1 GUI for user input



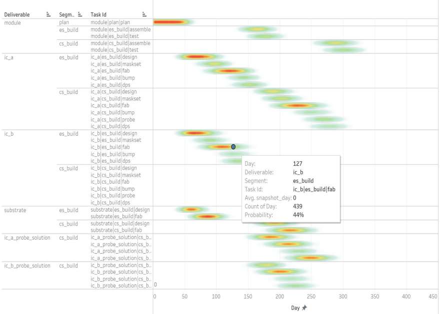
2 Data Structure and Task Dependencies



3 Monte Carlo Simulation Model



4 Tableau Dashboard for dynamic visualizations

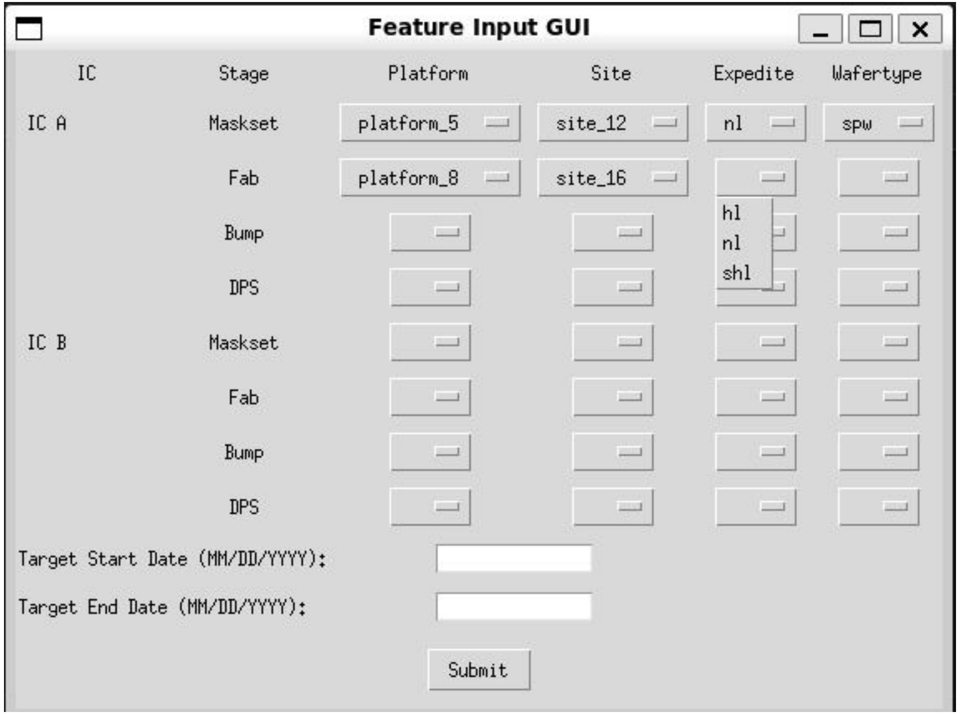


Dashboard/GUI Development

Purpose: Allows users to easily select the task features for each stage of the IC Manufacturing Build phases

- Dynamic Filtering of subsequent features based user selections and historical data

- Error Messages for incomplete or invalid field inputs



Data Structure

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The purpose of structuring the data allows to connect all key data needed for simulations, like task details, timelines, and dependencies.

Historical Data:

- Stores information like task durations, wafer counts, and priority levels.
- Tracks how actual lead times compare to targets to highlight variability.

Task Dependencies:

- Uses a Directed Acyclic Graph (DAG) to show how tasks depend on each other.
- Includes parallel workflows (e.g., IC A, IC B, PCB) to reflect real manufacturing processes.

Relational Database:

- Links tasks, workflows, and dependencies in a single system.
- Helps identify critical paths and bottlenecks.

How It Helps:

- Ensures simulations use clean, well-structured data.
- Adapts to new inputs, like deadlines or task priorities, for flexible planning.
- Supports tools like Gantt charts to visualize workflows.

Simulation

Key features include:

Probabilistic Task Durations

- Using historical data to model durations, provide variability and probabilities

Task Dependencies

- Simulates the workflow and ensures task follow their logical order

Predictions

- Improvement is seen as completed tasks reduce uncertainty for the remaining tasks and stages

Takeaways

- Identification of bottlenecks in those stages with high variability (like DPS and FAB)
- Probability distribution of meeting deadlines, enabling “what if “ scenarios

Simulation

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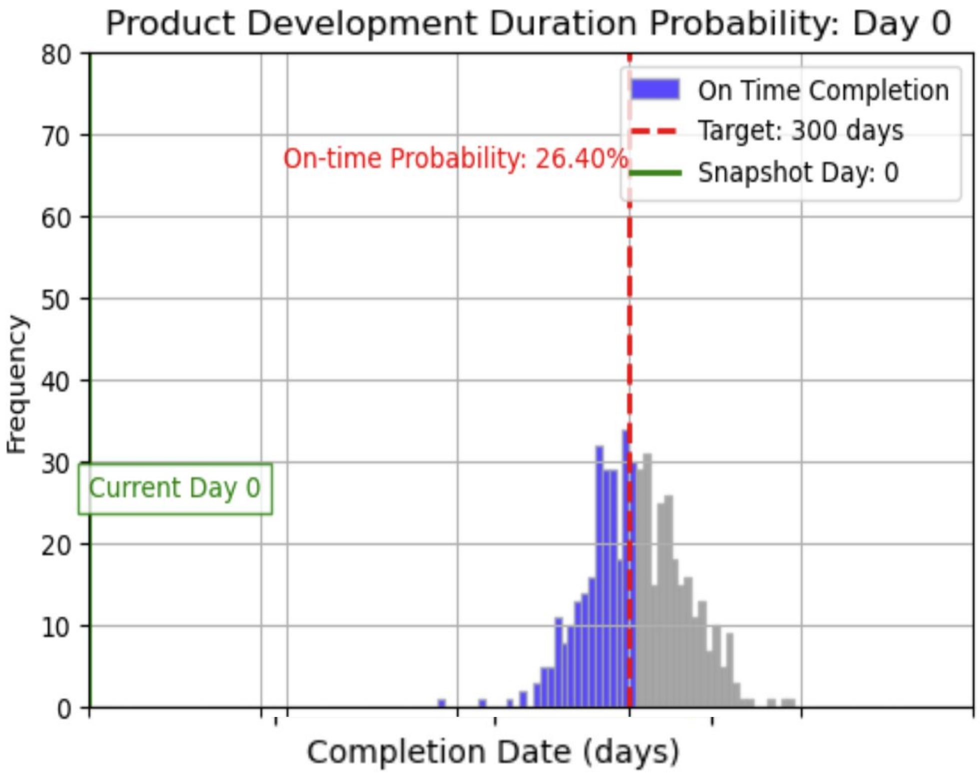
- Found through EDA, most lead time distributions for each cycle are normally distributed
- Will not have access to resource capacity data for project
- Two Main phases in simulation:
    - IC1 & IC2/Probe Solution
    - IC1/IC2 predictive lead times are input to simulation
    - Probe Solution data not obtained yet



Day 0

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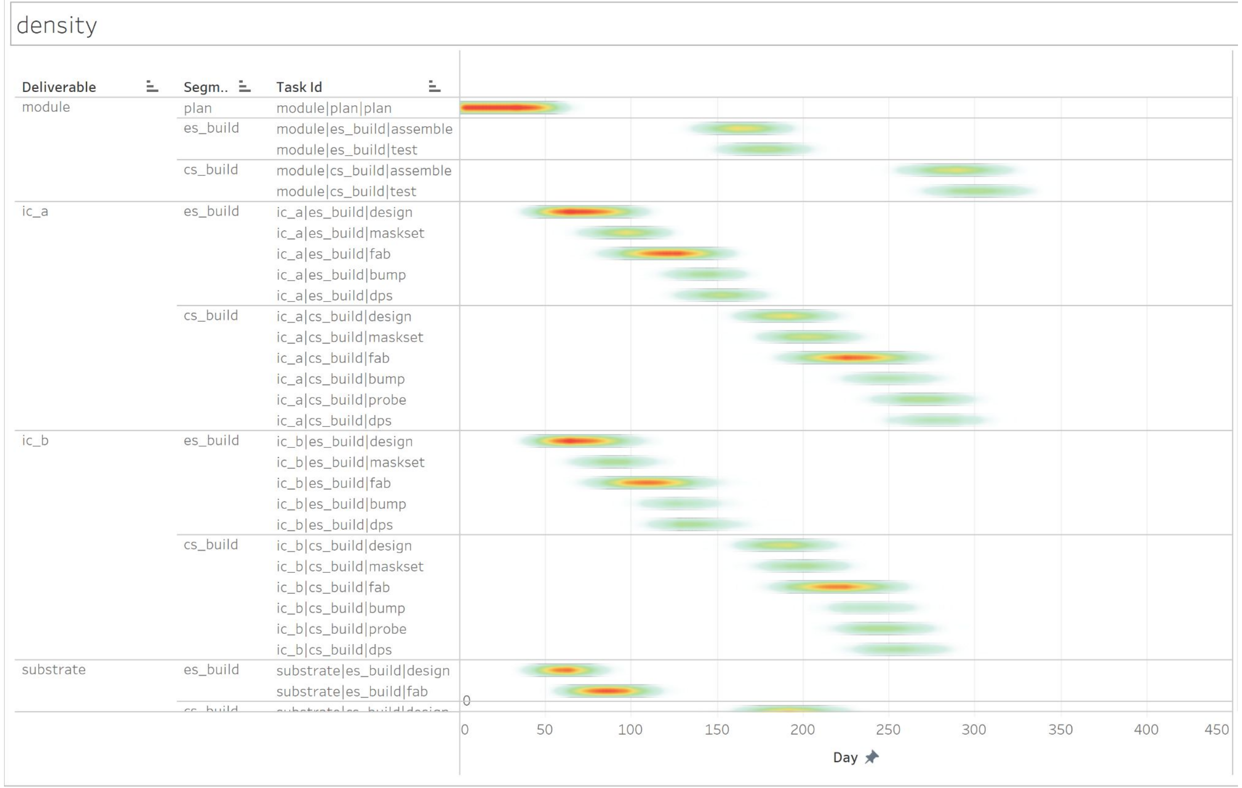
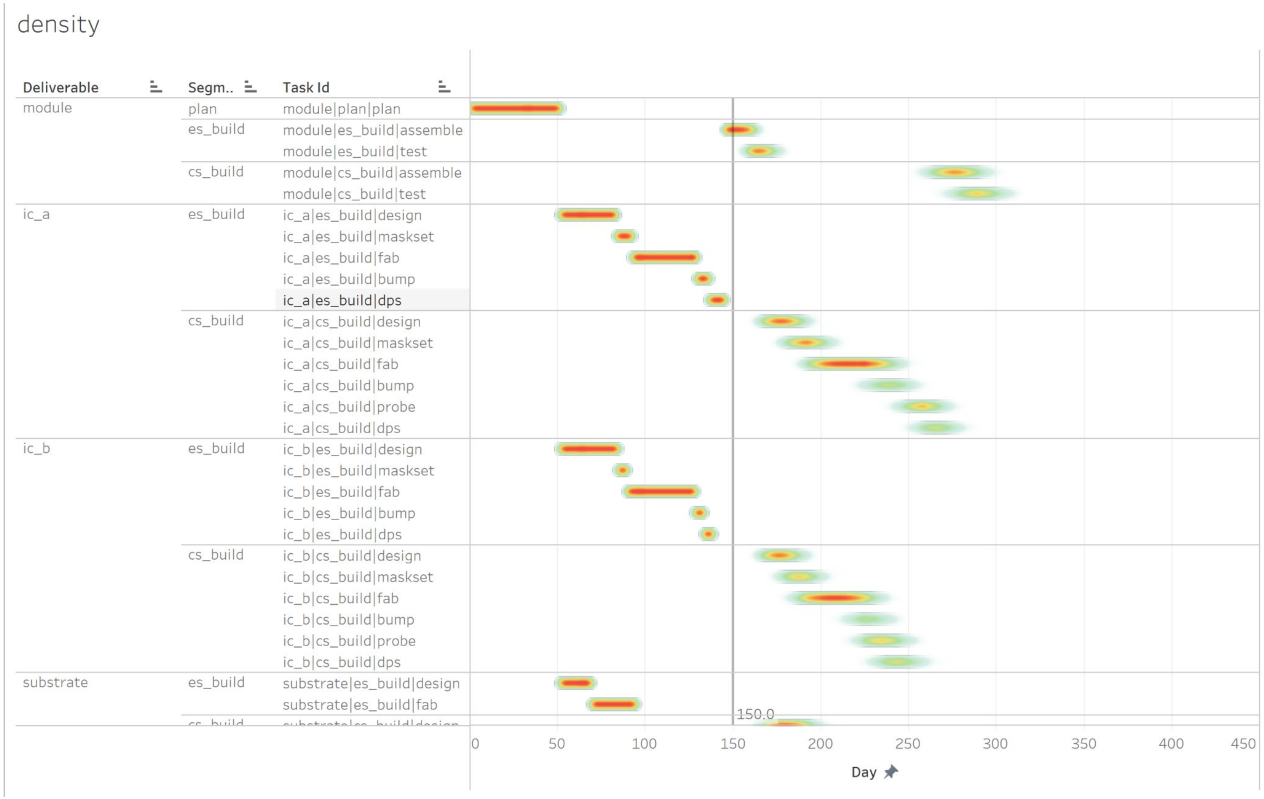


Day 150


density
Deliverable
Segm..
Task Id
module
plan
module|plan|plan
es_build
module|es_build|assemble
module|es_build|test
cs_build
module|cs_build|assemble
module|cs_build|test
ic_a
es_build
ic_a|es_build|design
ic_a|es_build|maskset
ic_a|es_build|fab
ic_a|es_build|bump
ic_a|es_build|dps
cs_build
ic_a|cs_build|design
ic_a|cs_build|maskset
ic_a|cs_build|fab
ic_a|cs_build|bump
ic_a|cs_build|probe
ic_a|cs_build|dps
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ic_b|es_build|design
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ic_b|cs_build|probe
ic_b|cs_build|dps
substrate
es_build
substrate|es_build|design
substrate|es_build|fab
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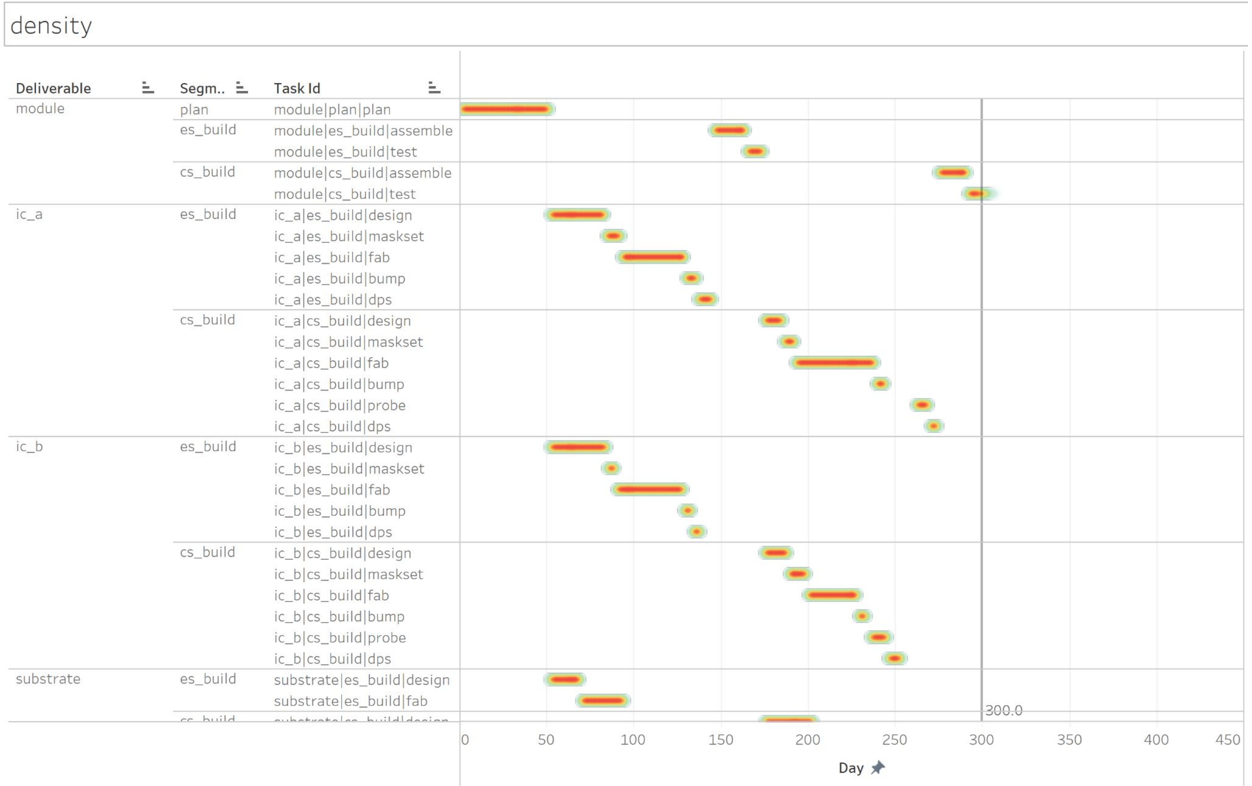
Day

Day 300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Deliverable
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Task Id
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plan
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es_build
module|es_build|assemble
module|es_build|test
cs_build
module|cs_build|assemble
module|cs_build|test
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es_build
ic_a|es_build|design
ic_a|es_build|maskset
ic_a|es_build|fab
ic_a|es_build|bump
ic_a|es_build|dps
cs_build
ic_a|cs_build|design
ic_a|cs_build|maskset
ic_a|cs_build|fab
ic_a|cs_build|bump
ic_a|cs_build|probe
ic_a|cs_build|dps
ic_b
es_build
ic_b|es_build|design
ic_b|es_build|maskset
ic_b|es_build|fab
ic_b|es_build|bump
ic_b|es_build|dps
cs_build
ic_b|cs_build|design
ic_b|cs_build|maskset
ic_b|cs_build|fab
ic_b|cs_build|bump
ic_b|cs_build|probe
ic_b|cs_build|dps
substrate
es_build
substrate|es_build|design
substrate|es_build|fab
300.0
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Day

Key Insights and Metrics

Bottlenecks Identified:

- Fab and DPS stages exhibit high variability (Standard dev: 7.09 & 11.21 days respectively)

Timeline Accuracy:

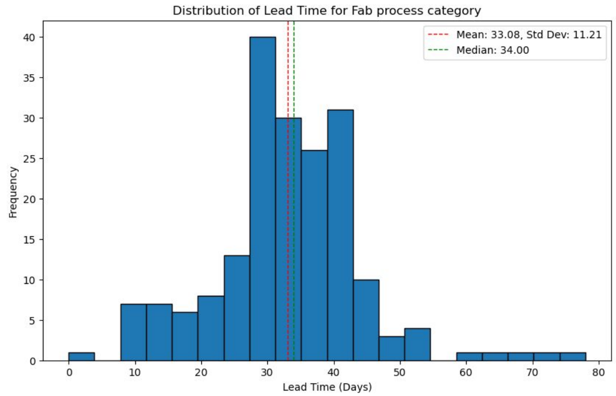
- Data-driven planning approach for internal timelines

Cost Savings:

- Increased monetary savings due to accurate planning

Improved Workflow:

- Reduced idle time at the IC stages via parallel processing



Future Work and Model Improvements

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- Tony - Describe future state of our work and potential improvements at Qualcomm

Conclusion

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Achievements:

- Developed a scalable, data-driven solution for timeline prediction
- Demonstrated improved accuracy and actionable insights

Future Directions:

- Explore Bayesian modeling for rare scenarios.
- Incorporate resource capacity constraints for better scheduling.
- Extend the solution to other industries.

Q&A

Questions and Discussion