Multithreaded Architectures Bibliography

Supercomputing '93 Tutorial

Friday, November 19, 1993 Portland, Oregon

Rishiyur S. Nikhil

Digital Equipment Corporation Cambridge Research Laboratory

General

[22] [55] [61] [89] [158]

Directory-based Cache Coherence

Directory schemes for distributed cache coherence: [3] [4] [2] [8] [36] [78] [79] [121] [144] [145] [159]

Stanford DASH: [101] [102] [103] [109]

Kendall Square Research KSR-1:

Kendall Square Research, 170 Tracer Ln., Waltham, MA 02154, USA

Data Diffusion Machine (COMA, or Cache-Only Memory Architecture, like the KSR-1): [69] [68]

MIT Alewife: [7] [5] [6] [37] [75] [98] [99]

Multithreading from the von Neumann side

Denelcor HEP: [91] [92] [96] [139] [138]

Horizon and Tera: [10] [9] [100] [148]

Dataflow/von Neumann Hybrids: [32] [33] [56] [87] [86] [88]

MIT J-Machine, Message-Driven Processors (MDPs): [45] [46] [43] [44]

Other: [107] [116] [149]

Multithreading from the dataflow side

Static dataflow: [47] [48] [49] [51] [53] [52] [50] [93]

Dynamic dataflow and MIT Tagged Token Dataflow Architecture (TTDA) [19] [18] [15] [23]

Manchester Dataflow: [67] [157]

ETL Sigma-1: [81] [80] [162] [163]

Explicit Token Stores (ETS), MIT Monsoon: [41] [77] [117] [118] [119]

ETL EM-4, EM-5: [95] [126] [127] [124] [123] [125] [160] [161]

MIT P-RISC and *T: [28] [76] [113] [115]

Other dataflow architectures: [12] [11] [63] [66] [94] [122] [147]

Id, Sisal and other dataflow languages

 $[1] \ [20] \ [17] \ [21] \ [24] \ [23] \ [25] \ [31] \ [30] \ [57] \ [64] \ [105] \ [106] \ [111] \ [112] \ [114]$

Id, Sisal and other dataflow language implementation

 $\begin{bmatrix} 29 \end{bmatrix} \ \begin{bmatrix} 35 \end{bmatrix} \ \begin{bmatrix} 42 \end{bmatrix} \ \begin{bmatrix} 58 \end{bmatrix} \ \begin{bmatrix} 62 \end{bmatrix} \ \begin{bmatrix} 70 \end{bmatrix} \ \begin{bmatrix} 72 \end{bmatrix} \ \begin{bmatrix} 71 \end{bmatrix} \ \begin{bmatrix} 82 \end{bmatrix} \ \begin{bmatrix} 83 \end{bmatrix} \ \begin{bmatrix} 110 \end{bmatrix} \ \begin{bmatrix} 120 \end{bmatrix} \ \begin{bmatrix} 130 \end{bmatrix} \ \begin{bmatrix} 131 \end{bmatrix} \ \begin{bmatrix} 132 \end{bmatrix} \ \begin{bmatrix} 133 \end{bmatrix} \ \begin{bmatrix} 137 \end{bmatrix} \ \begin{bmatrix} 140 \end{bmatrix} \ \begin{bmatrix} 142 \end{bmatrix} \ \begin{bmatrix} 141 \end{bmatrix} \ \begin{bmatrix} 150 \end{bmatrix} \ \begin{bmatrix} 151 \end{bmatrix} \ \begin{bmatrix} 153 \end{bmatrix} \ \begin{bmatrix} 152 \end{bmatrix} \ \begin{bmatrix} 155 \end{bmatrix}$

EM-4 message-passing and data-parallel software

 $[129]\ [128]\ [135]\ [136]$

Parallel Lisps

Multilisp [73] [74], Mul-T [97] [108], QLisp [65]

Parallell object-oriented languages

Concurrent Smalltalk [85] [84], ABCL [146], Acore [104]

Parallel Logic Programming Languages and Related Languages

[38] [59] [60] [134] [154]

Futures in C

Semi-C [90], Tera C [9] [34] [54]

Using dataflow to compile imperative languages

[27][26]

Dataflow Resource management

[13] [16] [14] [40] [39]

Active Messages, Basic Mechanisms for Fine-Grain Parallelism

[143] [156]

References

- [1] W. B. Ackerman. Data Flow Languages. *IEEE Computer*, February 1982.
- [2] S. V. Adve and M. D. Hill. High Performance Shared Memory, October 1992. Tutorial notes, ASPLOS V, Boston MA.
- [3] Adve, Sarita V. and Hill, Mark D. Implementing sequential consistency in cache-based systems. In *Int'l. Conf. on Parallel Processing*, 1990.
- [4] Adve, Sarita V. and Hill, Mark D. Weak ordering—a new definition. In *Proc.* 17th. Int'l. Symp. on Computer Architecture, May 1990.
- [5] A. Agarwal, D. Chaiken, G. D'Souza, K. Johnson, D. Kranz, J. Kubiatowicz, K. Kurihara, B.-H. Lim, G. Maa, D. Nussbaum, M. Parkin, and D. a. Yeung. The MIT Alewife Machine: A Large-Scale Distributed-Memory Multiprocessor. In Proc. Wkshp. on Multithreaded Computers, Supercomputing '91, Albuquerque, NM, November 1991.
- [6] A. Agarwal, J. Kubiatowicz, D. Kranz, B.-H. Lim, D. Yeung, G. D'Souza, and M. Parkin. Sparcle: An Evolutionary Processor Design for Multiprocessors. *IEEE Micro*, June 1993.
- [7] A. Agarwal, B.-H. Lim, D. Kranz, and J. Kubiatowicz. APRIL: A Processor Architecture for Multiprocessing. In *Proc.* 17th Ann. Intl. Symp. on Computer Architecture, Seattle, Washington, U.S.A., pages 104–114, May 28-31 1990.
- [8] A. Agarwal, R. Simoni, J. Hennessy, and M. Horowitz. An Evaluation of Directory Schemes for Cache Coherence. In Proc. 15th. Ann. Intl. Symp. on Computer Architecture, Hawaii, May 1988.
- [9] G. Alverson, R. Alverson, D. Callahan, B. Koblenz, A. Porterfield, and B. Smith. Integrated support for heterogeneous parallelism. In R. A. Iannucci, editor, *Multithreading: A Summary of the State of the Art*. Kluwer Academic, 1993.
- [10] R. Alverson, D. Callahan, D. Cummings, B. Koblenz, A. Porterfield, and B. Smith. The Tera Computer System. In *Proc. Intl. Conf. on Supercomputing, Amsterdam*, June 11-15 1990.
- [11] M. Amamiya. Foreword to the special issue on Data Flow Machines. *Journal of Information Processing*, 10(4):217–218, 1987.
- [12] Arvind and S. Brobst. The Evolution of Dataflow Architectures from Static Dataflow to P-RISC. In *Proc. Workshop on Massive Parallelism, Amalfi, Italy, October 1989.* Academic Press, 1990 (to appear).
- [13] Arvind and D. E. Culler. Managing Resources in a Parallel Machine. In *Proceedings of IFIP TC-10 Working Conference on Fifth Generation Computer Architecture, Manchester, England*. North-Holland, July 15-18 1985.
- [14] Arvind, D. E. Culler, and K. Ekanadham. The Price of Asynchronous Parallelism: An Analysis of Dataflow Architectures. In *Proceedings of CONPAR 88, Manchester, England*, September 1988.

- [15] Arvind, D. E. Culler, R. A. Iannucci, V. Kathail, K. Pingali, and R. E. Thomas. The Tagged Token Dataflow Architecture. Technical report, MIT Laboratory for Computer Science, 545 Technology Square, Cambridge, MA 02139, August 1983. Revised October, 1984.
- [16] Arvind, D. E. Culler, and G. K. Maa. Assessing the Benefits of Fine-grained Parallelism in Dataflow Programs. *International Journal of Supercomputer Applications*, 2(3), 1988.
- [17] Arvind and K. Ekanadham. Future Scientific Programming on Parallel Machines. In Proceedings of the International Conference on Supercomputing (ICS), Athens, Greece, Springer-Verlag LNCS 279, June 8-12 1987.
- [18] Arvind and K. Gostelow. The U-Interpreter. *IEEE Computer*, 15(2), February 1982.
- [19] Arvind, K. P. Gostelow, and W. Plouffe. An Asynchronous Programming Language and Computing Machine. Technical Report TR-114a, Dept. of Information and Computer Science, University of California, Irvine, CA, December 1978.
- [20] Arvind, K. P. Gostelow, and W. Plouffe. The (preliminary) Id report. Technical Report 114, Department of Information and Computer Science, University of California, Irvine, CA, 1978.
- [21] Arvind, S. Heller, and R. S. Nikhil. Programming Generality and Parallel Computers. In Biological and Artificial Intelligence Systems, E. Clementi and S. Chin (eds), pages 255–286. ESCOM Science Publishers, P.O.Box 214, 2300 AE Leiden, The Netherlands, 1988.
- [22] Arvind and R. A. Iannucci. Two Fundamental Issues in Multiprocessing. In Proceedings of DFVLR - Conference 1987 on Parallel Processing in Science and Engineering, Bonn-Bad Godesberg, W. Germany, Springer-Verlag LNCS 295, June 25-29 1987.
- [23] Arvind and R. S. Nikhil. Executing a Program on the MIT Tagged-Token Dataflow Architecture. *IEEE Transactions on Computers*, 39(3):300–318, March 1990.
- [24] Arvind, R. S. Nikhil, and K. K. Pingali. I-Structures: Data Structures for Parallel Computing. *ACM Transactions on Programming Languages and Systems*, 11(4):598–632, October 1989.
- [25] P. Barth, R. S. Nikhil, and Arvind. M-Structures: Extending a Parallel, Non-strict, Functional Language with State. In Proc. Functional Programming and Computer Architecture, Cambridge, MA, Springer Verlag LNCS 523, pages 538-568, August 28-30 1991.
- [26] M. Beck, R. Johnson, and K. K. Pingali. From Control Flow to Dataflow. *J. Parallel and Distributed Computing*, 12(2):118–129, June 1991.
- [27] M. Beck, K. K. Pingali, and A. Nicolau. Static Scheduling for Dynamic Dataflow Machines. Technical Report TR90-1076, Department of Computer Science, Cornell University, Ithaca, NY 14853-7501, USA, January 1990.
- [28] M. J. Beckerle. An Overview of the START (*T) Computer System. Technical Report MCRC-TR-28, Motorola Cambridge Research Center, One Kendall Square, Bldg. 200, Cambridge MA 02139, July 31 1992.

- [29] L. Bic, J. M. Roy, and M. Nagel. Exploiting Iteration-Level Parallelism in Dataflow Programs. Technical Report 91-57, Dept. of Information and Computer Science, University of California, Irvine, CA 92717, 1991.
- [30] A. Bohm, D. Cann, J. Feo, and R. Oldehoeft. SISAL 2.0 Reference Manual. Technical Report CS-91-118, Colorado State University, November 12 1991.
- [31] A. Bohm and J. Gurd. Iterative Instructions in the Manchester Dataflow Computer. *IEEE Trans. on Parallel and Distributed Systems*, 1(2):129–139, April 1990.
- [32] R. Buehrer and K. Ekanadham. Dataflow Principles in Multi-processor Systems. Technical report, ETH Zurich and Research Division, Yorktown Heights, IBM Corporation, July 1986.
- [33] R. Buehrer and K. Ekanadham. Incorporating Dataflow Ideas into von Neumann Processors for Parallel Execution. *IEEE Transactions on Computers*, C-36(12):1515–1522, December 1987.
- [34] D. Callahan and B. Smith. A Future-based Parallel Language for a General-purpose Highly-parallel Computer. In Languages and Compilers for Parallel Computing, D. Gelernter, A. Nicolau and D. Padua (eds.), pages 95–113. MIT Press, June 20-22 1990.
- [35] D. C. Cann. Compilation Techniques for High Performance Applicative Computation. PhD thesis, Colorado State University, May 1989. Technical Report Number CS-89-108.
- [36] D. Chaiken, C. Fields, K. Kurihara, and A. Agarwal. Director-based Cache Coherence in Large-Scale Multiprocessors. *IEEE Computer*, 23(6):49–59, June 1990.
- [37] D. Chaiken, J. Kubiatowicz, and A. Agarwal. LimitLESS Directories: A Scalable Cache Coherence Scheme. In *Proc. ASPLOS IV*, April 1991.
- [38] K. L. Clark and S. Gregory. PARLOG: Parallel Programming in Logic. ACM Trans. on Programming Languages and Systems, 8(1):1–49, January 1986.
- [39] D. E. Culler. Effective Dataflow Execution of Scientific Applications. PhD thesis, Laboratory for Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139, 1989 (expected).
- [40] D. E. Culler and Arvind. Resource Requirements of Dataflow Programs. In *Proc. 15th. Ann. Intl. Symp. on Computer Architecture, Honolulu, Hawaii*, May 1988.
- [41] D. E. Culler and G. M. Papadopoulos. The Explicit Token Store. *Journal of Parallel and Distributed Computing*, December 1990.
- [42] D. E. Culler, A. Sah, K. E. Schauser, T. von Eicken, and J. Wawrzynek. Fine-grain Parallelism with Minimal Hardware Support: A Compiler-Controlled Threaded Abstract Machine. In 4th Intl. Conf. on Architectural Support for Programming Languages and Operating Systems, pages 164–175, April 1991.
- [43] W. Dally. The J-Machine System. In Artificial Intelligence at MIT: Expanding Frontiers, vol 1., P.H. Winston and S.A.Shellard, eds. MIT Press, 1990.

- [44] W. Dally, S. Ahmend, P. Carrick, A. Chien, R. Davison, J. S. Fiske, G. Fyler, W. Horwat, J. S. Keen, S. Lear, R. A. Lethin, V. Mark, T. Nguyen, M. Noakes, and D. S. Nuth, Peter R. Wills. Design and Implementation of the Message-Driven Processor. In Proc. Brown/MIT Conf. on Advanced Research in VLSI and Parallel Systems, Brown University, Providence, RI, March 25-27 1992.
- [45] W. Dally, L. Chao, A. Chien, S. Hassoun, W. Horwat, J. Kaplan, P. Song, B. Totty, and S. Wills. Architecture of a Message-Driven Processor. In Proc. 14th. Ann. Intl. Symp. on Computer Architecture, Pittsburgh, PA, pages 189–196, June 1987.
- [46] W. Dally, A. Chien, S. Fiske, W. Horwat, J. Keen, P. Nuth, L. Jerry, and B. Totty. Message-Driven Processor Architecture, Version 11. Technical Report AI Memo No. 1069, MIT AI Lab, August 18 1988.
- [47] J. B. Dennis. First Version of a Data Flow Procedure Language. In G. Goos and J. Hartmanis, editors, *Proc. Programming Symposium*, *Paris 1974* (Lecture Notes in Computer Science 19, Springer Verlag). Spinger-Verlag, New York, 1974.
- [48] J. B. Dennis. Data Flow Supercomputers. *IEEE Computer*, pages 48–56, November 1980.
- [49] J. B. Dennis. Data Flow Ideas for Supercomputers. In *Proc. Comp Con '84, Twenty-eighth IEEE Computer Society International Conference*, pages 15–19. IEEE, 1984.
- [50] J. B. Dennis. The Evolution of "Static" Data-Flow Architecture. In Advanced Topics in Data-flow Computing, J-L. Gaudiot and L. Bic (eds.), pages 35–91. Prentice-Hall, 1991.
- [51] J. B. Dennis, G. Gao, and K. Todd. Modeling the Weather with a Data Flow Supercomputer. *IEEE Transactions on Computers*, July 1984.
- [52] J. B. Dennis and G. R. Gao. An Efficient Pipelined Dataflow Processor Architecture. In *Proc. Supercomputing Conference, Orlando, FL*, pages 368–373, November 14-18 1988.
- [53] J. B. Dennis, J. Stoy, and B. Guharoy. Vim: An Experimental Multiuser System Supporting Functional Programming. In Proc. Int'l Workshop on High-Level Computer Architecture, Los Angeles, CA, May 1984.
- [54] J. M. Draper. Compiling on Horizon. In *Prof. IEEE Supercomputing Conference, Florida*, pages 51–52, 1988.
- [55] R. Duncan. A Survey of Parallel Computer Architectures. *IEEE Computer*, pages 5–17, February 1990.
- [56] K. Ekanadham. Multi-tasking on a dataflow-like architecture. Technical Report RC 12307 (55198), IBM T.J.Watson Research Center, Yorktown Heights, New York, November 1986.
- [57] K. Ekanadham. A Perspective on Id, October 1989.
- [58] K. Ekanadham. Kudos. In Proc. 1st Ann. OSU Wkshp on Parallel Computing, Dept. of CIS, Ohio State University, Columbus, OH, March 21-23 1990.

- [59] I. Foster. Parallel Implementation of Parlog. Technical report, Dept. of Computing, Imperial College of Science and Technology, 180, Queen's Gate, London SW7 2BZ, July 1987.
- [60] Foster, Ian and Olson, Robert and Tuecke, Steven. Productive parallel programming: The pcn approach. *Scientific Programming*, 1:51–66, 1992.
- [61] D. Gajski, D. Padua, D. J. Kuck, and R. Kuhn. A Second Opinion of Data Flow Machines and Languages. *Computer*, pages 58–69, February 1982.
- [62] J.-L. Gaudiot. Structure Handling in Data-Flow Systems. *IEEE Transactions on Computers*, C-35(6):489–502, June 1986.
- [63] J.-L. Gaudiot and L. Bic (editors). Advanced Topics in Data-flow Computing. Prentice Hall, 1991.
- [64] J. R. Glauert. A Single Assignment Language for Data Flow Computing. Master's thesis, Dept. of Computer Science, University of Manchester, January 1978.
- [65] R. Goldman and R. P. Gabriel. Qlisp: Parallel processing in Lisp. *IEEE Software*, pages 51–59, July 1989.
- [66] V. Grafe, G. Davidson, J. Hoch, and V. Holmes. The Epsilon Dataflow Processor. In *Proc.* 16th. Ann. Intl. Symp. on Computer Architecture, Jerusalem, Israel, pages 36–45, May 29-31 1989.
- [67] J. R. Gurd, C. Kirkham, and I. Watson. The Manchester Prototype Dataflow Computer. Communications of the ACM, 28(1):34–52, January 1985.
- [68] E. Hagersten. Toward Scalable Cache Only Memory Architectures. PhD thesis, Swedish Institute for Computer Science, Stockholm, Sweden, November 1992.
- [69] E. Hagersten, A. Landin, and S. Haridi. DDM- A Cache-Only Memory Architecture. *IEEE Computer*, 25(9):44-54, September 1992.
- [70] M. Haines and A. Bohm. Towards a Distributed Memory Implementation of Sisal. Technical Report CS-91-123, Dept. of Computer Science, Colorado State University, November 7 1991.
- [71] M. Haines and A. Bohm. A Comparison of Explicit and Implicit Programming Styles for Distributed Memory Multiprocessors. Technical report, Dept. of Computer Science, Colorado State University, March 30 1993.
- [72] M. Haines and A. Bohm. Task Management, Virtual Shared Memory, and Multithreading in a Distributed Memory Implementation of Sisal. In Proc. PARLE '93, Munich, Germany, June 1993.
- [73] R. H. Halstead. Implementation of Multilisp: Lisp on a Multiprocessor. In *Proceedings of the ACM Conference on Lisp and Functional Programming, Austin, Texas*, pages 9–17, August 6-8 1984.
- [74] R. H. Halstead. Multilisp: A Language for Concurrent Symbolic Computation. ACM Transactions on Programming Languages and Systems, 7(4):501–539, October 1985.

- [75] R. H. Halstead Jr. and T. Fujita. MASA: A Multithreaded Processor Architecture for Parallel Symbolic Computing. In Proc. 15th. Ann. Intl. Symp. on Computer Architecture, Honolulu, Hawaii, June 1988.
- [76] D. S. Henry and C. F. Joerg. The Network Interface Chip. Technical Report CSG Memo 331, MIT Laboratory for Computer Science, 545 Technology Square, Cambridge MA 02139, USA, June 1991.
- [77] J. Hicks, D. Chiou, B. S. Ang, and Arvind. Performance Studies of the Monsoon Dataflow Processor. Technical Report CSG Memo 345-2, MIT Lab. for Computer Science, Computation Structures Group, October 12 1992.
- [78] M. D. Hill and J. R. Larus. Cache considerations for Multiprocessor Programmers. *Comm. of the ACM*, 33(8):97–102, August 1990.
- [79] M. D. Hill, J. R. Larus, S. K. Reinhardt, and D. A. Wood. Cooperative Shared Memory: Software and Hardware for Scalable Multiprocessors. In *Proc. ASPLOS V, Boston, MA*, pages 262–273, October 1992.
- [80] K. Hiraki, K. Nishida, S. Sekiguchi, T. Shimada, and T. Yiba. The SIGMA-1 Dataflow Supercomputer: A Challenge for New Generation Supercomputing Systems. *Journal of Information Processing*, 10(4):219–226, 1987.
- [81] K. Hiraki, S. Sekiguchi, and T. Shimada. System Architecture of a Dataflow Supercomputer. Technical report, Computer Systems Division, Electrotechnical Laboratory, 1-1-4 Umezono, Sakura-mura, Niihari-gun, Ibaraki, 305, Japan, 1987.
- [82] J. E. Hoch, D. M. Davenport, V. G. Grafe, and K. M. Steele. Compile-time partitioning of a non-strict language into sequential threads. In Symp. on Parallel and Distributed Processing. IEEE, Dec. 1991.
- [83] H. S. Hochheiser. A Schezoid Compiler for P-RISC. Master's thesis, Massachusetts Institute of Technology, Laboratory for Computer Science, February 1991.
- [84] W. Horwat. Concurrent Smalltalk on the Message-Driven Processor. Master's thesis, MIT, May 1989.
- [85] W. Horwat, A. A. Chien, and W. J. Dally. Experience with CST: Programming and Implementation. In Proc. ACM SIGPLAN 89 Conf. on Programming Language Design and Implentation, 1989.
- [86] R. A. Iannucci. A Dataflow/von Neumann Hybrid Architecture. Technical Report TR-418, MIT Laboratory for Computer Science, 545 Technology Square, Cambridge, MA 02139, May 1988. Ph.D. thesis.
- [87] R. A. Iannucci. Toward a Dataflow/von Neumann Hybrid Architecture. In Proc. 15th. Ann. Intl. Symp. on Computer Architecture, Honolulu, Hawaii, pages 131–140. IEEE/ACM, June 1988.

- [88] R. A. Iannucci. Parallel Machines: Parallel Machine Languages The Emergence of Hybrid Dataflow Computer Architectures. Kluwer Academic Publishers, Boston, MA., U.S.A., April 1990.
- [89] R. A. Iannucci, editor. Multithreading: A Summary of the State of the Art. Kluwer Academic, 1993 (expected).
- [90] K. Johnson. Semi-C Reference Manual, version 0.6. Technical Report Alewife Systems Memo 20, MIT Laboratory for Computer Science, 1992.
- [91] H. F. Jordan. Performance Measusrements on HEP- a pipelined MIMD computer. In *Proc.* 10th. Ann. Intl. Symp. on Computer Architecture, Stockolm, Sweden, pages 207–212, June 1983.
- [92] H. F. Jordan. HEP Architecture, Programming and Performance. In Parallel MIMD Computation: The HEP Supercomputer and its Applications (J.S. Kowalik, editor). MIT Press, 1985.
- [93] G. Kahn. The Semantics of a Simple Language for Parallel Programming. *Information Processing*, 1974.
- [94] R. M. Keller, G. Lindstrom, and S. Patil. An Architecture for a Loosely-Coupled Parallel Processor. Technical Report UUCS-78-105, Dept. of Computer Science, Univ. of Utah, October 1978.
- [95] Y. Kodama, S. Sakai, and Y. Yamaguchi. A Prototype of a Highly Parallel Dataflow Machine EM-4 and its Preliminary Evaluation. In *Prof. Info Japan*, 1990.
- [96] J. S. Kowalik (editor). Parallel MIMD Computation: HEP Supercomputer and its Applications. MIT Press, 1985.
- [97] D. A. Kranz, R. H. Halstead Jr., and E. Mohr. Mul-T: A High Performance Parallel Lisp. In *Proc. ACM Symp. on Programming Language Design and Implementation, Portland, Oregon*, June 1989.
- [98] D. A. Kranz, K. Johnson, A. Agarwal, J. Kubiatowicz, and B.-H. Lim. Integrating Message-Passing and Shared-Memory: Early Experience. In Proc. Principles and Practice of Parallel Programming (PPoPP), May 1993.
- [99] J. Kubiatowicz and A. Agarwal. Anatomy of a message in the alewife multiprocessor. In *Proc. Intl. Conf. on Supercomputing, Tokyo, Japan*, June 1993.
- [100] J. T. Kuehn and B. J. Smith. The Horizon Supercomputing System: Architecture and Software. In *Proc. IEEE Supercomputing Conference*, Florida, pages 28–34, 1988.
- [101] D. Lenoski, J. Laudon, K. Gharachorloo, A. Gupta, and J. Hennessy. The Directory-Based Cache Coherence Protocol for the DASH Multiprocessor. In Proc. 17th. Ann. Intl. Symp. on Computer Architetecture, Seattle, Washington, pages 148–159, May 28-31 1990.

- [102] D. Lenoski, J. Laudon, K. Gharachorloo, W.-D. Weber, A. Gupta, J. Hennessy, M. Horowitz, and M. S. a. Lam. The Stanford DASH Multiprocessor. *IEEE Computer*, pages 63–79, March 1992.
- [103] D. Lenoski, J. Laudon, T. Joe, D. Nakahira, L. Stevens, A. Gupta, and J. Hennessy. The DASH Prototype: Implementation and Performance. In Proc. 19th. Ann. Intl. Symp. on Computer Architecture, Gold Coast, Australia, pages 92–103, May 19-21 1992.
- [104] C. R. Manning. Introduction to Programming Actors in Acore. In C. Hewitt, G. Agha, C. Manning, and J. Inman, editors, Towards Open Information Systems Science. MIT Press, Cambridge, MA, U.S.A., 1990.
- [105] J. McGraw. The VAL Language: Description and Analysis. ACM Transactions on Programming Languages and Systems, 4(1):44–82, January 1982.
- [106] J. McGraw, S. Skedzielewski, S. Allan, D. Grit, R. Oldehoeft, J. Glauert, P. Hohensee, and I. Dobes. SISAL Reference Manual. Technical report, Lawrence Livermore National Laboratory, 1984.
- [107] E. F. Miller Jr. A Multiple-Stream Registerless Shared-Resource Processor. *IEEE Trans. on Computers*, C-23(3):277–285, March 1974.
- [108] E. Mohr, D. Kranz, and R. Halstead Jr. Lazy Task Creation: A Technique for Increasing the Granularity of Parallel Programs. *IEEE Trans. on Parallel and Distributed Systems*, 2(3):264–280, July 1991.
- [109] T. Mowry and A. Gupta. Tolerating Latency Through Software-Controlled Prefetching in Shared-Memory Multiprocessors. *J. Parallel and Distributed Computing*, 12(2):87–106, June 1991. Special issue: Shared-Memory Multiprocessors.
- [110] R. S. Nikhil. The Parallel Programming Language Id and its Compilation for Parallel Machines. Technical Report CSG Memo 313, MIT Laboratory for Computer Science, 545 Technology Square, Cambridge, MA 02139, USA, July 30 1990. Presented at Workshop on Massive Parallelism, Amalfi, Italy, October 1989.
- [111] R. S. Nikhil. Dataflow Programming Languages. In *Proc. 13th IMACS World Congress on Computation and Applied Mathematics, Trinity College, Dublin, Ireland*, pages 740–741, July 22-26 1991.
- [112] R. S. Nikhil. Id (Version 90.1) Reference Manual. Technical Report CSG Memo 284-2, MIT Laboratory for Computer Science, 545 Technology Square, Cambridge, MA 02139, USA, July 15 1991.
- [113] R. S. Nikhil and Arvind. Can dataflow subsume von Neumann computing? In *Proc. 16th. Ann. Intl. Symp. on Computer Architecture, Jerusalem, Israel*, pages 262–272, May 29-31 1989.
- [114] R. S. Nikhil and Arvind. *Programming in Id: a parallel programming language*. 1993. Textbook on implicit parallel programming. In preparation.

- [115] R. S. Nikhil, G. M. Papadopoulos, and Arvind. *T: A Multithreaded Massively Parallel Architecture. In Proc. 19th. Ann. Intl. Symp. on Computer Architecture, Queensland, Australia, May 1992.
- [116] P. R. Nuth and W. J. Dally. The Named State Processor. Technical report, AI Lab, MIT, 545 Technology Square, Cambridge, MA 02139, November 22 1989.
- [117] G. M. Papadopoulos. Implementation of a General-Purpose Dataflow Multiprocessor. MIT Press, 1991.
- [118] G. M. Papadopoulos and D. E. Culler. Monsoon: An Explicit Token Store Architecture. In *Proc. 17th. Intl. Symp. on Computer Architecture, Seattle, WA*, May 1990.
- [119] G. M. Papadopoulos and K. R. Traub. Multithreading: A Revisionist View of Dataflow Architectures. In *Proc. 18th. Intl. Symp. on Computer Architecture, Toronto, Canada*, March 1991.
- [120] J. E. Ranelletti. Graph Transformation Algorithms for Array Memory Optimization in Applicative Languages. PhD thesis, Lawrence Livermore Laboratory, University of California, 1987.
- [121] S. K. Reinhardt, M. D. Hill, J. R. Larus, A. R. Lebeck, J. C. Lewis, and D. A. Wood. The Wisconsin Wind Tunnel: Virtual Prototyping of Parallel Computers. In *Proc. ACM SIGMETRICS Conference*, Santa Clara, CA, May 1993.
- [122] J. Rumbaugh. A Data Flow Multiprocessor. *IEEE Trans. on Computers*, C-26(2):138–146, February 1977.
- [123] S. Sakai, K. Hiraki, Y. Yamaguchi, Y. Kodama, and T. Yuba. Pipeline Optimization of a Data-Flow Machine. In *Advanced Topics in Data-Flow Computing*, *J.L. Gaudiot and L. Bic (eds.)*, pages 225–246, 1991.
- [124] S. Sakai, Y. Kodama, and Y. Yamaguchi. Architectural Design of a Parallel Supercomputer EM-5. In *Proc. Japan Soc. Parallel Proc., Kobe Japan*, pages 149–156, May 14-16 1991.
- [125] S. Sakai, Y. Kodama, and Y. Yamaguchi. Prototype Implementation of a Highly Parallel Dataflow Machine EM-4. In *Proc. IPPS*, 1991.
- [126] S. Sakai, Y. Yamaguchi, K. Hiraki, Y. Kodama, and T. Yuba. An Architecture of a Dataflow Single Chip Processor. In *Proc. 16th Ann. Intl. Symp. on Computer Architecture, Jerusalem, Israel*, pages 46–53, May28-June 1 1989.
- [127] S. Sakai, Y. Yamaguchi, K. Hiraki, Y. Kodama, and T. Yuba. Design of the Dataflow Single-Chip Processor EMC-R. *Journal of Information Processing*, 13(2), 1990.
- [128] M. Sato, Y. Kodama, S. Sakai, and Y. Yamaguchi. EM-C: A Parallel Programming Language for Explicit-Switch Threads in a Distributed Global Address Space of the EM-4 Multiprocessor. Technical report, ETL, Japan, 1993.

- [129] M. Sato, Y. Kodama, S. Sakai, Y. Yamaguchi, and Y. Koumura. Thread-based programming for the em-4 hybrid dataflow machine. In *Proc. 19th. Ann. Intl. Symp. on Computer Architecture, Gold Coast, Australia*, pages 146–155, May 19-21 1992.
- [130] K. E. Schauser. Compiling Dataflow into Threads. Master's thesis, Computer Science Division, Univ. of California, Berkeley, CA 94720, July 2 1991. Report No. UCB/CSD 91/644.
- [131] K. E. Schauser, D. E. Culler, and T. von Eicken. Compiler-Controlled Multithreading for Lenient Parallel Languages. In Proc. 5th ACM Conf. on Functional Programming Languages and Computer Architecture, Cambridge, MA, pages 50–72, August 1991. Springer-Verlag LNCS 523.
- [132] S. Sekiguchi, T. Shimada, and K. Hiraki. A Design of Practical Dataflow Language DFC II and its Data Structures. Technical Report TR-90-16, Electrotechnical Laboratory, Japan, 1-1-4, Umezono, Sakura-mura, Niihari-gun, Ibaraki, 305, Japan, April 23 1990.
- [133] S. Sekiguchi, T. Shimada, and K. Hiraki. Sequential Description and Parallel Execution Language DFC II for Dataflow Supercomputers. In *Proc. ICS 91*, 1991.
- [134] E. Shapiro. The Family of Concurrent Logic Programming Languages. *ACM Computing Surveys*, 21(3):412–510, 1989.
- [135] A. Shaw, Y. Kodama, M. Sato, S. Sakai, and Y. Yamaguchi. Data-Parallel Programming on the EM-4 Dataflow Parallel Supercomputer. In *Joint Symp. on Parallel Processing, Yokohama*, June 1992.
- [136] A. Shaw, Y. Kodama, M. Sato, S. Sakai, and Y. Yamaguchi. Performance of Data-Parallel Primitives on the EM-4 Dataflow Parallel Supercomputer. In *Proc. Frontiers of Parallel Computation, MacLean, VA*, October 1992.
- [137] S. Skedzielewski and J. Glauert. IF1: An Intermediate Form for Applicative Languages. Technical Report M170, Lawrence Livermore National Laboratory, Livermore, California, July 31 1985.
- [138] B. Smith. The Architecture of the HEP. In Parallel MIMD Computation: HEP Supercomputer and its Applications (J.S. Kowalik, editor). MIT Press, 1985.
- [139] B. J. Smith. Architecture and Applications of the HEP multiprocessor computer system. In Real Time Signal Processing IV, Proc. SPIE, volume 298, August 1981.
- [140] E. Spertus. Dataflow Computation for the J-Machine. Technical Report AI TR 1233, MIT AI Lab, May 1990.
- [141] E. Spertus. Execution of Dataflow Programs on General-Purpose Hardware. Master's thesis, Dept. of Electrical Engineering and Computer Science, MIT, August 1992.
- [142] E. Spertus and W. J. Dally. Experiences Implementing Dataflow on a General-Purpose Parallel Computer. In *Proc. Intl. Conf. on Parallel Processing*, 1991.

- [143] E. Spertus, S. C. Goldstein, K. E. Schauser, T. von Eicken, D. E. Culler, and W. J. Dally. Evaluation of Mechanisms for Fine-Grained Parallel Programs in the J-Machine and the CM-5. In Proc. 20th. Ann. Intl. Symp. on Computer Architecture, San Diego, CA, May 17-19 1993.
- [144] P. Stenstrom. A Survey of Cache Coherence Schemes for Multiprocessors. *IEEE Computer*, 23(6):12–25, June 1990.
- [145] P. Stenstrom, T. Joe, and A. Gupta. Comparative Performance Evaluation of Cache-Coherent NUMA and COMA Architectures. In Proc. 19th. Ann. Intl. Symp. on Computer Architecture, Gold Coast, Australia, pages 80–91, May 19-21 1992.
- [146] K. Taura, S. Matsuoka, and A. Yonezawa. An Efficient Implementation Scheme of Concurrent Object-Oriented Languages on Stock Multicomputers. In 4th. ACM Symp. on Principles and Practice of Parallel Programming (PPoPP), pages 218–228, May 19-22 1993.
- [147] H. Terada, H. Nishikawa, K. Asada, T. Okamoto, S. Miyata, H. Asano, T. Tokura, M. Shimizu, S. Hara, S. Komori, and K. Shima. Design Philosophy of a Data-driven Processor: Q-p. Journal of Information Processing, 10(4):245–251, 1987.
- [148] M. R. Thistle and B. J. Smith. A Processor Architecture for Horizon. In *Prof. IEEE Super-computing Conference*, Florida, pages 35–41, 1988.
- [149] J. Thornton. Parallel Operations in the Control Data 6600. In *Proc. Spring Joint Computer Conference*, pages 33–39, 1964.
- [150] K. R. Traub. A Compiler for the MIT Tagged-Token Dataflow Architecture. Technical Report LCS TR-370, MIT Laboratory for Computer Science, 545 Technology Square, Cambridge, MA 02139, August 1986.
- [151] K. R. Traub. Compilation as Partitioning: A New Approach to Compiling Non-Strict Functional Languages. In *Proceedings of the Conference on Functional Programming Languages and Computer Architecture, London*, pages 75–88, September 1989.
- [152] K. R. Traub. Implementation of Non-Strict Functional Programming Languages. MIT Press (Research Monographs in Parallel and Distributed Computing), 1991.
- [153] K. R. Traub. Multi-thread Code Generation for Dataflow Architectures from Non-Strict Programs. In *Proc. 5th ACM Conf. on Functional Programming Languages and Computer Architecture*, Cambridge, MA, pages 73–101, August 1991. Springer-Verlag LNCS 523.
- [154] K. Ueda and T. Chikayama. Design of the Kernel Language for the Parallel Inference Machine. The Computer J., 33(6):494–500, 1990.
- [155] A. H. Veen and R. van den Born. Compiling C for the DTN Dataflow Computer. In Advanced Topics in Data-Flow Computing, J.L. Gaudiot and L.Bic, editors, pages 265–304. Prentice Hall, 1991.
- [156] T. von Eicken, D. E. Culler, S. C. Goldstein, and K. E. Schauser. Active Messages: a Mechanism for Integrated Communication and Computation. In Proc. 19th. Ann. Intl. Symp. on Computer Architecture, Gold Coast, Australia, pages 256–266, May 1992.

- [157] I. Watson and J. Gurd. A Practical Dataflow Computer. *IEEE Computer*, pages 51–57, February 1982.
- [158] W.-D. Weber and A. Gupta. Exploring the Benefits of Multiple Hardware Contexts in Multiprocessor Architecture: Preliminary Results. In Proc. 16th. Ann. Intl. Symp. on Computer Architecture, Jerusalem, Israel, pages 273–280, May 29-31 1989.
- [159] D. A. Wood, S. Chandra, B. Falsafi, M. D. Hill, J. R. Larus, A. R. Lebeck, J. C. Lewis, S. Mukerjee, S. Palacharla, and S. K. Reinhardt. Mechanisms for Cooperative Shared Memory. In Proc. 21st ISCA, San Diego, CA, May 1993.
- [160] Y. Yamaguchi, S. Sakai, K. Hiraki, Y. Kodama, and T. Yuba. An Architectural Design of a Highly Parallel Dataflow Machine. In *Proc. Information Processing 89, San Francisco*, USA, pages 1155–1160, August 28-September 1 1989.
- [161] Y. Yamaguchi, S. Sakai, and Y. Kodama. Synchronization Mechanisms of a Highly Parallel Dataflow Machine EM-4. *IEICE Transactions*, E 74(1):204–213, January 1991.
- [162] T. Yuba, T. Shimada, K. Hiraki, and H. Kashiwagi. Sigma-1: A Dataflow Computer For Scientific Computation. Technical report, Electrotechnical Laboratory, 1-1-4 Umesono, Sakuramura, Niiharigun, Ibaraki 305, Japan, 1984.
- [163] T. Yuba, T. Shimada, Y. Yamaguchi, K. Hiraki, S. Sakai, S. Sekiguchi, and Y. Kodama. Dataflow Computer Development at the Electrotechnical Laboratory. In *InfoJapan '90*, 1990.