

5118007-02 Computer Architecture

Introduction & Backgrounds

(Ch. 1 Computer Abstractions and Technology)

5 Mar 2024

Shin Hong

Learning Objectives

- get an overview of the general structure of computer
- understand key ideas in computer system designs
 - abstraction (instruction set architecture)
 - memory hierarchy
- comprehend different notions of computer performance

George Boole



Formulate a calculus of reasoning

- Claim that logic should be considered as a branch of math, rather than a part of philosophy
- Argue that there are math laws to express the operation of human mind
- Showed that Aristotle's syllogistic logic could be rendered as algebraic equitation

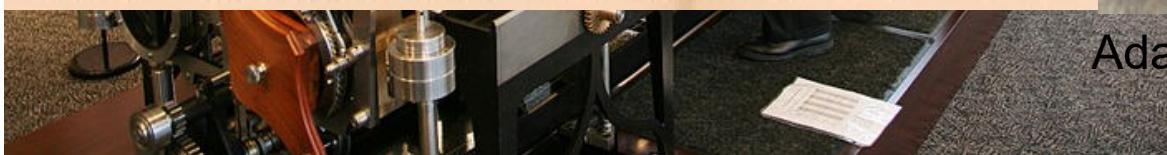
George Boole (1815--1864)

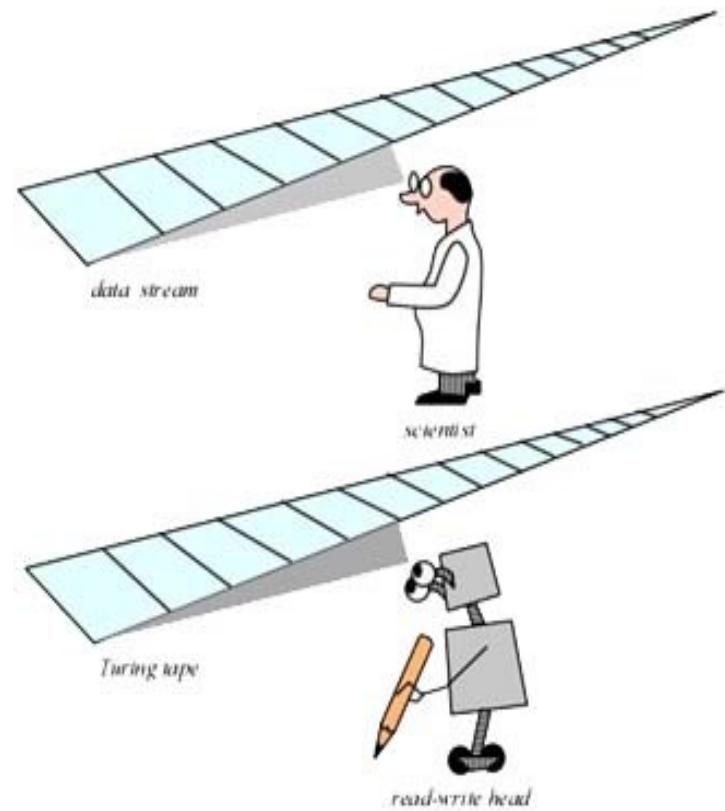
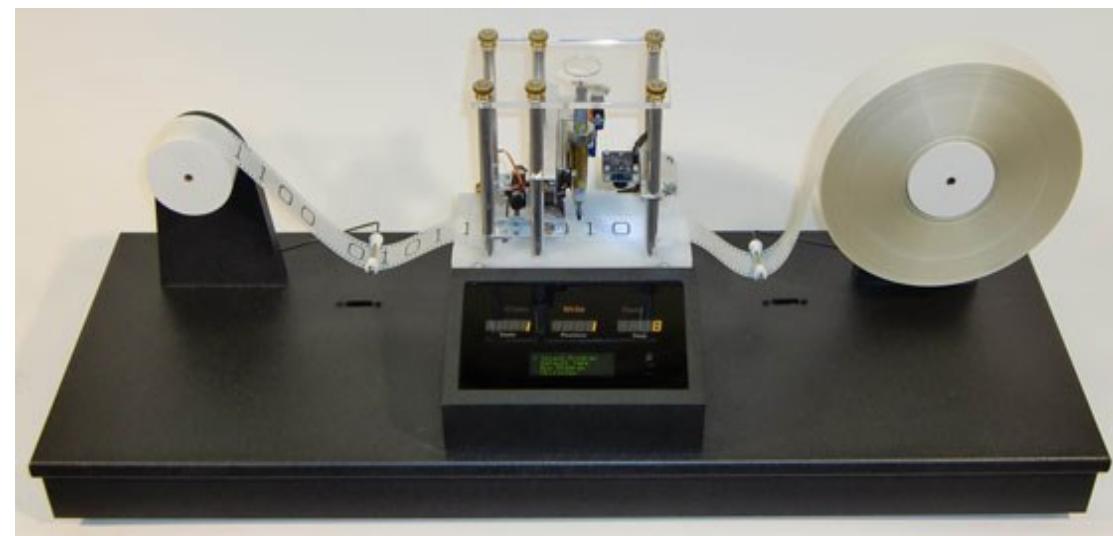
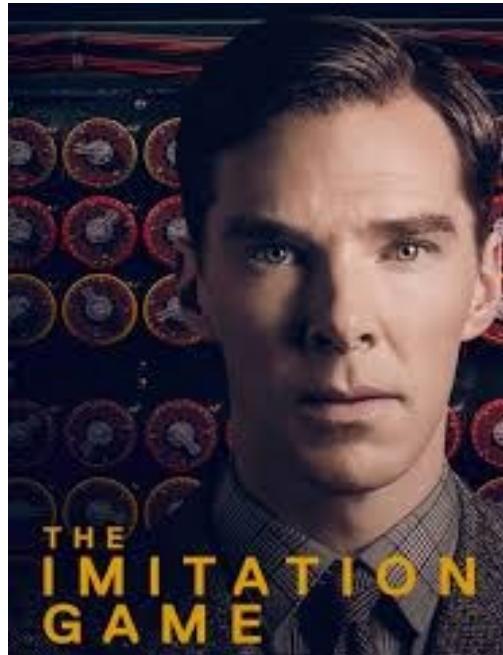
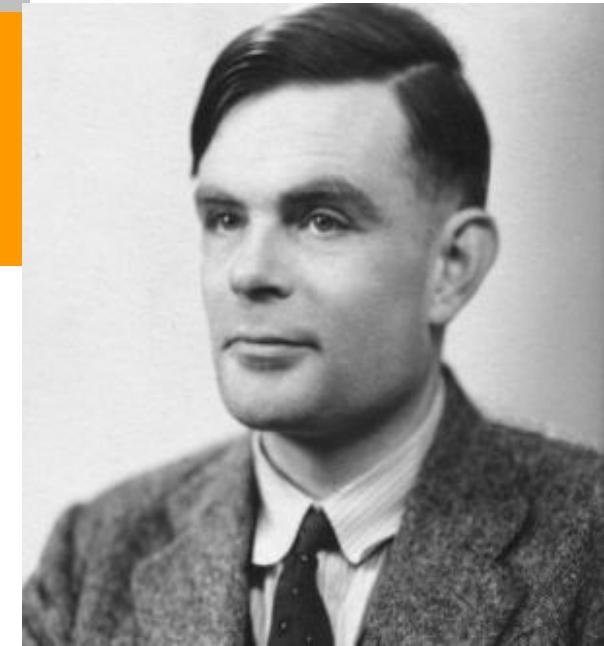
A Brief History of Computing by G. O'Regan

Charles Babbage



Ada Lovelace (1815–1852)





Mathematical Model of Computing



Kurt Gödel



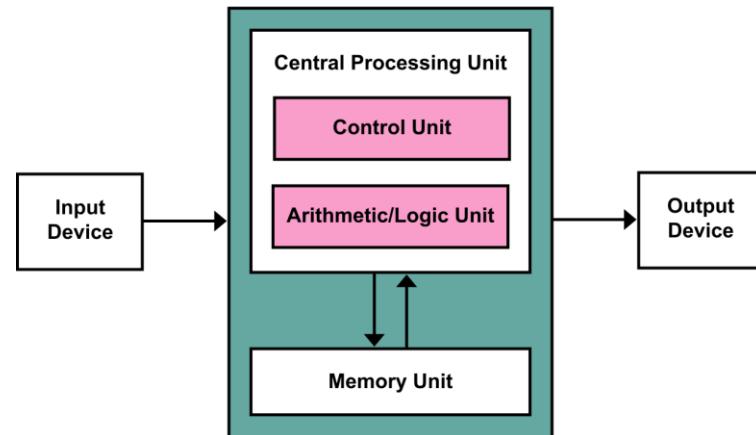
Alan Turing



Alonzo Church

Modern Computer Model

- Memory is a map from addresses to values
- A value is either a number or instruction
 - number
 - instruction
 - receive an input
 - produce an output
 - evaluate an expression over memory addresses
 - assign a value to a memory address
 - jump to a memory address
 - finish
- A processor loads and executes instructions from address



John von Neumann (1903— 1957)

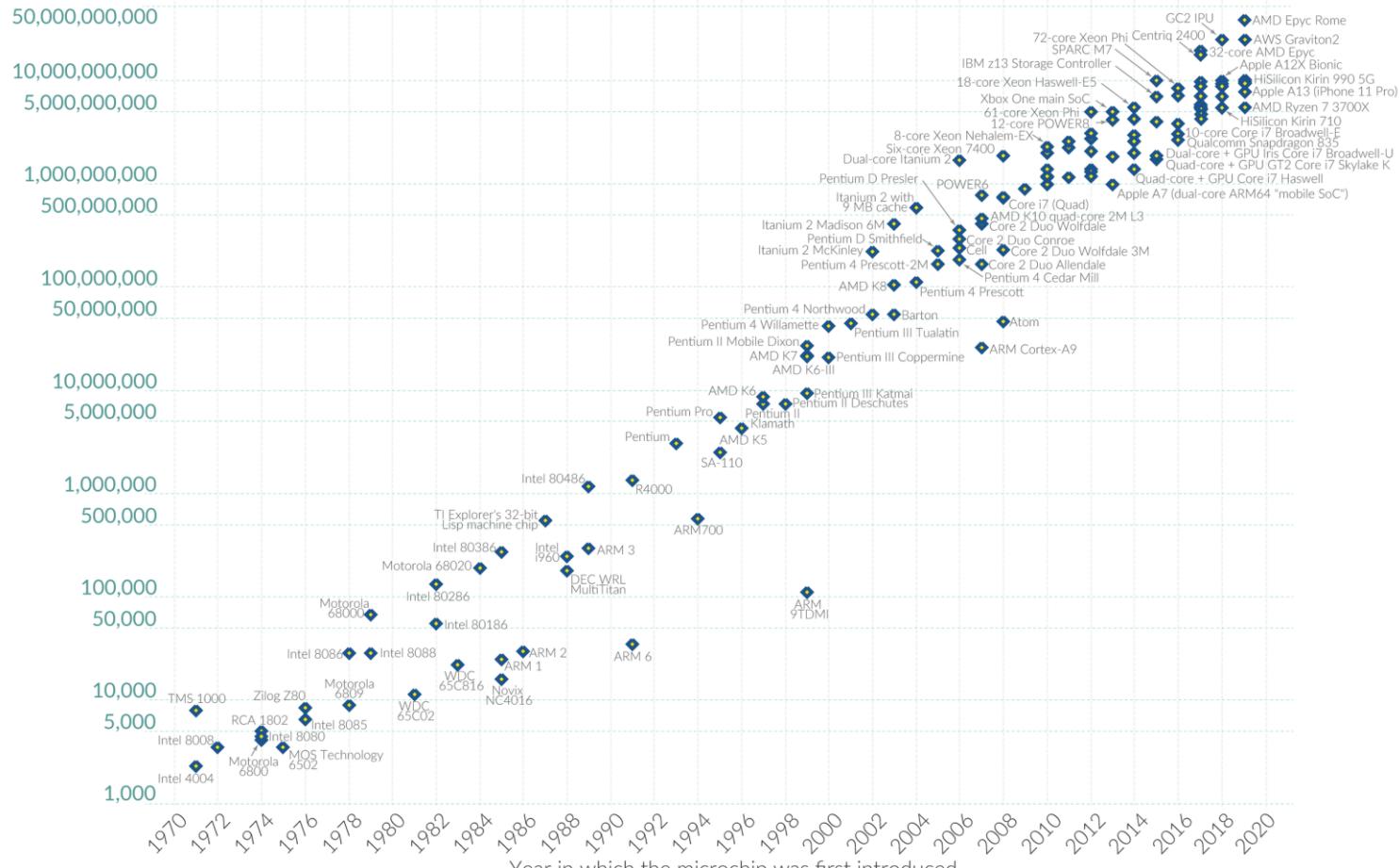
Innovations in Semiconductor Technology

Moore's Law: The number of transistors on microchips doubles every two years

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

Our World
in Data

Transistor count

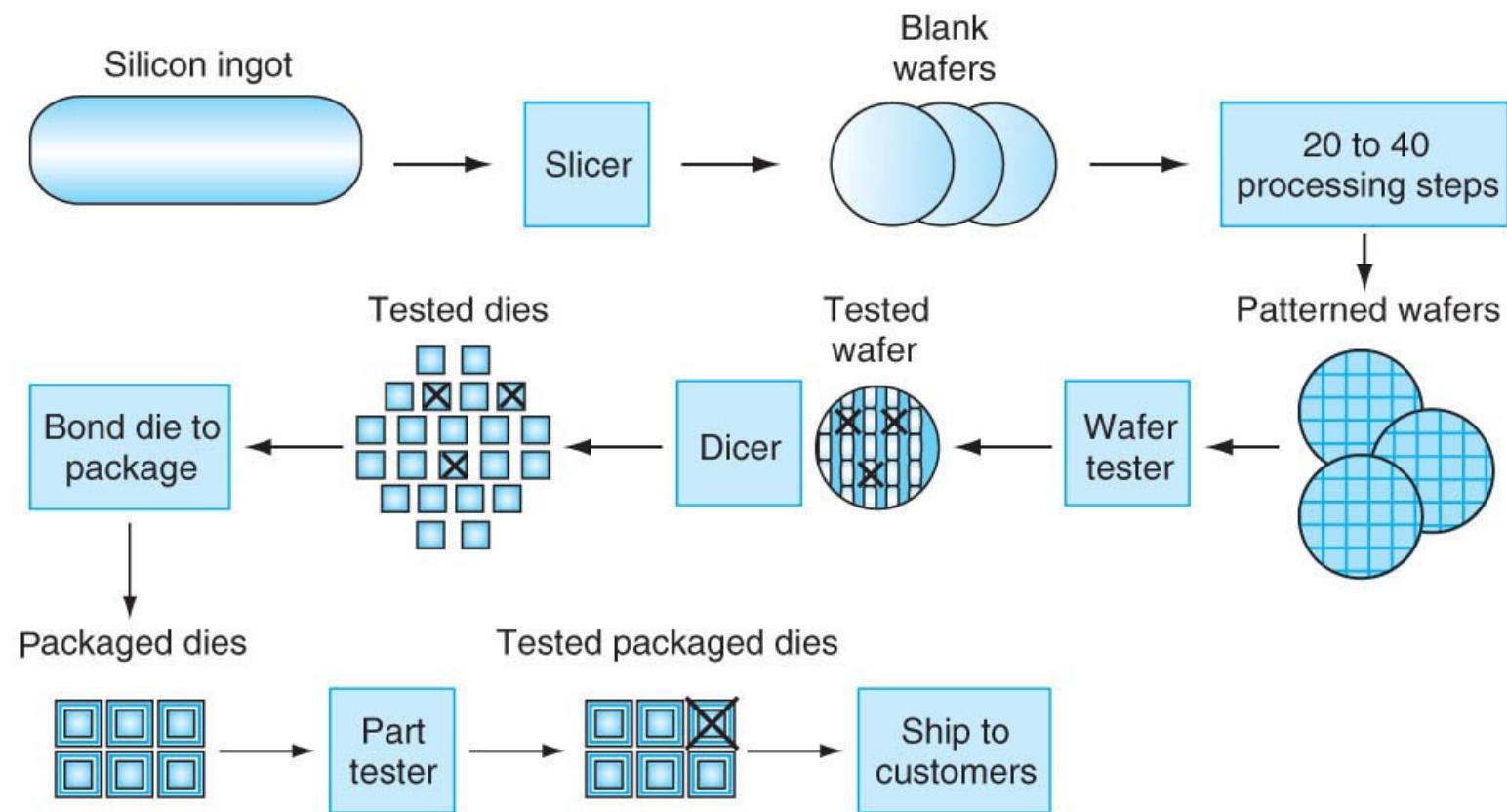


Data source: Wikipedia ([wikipedia.org/wiki/Transistor_count](https://en.wikipedia.org/wiki/Transistor_count))

OurWorldInData.org – Research and data to make progress against the world's largest problems.

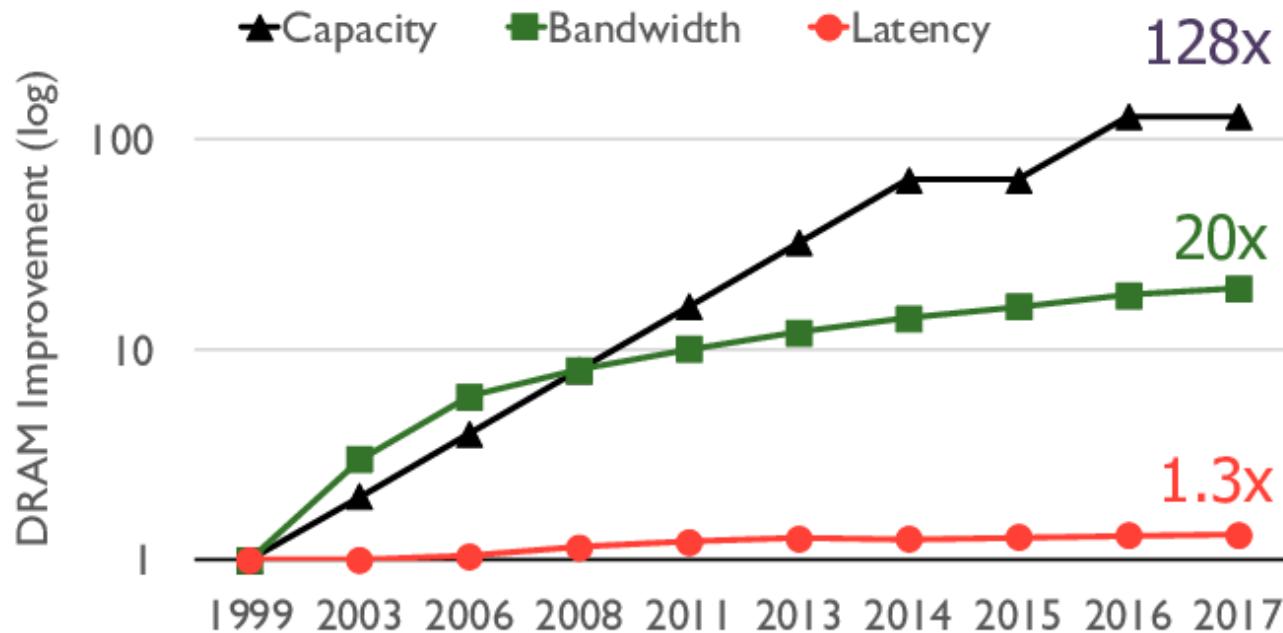
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Semiconductor Manufacturing Process



Innovations in Semiconductor Technology

DRAM Capacity, Bandwidth & Latency



Innovations in Semiconductor Technology

경제 산업·재계

삼성 2나노 반도체 2025년 양산... 공정 로드맵 첫 공개

'삼성 파운드리 포럼'서 2nm 양산 로드맵 공개

기자 [옥기원](#)

수정 2023-06-28 17:29 등록 2023-06-28 17:29



삼성전자가 27일(현지시간) 미국 실리콘밸리에서 개최한 '삼성 파운드리 포럼 2023'에서 최시영 파운드리 사업부 사장이

OpenAI chief looking to raise trillions to reshape semiconductor sector: WSJ

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AFP News

9 February 2024 · 2-min read

In this article:

Sam Altman
American venture-c...

Masayoshi Son
Japanese businessm...

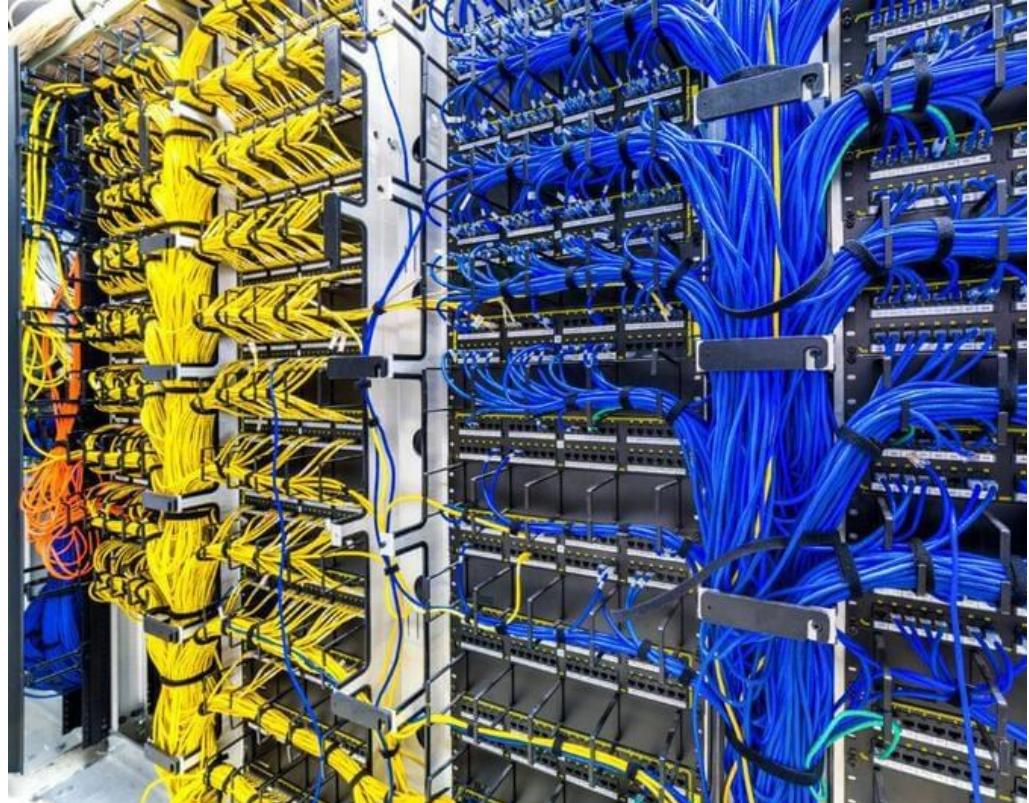
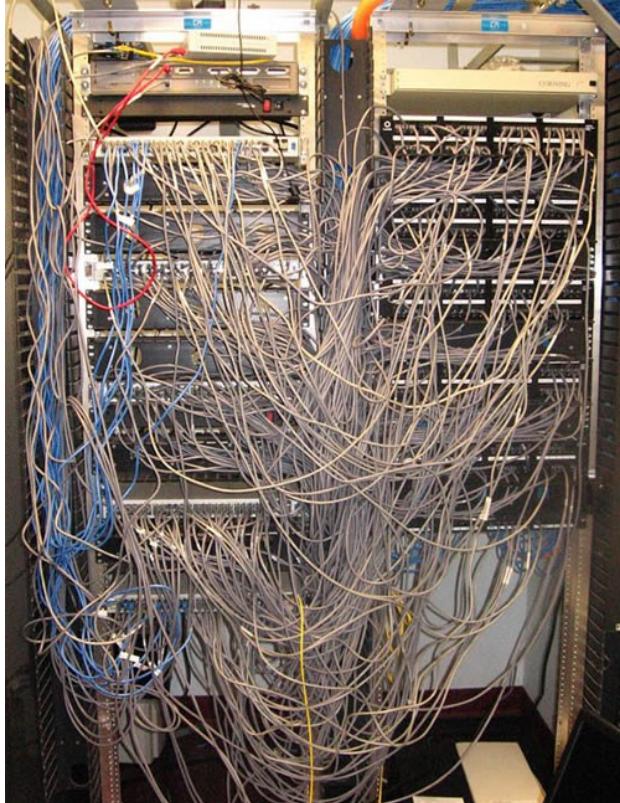


Sam Altman has reportedly held talks with potential investors including the UAE government (Fabrice COFFRINI)

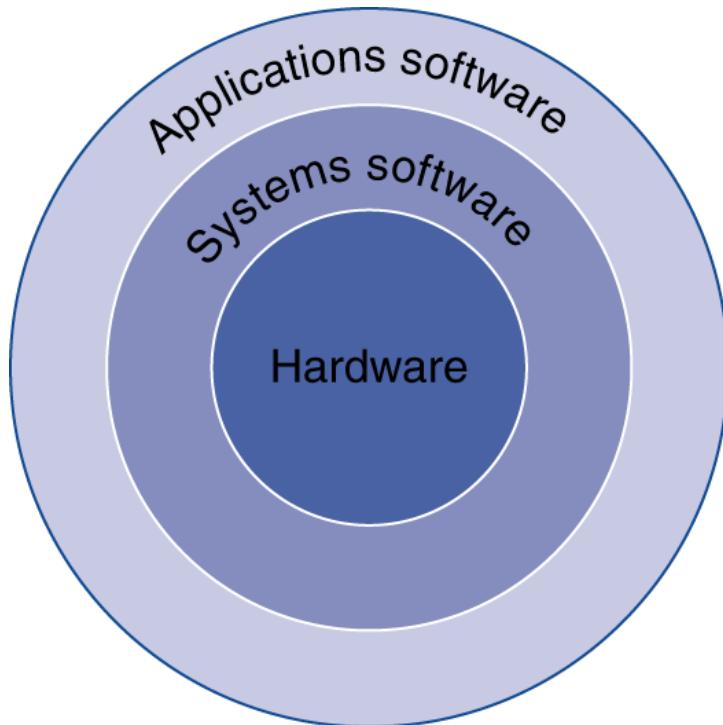
OpenAI chief Sam Altman is seeking to raise trillions

Abstraction

- Define an interface that hides implementation details and offers functional primitives

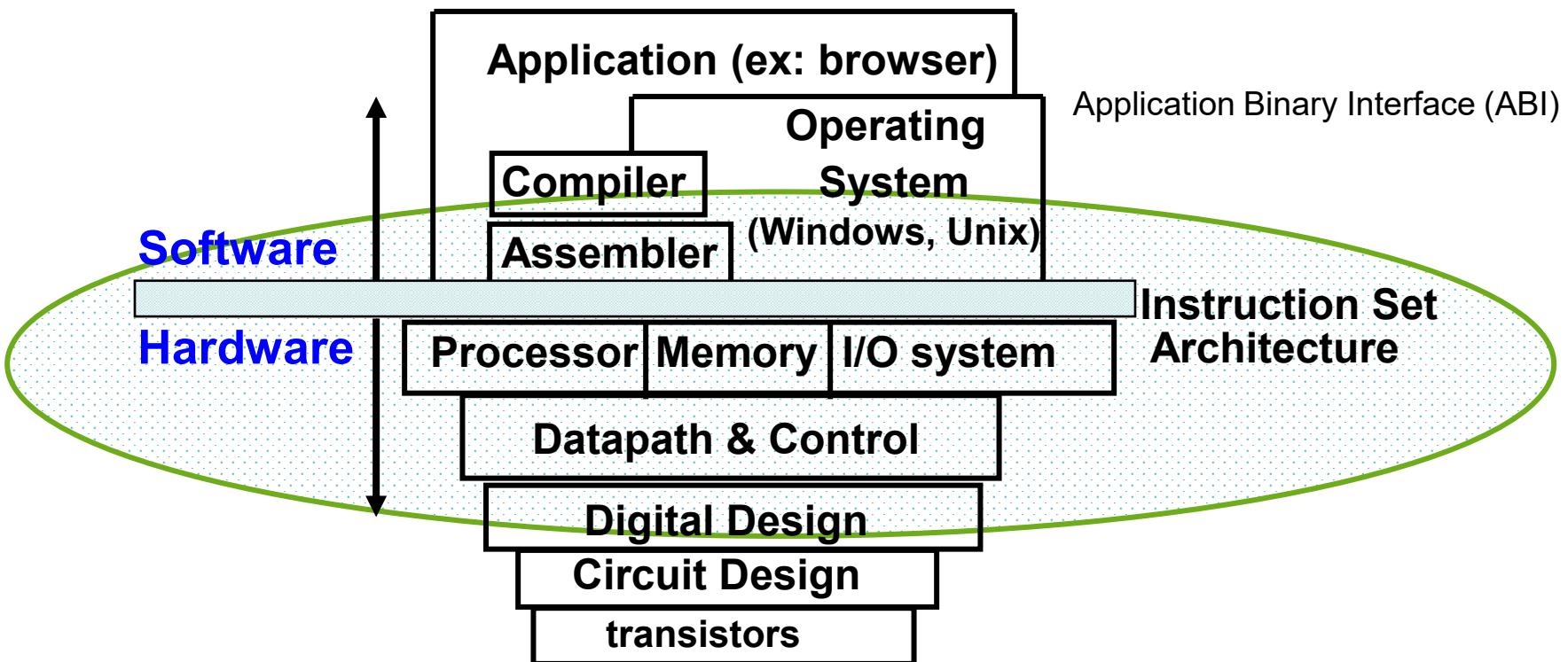


Below Your Program

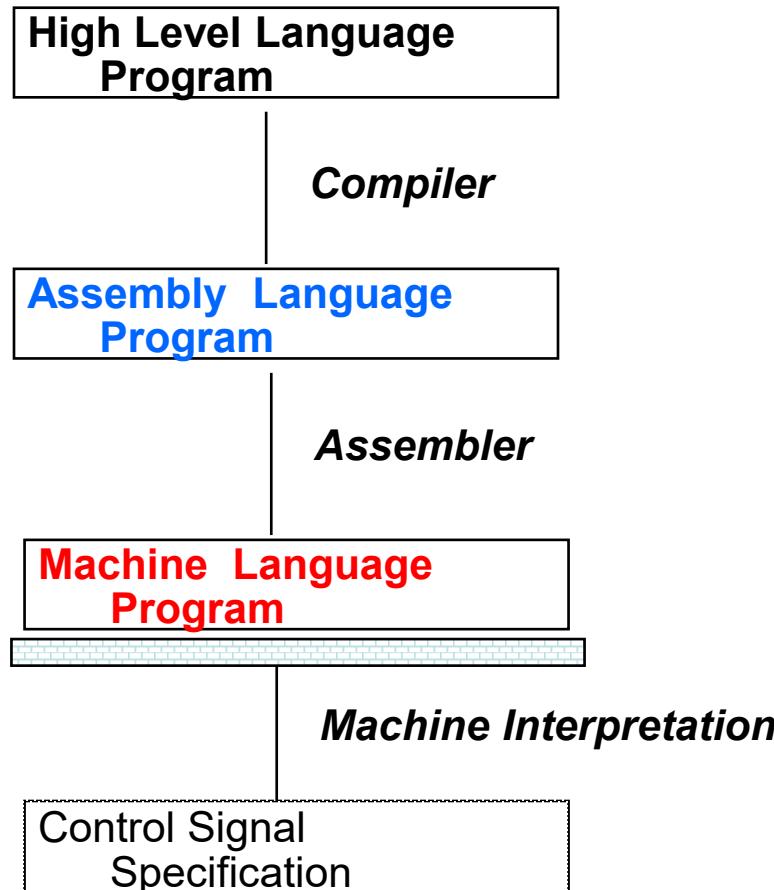


- Application software
- System software
 - Compiler: translates HLL code to machine code
 - Operating System: service code
 - Handling input/output
 - Managing memory and storage
 - Scheduling tasks & sharing resources
- Hardware
 - Processor, memory, I/O controllers

Cross Section View



Program Code Representations



`temp = v[k];`

`v[k] = v[k+1];`

`v[k+1] = temp;`

“instruction”

IW	\$15,	0(\$2)
IW	\$16,	4(\$2)
SW	\$16,	0(\$2)
SW	\$15,	4(\$2)

0000 1001 1100 0110 1010 1111 0101 1000
0000 1001 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
1100 0110 0000 1001 1100 0110 1010 1111

High and low signals on control lines

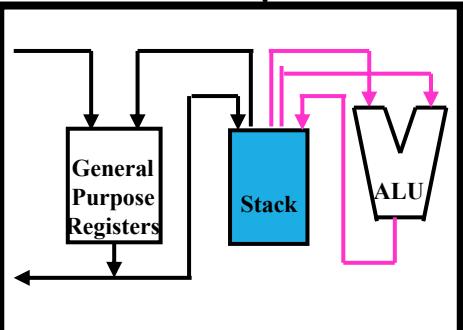
Instruction Set Architecture (ISA)

$$C = A + B;$$

ISA 1 ISA 2 ISA 3

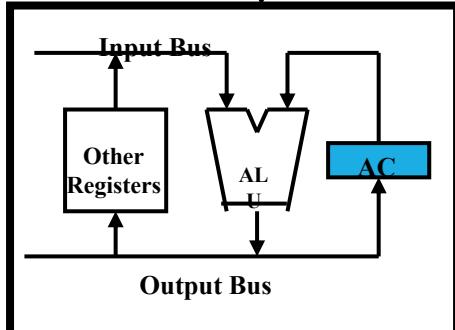
push A
push B
add
pop C

1100 1001 1100 0110
1010 1011 0101 1010
1100 0110 1010 1111
0101 1010 0000 1001



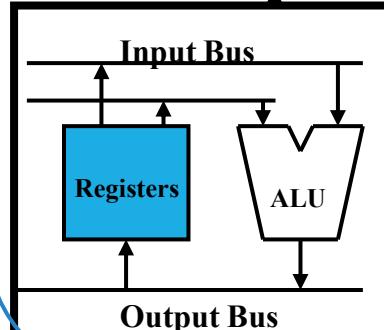
load A
add B
store C

0110 1001 1010 0110
1010 1111 0101 1000
1010 0110 1010 1111

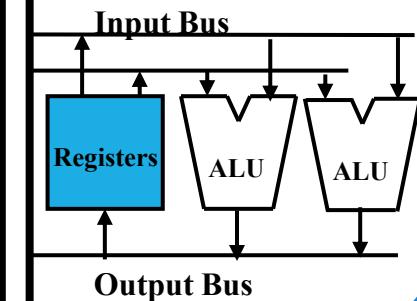


ld R1, A
ld R2, B
add R3,R1,R2
st C,R3

0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111

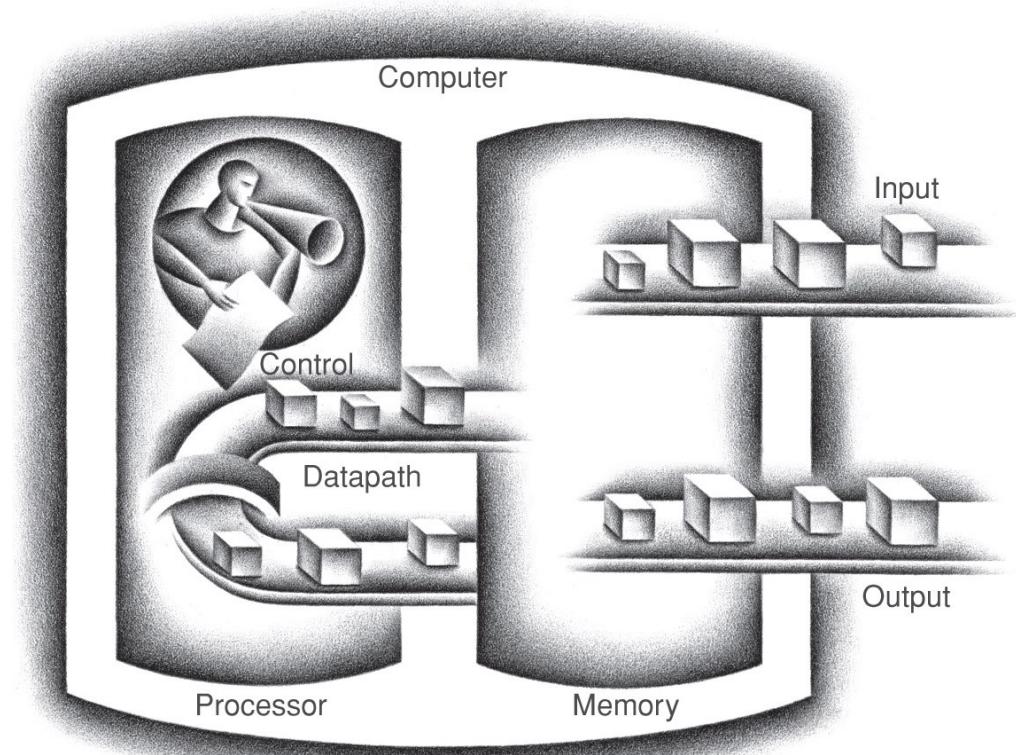


ISA 3



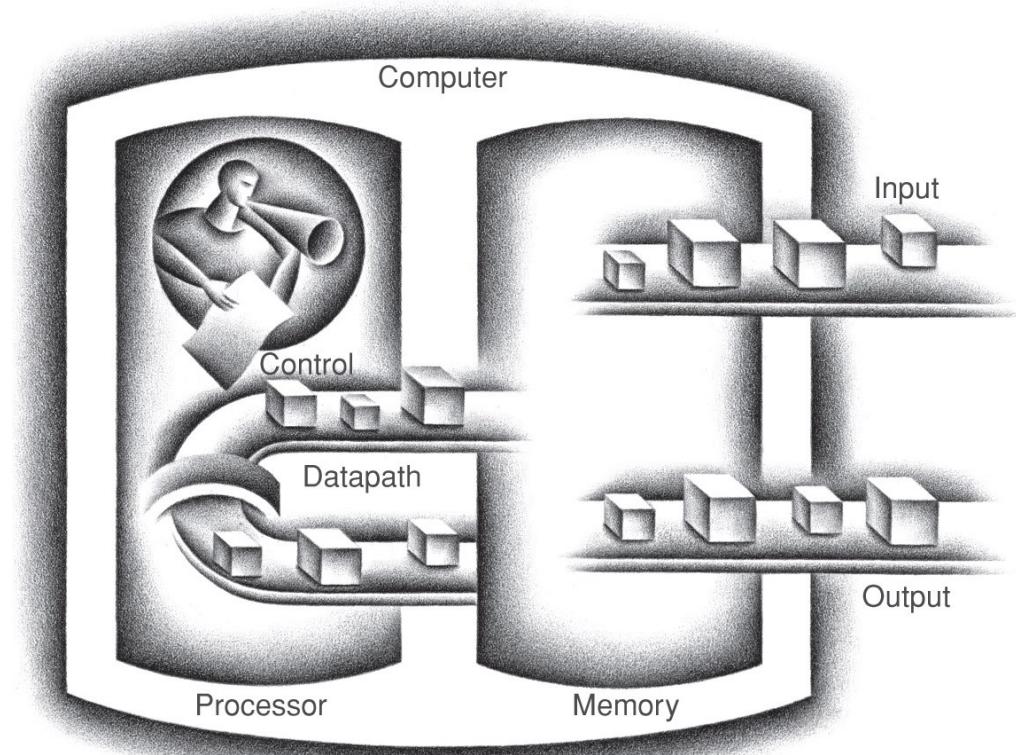
Computer System Organization

- Five conceptual components
 - Input
 - Output
 - Datapath
 - Control
 - Memory



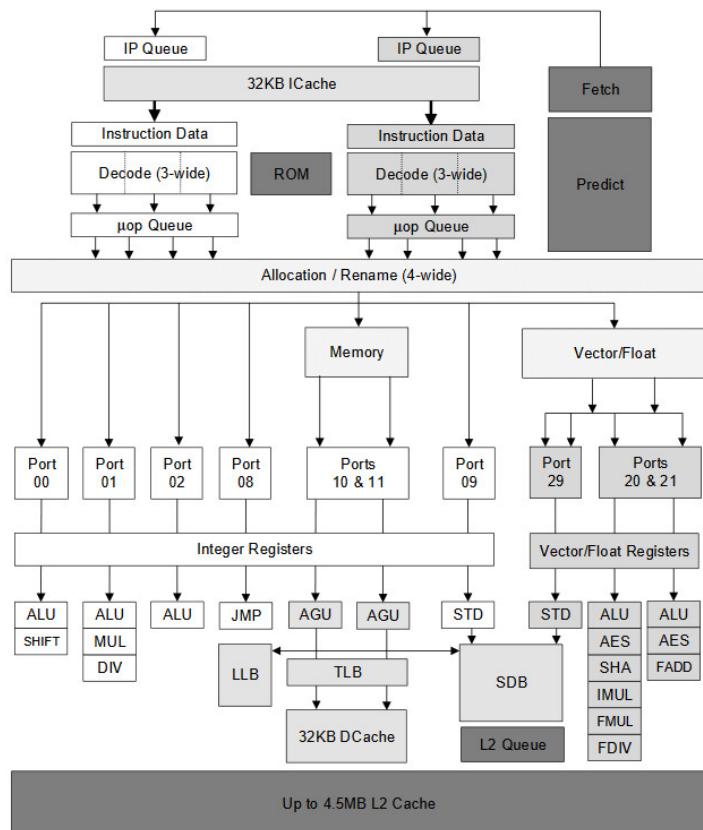
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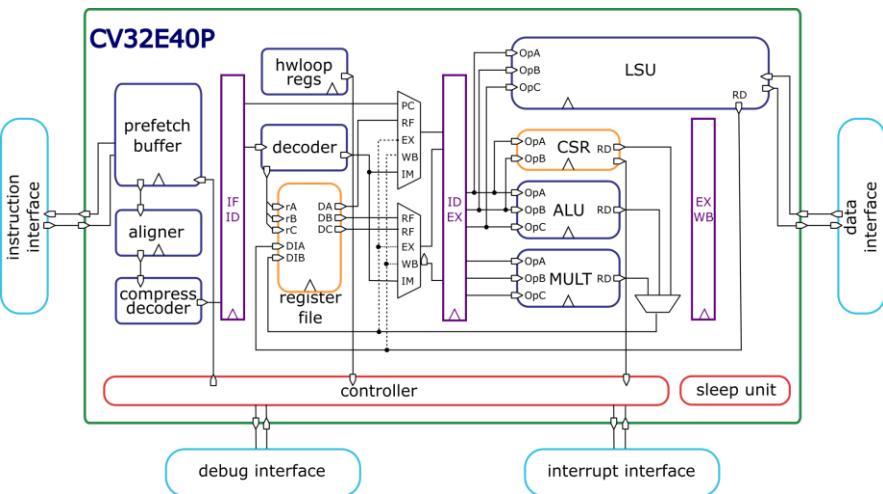
Modern Computer Architecture

- x86/x64



<https://www.techpowerup.com/267466/intel-updates-x86-x64-software-developer-manual-with-tremont-architecture-details>

- CV32E40P: 32-bit RISC-V



https://docs.openhwgroup.org/projects/cv32e40p-user-manual/en/cv32e40p_v1.0.0_doc/intro.html