

5118007-02 Computer Architecture

Ch. 3 Arithmetic for Computers

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Integer Arithmetic

- addition and subtraction
 - dealing with overflow
- multiplication
- division

Addition

- Digits are added bit-by-bit from right to left, considering carries passed from the right

$$\begin{array}{r} 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0111_{\text{two}} = 7_{\text{ten}} \\ + \quad 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0110_{\text{two}} = 6_{\text{ten}} \\ \hline = \quad 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 0000 \ 1101_{\text{two}} = 13_{\text{ten}} \end{array}$$

Subtraction

- A subtraction is basically the same as a combination of negation and addition

$$\begin{array}{r} 0000 \quad 0111_{\text{two}} = 7_{\text{ten}} \\ + \quad 1111 \quad 1010_{\text{two}} = -6_{\text{ten}} \\ \hline = \quad 0000 \quad 0001_{\text{two}} = 1_{\text{ten}} \end{array}$$

Overflow (1/2)

- An overflow occurs when the resulting value cannot be represented within given bits
 - only when adding two numbers of the same sign, and not possible when two numbers of different signs are added
- Overflow for signed numbers
 - adding two positive numbers yields a negative number
 - subtracting two negative numbers yields a positive number
 - the occurrence of overflow with add, addi, sub instructions causes an exception

Overflow (2/2)

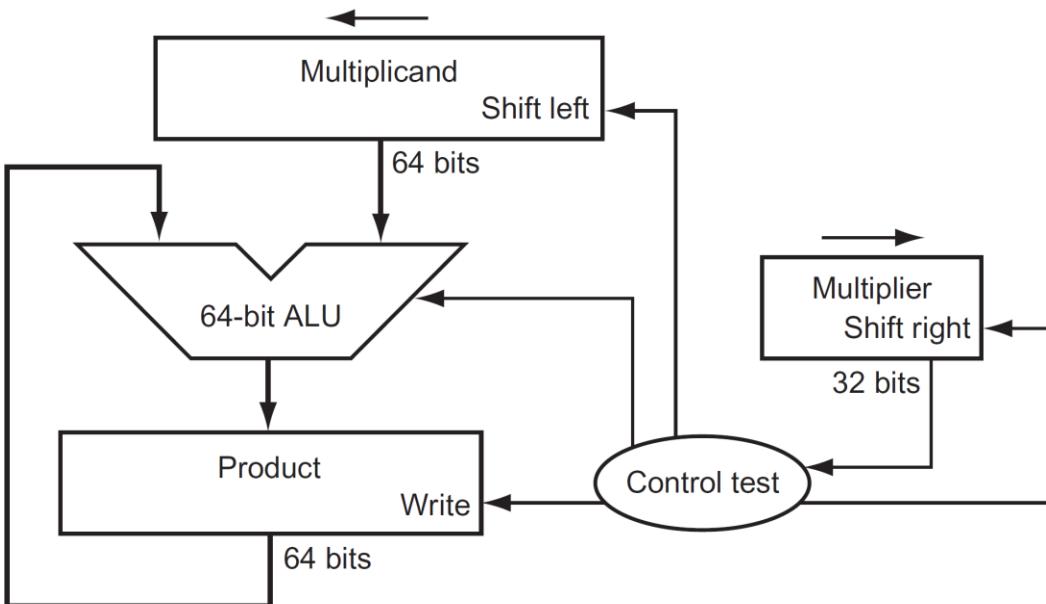
- Overflow for signed numbers
 - addition of two numbers yields a smaller number
 - subtraction of two numbers yields a greater number
 - overflow with addu, addiu, subu do not cause exception, thus C compiler uses these instructions for arithmetics.

Multiplication

$$\begin{array}{r} \text{Multiplicand} & 1000_{\text{ten}} \\ \text{Multiplier} & \times \quad \underline{1001_{\text{ten}}} \\ & 1000 \\ & 0000 \\ & 0000 \\ & 1000 \\ \hline \text{Product} & 1001000_{\text{ten}} \end{array}$$

- Basically, multiplication can be implemented as a sequential operations of right-shifts, left-shifts and additions
- Multiplication of a n -bits multiplicand and a m -bits multiplier produces a $n+m$ product
 - overflow may occur

Sequential Multiplication Hardware



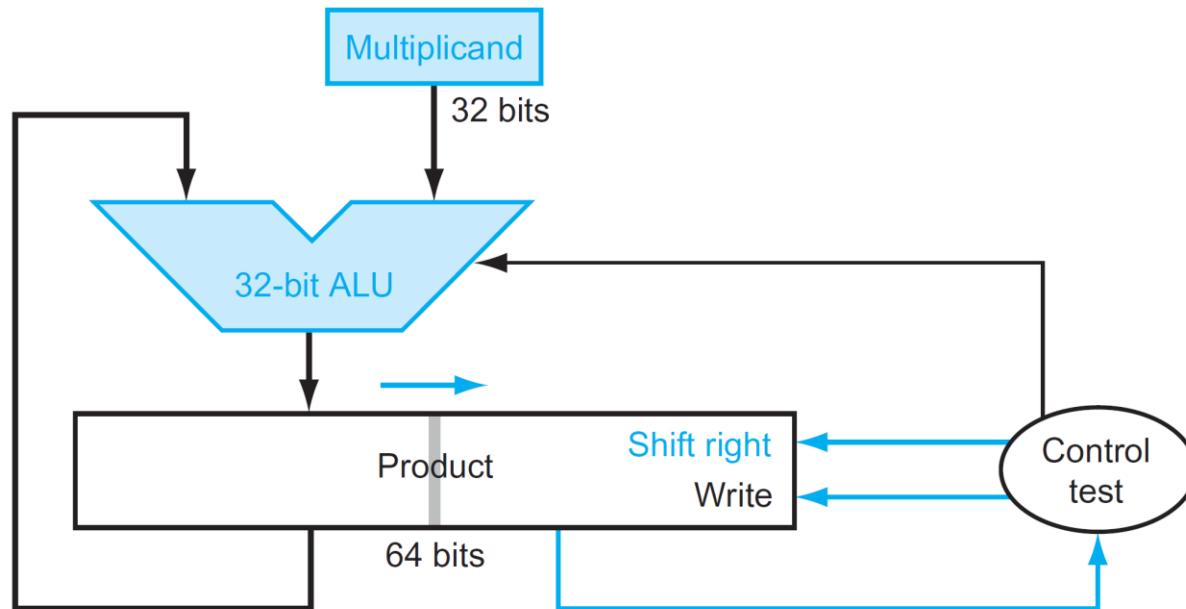
```
foreach bit of multiplier begin
    if the LSB of multiplier is 1 then
        add multiplicand and product;
    end-if
    shift-left the multiplicand ;
    shift-right a multiplier ;
end-for
```

Example

- Multiply $0010_{(2)}$ and $0011_{(2)}$

Iteration	Step	Multiplier	Multiplicand	Product
0	Initial values	001①	0000 0010	0000 0000
1	1a: 1 \Rightarrow Prod = Prod + Mcand	0011	0000 0010	0000 0010
	2: Shift left Multiplicand	0011	0000 0100	0000 0010
	3: Shift right Multiplier	000①	0000 0100	0000 0010
2	1a: 1 \Rightarrow Prod = Prod + Mcand	0001	0000 0100	0000 0110
	2: Shift left Multiplicand	0001	0000 1000	0000 0110
	3: Shift right Multiplier	000①	0000 1000	0000 0110
3	1: 0 \Rightarrow No operation	0000	0000 1000	0000 0110
	2: Shift left Multiplicand	0000	0001 0000	0000 0110
	3: Shift right Multiplier	000①	0001 0000	0000 0110
4	1: 0 \Rightarrow No operation	0000	0001 0000	0000 0110
	2: Shift left Multiplicand	0000	0010 0000	0000 0110
	3: Shift right Multiplier	000①	0010 0000	0000 0110

Refined Version



Signed Multiplication

- Naive approach
 - store the signs of multiplicand and multiplier respectively
 - convert them to positive numbers
 - perform multiplication
 - apply the proper sign to the product
- Interestingly, the aforementioned multiplication algorithm works sound for two's complements
 - https://pages.cs.wisc.edu/~markhill/cs354/Fall2008/beyond354/int_mult.html

No Thinking Method

- sign-extend to both multiplicand and multiplier before multiplication

$$\begin{array}{r} 1111 \ 1111 \\ \times \ 1111 \ 1001 \\ \hline 11111111 \\ 00000000 \\ 00000000 \\ 11111111 \\ 11111111 \\ 11111111 \\ + \ 11111111 \\ \hline 1 \ 00000000111 \end{array}$$

$$\begin{array}{r} -1 \\ \times \ -7 \\ \hline 7 \end{array}$$

WRONG !
0011 (3)
 $\times 1011 (-5)$

0011
0011
0000
+ 0011

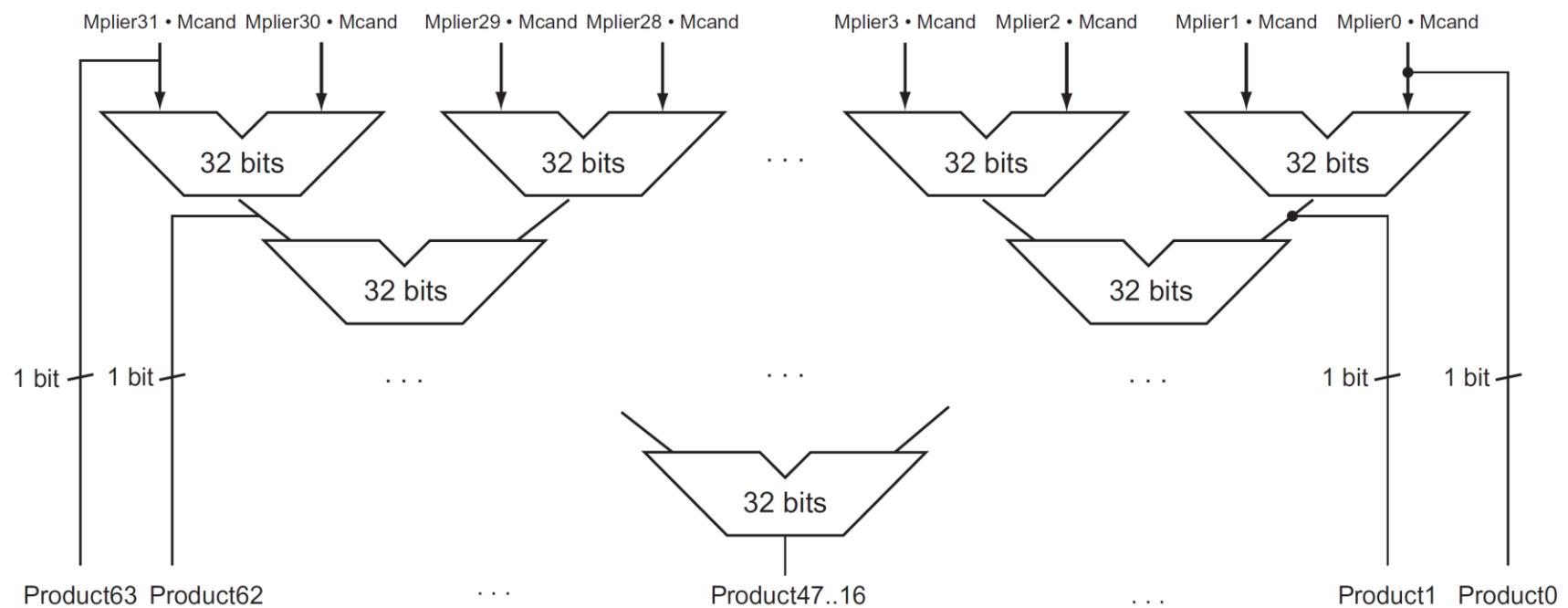
0100001
not -15 in any representation!

Sign extended:
0000 0011 (3)
 $\times 1111 \ 1011 (-5)$

00000011
00000011
00000000
00000011
00000011
00000011
00000011
+ 00000011

1011110001

Fast Multiplication with Large Circuits



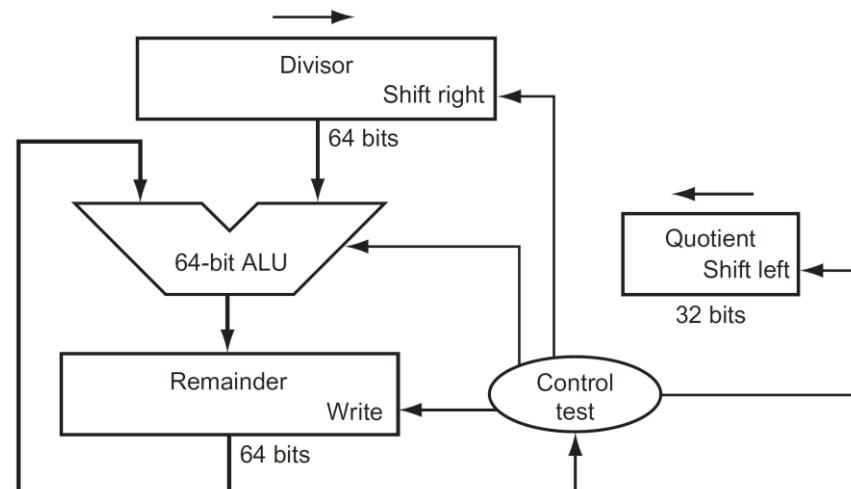
Division

- Division can be implemented as a series of shift-right, shift-left and subtraction

$$\begin{array}{r} \text{Quotient} \\ 1001_{\text{ten}} \\ \hline \text{Divisor } 1000_{\text{ten}} \overline{)1001010_{\text{ten}}} \\ -1000 \\ \hline 10 \\ 101 \\ 1010 \\ -1000 \\ \hline 10_{\text{ten}} \end{array}$$

Dividend

Remainder



Example: $0111_{(2)}$ / $0010_{(2)}$

Iteration	Step	Quotient	Divisor	Reminder
0	Initial values	0000	0010 0000	0000 0111
1	1: Rem = Rem – Div	0000	0010 0000	①110 0111
	2b: Rem < 0 \Rightarrow +Div, sll Q, Q0 = 0	0000	0010 0000	0000 0111
	3: Shift Div right	0000	0001 0000	0000 0111
2	1: Rem = Rem – Div	0000	0001 0000	①111 0111
	2b: Rem < 0 \Rightarrow +Div, sll Q, Q0 = 0	0000	0001 0000	0000 0111
	3: Shift Div right	0000	0000 1000	0000 0111
3	1: Rem = Rem – Div	0000	0000 1000	①111 1111
	2b: Rem < 0 \Rightarrow +Div, sll Q, Q0 = 0	0000	0000 1000	0000 0111
	3: Shift Div right	0000	0000 0100	0000 0111
4	1: Rem = Rem – Div	0000	0000 0100	②000 0011
	2a: Rem \geq 0 \Rightarrow sll Q, Q0 = 1	0001	0000 0100	0000 0011
	3: Shift Div right	0001	0000 0010	0000 0011
5	1: Rem = Rem – Div	0001	0000 0010	②000 0001
	2a: Rem \geq 0 \Rightarrow sll Q, Q0 = 1	0011	0000 0010	0000 0001
	3: Shift Div right	0011	0000 0001	0000 0001

Faster Implementation

