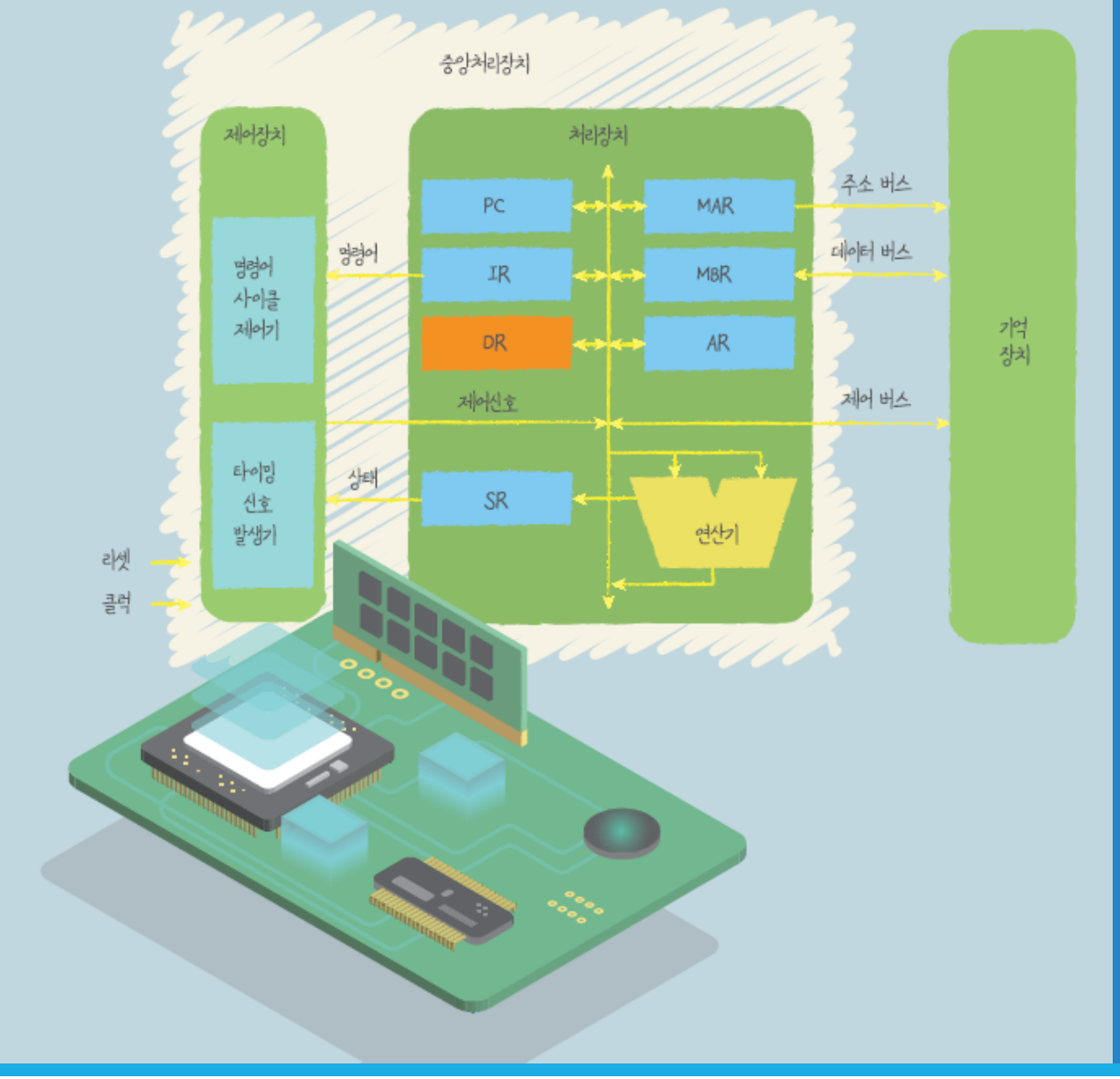
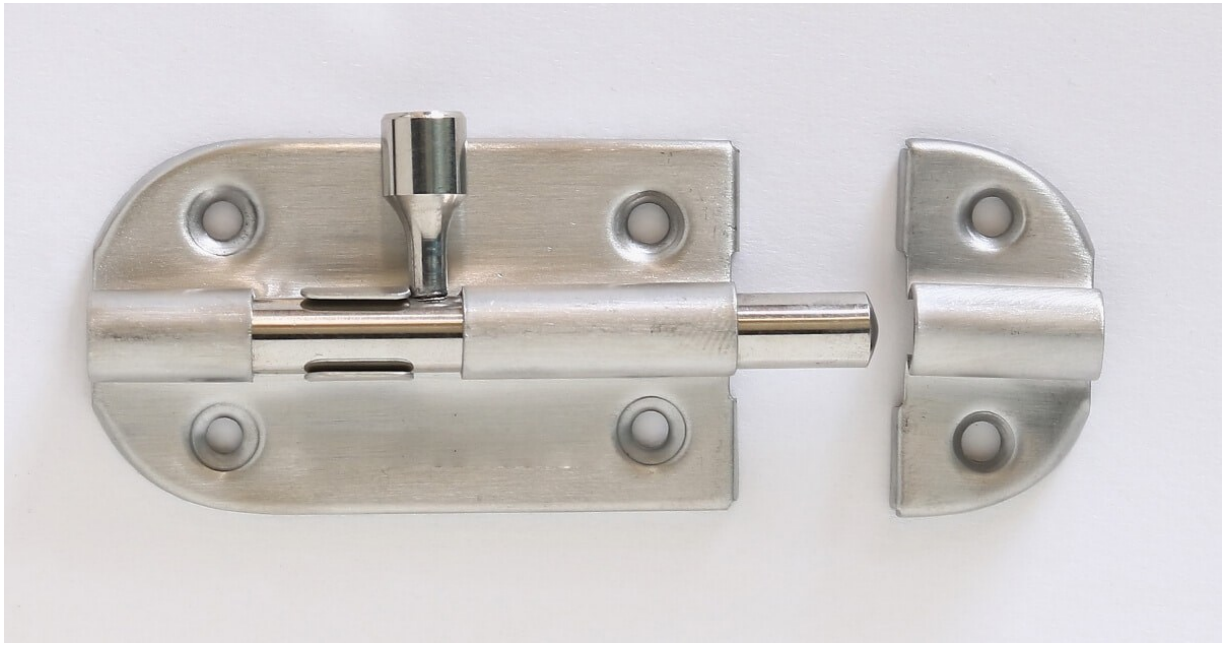


Sequential Logic

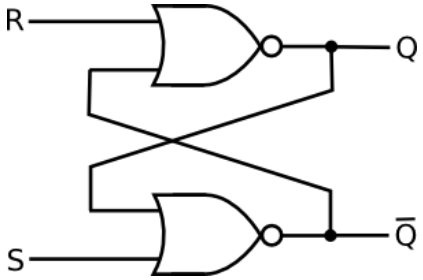
From Prof. Joongnam Jeon's lecture slides

Latch

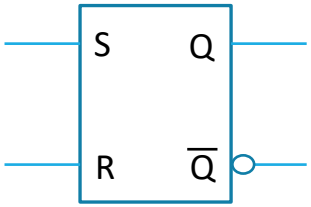
- one-bit memory device



NOR Latch

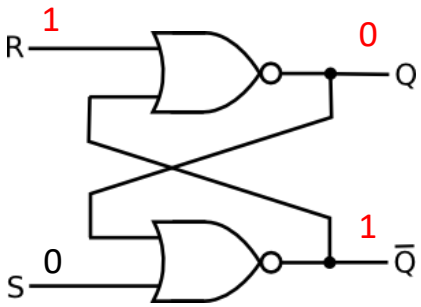


(a) NOR 래치 구조

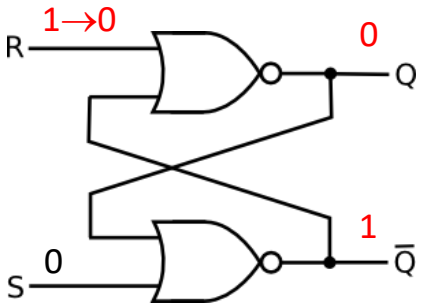


(b) 블록도

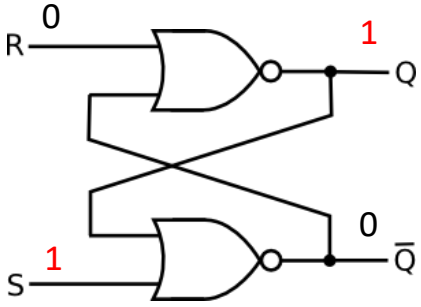
S	R	Q	동작 설명
0	0	Q_0	steady
0	1	0	0 (reset)
1	0	1	1 (set)
1	1	-	unused



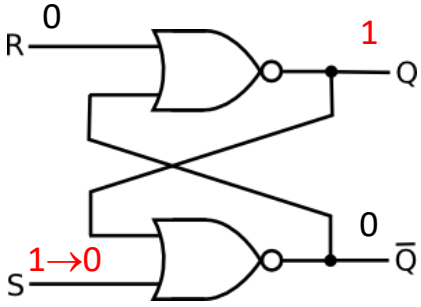
(a) 리셋



(b) 리셋 유지

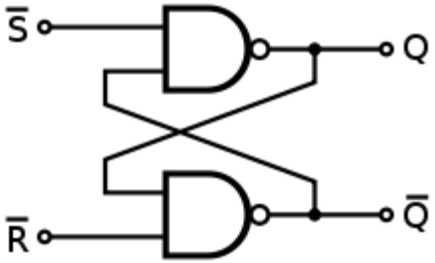


(c) 셋

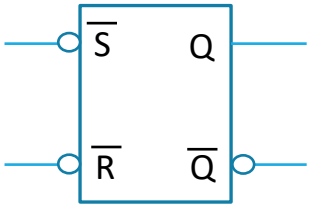


(d) 셋 유지

NAND Latch

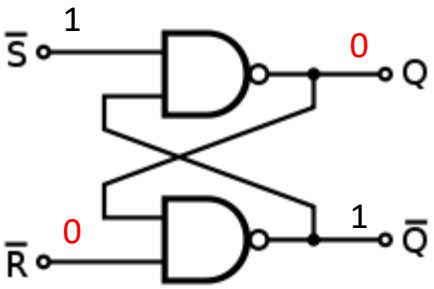


(a) NAND 래치 구조

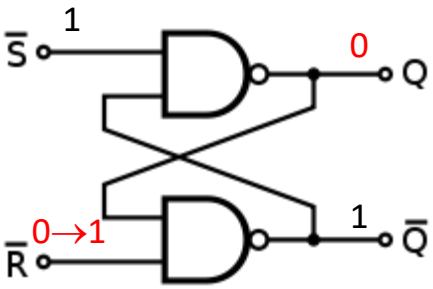


(b) 블록도

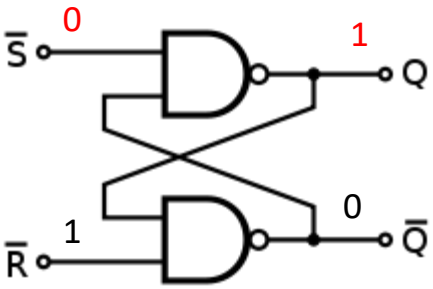
/S	/R	Q	동작 설명
1	1	Q_0	steady
1	0	0	0 (reset)
0	1	1	1 (set)
0	0	-	Not available



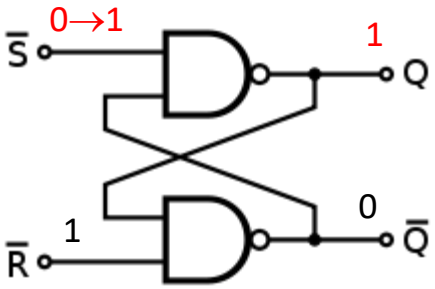
(a) 리셋



(b) 리셋 유지

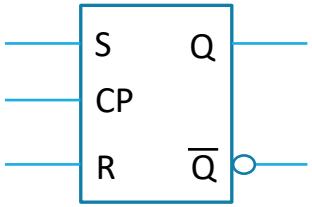


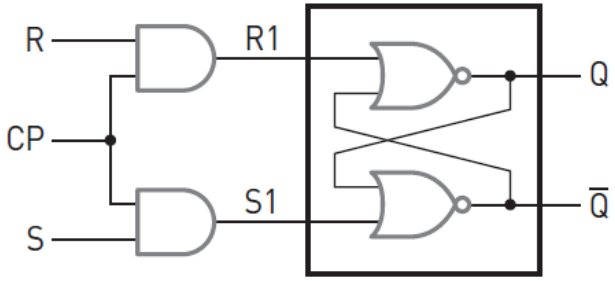
(c) 셋

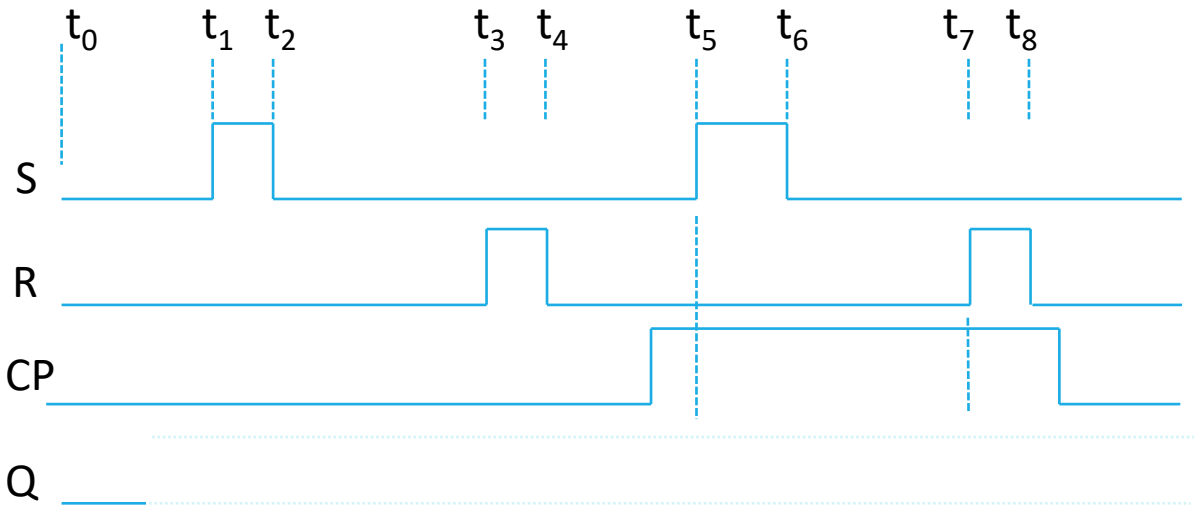


(d) 셋 유지

Clocked SR latch

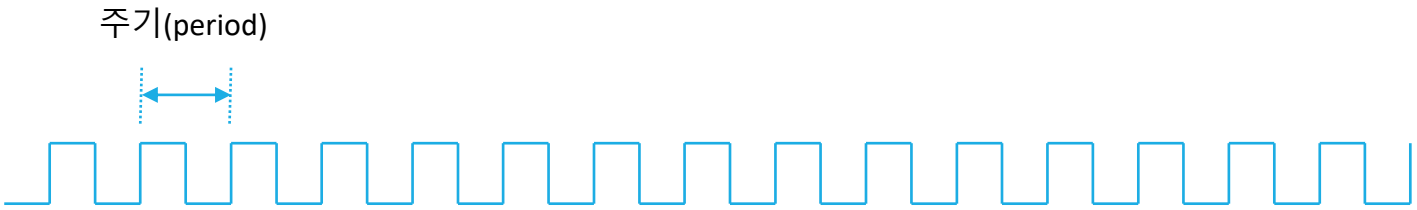




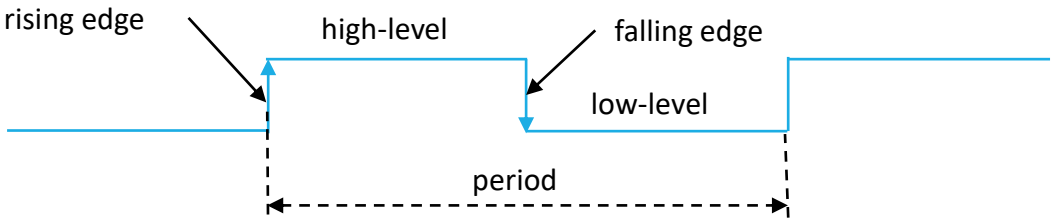


Clock Pulse

- Oscillator: generate periodic pulse
  - alternate 0 and 1 repeatedly
- Period: a time interval between two adjacent rising edges
- Frequency = 1/Period

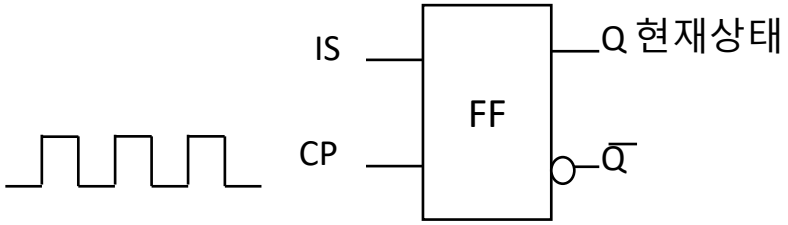


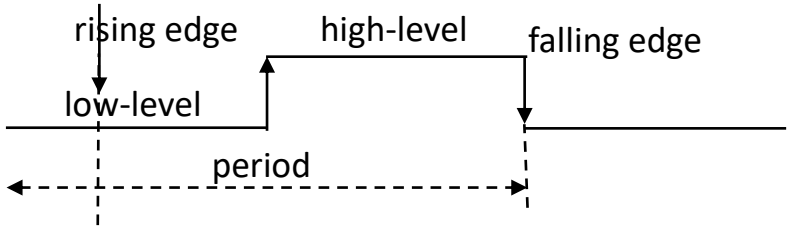
(a) 클럭 펄스



(b) 한 주기

Flip-Flop

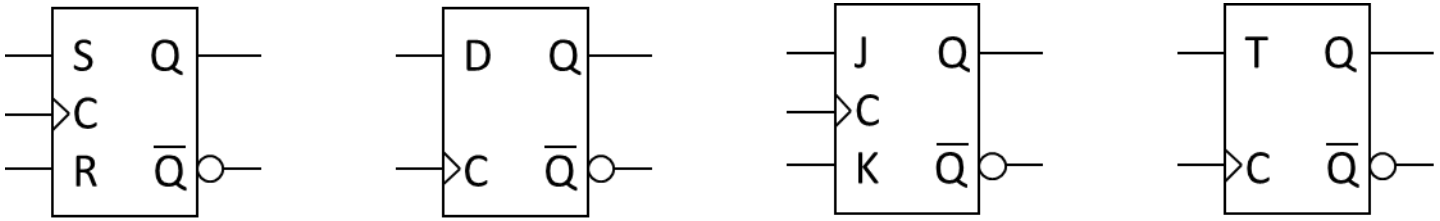




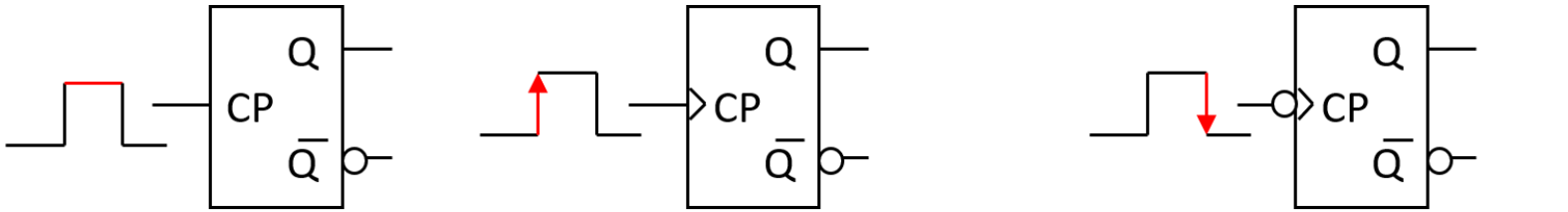
- Flip-flop
  - one-bit memory
  - the current state is the input signal at the latest clock rise
  - after the clock rise, the state is updated as the input signal

Different Types of Flip-Flop

- By control signal: SR-FF, D-FF, JK-FF, T-FF
- By clock pulse: Rising-edge, Falling-edge

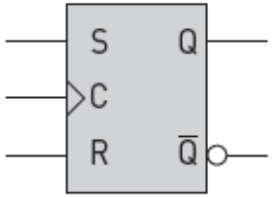


(a) SR-FF (b) D-FF (c) JK-FF (d) T-FF



(a) Latch or Level Trigger (b) Positive Edge Trigger (c) Negative Edge Trigger

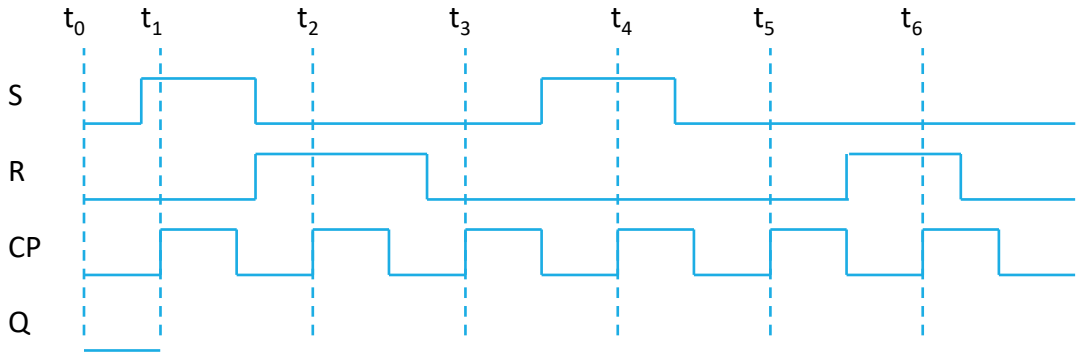
SR-플립플롭



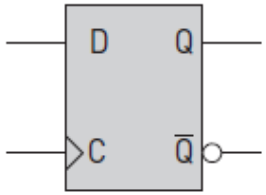
[그림 5-13] SR-플립플롭

SR-FF 특성표

CP	S	R	Q(t+1)	설명
↑	0	0	Q(t)	
↑	0	1	0	
↑	1	0	1	
↑	1	1	-	



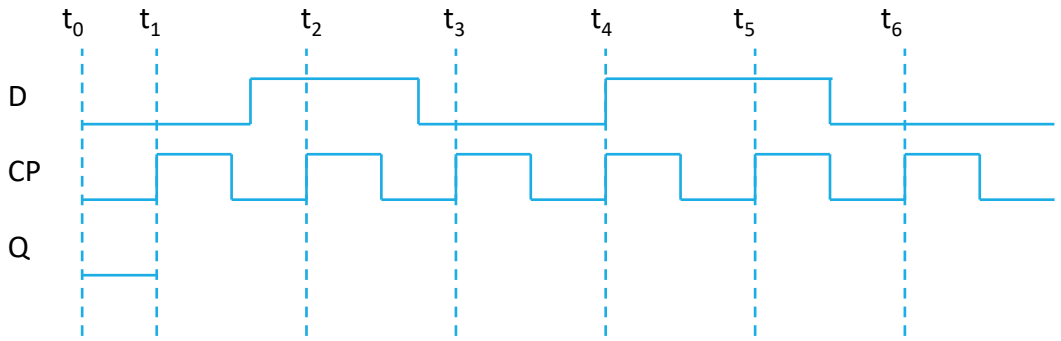
D-플립플롭



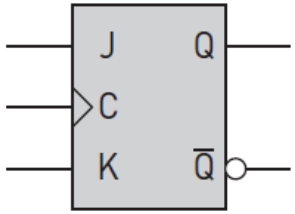
[그림 5-15] D-플립플롭

D-FF 특성표

CP	D	Q(t+1)	설명
↑	0	0	
↑	1	1	



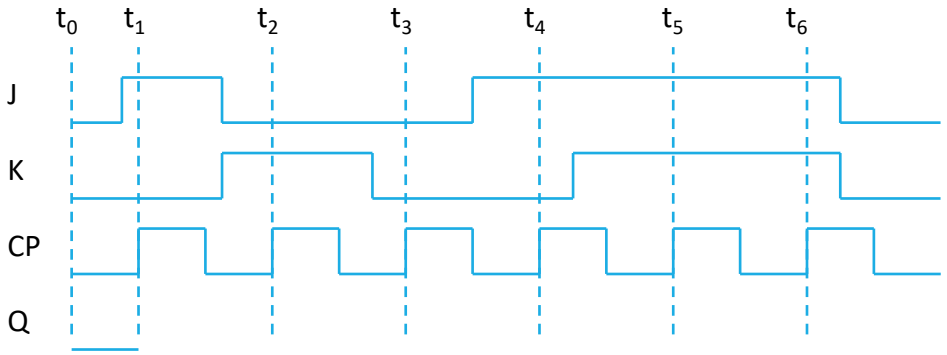
JK-플립플롭



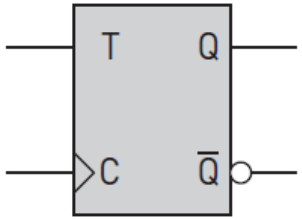
[그림 5-17] JK-플립플롭

JK-FF 특성표

CP	J	K	Q(t+1)	설명
↑	0	0	$Q(t)$	
↑	0	1	0	
↑	1	0	1	
↑	1	1	$\overline{Q(t)}$	



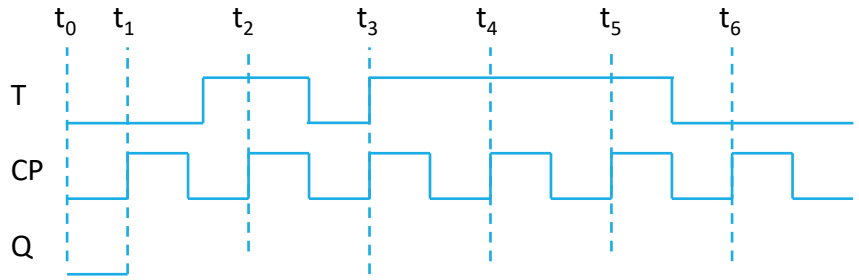
T-플립플롭



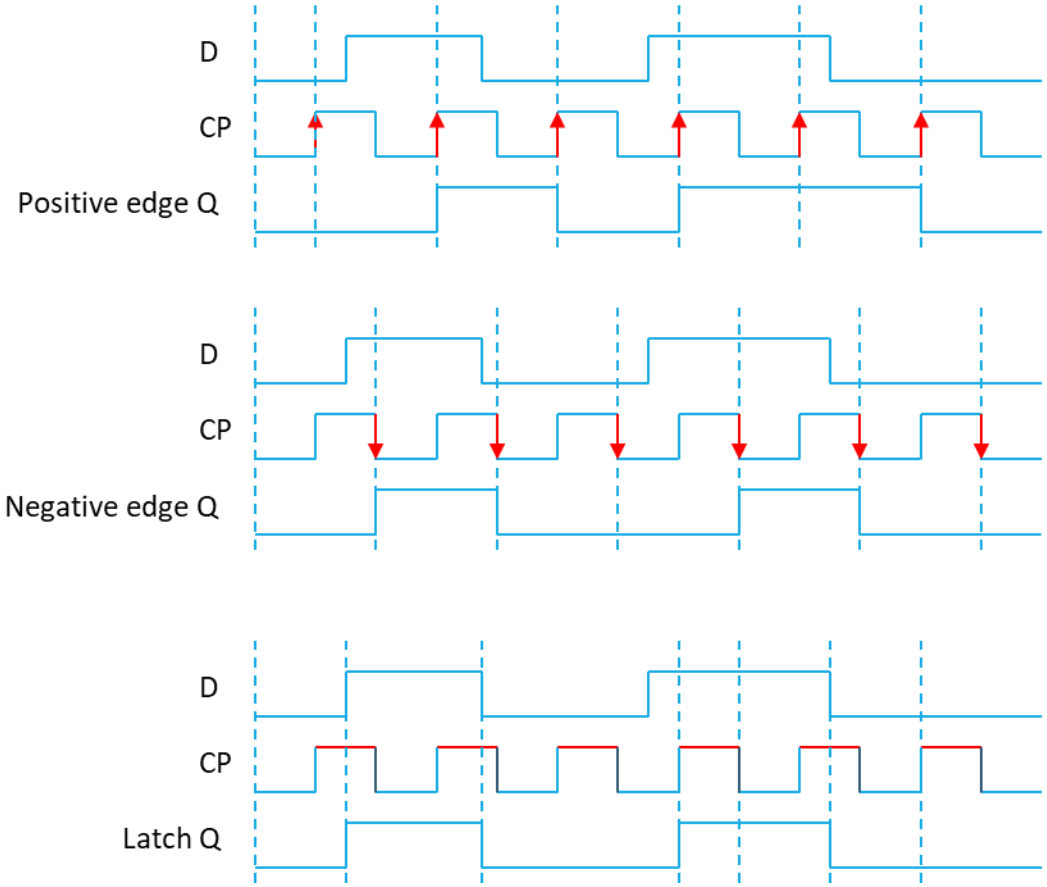
[그림 5-19] T-플립플롭

T-FF 특성표

CP	T	Q(t+1)	설명
↑	0	$Q(t)$	
↑	1	$\overline{Q(t)}$	

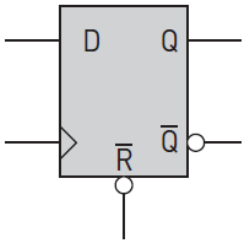


Latch vs. Flip-flop



Asynchronous Reset

- synchronous control: update only with clock pulse signal
- asynchronous control: update with or without clock pulse signal



[그림 5-21] 리셋 기능이 있는 D-플립플롭

/R	CP	D	Q	설명
0	x	x	0	Async .reset
1	↑	0	0	Clear
1	↑	1	1	Set