

COMPUTER ORGANISATIONAL AND ARCHITECTURE LABORATORY ASSIGNMENT

ASSIGNMENT - 3

Design Report

Group no - 13

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PART 1

[Unsigned Array Multiplier]

Hardware Requirements:

LUT6	29	LUT
LUT4	15	LUT
OBUF	12	IO
IBUF	12	IO
LUT2	9	LUT
LUT3	2	LUT
LUT5	1	LUT

Path Delays

Max setup time:

Fanout:10	From:b[1]	To:product[10]	Total Delay:6.906ns	Logic Delay:3.320ns	Net Delay:3.586ns
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Max hold time:

Fanout:15	From:a[1]	To:product[6]	Total Delay:1.888ns	Logic Delay:1.382ns	Net Delay:0.506ns
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PART 2

[Unsigned Left-Shift Sequential Multiplier]

Hardware Requirements:

OBUF	36	IO
FDRE	30	Flop & Latch
IBUF	14	IO
LUT2	12	LUT
LUT3	10	LUT
CARRY4	3	CarryLogic
LUT1	1	LUT
BUFG	1	Clock

Path Delays

Max setup time:

Fanout:13	From:A/Q_reg[0]/C	To:Qa[0]	Total Delay:2.946ns	Logic Delay:2.512ns	Net Delay:0.434ns
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Max hold time:

Fanout:4	From:A/Q_reg[9]/C	To:product_reg[1]/CE	Total Delay:0.231ns	Logic Delay:0.100ns	Net Delay:0.131ns
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PART 3

[Unsigned Right-Shift Sequential Multiplier]

Hardware Requirements:

FDRE	19	Flop & Latch
IBUF	14	IO
OBUF	13	IO
LUT4	11	LUT
LUT2	9	LUT
LUT3	6	LUT
FDSE	3	Flop & Latch
CARRY4	2	CarryLogic
LUT5	1	LUT
LUT1	1	LUT
BUFG	1	Clock

Path Delays

Max setup time:

Fanout:3	From:Count_reg[0]/C	To:Run	Total Delay:3.407ns	Logic Delay:2.533ns	Net Delay:0.854ns
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Max hold time:

Fanout:6	From:Count_reg[0]/C	To:Count_reg[0]/D	Total Delay:0.283ns	Logic Delay:0.164ns	Net Delay:0.119ns
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