COMPUTER ORGANISATIONAL AND ARCHITECTURE LABORATORY ASSIGNMENT

ASSIGNMENT - 2

Design Report

Group no - 13
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PART 1
[Ripple Carry Adder]

Hardware Requirements:

IBUF 17 IO
OBUF 9 IO
LUT5 8 LUT
LUT6 3 LUT
LUT4 3 LUT
LUT3 1 LUT

Critical Path Delay: 4.784 ns

Obtained from setup time:

Path 1	Levels:6	Routes:7	Fanout:3	From:a[0]	To: sum[7]	Total Delay: 4.784 ns	Logic Delay: 3.131 ns	Net Delay: 1.653 ns	Source clock: Input port clock

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PART 2
[Hybrid Adder]

Hardware Requirements:

IBUF 17 IO
OBUF 9 IO
LUT5 8 LUT
LUT6 3 LUT
LUT4 3 LUT
LUT3 1 LUT

Critical Path Delay: 4.766 ns

Obtained from setup time:

Path1	Levels:6	Routes:7	Fanout:4	From :cin	To: cout	Total Delay: 4.766 ns	Logic Delay: 3.113 ns	Net Delay: 1.653 ns	Source clock: Input port clock

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PART 3
[Bit Serial Adder]

Hardware Requirements:

FDRE 27 Flop & Latch
IBUF 18 IO
LUT3 15 LUT
OBUF 10 IO
LUT4 3 LUT
LUT1 2 LUT
FDSE 2 Flop & Latch
LUT6 1 LUT

LUT5 1 LUT
LUT2 1 LUT
BUFG 1 Clockp

Critical Path Delay: 3.407 ns

Obtained from setup time:

Path 1	Levels:3	Routes:3	Fanout:6	From: Count_reg[0]/C	To: cout	Total Delay: 3.407 ns	Logic Delay: 2.553 ns	Net Delay: 0.854 ns	
