COMPUTER ORGANISATIONAL AND ARCHITECTURE LABORATORY ASSIGNMENT

ASSIGNMENT - 5

Design Report

Group no - 13
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PART 1
[4-bit ALU]

Hardware Requirements:

LUT6	21	LUT
IBUF	14	IO
LDCE	12	Flop & Latch
LUT5	11	LUT
OBUF	7	IO
LUT4	7	LUT
LUT2	6	LUT
MUXF7	3	MuxFx
LUT3	2	LUT
BUFG	1	Clock

Path Delays

Max setup time:

High Fanout: 4

Levels: 5

Routes: 6

From: cin

To: F[3]

Total Delay: 5.309

Logic Delay: 3.451

Net Delay: 1.858

Max hold time:

High Fanout: 8

Levels: 2

Routes: 3

From: A[0]

To: T1_reg[0]/D

Total Delay: 0.368

Logic Delay: 0.122

Net Delay: 0.246

PART 2
[16-bit ALU]

Hardware Requirements:

Name	Slice LUTs	Slice Registers	F7 Muxes	Bonded IOB	BUFGCT RL
ALU_16bit	156	48	12	55	1
A1	37	12	3	0	0
A2	34	12	3	0	0
A3	34	12	3	0	0
A4	35	12	3	0	0

Path Delays

Max setup time:

High Fanout: 7

Levels: 7

Routes: 7

From: A1/T2_reg[1]/G

To: F[14]

Total Delay: 6.262

Logic Delay: 3.079

Net Delay: 3.184

Max hold time:

High Fanout: 8

Levels: 2

Routes: 3

From: A[0]

To: A1/T2_reg[0]/D

Total Delay: 0.368

Logic Delay: 0.122

Net Delay: 0.246

PART 3
[Carry Select Adder]

Hardware Requirements:

IBUF	33	IO
OBUF	17	IO
LUT5	16	LUT
LUT3	9	LUT
LUT6	6	LUT
LUT4	6	LUT

Path Delays

Max setup time:

High Fanout: 5
Levels: 6
Routes: 7
From: b[10]
To: sum[15]
Total Delay: 6.060
Logic Delay: 3.510
Net Delay: 2.550

Max hold time:

High Fanout: 6
Levels: 3
Routes: 4
From: a[12]
To: sum[12]
Total Delay: 1.905
Logic Delay: 1.413
Net Delay: 0.492

PART 4
[Carry Save Adder]

Hardware Requirements:

IBUF	144	IO
LUT3	106	LUT
LUT5	77	LUT
LUT6	62	LUT
OBUF	21	IO
LUT2	12	LUT
LUT4	4	LUT

Path Delays

Max setup time:

High Fanout: 5

Levels: 9

Routes: 10

From: a8[4]

To: sum[13]

Total Delay: 8.301

Logic Delay: 3.663

Net Delay: 4.638

Max hold time:

High Fanout: 4

Levels: 5

Routes: 6

From: a7[12]

To: sum[15]

Total Delay: 2.302

Logic Delay: 1.471

Net Delay: 0.832
