

Take Home Assignment 2

1. /* Including header files */

```
#include <stdio.h>
```

```
#include <stdlib.h>
```

```
#include <unistd.h>
```

```
#include <sys/wait.h>
```

```
#include <sys/shm.h>
```

```
#include <sys/types.h>
```

/* for vfork() syscall */

/* for wait() syscall */

/* function to count the number of words in a file pointed
by file descriptor file */

/* Using '\n' and ' ' as indicator of word separators */

```
int countWords(FILE *file) {
```

```
    int count = 0, seen = 0;
```

```
    char character;
```

```
    while ((character = fgetc(file)) != EOF) {
```

```
        if (character == ' ' || character == '\n' || character ==  
            '=' || character == '#' || character == '.' || character ==  
            '?' || character == '(') seen = 1;  
        else if (seen) {
```

```
            count++; // counting # of characters
```

```
            seen = 0; } }
```

end

~~return count;~~

```
if (seen)
    count++;
return (count); /* Returning No. of characters */
```

int main() {

```
int pid, word_count = 0; /* process id & word count */
FILE *current_file = fopen ("test.txt", "r");
pid = vfork();
```

```
if (pid == -1)           /* Error in forking process */
    exit (-1);
else if (pid == 0)        /* Child process */
{
```

```
word_count = countWords (current_file);
```

```
printf ("Child process found that number of words
is : %d\n", word_count);
```

```
exit (0);
```

```
} else                  /* Parent process */
```

```
wait (NULL);
```

```
printf ("Total Number of words: %i\n", word_count);
```

2.

- (a) FCFS - Does not discriminate in favour of short processes.
Process that request CPU first is allocated CPU first. Ready list is maintained as FIFO queue. Hence if a process with large CPU burst comes first, it is allocated the CPU until it releases CPU voluntarily irrespective of if all other upcoming processes are of shorter CPU burst.
- (b) RR - Does not discriminate in favour of short processes.
Ready queue is a circular queue. So processes are allocated CPU in the order in which they come in a circular manner for time slice. So it does not favor shorter processes in any way.
- (c) Multi-level feedback Queue - discriminates in favor of short-processes. Long running processes move to lower priority queues which are executed only when all higher priority queues have completed execution and are empty. This delays the CPU allocation for long processes.

(i)

3. (a) Given, 10 processes = $P_1, P_2 \dots$

P_{10} [order in which they are present in ready queue]

Computation time of each loop = 50 msec

I/O operation takes 200 msec

Time slice = 50 msec \Rightarrow 1 loop of a process P_i can be computed in one time slice.

Scheduling overhead = 3 msec

Following Round Robin algorithm,

Response time for the 1st iteration = $(3 + 50)i$ [$i=1, 2, 10$]

↑ ↑
 scheduling time
 overhead slice

Then 1st loop enters into I/O operation and P_{i+1} is scheduled and so onii) Response time for i th iteration = $(53)i$ for i th process
 $i = [1, 10]$ Santt chart-

0 3 53 53 10 10 10

Pi leaves CPU at $(53)i$ for 1st loop

after

$$(53 \times 10) - 200$$

$$= 330 \text{ ms}$$

So 2nd iteration of P_i starts

$$473 + 12 + 10 + 10$$

∴ Response time in the 1st and subsequent iteration
for all processes = 330 ms.

(b) Time slice = 20 msec

For 1st iteration:

$$(10 \times 23 + 10 \times 23 + 13) \text{ msec}$$

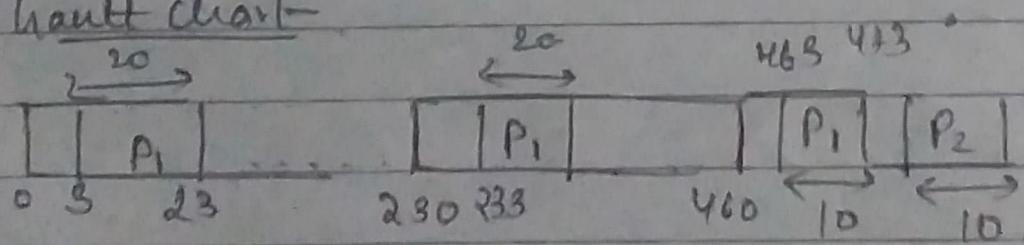
↓ ↓
 10 = processes 10 + 3
 23 = 20 + 3 ↑
 time overhead ↓
 slice the iteration has only 10 msec left
 for computation

For i th power,

$$(10 \times 23 + 10 \times 23 + 13i) = (\underline{\underline{460 + 13i}}) \text{ msec}$$

∴ Response time in the first iteration = $(460 + 13i)$ msec
for process P_i
 $(473, 486, \dots \text{ msec})$

(iii) Hantt chart



∴ 2nd process is ready 13 s after the 1st process finishes I/O
Similarly 3rd process is ready 26 sec after 1st process finishes I/O

Finally, arrival time = $13(i-1)$ for $i=[1, 10]$

arrival time.

$$473 - \underbrace{13(i-1)}_{\text{arrival time}} + 13(i-1) \\ = 473 \text{ msec for all processes.}$$

4. (a) (i) FCFS

	P1	P2	P3	P4	P5	
0	4	5	13	17	19	→ (in ms)

(ii) SJF

	P1	P2	P3	P5	P4	
0	4	5	13	15	19	→ (in ms)

(iii) pre-emptive SJF

	P1	P2	P1	P1	P3	P4	P5	P4	P3	
0	2	3	4	5	6	7	9	12	19	→ (in ms)

(iv) RR (with time quantum = 2)

	P1	P2	P1	P3	P4	P5	P3	P4	P3	
0	2	3	5	7	9	11	13	15	19	→ (in ms)

(b) (i) For FCFS,

P₁ P₂ P₃ P₄ P₅

$$\text{Average turnaround time} = \frac{(4-0)+(5-2)+(13-4)+(17-6)+(19-7)}{5}$$

$$= \frac{39}{5} = 7.8 \text{ ms}$$

For SJF, $P_1 = 4 - 0 = 4 \text{ ms}$ $P_4 = 19 - 6 = 13 \text{ ms}$
 $P_2 = 5 - 2 = 3 \text{ ms}$ $P_5 = 15 - 7 = 8 \text{ ms}$
 $P_3 = 13 - 4 = 9 \text{ ms}$

Average turnaround time = $\frac{4 + 3 + 9 + 13 + 8}{5} = \frac{37}{5}$
 $= 7.4 \text{ ms}$

For pre-emptive SJF,

$P_1 = 5 - 0 = 5 \text{ ms}$ $P_4 = 12 - 6 = 6 \text{ ms}$
 $P_2 = 3 - 2 = 1 \text{ ms}$ $P_5 = 9 - 7 = 2 \text{ ms}$
 $P_3 = 19 - 4 = 15 \text{ ms}$

Average turnaround time = $\frac{5 + 1 + 15 + 6 + 2}{5} = \frac{29}{5} = 5.8 \text{ ms}$

For RR,

$P_1 = 5 - 0 \text{ ms} = 5 \text{ ms}$; $P_4 = 15 - 6 \text{ ms} = 9 \text{ ms}$
 $P_2 = 3 - 2 \text{ ms} = 1 \text{ ms}$; $P_5 = 11 - 7 \text{ ms} = 4 \text{ ms}$
 $P_3 = 19 - 4 \text{ ms} = 15 \text{ ms}$

Average turnaround time = $\frac{5 + 1 + 15 + 9 + 4}{5} = \frac{34}{5} = 6.8 \text{ ms}$

4.(b)(c)ii) For FCFS,

$P_1 = 0 - 0 = 0 \text{ ms}$, $P_2 = 4 - 2 = 2 \text{ ms}$, $P_3 = 5 - 4 = 1 \text{ ms}$

$$P_4 = 13 - 6 = 7 \text{ ms}$$

$$P_5 = 17 - 7 = 10 \text{ ms}$$

$$\therefore \text{Average Waiting time} = \frac{0+2+1+7+10}{5} = 4 \text{ ms}$$

For SJF,

$$P_1 = 0 - 0 = 0 \text{ ms}$$

$$P_2 = 4 - 2 = 2 \text{ ms}$$

$$P_3 = 5 - 4 = 1 \text{ ms}$$

$$P_4 = 15 - 6 = 9 \text{ ms}$$

$$P_5 = 13 - 7 = 6 \text{ ms}$$

$$\therefore \text{Average Waiting time} = \frac{0+2+1+9+6}{5} = \underline{\underline{3.6 \text{ ms}}}$$

For preemptive SJF,

$$P_1 = (3-2) + (0-0) = 1 \text{ ms}$$

$$P_2 = (2-2) = 0 \text{ ms}$$

$$P_3 = (12-6) + (5-4) = 7 \text{ ms}$$

$$P_4 = (9-7) + (6-6) = 2 \text{ ms}$$

$$P_5 = (4-7) = 0 \text{ ms}$$

$$\text{Average Waiting time} = \frac{1+0+7+2+0}{5} = 2 \text{ ms}$$

For RR,

$$P_1 = (3-2) + (0-0) = 1 \text{ ms}$$

$$P_2 = (2-2) = 0 \text{ ms}$$

$$P_3 = (15-13) + (11-7) + (5-4) = 7 \text{ ms}$$

$$P_4 = (13-9) + (7-6) = 5 \text{ ms}$$

$$P_5 = (9-7) = 2 \text{ ms}$$

$$\text{Average Waiting time} = \frac{1+0+7+5+2}{5} = \frac{15}{5} = 3 \text{ ms}$$

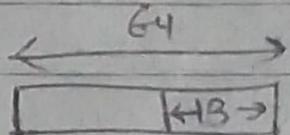
5. (a) $\text{RAM} = 128 \text{ kB} = 2^{37} \text{ bytes}$

Given, Page size = 8 kB = 2^{13} bytes

\therefore No. of frames in RAM (physical Memory) = $\frac{2^{37}}{2^{13}}$ bytes

$$\left[\frac{\text{RAM size}}{\text{Page size}} \right] = 2^{24} \text{ frames}$$

Given, 64 bit address space is used.



\therefore Logical address space has 2^{64} byte memory locations.

$$\begin{aligned} \therefore \text{No. of entries in the page table} &= \frac{2^{64}}{2^{13}} \quad \left. \begin{array}{l} \text{logical space} \\ \text{Page size} \end{array} \right\} \\ &= \underline{\underline{2^{51}}} \end{aligned}$$

Each page table entry contains frame no. of RAM.

All frame no. range from (0 to $2^{24}-1$) = 24 bits needed

\therefore Each page table entry is of 24 bits = 3 bytes

$$\therefore \text{Total page table size} = \underline{\underline{3 \times 2^{51} \text{ bytes}}}$$

[Ignoring valid-invalid bit and dirty bit]

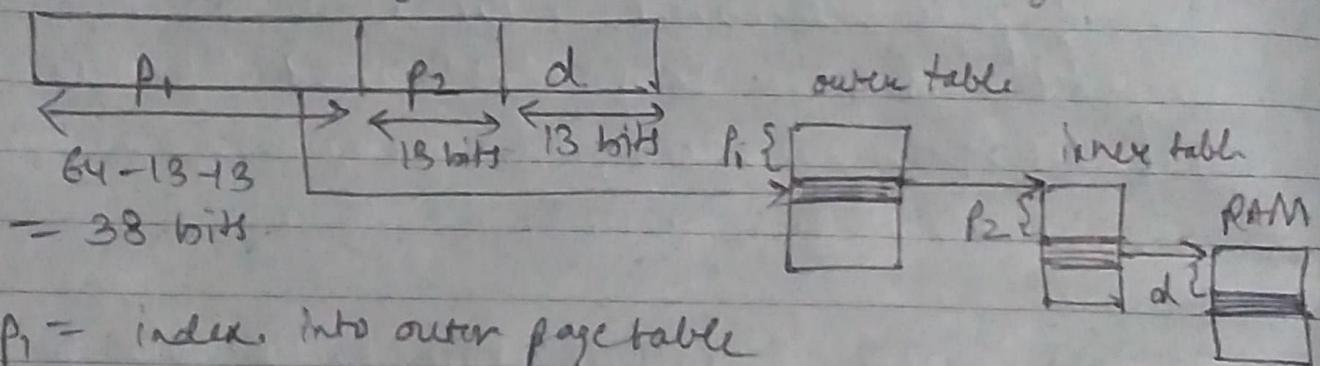
$$5.(b) \text{ RAM} = 128 \text{ GB} = 2^{37} \text{ bytes}$$

$$\text{Given page size} = 8 \text{ KB} = 2^{13} \text{ bytes}$$

$$\therefore \# \text{ of frames in RAM} = \frac{\text{RAM size}}{\text{Page size}} = \frac{2^{37}}{2^{13}} = 2^{24} \text{ frames.}$$

logical address space = 64 bits

Dividing address space into p_1 (page number of outer table), p_2 (page number of inner table) and d (page offset)



p_1 = index into outer page table

p_2 = index into inner page table

d = offset of frame in RAM

\therefore No. of entries in inner page table = 2^{13}

Each entry size in inner page table = ~~24~~ 24 bits

(1 byte frame = 2^{24})

≈ 3 bytes

\therefore Size of inner page table = (3×2^{13}) bytes = 24 KB

No. of entries in outer page table = 2^{38}

Each entry size in outer page table = 13 bits

(as inner page table
has 2^{13} entries)

~ 2 bytes

∴ Size of outer page table = 2×2^{38} bytes

$$= 2^{39} \text{ bytes.} = \underline{\underline{512 \text{ GB}}}$$

∴ Total size of outer and inner = $\underline{\underline{(2^{39} + 3 \times 2^{13})}}$ bytes
page tables

$$= 512 \text{ GB} + 24 \text{ kB}$$

$$\sim \underline{\underline{512 \text{ GB}}}$$

6. (a)

PAGE NO.

DATE: / /

Following Algorithms can be used to minimise page faults.

- Least Frequently Used (LFU): Replace page having smallest count of (number of references made to it).
(Implemented in software level)
- Most Frequently Used (MFU): Replace page that is referenced maximum number of times. A page with smaller count is yet to be used. (Implemented on software level)
- Least Recently Used (LRU): Associate time of last use with each page and replace page that has not been used in the most amount of time. (Implemented on software level)
- Optimal Algorithm: Replace page that will not be used for the longest period of time. (Implemented on software level)

→ thrashing: From busy swapping pages in and out. Minimising thrashing minimises page fault rate. (Software)

→ Locality Model: Allocate enough frames to a process to accommodate its current locality. Minimises thrashing, hence minimises page fault rate. (Software)

→ Working-Set Model: Using page replacement depending upon the working-set value of a process (total number of pages referenced in the recent recent working-set window). Do if total demand of frames across all $P_i >$ memory size, thrashing occurs. So suspend or swap out one of the processes. (Software)

→ Page fault frequency: Page fault rate varies with the number of frames for process. Maintain rate between upper and lower bound (acceptable rate) to allow enough frames of the process to be in memory. (Software)

(b) → Dirty bit: Associate dirty bit with each page to know if a page has been modified while in memory. Supports deciding if the page needs to be swapped out before replacing it as swapping out has overhead, thus decreasing time of page fault. (Software)

→ Swap Space : Using swap space avoids the access from the disk directly. Data transfer rate is comparatively lower. When bringing pages from Swap space decreases the extra overhead from the disk.
(Hardware implementation)

7.

Suppose process P causes a page fault, then

- a) trap is sent to the operating system
- b) Save the user registers and process state of P
- c) determine that the interrupt was a page fault
- d) Check that the page reference is legal and determine location of page on disk
- e) Change state of process P to waiting
- f) Issue a read from the disk after checking for free frame
- g) if there is no free space, Select page of another process Q as victim page
- h) if the dirty bit of victim page is 1, write frame to disk
- i) Now issue a read from the disk for desired page of P
- j) While P is waiting, allocate CPU to some other process
- k) Issue an interrupt from the disk I/O subsystem as reading page is completed
- l) Save the registers and process state of the other process that was running
- m) determine that the interrupt was from disk
- n) Change the valid bit to '1' for the victim page in the page table of Q.
- o) Change the valid bit to 'v' for the page that causes page fault in the page table of P and assign ^{victim} frame no. to the entry.
- p) Wait for the CPU to be allocated to P again
- q) When P is allocated again to CPU, restore the user registers, process state and new page table of P and then resume the

PAGE NO.

DATE: / /

interrupted instruction. Mal-caused page fault.