

CMOS Static RAM 16K (2K x 8-Bit)

IDT6116SA IDT6116LA

Features

- High-speed access and chip select times
 - Military: 20/25/35/45/55/70/90/120/150ns (max.)
 - Industrial: 20/25ns (max.)
 - Commercial: 15/20/25ns (max.)
- Low-power consumption
- Battery backup operation
 - 2V data retention voltage (LA version only)
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- **◆** Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in ceramic 24-pin DIP, ceramic and plastic 24-pin Thin Dip and 24-pin SOIC
- Military product compliant to MIL-STD-833, Class B

Description

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using high-performance, high-reliability CMOS technology.

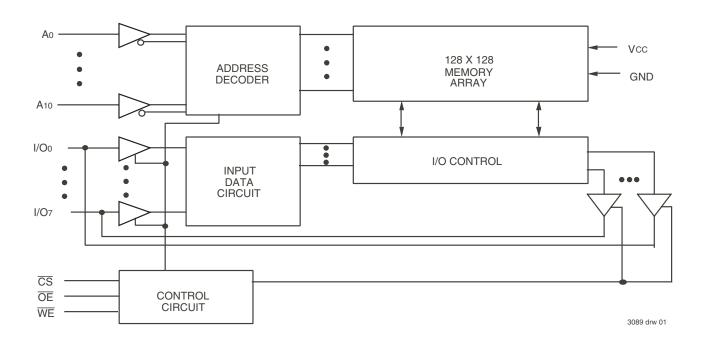
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When \overline{CS} goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as \overline{CS} remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only $1\mu W$ to $4\mu W$ operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT6116SA/LA is packaged in 24-pin 300mil plastic DIP, 24-pin 600mil and 300mil ceramic DIP, or 24-lead gull-wing SOIC providing high board-level packing densities.

Military grade product is manufactured in compliance to MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

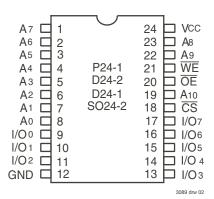
Functional Block Diagram



FEBRUARY 2013

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Pin Configurations



DIP/SOIC Top View

Pin Description

Name	Description
A0 - A10	Address Inputs
I/O0 - I/O7	Data Input/Output
<u>CS</u>	Chip Select
WE	Write Enable
ŌĒ	Output Enable
Vcc	Power
GND	Ground

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Capacitance (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
Cvo	I/O Capacitance	Vout = 0V	8	pF

NOTF.

3089 tbl 03

 This parameter is determined by device characterization, but is not production tested

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
Та	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
Tstg	Storage Temperature	-55 to +125	-65 to +150	°C
Рт	Power Dissipation	1.0	1.0	W
Іоит	DC Output Current	50	50	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS
 may cause permanent damage to the device. This is a stress rating only and
 functional operation of the device at these or any other conditions above those
 indicated in the operational sections of this specification is not implied. Exposure
 to absolute maximum rating conditions for extended periods may affect
 reliability.
- 2. VTERM must not exceed Vcc +0.5V.

Truth Table⁽¹⁾

TI GUI TGDIO	<u> </u>			
Mode	<u>cs</u>	ŌĒ	WE	I/O
Standby	Н	Х	Х	High-Z
Read	L	L	Н	DATAout
Read	L	Н	Н	High-Z
Write	L	Х	L	DATAIN

NOTE:

1. H = VIH, L = VIL, X = Don't Care.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5 ⁽²⁾	٧
GND	Ground	0	0	0	٧
VIH	Input High Voltage	2.2	3.5	Vcc +0.5	٧
VIL	Input Low Voltage	-0.5 ⁽¹⁾	_	0.8	V

3089 tbl 0

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NOTES

- 1. VIL (min.) = -3.0V for pulse width less than 20ns, once per cycle.
- 2. VIN must not exceed Vcc +0.5V.

DC Electrical Characteristics

 $(VCC = 5.0V \pm 10\%)$

				IDT61	16SA	IDT61		
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Unit
lu	Input Leakage Current	Vcc = Max., Vin = GND to Vcc	MIL. COM'L & IND		10 5		5 2	μΑ
lto	Output Leakage Current	$V_{CC} = Max., \overline{CS} = V_{IH},$ $V_{OUT} = GND \text{ to } V_{CC}$	MIL. COM'L & IND		10 5		5 2	μΑ
Vol	Output Low Voltage	IoL = 8mA, Vcc = Min.		_	0.4		0.4	V
Vон	Output High Voltage	IOH = -4mA, Vcc = Min.		2.4	_	2.4	_	V

3089 tbl 07

DC Electrical Characteristics(1)

 $(VCC = 5.0V \pm 10\%, VLC = 0.2V, VHC = VCC - 0.2V)$

			6116SA15		SA20 LA20		SA25 LA25	
123Symbol	Parameter	Power	Com'l Only	Com'l & Ind	Mil	Com'l & Ind	Mil	Unit
ICC1	Operating Power Supply Current CS < V⊩, Outputs Open	SA	105	105	130	100	90	mA
	Vcc = Max., f = 0	LA		95	120	95	85	
ICC2	Dynamic Operating Current CS < V⊩, Outputs Open	SA	150	130	150	120	135	mA
	Vcc = Max., f = fmax ⁽²⁾	LA		120	140	110	125	
ISB	Standby Power Supply Current (TTL Level)	SA	40	40	50	40	45	mA
	$\overline{CS} \ge VIH$, Outputs Open $VCC = Max.$, $f = f_{MAX}^{(2)}$	LA	—	35	45	35	40	
ISB1	Full Standby Power Supply Current (CMOS Level)	SA	2	2	10	2	10	mA
	$\overline{CS} \ge VHC$, $VCC = Max$., $VIN \le VLC$ or $VIN \ge VHC$, $f = 0$	LA		0.1	0.9	0.1	0.9	

NOTES:

- 1. All values are maximum guaranteed values.
- 2. $f_{MAX} = 1/t_{RC}$, only address inputs are cycling at f_{MAX} , f = 0 means address inputs are not changing.

DC Electrical Characteristics $^{(1)}$ (continued) (Vcc = 5.0V \pm 10%, VLc = 0.2V, VHc = Vcc - 0.2V)

			6116SA35 6116LA35	6116SA45 6116LA45	6116SA55 6116LA55	6116SA70 6116LA70	6116SA90 6116LA90	6116SA120 6116LA120	6116SA150 6116LA150	
Symbol	Parameter	Power	Mil Only	Mil Only	Unit					
ICC1	Operating Power Supply Current, CS ≤ VIL,	SA	90	90	90	90	90	90	90	mA
Outputs Open Vcc = Max., f = 0		LA	85	85	85	85	85	85	85	
ICC2	Dynamic Operating Current, CS ≤ V _{IL} ,	SA	115	100	100	100	100	100	90	mA
Outputs Open Vcc = Max., f = fmax ⁽²⁾		LA	105	95	90	90	85	85	85	
ISB	Standby Power Supply Current (TTL Level)	SA	35	25	25	25	25	25	25	mA
	$\overline{\text{CS}} \ge \text{VIH}$, Outputs Open $\text{Vcc} = \text{Max.}$, $f = \text{fmax}^{(2)}$	LA	30	20	20	20	25	15	15	
ISB1	Full Standby Power Supply <u>Current</u> (CMOS Level), <u>CS</u> ≥ VHC,	SA	10	10	10	10	10	10	10	mA
	Vcc = Max., Vin ≤ Vlc or Vin ≥ VHC, f = 0	LA	0.9	0.9	0.9	0.9	0.9	0.9	0.9	

3089 tbl 09

- 1. All values are maximum guaranteed values.
- 2. fMAX = 1/tRC, only address inputs are toggling at fMAX, f = 0 means address inputs are not changing.

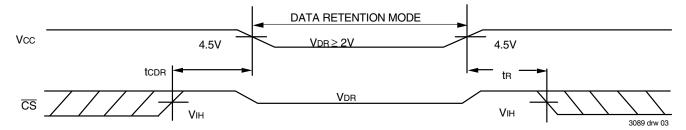
Data Retention Characteristics Over All Temperature Ranges (LA Version Only) (VLC = 0.2V, VHC = VCC - 0.2V)

						Тур. ⁽¹⁾ Vcc @		Max. Vcc @	
Symbol	Parameter	Test Condition		Min.	2.0V	3.0V	2.0V	3.0V	Unit
VDR	Vcc for Data Retention	_	_		_	_		_	V
ICCDR	Data Retention Current		MIL. COM'L.	_	0.5 0.5	1.5 1.5	200 20	300 30	μΑ
tcdr ⁽³⁾	Chip Deselect to Data Retention Time	$\overline{\text{CS}} \geq \text{VHC}$ $\text{VIN} \geq \text{VHC or } \leq$	V LC	_	0		_		ns
tR ⁽³⁾	Operation Recovery Time			trc ⁽²⁾	_	_	_	_	ns
ltul	Input Leakage Current				_		2	2	μΑ

NOTES:

- 1. $TA = + 25^{\circ}C$
- 2. tRC = Read Cycle Time.
- 3. This parameter is guaranteed by device characterization, but is not production tested.

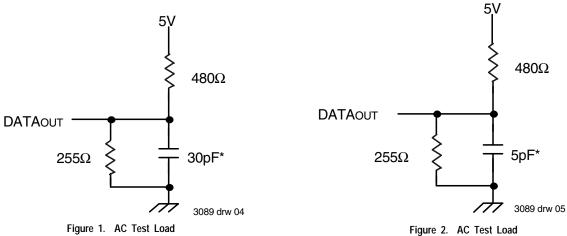
Low Vcc Data Retention Waveform



AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

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*Including scope and jig.

AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges)

		6116SA15 ⁽¹⁾		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 ⁽²⁾ 6116LA35 ⁽²⁾		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Мах.	Min.	Мах.	Unit
Read Cyc										
trc	Read Cycle Time	15	_	20	_	25		35	_	ns
taa	Address Access Time	_	15	_	19	_	25	_	35	ns
tacs	Chip Select Access Time	_	15	_	20		25	_	35	ns
tclz(3)	Chip Select to Output in Low-Z	5	_	5	_	5	_	5	_	ns
toE	Output Enable to Output Valid	_	10	_	10	_	13	_	20	ns
toLz ⁽³⁾	Output Enable to Output in Low-Z	0	_	0	_	5	_	5	_	ns
tcHZ ⁽³⁾	Chip Deselect to Output in High-Z	_	10	_	11	_	12	_	15	ns
tonz ⁽³⁾	Output Disable to Output in High-Z	_	8	_	8	_	10	_	13	ns
toн	Output Hold from Address Change	5	_	5	_	5	_	5	_	ns
tpu ⁽³⁾	Chip Select to Power Up Time	0	_	0		0	_	0	_	ns
tPD ⁽³⁾	Chip Deselect to Power Down Time	_	15	_	20	_	25	_	35	ns

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AC Electrical Characteristics ($Vcc = 5V \pm 10\%$, All Temperature Ranges) (continued)

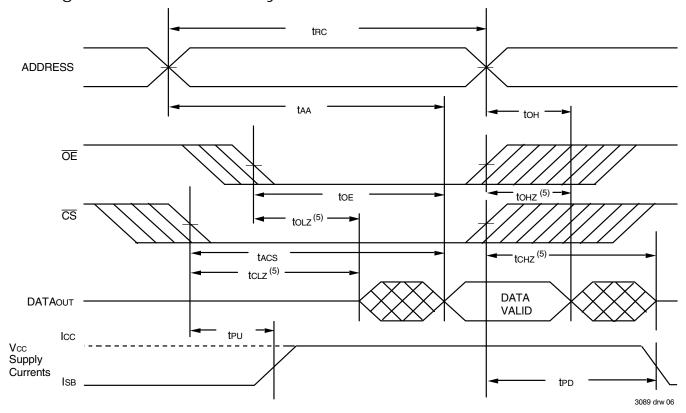
		ı	A45 ⁽²⁾	l l		6116SA70 ⁽²⁾ 6116LA70 ⁽²⁾		6116SA90 ⁽²⁾ 6116LA90 ⁽²⁾		6116SA120 ⁽²⁾ 6116LA120 ⁽²⁾		6116SA150 ⁽²⁾ 6116LA150 ⁽²⁾		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cyc	Read Cycle													
trc	Read Cycle Time	45	_	55	_	70	_	90	_	120	_	150	_	ns
taa	Address Access Time	_	45	_	55	_	70	_	90	_	120	_	150	ns
tacs	Chip Select Access Time		45	_	50	_	65		90	_	120		150	ns
tclz ⁽³⁾	Chip Select to Output in Low-Z	5	_	5	_	5	_	5	_	5	_	5	_	ns
toe	Output Enable to Output Valid	_	25		40	_	50	_	60	_	80	_	100	ns
toLZ ⁽³⁾	Output Enable to Output in Low-Z	5	_	5	_	5	_	5	_	5	_	5	_	ns
tcHZ ⁽³⁾	Chip Deselect to Output in High-Z	_	20	_	30	_	35	_	40	_	40	_	40	ns
tonz ⁽³⁾	Output Disable to Output in High-Z	_	15	_	30	_	35	_	40	_	40	_	40	ns
tон	Output Hold from Address Change	5	_	5	_	5	_	5	_	5	_	5	_	ns

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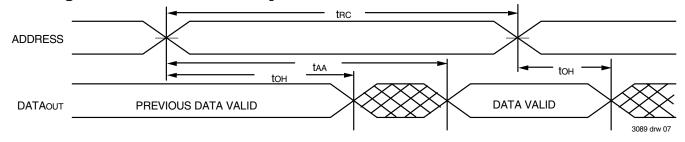
NOTES:

- 1. 0° C to +70°C temperature range only.
- 2. -55°C to +125°C temperature range only.
- 3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

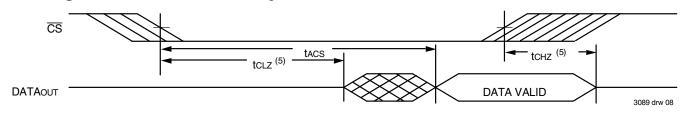
Timing Waveform of Read Cycle No. 1^(1,3)



Timing Waveform of Read Cycle No. 2^(1,2,4)



Timing Waveform of Read Cycle No. 3^(1,3,4)



NOTES:

- 1. WE is HIGH for Read cycle.
- 2. Device is continously selected, $\overline{\text{CS}}$ is LOW.
- 3. Address valid prior to or coincident with $\overline{\text{CS}}$ transition LOW.
- OE is LOW.
- 5. Transition is measured ±500mV from steady state.

AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges)

		6116SA15 ⁽¹⁾					SA25 LA25	6116SA35 ⁽²⁾ 6116LA35 ⁽²⁾		
Symbol	Parameter	Min.	Мах.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cyc	Write Cycle									
twc	Write Cycle Time	15	_	20	_	25	_	35	_	ns
tcw	Chip Select to End-of-Write	13	_	15	_	17	_	25	_	ns
taw	Address Valid to End-of-Write	14	_	15	_	17	_	25	_	ns
tas	Address Set-up Time	0	_	0	_	0	_	0	_	ns
twp	Write Pulse Width	12	_	12	_	15	_	20	_	ns
twr	Write Recovery Time	0	_	0	_	0	_	0	_	ns
twHz ⁽³⁾	Write to Output in High-Z	_	7	_	8	_	16	_	20	ns
tow	Data to Write Time Overlap	12	_	12	_	13	_	15	_	ns
tDH ⁽⁴⁾	Data Hold from Write Time	0	_	0	_	0	_	0	_	ns
tow ^(3,4)	Output Active from End-of-Write	0	_	0	_	0	_	0	_	ns

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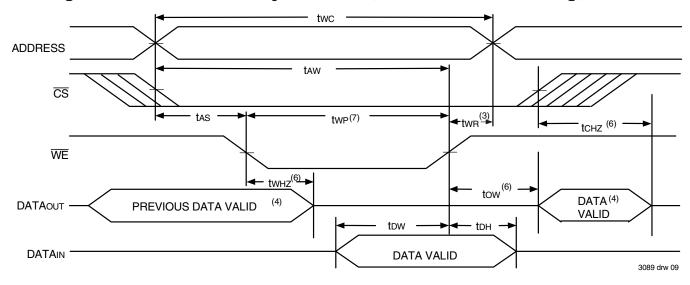
AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges)(con't)

		1	A45 ⁽²⁾	6116SA55 ⁽²⁾ 6116LA55 ⁽²⁾					A90 ⁽²⁾ A90 ⁽²⁾	6116SA120 ⁽²⁾ 6116LA120 ⁽²⁾		6116SA150 ⁽²⁾ 6116LA150 ⁽²⁾		
Symbol	Parameter	Min.	Max.	Min.	Мах.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cy	Write Cycle													
twc	Write Cycle Time	45	_	55		70	_	90	_	120		150		ns
tcw	Chip Select to End-of-Write	30	_	40	_	40	_	55	_	70	_	90	_	ns
taw	Address Valid to End-of-Write	30	_	45	_	65	_	80	_	105	_	120	_	ns
tas	Address Set-up Time	0	_	5	_	15	_	15	_	20	_	20	_	ns
twp	Write Pulse Width	25	_	40	_	40	_	55	_	70	_	90		ns
twr	Write Recovery Time	0	_	5	_	5	_	5		5	_	10		ns
twHZ ⁽³⁾	Write to Output in High-Z	_	25	_	30	_	35	_	40	_	40	_	40	ns
tow	Data to Write Time Overlap	20	_	25	_	30	_	30	_	35	_	40		ns
tDH ⁽⁴⁾	Data Hold from Write Time	0	_	5	_	5	_	5	_	5	_	10	_	ns
tow ^(3,4)	Output Active from End-of-Write	0	_	0	_	0	_	0		0	_	0		ns

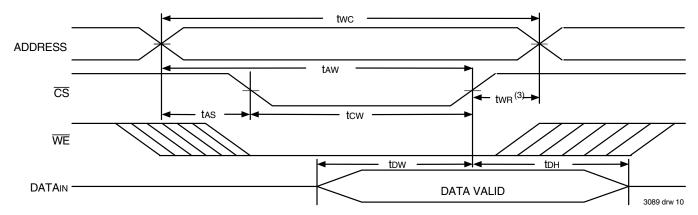
NOTES:

- 1. 0° C to $+70^{\circ}$ C temperature range only.
- 2. -55°C to +125°C temperature range only.
- 3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
- 4. The specification for toh must be met by the device supplying write data to the RAM under all operation conditions. Although toh and tow values will vary over voltage and temperature, the actual toh will always be smaller than the actual tow.

Timing Waveform of Write Cycle No. 1 (WE Controlled Timing)(1,2,5,7)



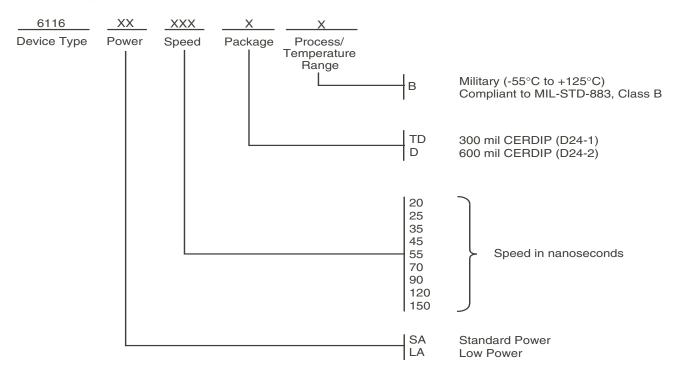
Timing Waveform of Write Cycle No. 2 (CS Controlled Timing)(1,2,3,5,7)



NOTES:

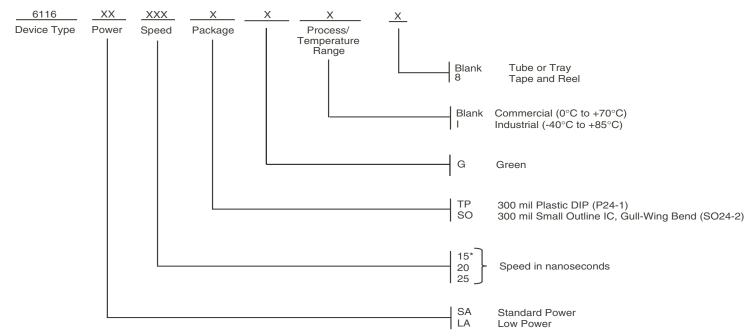
- 1. WE or CS must be HIGH during all address transitions.
- 2. A write occurs during the overlap of a LOW $\overline{\text{CS}}$ and a LOW $\overline{\text{WE}}$.
- 3. twn is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going HIGH to the end of the write cycle.
- 4. During this period, the I/O pins are in the output state and the in $\underline{\text{put}}$ signals must not be applied.
- 5. If the CS LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in the high-impedance state.
- 6. Transition is measured ±500mV from steady state.
- 7. $\overline{\text{OE}}$ is continuously HIGH. If $\overline{\text{OE}}$ is LOW during a $\overline{\text{WE}}$ controlled write cycle, the write pulse width must be the larger of twp or (tw+z + tow) to allow the I/O drivers to turn off and data to be placed on the bus for the required tow. If $\overline{\text{OE}}$ is HIGH during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse is the specified twp. For a $\overline{\text{CS}}$ controlled write cycle, $\overline{\text{OE}}$ may be LOW with no degradation to tcw.

Ordering Information — Military



3089 drw 11

Ordering Information — Commercial & Industrial



*Available in commercial temperature range and standard power only.

3089 drw 12

Datasheet Document History

01/07/00	D= 1 2 4 10	Updated to newformat
	Pg. 1, 3, 4, 10	Added Industrial Temperature range offerings
	Pg. 9, 10	Separated ordering information into military, commercial, and industrial temperature range offerings
00/00/00	Pg. 11	Added Datasheet Document History
08/09/00		Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"
12/30/03	Pg. 3,10	Corrected Industrial temp from -45C to -40C.
03/31/05	Pg. 10	Added "Restricted hazardous substance device" to ordering information.
11/15/06	Pg. 3	Changed power limits for commercial and industrial on speed grades 25ns and 35ns.
	Pg.4	Changed power limits for commercial and industrial on speed grade 45ns. Refer to
	-	PCN SR-0602-02.
04/26/11	Pg.1,2,3,4,6,10	Updated "Restricted hazardous substance device" to "Green". Obsoleted 24-pin SOJ, 24-pin 600 mil and 35ns, 45ns for Industrial & Commercial.
05/01/13	Pg. 1	Description paragraph 4, package information. Changed text to read "The IDT6116SA/LA is packaged in 24-pin 300mil plastic DIP, 24-pin 600mil and 300mil ceramic DIP, or 24-lead gull-wing SOIC providing high board-level packing densities". Removed IDT in reference to fabrication.
	Pg. 3	Updated DC Elec Chars ($Vcc = 5.0V \pm 10\%$) table by adding industrial to the Test Conditions. Updated DC Elec Chars ($Vcc = 5.0V \pm 10\%$, $VLc = 0.2V$, $VHc + Vcc - 0.2V$) table by removing the LA power for the 15ns speed.
	Pg. 10	$Removed footnote \ "*Available in 300mil packaging only" from the \textit{Military ordering information}.$



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