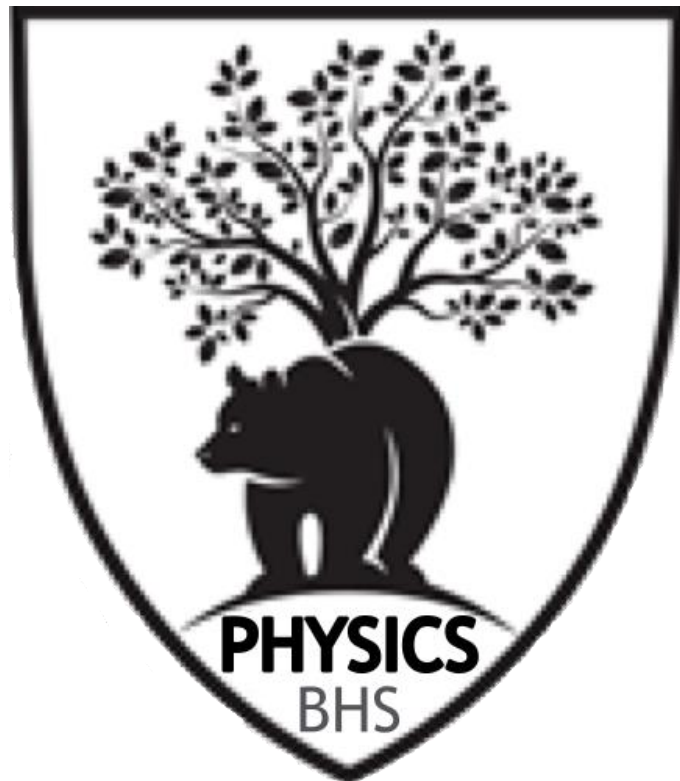


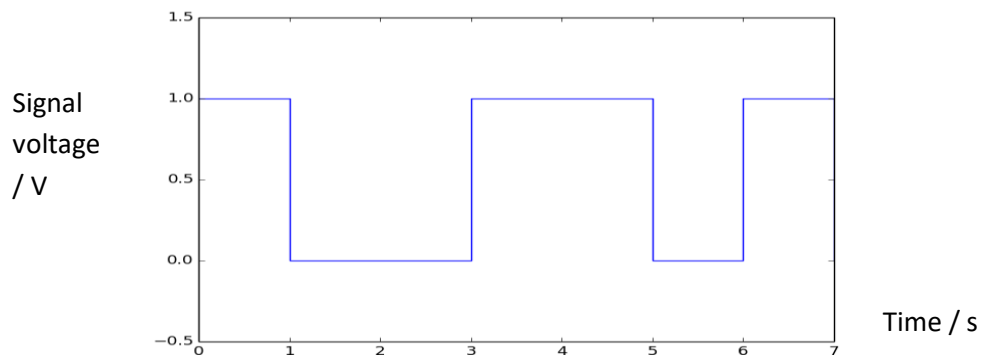
**Name:**



**Practical Electronics**  
**Block 5**  
**Logic**

# Digital Electronics (Logic Control)

Modern electronics is predominately digital electronics where there are only two values or **states** – either on or off. This is a binary system where the *on* state can be represented by a *1* or *high*. The *off* state can be represented by a *0* or *low*.

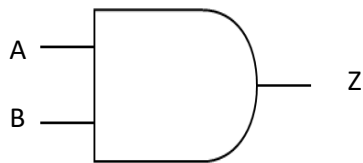


In this graph, the signal is switching between a high state (1) to a low state (0) and this switching happens almost instantly. The signal does not exist in a voltage level in between. It is a digital signal.

## LOGIC GATES

We are now going to investigate the main logic gates we will encounter in this course. The expected behaviour of the gates can be described in a truth table as shown.

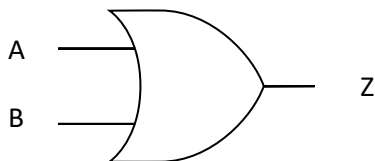
- **AND**



$Z = 1$  when  $A = 1$  **AND**  $B = 1$

A	B	Z
0	0	
0	1	
1	0	
1	1	

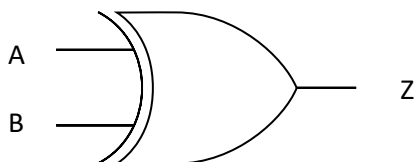
- **OR**



$Z = 1$  when either  $A = 1$  **OR**  $B = 1$  **OR** both  $= 1$

A	B	Z
0	0	
0	1	
1	0	
1	1	

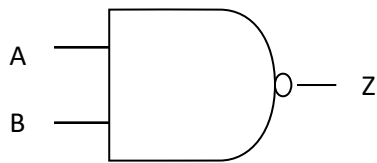
- **XOR** (Exclusively OR)



$Z = 1$  when either  $A = 1$  **OR**  $B = 1$  **but not** both  $= 1$

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

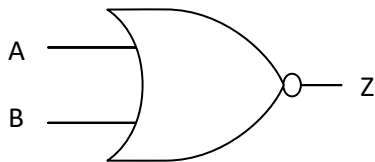
- **NAND** (not AND)



A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

$Z = 1$  when  $(A = 1 \text{ AND } B = 1)$  is not true

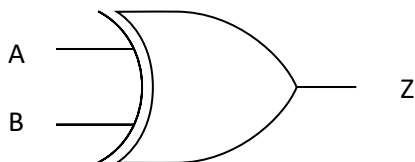
- **NOR** Gate (not OR)



A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

$Z = 1$  when  $(A = 1 \text{ OR } B = 1 \text{ OR both} = 1)$  is not true

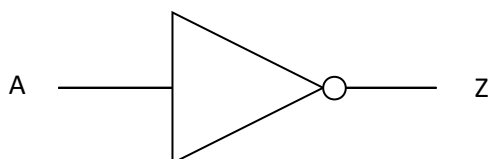
- **XNOR** Gate (Exclusively not OR)



A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

$Z = 1$  when  $(A = 1 \text{ OR } B = 1 \text{ but not both} = 1)$  is not true

- **NOT** (also known as an *inverter*)

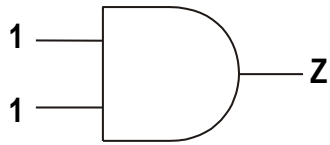


A	Z
0	
1	

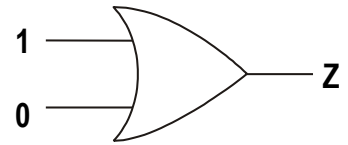
$Z = 1$  when  $A = 0$

Task: For each of the following examples, state whether the output Z is at logic 0 or logic 1.

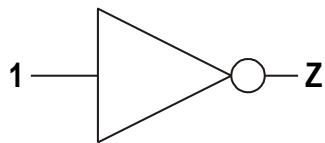
(a)



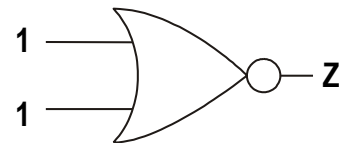
(b)



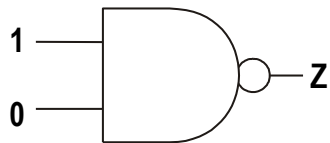
(c)



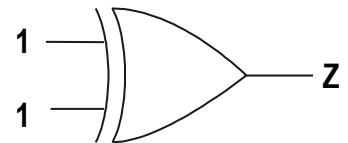
(d)



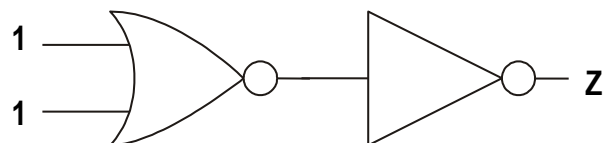
(e)



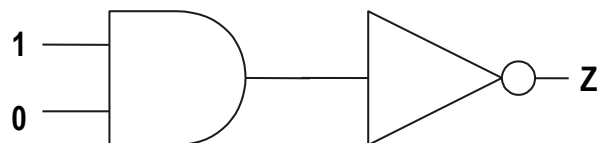
(f)



(g)



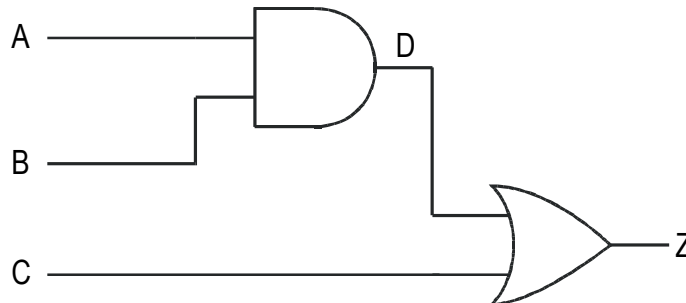
(h)



## Logic Systems

### **Worked example**

The example below shows a logic diagram that has two logic gates. There are three inputs, so this gives eight combinations in the truth table.



#### *Stage 1*

Draw up the results for point D. (This is the output from the AND gate, being fed by inputs A and B only.)

A	B	C	D	Z
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	0	
1	0	0	0	
1	0	1	0	
1	1	0	1	
1	1	1	1	

#### *Stage 2*

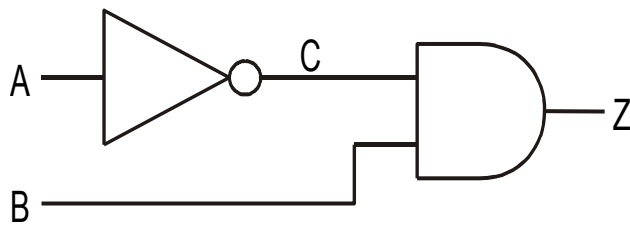
Draw up the results for point Z. (This is the output from the OR gate, being fed by output D and input C only.)

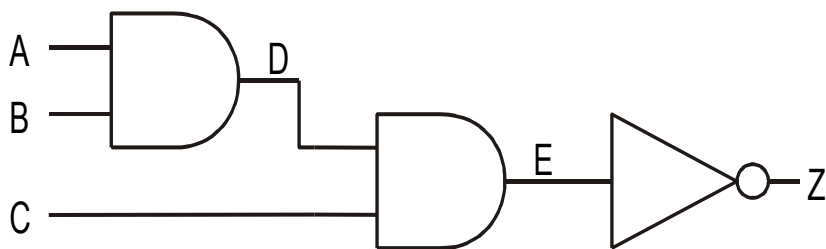
A	B	C	D	Z
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	1

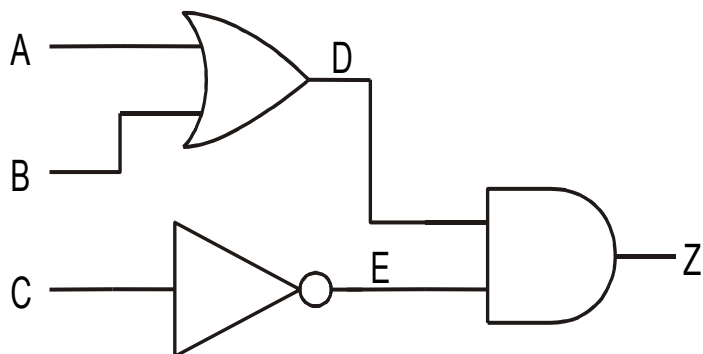
By following this technique, logic system problems can be solved easily.

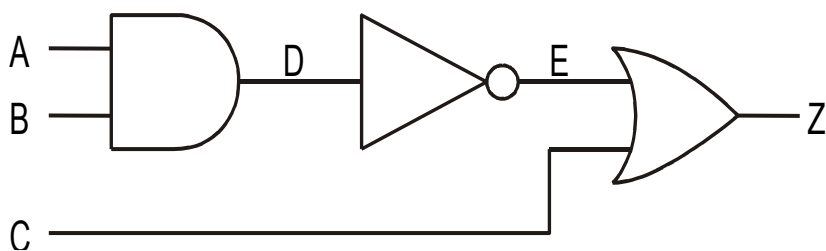
You could use a circuit simulation program to check your results.

Task: Draw up a truth table for each of the following logic systems.



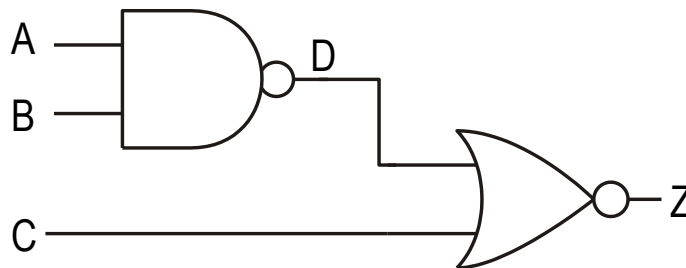




## Dealing with NAND and NOR gates in combinational logic

It can be confusing to have to remember the basic truth tables for NAND and NOR gates. However, as it is easy to remember AND and OR truth tables, we can use this to help. As we know the NAND gate is an inverted AND gate, we simply reverse (invert) the answers in the AND gate truth table to get the results for a NAND gate. We can use the same technique for NOR and OR.

### Worked example

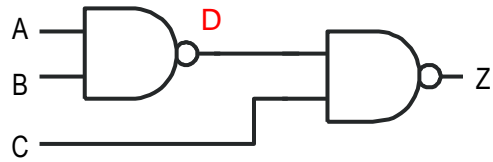
If we try and draw up the truth table for the system shown below, we must add some extra columns for the 'pretend' results.

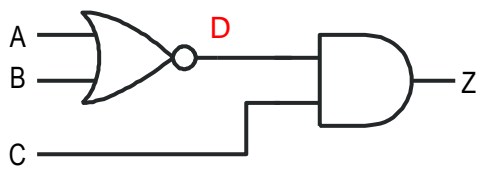


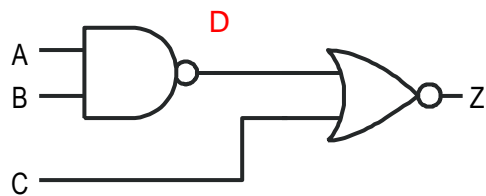
A and B feed the NAND gate, but we treat it as an AND (see the extra column of the truth table). Then, to obtain the results for D, we simply invert the results obtained in our 'pretend' column. Now, C and D feed the next gate, which is a NOR. We 'pretend' it is an OR gate (see the extra column in the truth table) and then invert the answers to obtain column Z.

Column for			Column for			
D as an			Z as an			
AND gate			OR gate			
A	B	C	A AND B	D	C OR D	Z
0	0	0	0	1	1	0
0	0	1	0	1	1	0
0	1	0	0	1	1	0
0	1	1	0	1	1	0
1	0	0	0	1	1	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	0	1	0

Task: Draw up a truth table for each of the following logic systems.




## Logic Systems for Design Problems

### Worked example

A burglar alarm system is to sound if a master switch is on and either a light beam is broken or if somebody stands on a pressure pad.

Draw a block diagram, logic diagram and a truth table for this system.

### Solution

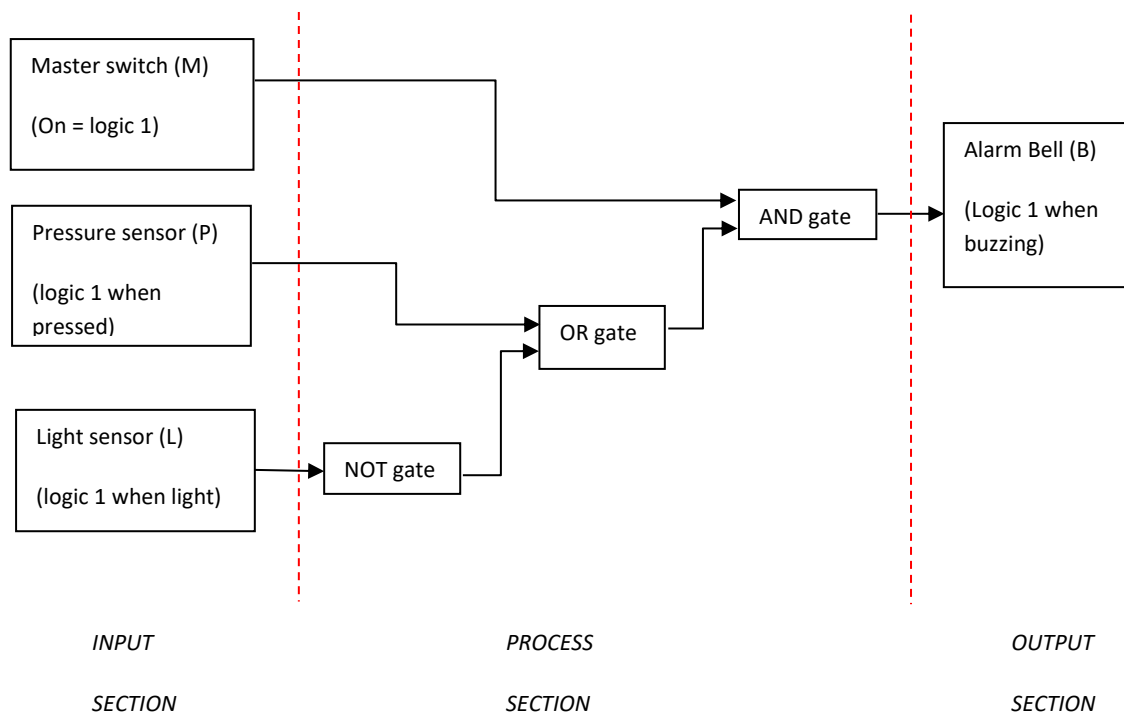
Read the specification carefully. You should notice that it has *three* inputs. These are:

- a master switch (M)
- a light sensor (L), and
- a pressure pad (P).

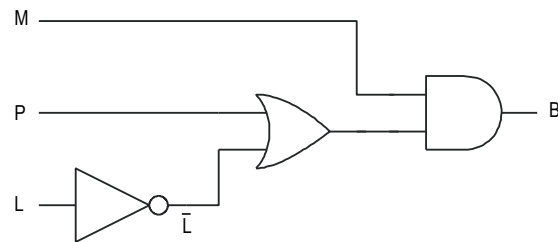
It has *one* output, an alarm bell (B).

Note: The alarm has to be triggered when the light beam is broken and so a NOT gate is needed.

In other words, you need a two-input AND gate that is fed directly from M and also from a two-input OR gate that is fed from L (through an inverter) and P. The block diagram is shown below:



The simplified logic gate system is shown below:



The truth table for this system is shown below. Again, all you have to do is read the specification carefully and then read across each row, one at a time, and decide whether the bell should be ringing or not. There are some short cuts. For example, in the first four rows the master switch is off; therefore, the bell must be at logic 0 – even if there is a burglar in the house.

M	L	P	NOT L	P OR (NOT L)	B
0	0	0	1	1	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	0	1	1

The bell should go to logic 1 if the master switch is at 1 **and** either the light beam goes to logic 0 **or** the pressure pad goes to logic 1.

TASK: Draw a block diagram, logic diagram and truth table for the following system design problems. In all tasks, assume only 2 input gates allowed. Mark the input, process and output sections of the block diagrams.

1. A drill is to operate (logic 1 when on) if an isolator is closed (logic 1 when closed), a guard is in place (logic 1 when closed), and a foot pedal is operated (logic 1 when pressed).

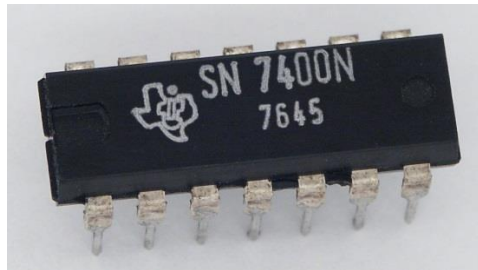
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

2. An automatic central heating system is to heat the radiators (logic 1 when on) if the mains switch is on (logic 1 when on), the timing control switch is closed (logic 1 when closed) and the override button (logic 1 when selected) is not selected.

0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

## LOGIC GATE INTEGRATED CHIPS (ICs)

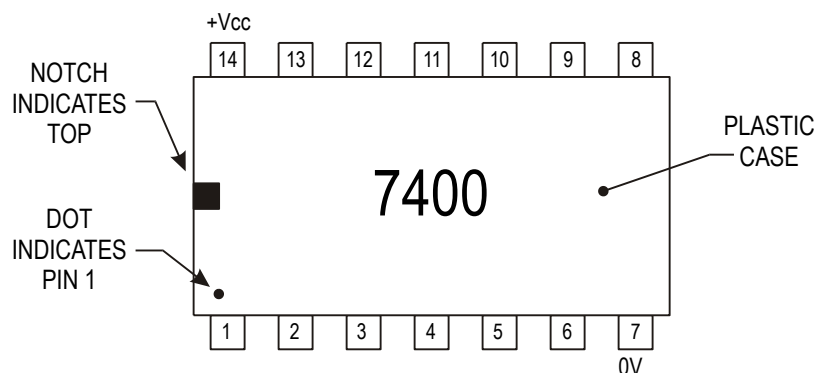
Logic gates come as packages on integrated chips (ICs) with each IC containing many resistors, transistors, and other components squeezed onto the chip. The ICs we will use are known as the 7400 series, part of the TTL (transistor-transistor logic) range of chips.



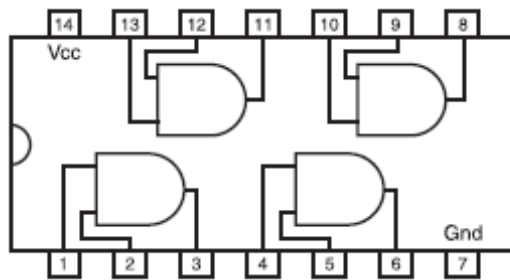
**TTL chips require a stable 5V supply to work properly.** Any unconnected pins automatically go to logic 1. In other words, if a wire connected to a pin is connected to the 0-volt rail (logic 0), it will go to logic 0. If the wire is disconnected from the 0-volt rail it will go to logic 1. However, it is good practice to connect pins to 'high' or 'low' as needed.

### Pin Diagrams

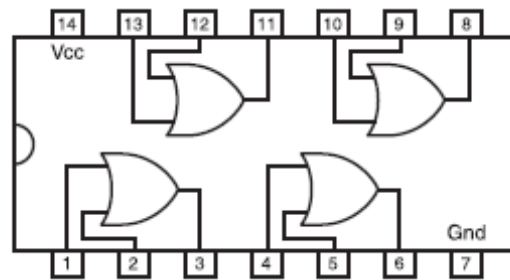
The 7400 series of chips are 14 pin ICs and each IC comes with its own identification code and pin layout diagram.



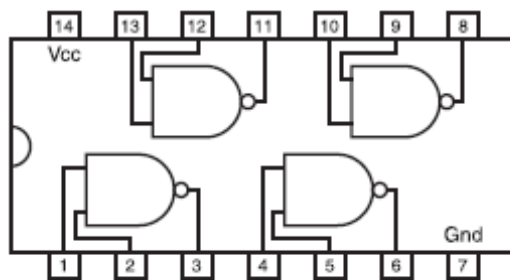
**Pin 7 is always ground (0V) and pin 14 is always +Vcc (+5V)**



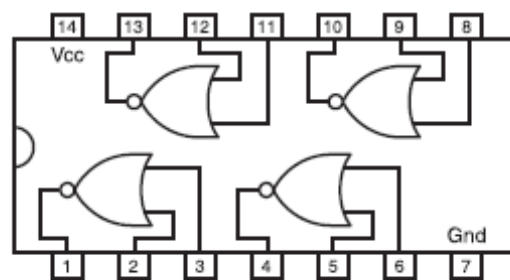
7408 Quad 2 input  
AND Gates



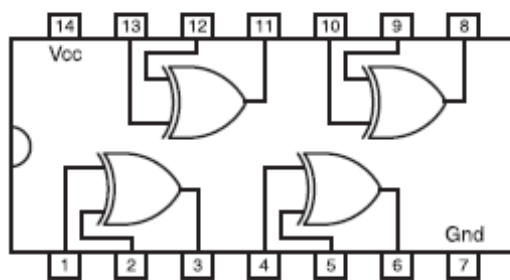
7432 Quad 2 input  
OR Gates



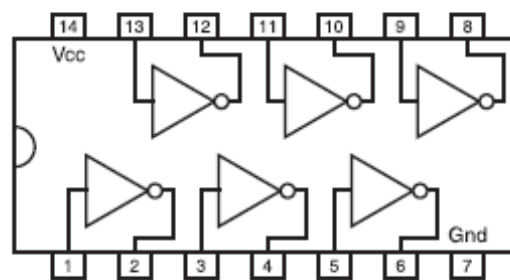
7400 Quad 2 input  
NAND Gates



7402 Quad 2 input  
NOR Gates



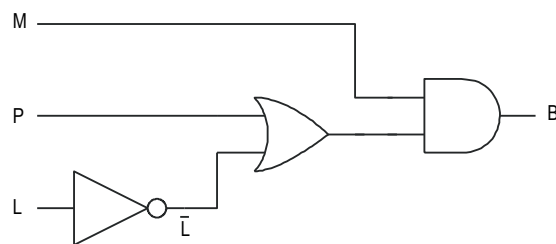
7486 Quad 2 input  
XOR Gates



7404 Hex NOT Gates  
(Inverters)

## **Practical Task**

Let's look again at the burglar alarm example problem on page 10



## **Step 1 – Full Circuit Design**

### **Pull-up/ pull-down resistors**

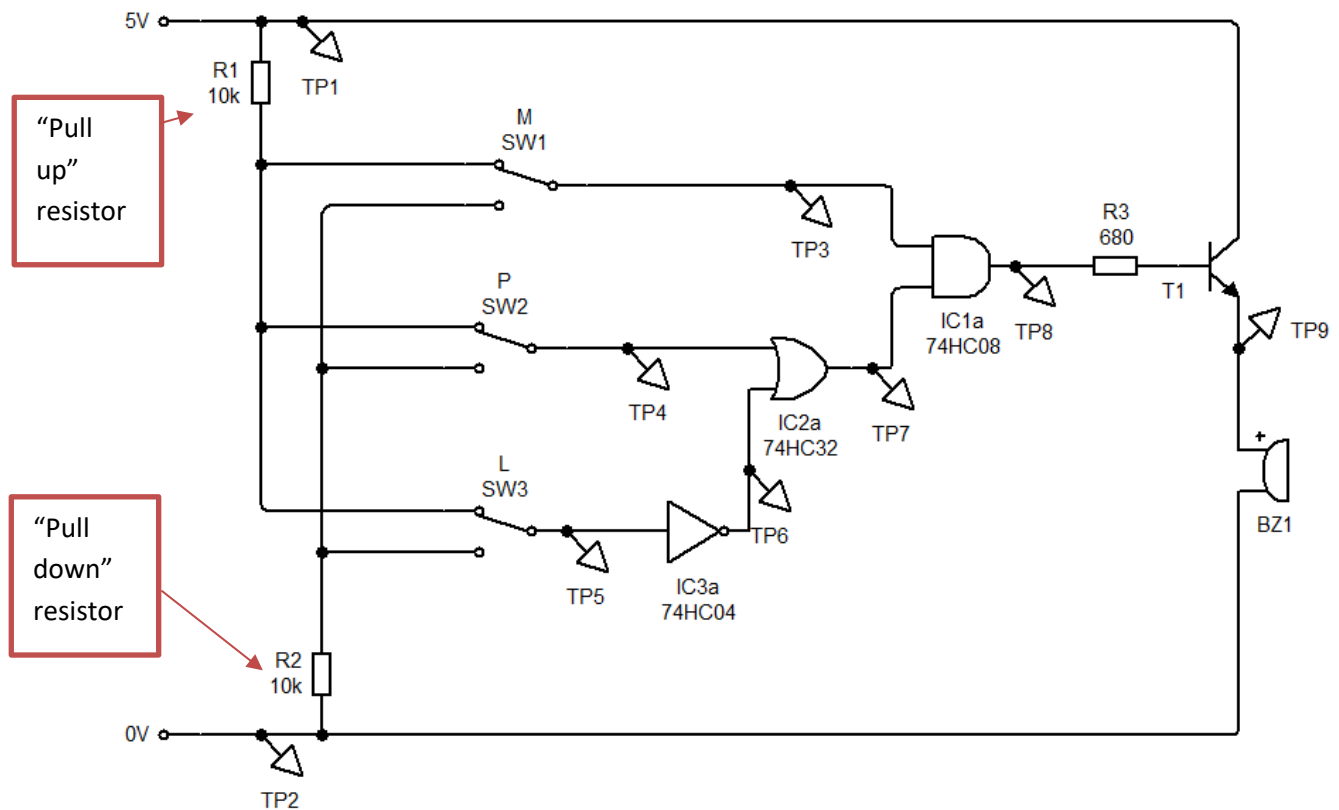
The pull up and pull down resistors are there to ensure the input the logic gate is indeed pulled up to +Vs or pulled down to 0V as required. These must be included when using a switch as a direct input component.

### **Test Points**

Test points are included at all significant reference points where the voltage level is important to measure/know e.g. power rails and all input and outputs. Test point reference tables can be created for ease of use.

Test Point	Description
1	Voltage at positive power rail
2	Voltage at ground power rail
3	Master switch output / AND gate input
4	Pressure pad switch output / OR gate input
5	Light sensor switch output / NOT gate input
6	NOT gate output / OR gate input
7	OR gate output / AND gate input
8	AND gate output / base voltage to transistor
9	voltage across buzzer

We can design a basic circuit to the above solution by using slide switches (SPDT) as inputs.



## Step 2 - Simulation

Create the above circuit in Yenka. Save as *Burglar Alarm*.

Printout/screenshot a copy of your simulation circuit diagram and paste on next page.

Mark on the diagram the input, process and output.

[insert simulation circuit here]

Simulate the circuit and test the circuits operation. Complete the tables below.

SIMULATION FUNCTIONALITY TEST			
What will be tested		Result	Comments
TP 1	Voltage at +V rail / V		
TP 2	Voltage at 0V rail / V		
TP 3	Voltage at Master Switch (SW1) Output / Input to AND gate / V	When High: When Low:	
TP 4	Voltage at Pressure Pad (SW2) output / Input to OR gate / V	When High: When Low:	
TP 5	Voltage at Light Sensor (SW3) output / Input to NOT gate / V	When High: When Low:	
TP 6	Voltage at output of NOT gate / Input to OR gate / V	When High: When Low:	
TP 7	Voltage at output of OR gate / Input to AND gate / V	When High: When Low:	
TP 8	Voltage at output of AND gate / V	When High: When Low:	
TP 9	Voltage across buzzer / V	When High: When Low:	
	Current in buzzer when on / mA		

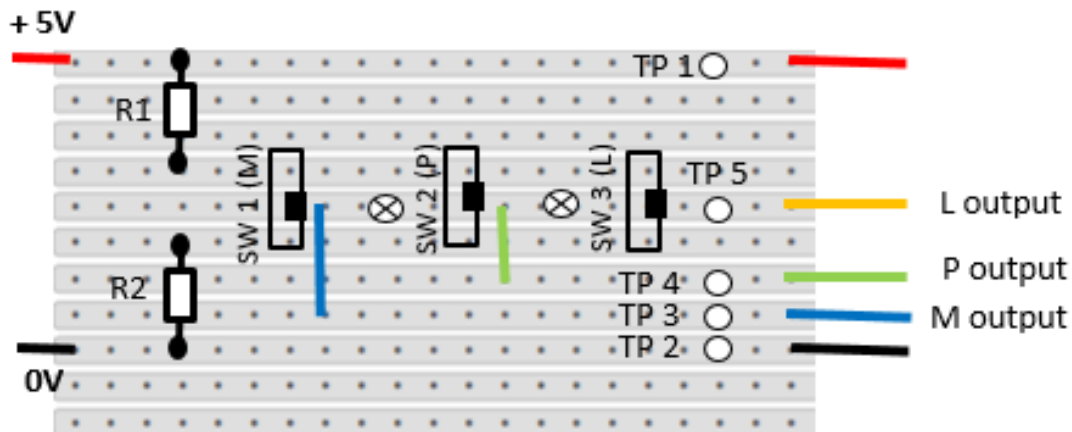
[illegible]

### Step 3 - Construction

#### Stripboard

You will construct and test each board separately.

#### Input board



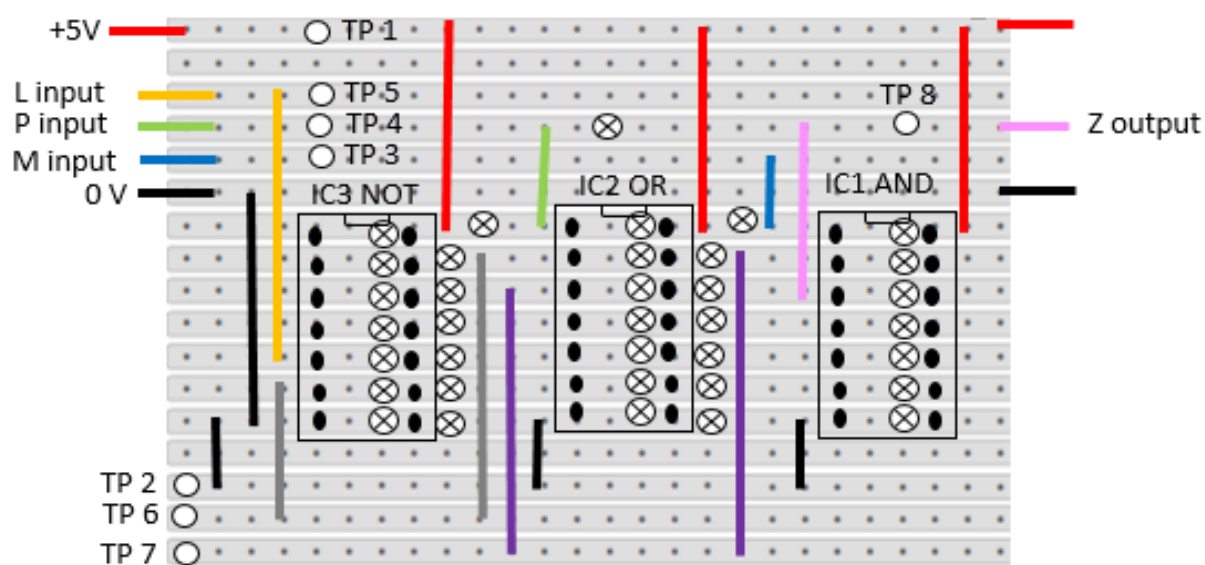
#### INPUT BOARD PRE-POWER UP CHECK LIST

What will be tested	Result	Any changes made?

#### INPUT BOARD FUNCTIONALITY TEST

What will be tested		Result	Comments?
TP 1	Voltage at positive supply rail / V		
TP 2	Voltage at ground supply rail / V		
TP 3	Voltage at Master Switch (SW1) Output / V	When High: When Low:	
TP 4	Voltage at Pressure Pad (SW2) output / V	When High: When Low:	
TP 5	Voltage at Light Sensor (SW3) output / V	When High: When Low:	

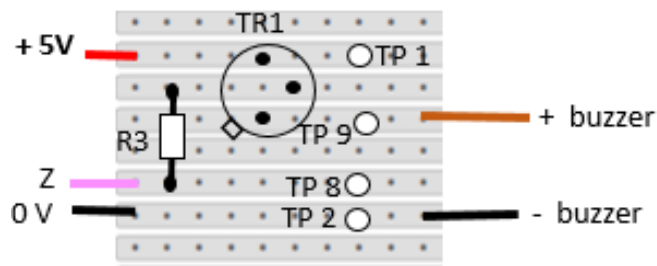
## Process board



PROCESS BOARD PRE-POWER UP CHECK LIST		
What will be tested	Result	Any changes made?

PROCESS BOARD FUNCTIONALITY TEST			
What will be tested		Result	Comments?
TP 1	Voltage at +V rail / V (PIN 14 for all ICs)		
TP 2	Voltage at 0V rail / V (PIN 7 for all ICs)		
TP 3	Voltage at Master Switch (SW1) Output / Input to AND gate PIN 1 / V	When High: When Low:	
TP 4	Voltage at Pressure Pad (SW2) output / Input to OR gate PIN 1 / V	When High: When Low:	
TP 5	Voltage at Light Sensor (SW3) output / Input to NOT gate PIN 5 / V	When High: When Low:	
TP 6	Voltage at output of NOT gate PIN 6 / Input to OR gate PIN 2 / V	When High: When Low:	
TP 7	Voltage at output of OR gate PIN 3 / Input to AND gate PIN 2 / V	When High: When Low:	
TP 8	Voltage at output of AND gate PIN 3 / V	When High: When Low:	

## Output Board



OUTPUT BOARD PRE-POWER UP CHECK LIST		
What will be tested	Result	Any changes made?

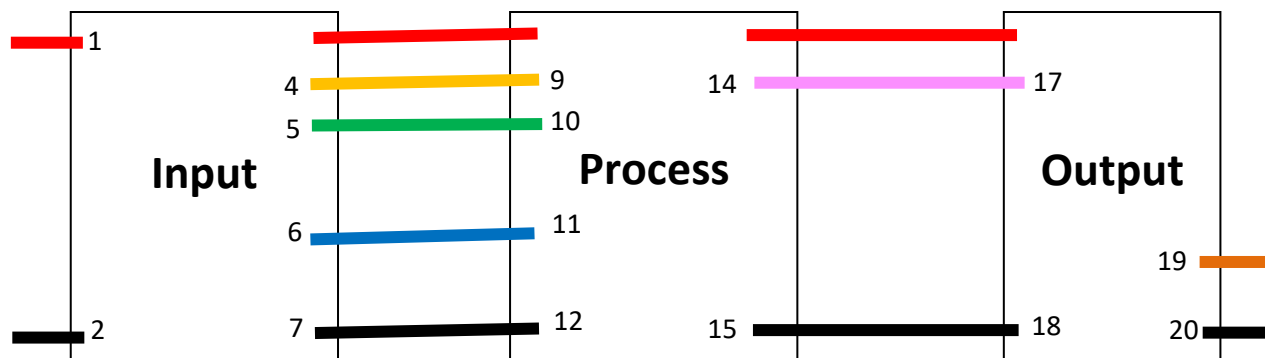
OUTPUT BOARD FUNCTIONALITY TEST			
What will be tested		Result	Comments?
TP 1	Voltage at +V rail / V (PIN 14 for all ICs)		
TP 2	Voltage at 0V rail / V (PIN 7 for all ICs)		
TP 8	Voltage at base of transistor / Voltage of input Z / V	When High: When Low:	
TP 9	Voltage at emitter of transistor / p.d across buzzer / V	When Z High: When Z Low:	
	Current in buzzer when on / mA		

## Wiring looms

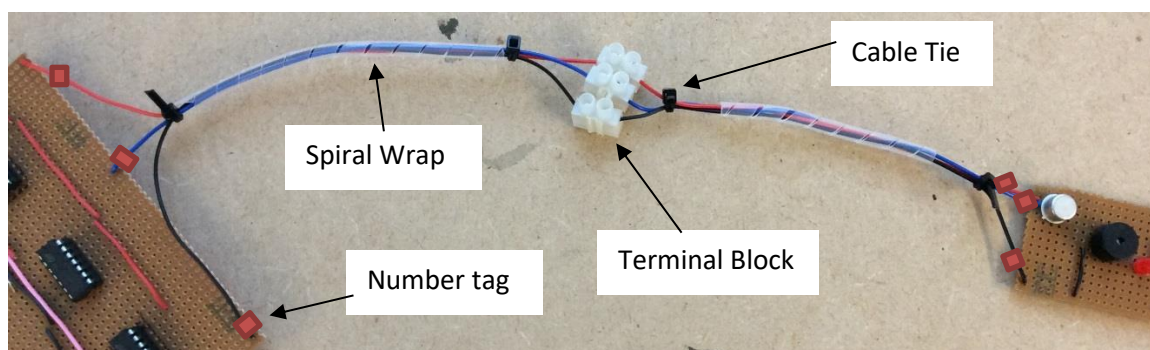
You should now have three strip boards, all individually tested and working, with any fixes carried out and commented/evaluated.

The next step is to loom them together. You will see from the diagrams that the different connections are colour coded using colour wires. They should also be number tagged on completion of the looms. This is industry practice to allow connections between distant terminals to be identified.

These connections, with their wire colours and number tags, can be shown in a simple block diagram for reference.



Wire Tag Number	Wire colour	Connection
1	Red	Positive supply rail
2	Black	Ground rail
3	Red	Positive supply rail
4		Light sensor (SW3) output
5		Pressure Pad (SW2) output
6		Master Switch (SW1) output
7	Black	Ground rail
8	Red	Positive supply rail
9		Light sensor (SW3) input to NOT gate
10		Pressure Pad (SW2) input to OR gate
11		Master Switch (SW1) input to AND gate
12	Black	Ground rail
13	Red	Positive supply rail
14		Output from AND gate
15	Black	Ground rail
16	Red	Positive supply rail
17		Input to base of transistor
18	Black	Ground rail
19		Emitter connection to buzzer
20	Black	Ground rail



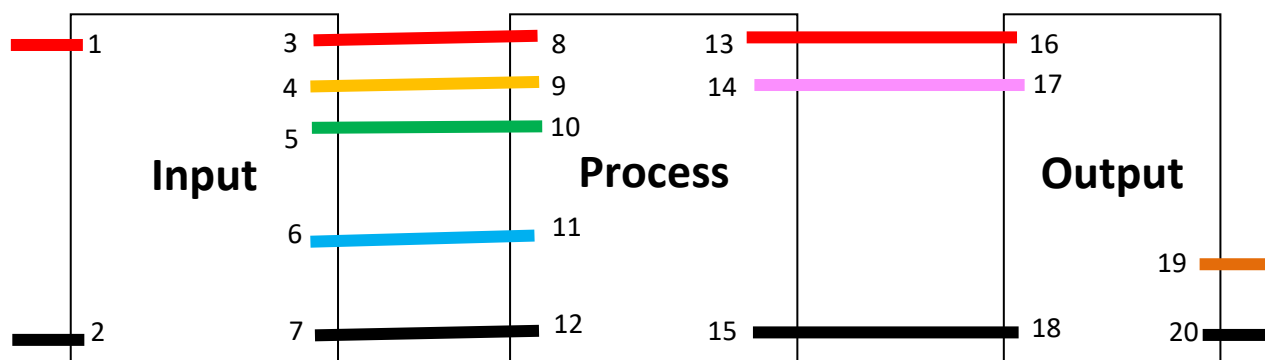
## Loom Testing

Once loomed, you need to check the electrical reliability and security of wiring. Again this is best done, following a PRE-POWER test plan.

LOOM PRE-POWER UP CHECK LIST		
What will be tested	Result	Any changes made?
Security of all wiring into and out of INPUT board		
Security of all wiring into and out of PROCESS board		
Security of all wiring into and out of OUTPUT board		
Security of wiring at all terminal blocks		
All wires number tagged and colour coded as planned		
Neatness of loom of high standard		

Continuity of wiring loom connections – use a continuity (bleep) tester to test the continuity of wiring between the boards.

When tested and correct, highlight (or tick) the wire on the diagram below to confirm tested as correct. Make any changes if you need to and make a record of it.



## Evaluation of looms

### Overall testing stage

Once wired and loomed, the last stage is to test the whole project as one circuit to see if it is functioning as expected.

CIRCUIT FUNCTIONALITY TEST			
What will be tested		Result	Comments?
TP 1	Voltage at +V rail / V		
TP 2	Voltage at 0V rail / V		
TP 3	Voltage at Master Switch (SW1) Output / Input to AND gate / V	When High: When Low:	
TP 4	Voltage at Pressure Pad (SW2) output / Input to OR gate / V	When High: When Low:	
TP 5	Voltage at Light Sensor (SW3) output / Input to NOT gate / V	When High: When Low:	
TP 6	Voltage at output of NOT gate / Input to OR gate / V	When High: When Low:	
TP 7	Voltage at output of OR gate / Input to AND gate / V	When High: When Low:	
TP 8	Voltage at output of AND gate / V	When High: When Low:	
TP 9	Voltage across buzzer / V	When High: When Low:	
	Current in buzzer when on / mA		

## Evaluation

What went well?

What could be improved?

# LOGBOOK

Date:	
What I Did:	
Next Steps	

Date:	
What I Did:	
Next Steps	

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# TEACHER USE ONLY

Section			Comments	Score
Analysis (5)	Simulation	Complete and functional and fully labelled- 2 marks		2
	Component list	0 Errors - 3 Marks 1 or 2 Error - 2 Marks 3 or 4 Errors - 1 Marks		3
Construction (31)	Fully Constricted input subsystem	Layout Fully constructed and fitting all components accurately - 4 marks.		4
	Fully Constricted Process subsystem			4
	Fully Constricted Output subsystem	Construction partially incomplete - 1 mark		4
	Quality of soldering			3
	Neatness of subsystem Layout	Layout followed and standard conventions used (e.g. colour coding)		3
	Labelling of subsystem	Board functions		1
		ICs labelled		1
		Swich Functions		1

Section			Comments	Score
	Use of Test Points	Test points inserted at appropriate locations		2
		Test points labelled [or annotated on a photo]		1
		List of Test points and results		1
	Safe Working	Holding soldering iron correctly		1
		use of stand and sponge		1
		Use of eye Protection		1
	Working Independently	(1 less per direct intervention)		3
Wiring (13)	Wiring and assembly complete, electrically reliable.	Boards can be turned over with no degradation of function		1
		Input, Output, and Process subsystems can be easily detached from each other		1
		No dry joints or lifted tracks at wire join		1
		All wiring secure		1
	Neatness of construction.	wiring numbered or colour coded		1
		wiring schedule used		1
		spiral wrap used		1

Section			Comments	Score
	Working safely.	Holding soldering iron correctly		1
		use of stand and sponge		1
		not burning oneself or others		1
	Working independently	(1 less per direct intervention)		3
Testing (5)	Test Planning	pre-power up checklist		1
	Testing and Repair	completing and recording pre power up checks		1
		completing and recording power up checks		1
		completing and recording testing against specification checks		1
		repairs (or nil) noted		1
Reporting (5)	Record of Progress and Planning (log)	complete logbook with no gaps		1
		accurate record		1
		record updated regularly		1
	Evaluation	what went well		1
		what was difficult OR if not functional suggestions on how to fix it if you had time		1
			Total	/59