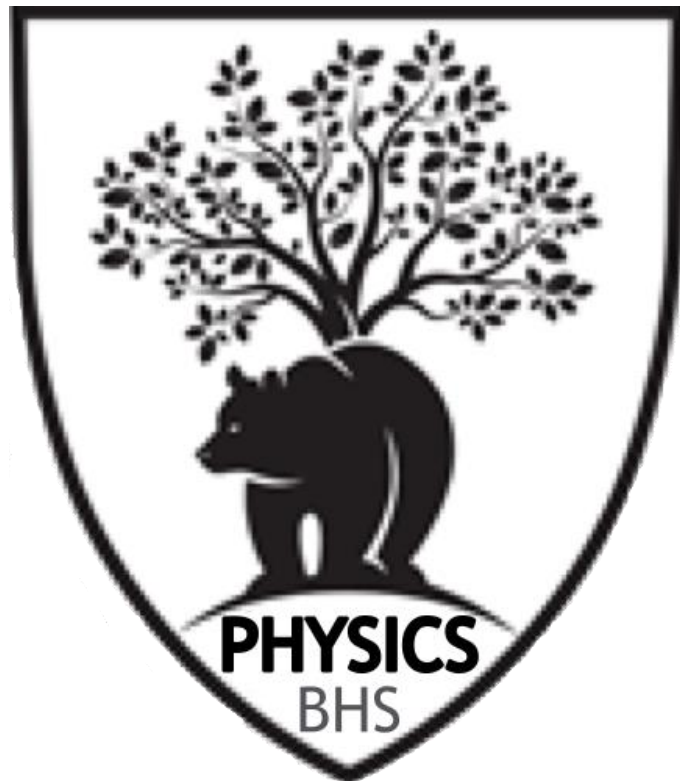


Name:



Practical Electronics

Block 6

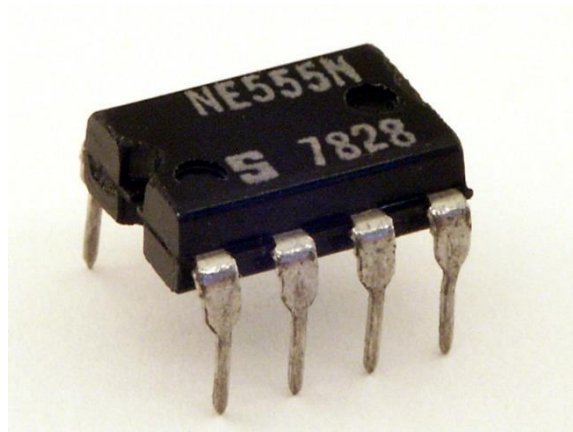
Oscillators and Amplifiers

With Mock Assignment

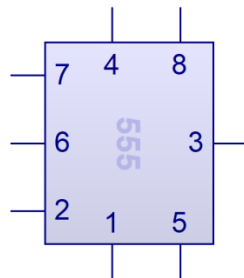
Digital Oscillators

In electronic circuits, it is often useful to have the ability to control when a system goes high or low after a pre-determined time (a set delay) or have it **oscillate** between high and low states in a regular controlled way i.e have a set frequency.

One integrated chip that is able to do precision timing (from microseconds to hours) is the 555 timer. This was created in 1971 and is the most widely used IC in history due to its cheap construction costs and its multiple functions.



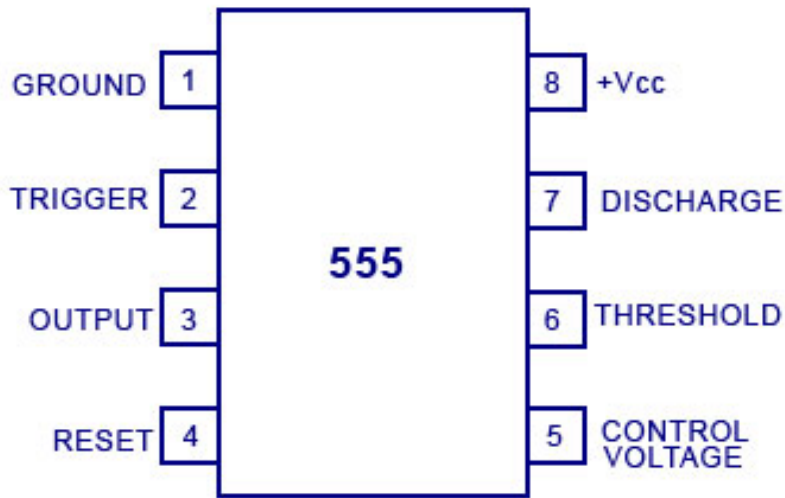
The circuit diagram for a 555 timer looks like this:



This is designed to allow easy creation of circuit diagrams as it arranges pins in a useful arrangement. You must always refer to the pinout diagram when constructing to ensure correct physical pin arrangement and connections.

Pin Diagrams

The 555 timer is an 8 pin IC and below is the pin layout diagram.

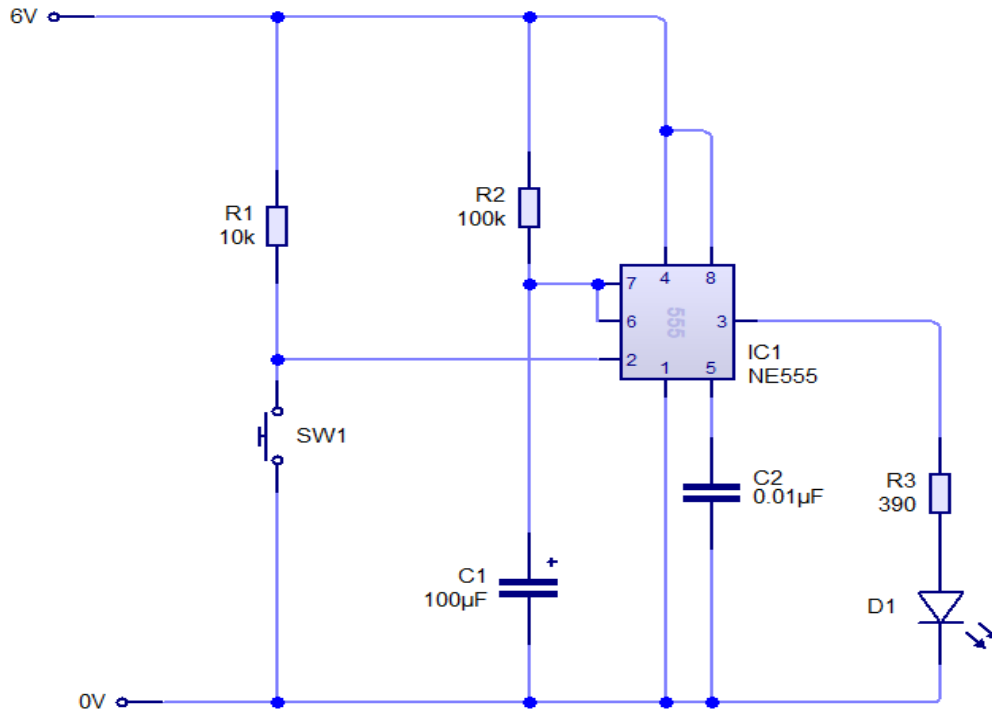


Pin 1 is always ground (0V) and pin 8 is always +Vcc (+4.5V to 15V)

| Pin Number | Purpose | Description |
|------------|------------------|--|
| 1 | Ground | Always connected to the ground rail (0V) |
| 2 | Trigger | When you apply a low voltage to pin 2, it triggers the internal timing circuit to start working. |
| 3 | Output | This is where the output waveform appears. |
| 4 | Reset | If a low voltage is applied to pin 4, the timing function is reset and output goes low again. This is often attached to the positive rail when not required. |
| 5 | Control | This can be used to override the internal trigger circuit. We don't need this function, so will ALWAYS connect pin 5 to ground via a 0.01 μ F capacitor. |
| 6 | Threshold | When the voltage applied to pin 6 reaches a certain level, usually $\frac{2}{3} V_{CC}$, the timing cycle ends and the output goes low. A resistor between positive rail and pin 6 influences the length of the timing cycle. |
| 7 | Discharge | A capacitor between pin 7 and the ground rail also influences the length of the timing cycle. |
| 8 | +V _{CC} | Always connected to the positive supply (4.5V – 15V max) |

555 Timer in Mono-stable Mode

This type of circuit is used when a single timed output is required either as a *time delay* or for something to be *on for a certain period only*.



The 555 timer output, pin 3, is usually in a low state (0V). When set up in mono-stable mode, the 555 timer can be triggered (by applying a LOW voltage at pin 2) to produce a high output at pin 3 for a pre-determined time, known as a pulse, before falling back to ground. It is sometimes referred to as a *one shot pulse*. The pre-determined length of pulse, the width, is determined by the values of R₁ and C₁.

$$T \approx 1.1 \times R \times C$$

Where T is length of pulse in seconds,

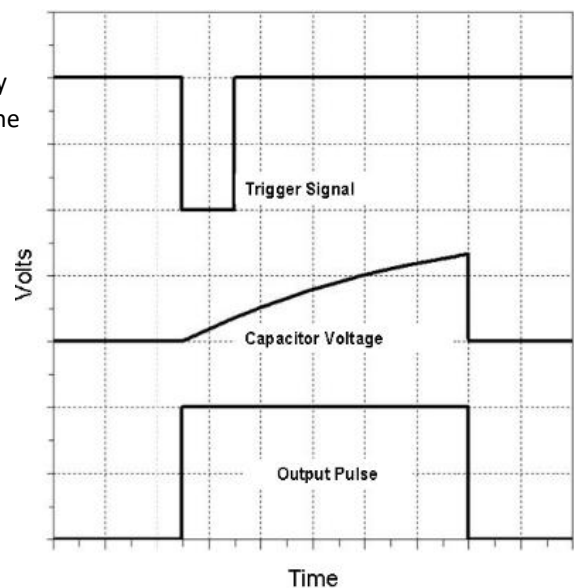
R is value of resistor in ohms,

C is value of capacitor in farads.

Low signal applied at pin 2 by pressing switch. This starts the timer.

Capacitor starts to charge when 555 triggered. Time to charge depends on values of R and C.

When capacitor starts to charge, output goes high. When capacitor voltage reaches $\frac{2}{3} V_{CC}$, output goes low again.



Simulation

Create the above circuit in Yenka. Save as *Monostable 555 Timer*.

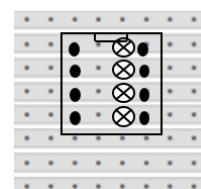
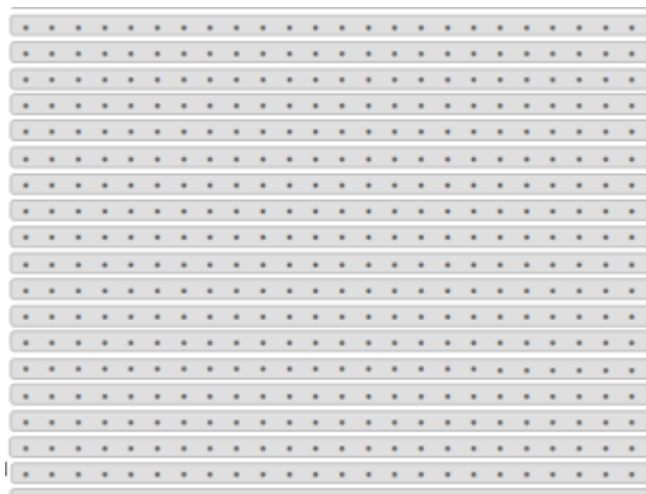
Add in test points at appropriate places with reference to the test point table below.

| Test Point | Description |
|------------|--------------------------------|
| 1 | Voltage at positive power rail |
| 2 | Voltage at ground rail |
| 3 | Output at pin 3 |

| SIMULATION FUNCTIONALITY TEST | | | | |
|--------------------------------|------------------------------|-------------------------------|-----------------------------|----------|
| What will be tested | | Result | | Comments |
| TP 1 | Voltage at +V rail / V | | | |
| TP 2 | Voltage at 0V rail / V | | | |
| TP 3 | Voltage at output / V | When High: When Low: | | |
| Voltage across LED / V | | When High: When Low: | | |
| Resistor value / k Ω | Capacitor value / μ F | Calculated pulse width / s | Pulse width measured / s | |
| 100 | 100 | | | |
| 100 | 47 | | | |
| 100 | 22 | | | |
| 10 | 100 | | | |

EvaluationStripboard Layout Diagram

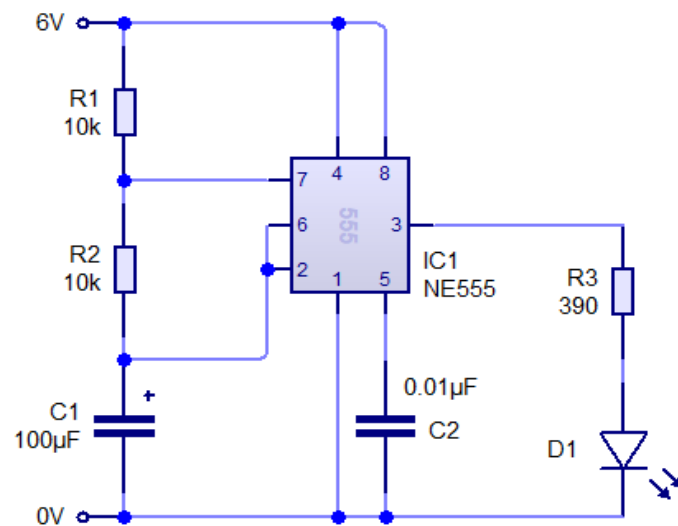
Create a stripboard layout for the mono-stable 555 timer.



The 555 is an 8 pin IC so will be mounted on an 8 pin DIL socket

555 Timer in Astable Mode (Oscillator)

This type of circuit is used to produce a continuous series of voltage pulses that oscillate between the high and low states, i.e. create a square wave output waveform at pin 3. It works as an electronic **oscillator**.



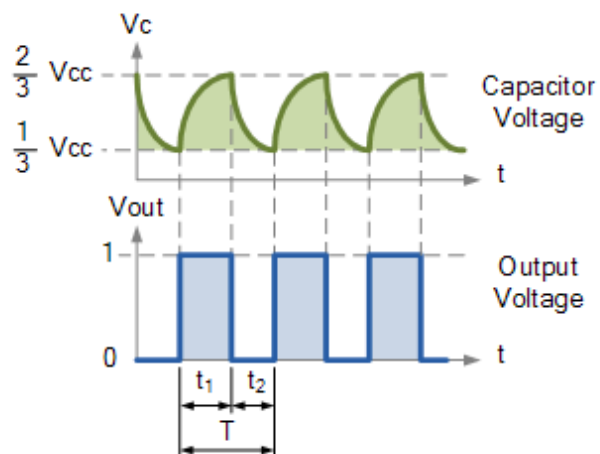
The length of time for one complete oscillation is determined by the values of R_1 , R_2 and C_1 .

$$T \approx 0.7 \times (R_1 + 2R_2) \times C_1$$

Where T is length of oscillation in seconds,

R is value of resistors in ohms,

C is value of capacitor in farads.



The width of the high part and low part of the pulse can be set as different times. In this course, this is not necessary.

In general,

- when $R_2 = R_1$, the high part will be twice as long as the low part.
- When R_2 is much greater than R_1 , the high and low pulse widths are fairly equal.

Simulation

Create the above circuit in Yenka. Save as *Astable 555 Timer*.

Add in test points at appropriate places with reference to the test point table below.

| Test Point | Description |
|------------|--------------------------------|
| 1 | Voltage at positive power rail |
| 2 | Voltage at ground rail |
| 3 | Output at pin 3 |

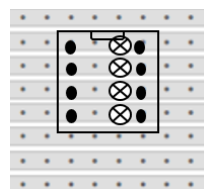
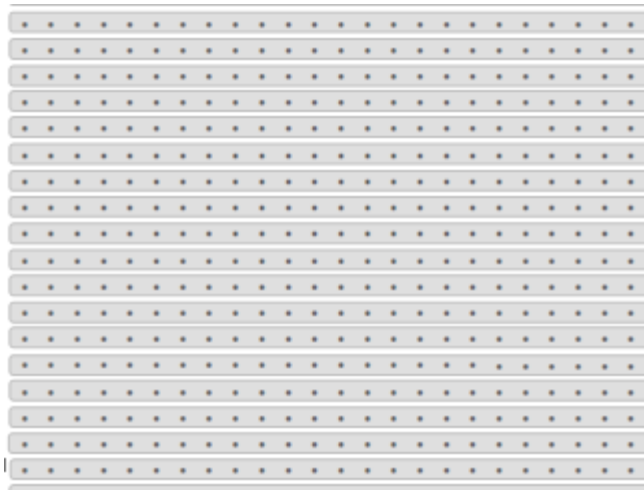
Simulate the circuit and test the circuits operation. Use the probe and graph function to measure the output pulse width. Complete the tables below.

| SIMULATION FUNCTIONALITY TEST | | | |
|-------------------------------|------------------------|-------------------------|----------|
| What will be tested | | Result | Comments |
| TP 1 | Voltage at +V rail / V | | |
| TP 2 | Voltage at 0V rail / V | | |
| TP 3 | Voltage at output / V | When High: When Low: | |
| Voltage across LED / V | | When High: When Low: | |

| R_1 / k Ω | R_2 / k Ω | C_1 / μ F | Calculated oscillation width / s | Measured oscillation width / s | Measured width of high part / s | Measured width of low part / s |
|--------------------|--------------------|-----------------|----------------------------------|--------------------------------|---------------------------------|--------------------------------|
| 10 | 10 | 100 | 2.1 | | | |
| 10 | 10 | 47 | 0.99 | | | |
| 5.6 | 5.6 | 100 | 1.2 | | | |
| 1 | 10 | 100 | 1.5 | | | |

Stripboard Layout Diagram

Create a stripboard layout for the astable 555 timer.



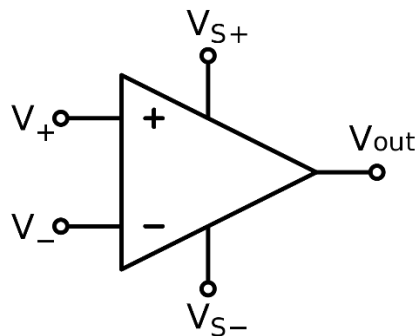
The 555 is an 8 pin IC so will be mounted on an 8 pin DIL socket

The Operational Amplifier – LM741 Op-Amp

A very versatile and popular IC used with analogue signals is known as an operational amplifier, the op-amp. The op-amp comes in many IC packages but the one we will use is the LM741.



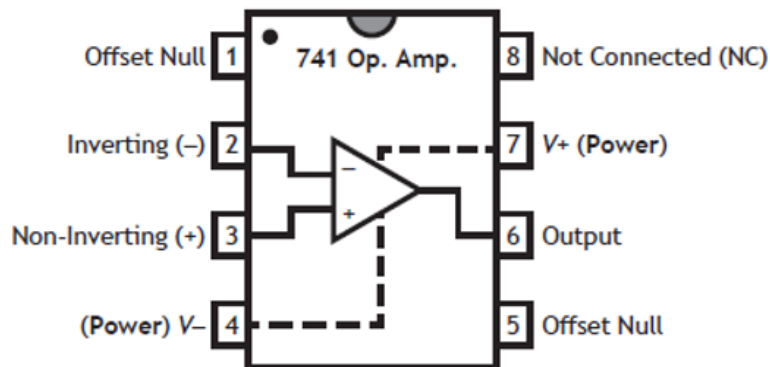
The circuit diagram for an op-amp looks like this:



This is designed to allow easy creation of circuit diagrams as it arranges pins in a useful arrangement. You must always refer to the pinout diagram when constructing to ensure correct physical pin arrangement and connections.

Pin Diagrams

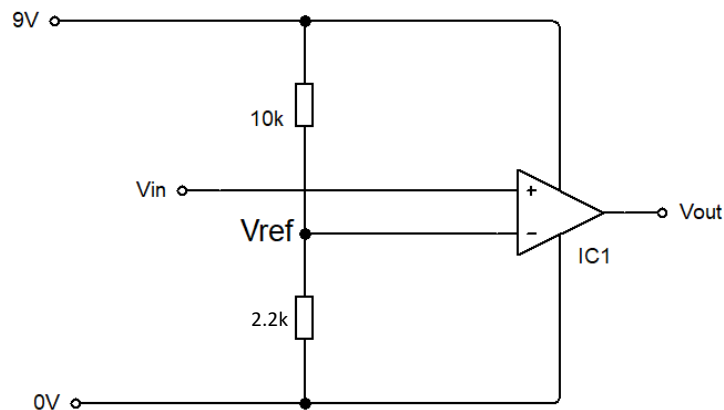
The LM741 is an 8 pin IC and below is the pin layout diagram.



| Pin Number | Purpose | Description |
|------------|-----------------------|---|
| 1 | Offset Null | Used to set output to zero. Not required for this course. |
| 2 | Inverting INPUT | One of the input pins we will use |
| 3 | Non-inverting INPUT | One of the input pins we will use |
| 4 | Power (NEGATIVE RAIL) | Should be connected between -15V to 0V |
| 5 | Offset Null | Used to set output to zero. Not required for this course. |
| 6 | OUTPUT | This is where the output signal comes out |
| 7 | Power (POSITIVE RAIL) | Should be connected between +9 to +15V |
| 8 | Not connected | Unused pin – no function |

The power rail values depend very much on the required operation and purpose of the op-amp circuit designed.

741 Op-Amp in Comparator Mode

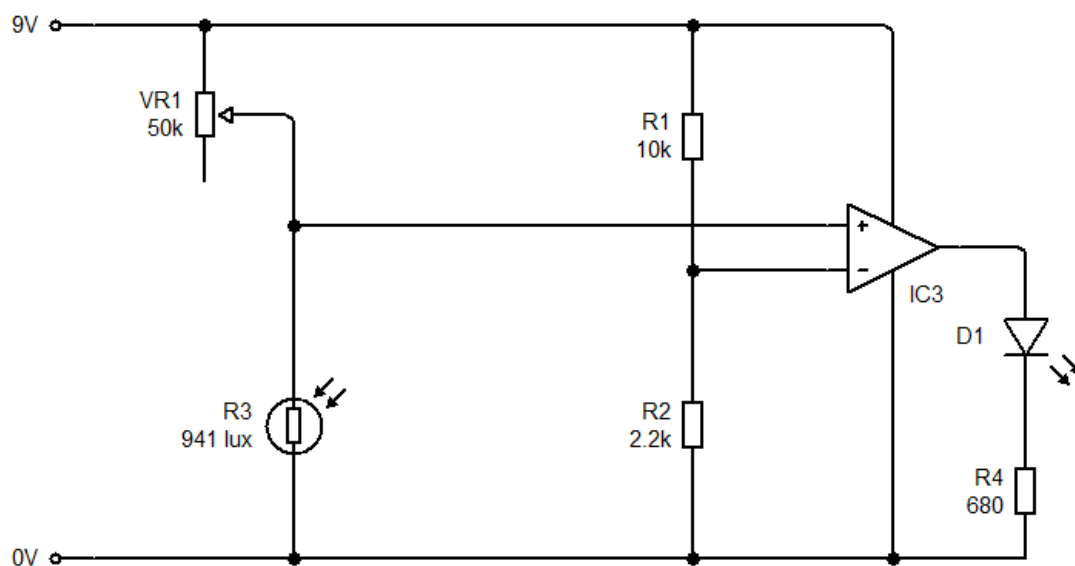


When in comparator mode, the op-amp compares the voltage at the non-inverting input (V_{in}) to the voltage at the inverting input (V_{ref}) and amplifies the signal.

If V_{in} is greater than V_{ref} , then V_{out} rises to the positive saturation level (approaches V_{CC})

If V_{in} is less than V_{ref} , then V_{out} rises to the negative saturation level (approaches V_-)

Comparator Mode op-amp Light Sensor



Description:

Simulation

Create the above circuit in Yenka. Save as *Comparator Mode light sensor*.

Add in test points at appropriate places with reference to the test point table below.

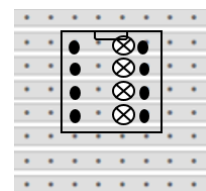
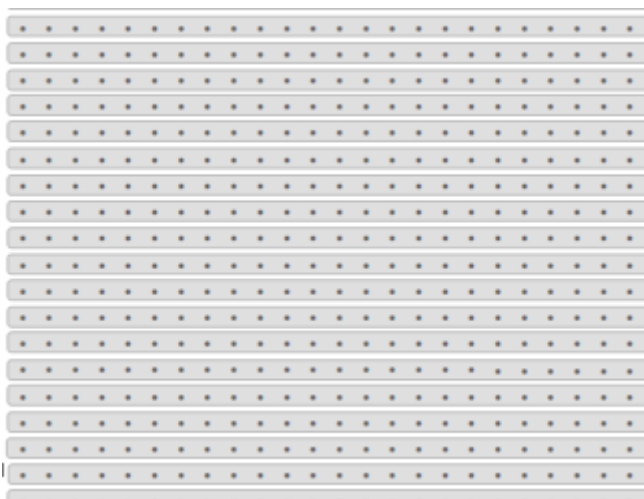
| Test Point | Description |
|------------|--|
| 1 | Voltage at positive power rail |
| 2 | Voltage at ground rail |
| 3 | Voltage at non-inverting input (PIN 3), V_{in} |
| 4 | Voltage at inverting input (PIN 2), V_{ref} |

Simulate the circuit and test the circuits operation.

| SIMULATION FUNCTIONALITY TEST | | | |
|-------------------------------|---|---|----------|
| What will be tested | | Result | Comments |
| TP 1 | Voltage at +V rail / V | | |
| TP 2 | Voltage at ground rail / V | | |
| TP 3 | Voltage at non-inverting input, V_{in} | When light levels increase: When light levels decrease: | |
| TP 4 | Voltage at inverting input, V_{ref} / V | | |
| TP 5 | V_{out} / V | When V_{in} greater than V_{ref} : When V_{in} less than V_{ref} : | |

Stripboard Layout Diagram

Create a stripboard layout for the comparator mode light sensor.



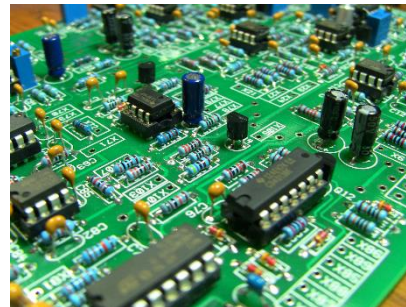
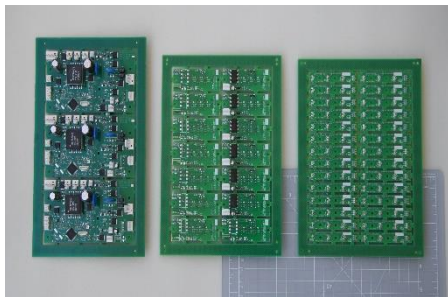
The 741 op-amp is an 8 pin IC so will be mounted on an 8 pin DIL

Have it checked by the teacher.

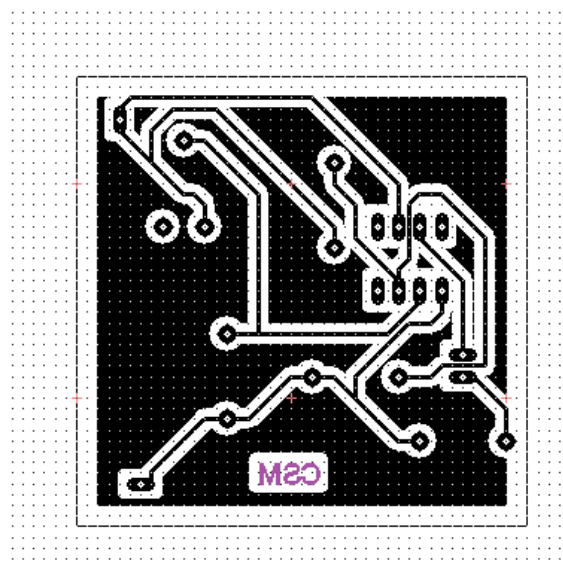
Printed Circuit Boards

A printed circuit board, or PCB, is the most widely used process for constructing permanent circuits. The most basic type of PCB is the single layer PCB which consists of a base of non-conducting material with a layer of copper on top. A circuit design is etched (non-essential copper is chemically removed) onto the copper face, using a mask, leaving behind the necessary tracks, pads and other features. The components are then soldered on the board to complete the circuit.

PCBs allow for fast mass production of circuits and is very cost effective.



The design of the mask, and therefore the circuit tracks, can be very time consuming and is mostly done using CAD software.



The mask is printed onto acetate sheet and placed carefully over the copper side of the PCB. Strong UV light is shone on to the mask/PCB board and the black ink absorbs the UV whilst UV passes straight through the clear parts and strikes the copper. This weakens the copper bonds. The PCB is then placed in an etching chemical which reacts with the copper. The copper that was exposed to the UV reacts more readily and is removed whilst the non-exposed copper remains intact. This is how the tracks are created. Holes are then drilled for the placement of the components on the top side.

N5 PRACTICAL ELECTRONICS

MOCK ASSIGNMENT

INSTRUCTIONS FOR CANDIDATES

This practical activity is worth 70 marks.

In this assessment, you will have to:

analyse a problem
↓
design and simulate a solution
↓
construct a solution
↓
test the solution
↓
report on the solution

Marks will be awarded for **each** stage.

You will be provided with:

- ◆ a description of the problem you must solve
- ◆ descriptions of what you must do for each stage of the practical activity
- ◆ information about the evidence that you need to provide

Throughout the task, you are required to keep a record of progress. This could be an informal log or diary, and could be handwritten or kept electronically. It should explain what you have done, describing any help you required, and listing any evidence you have produced (eg printouts, sketches, photographs). You should update your record of progress after each stage of the practical activity.

Make sure you date and label all evidence and store it in a safe place.

After each stage of the task, your assessor should check your work before you move on to the next stage.

FLASHING LIGHTS: THE PROBLEM

It is important that electronic systems do not overheat.

The technician at **Berwickshire Electrical** is deaf, therefore needs a Visual warning if the system overheats. As it is very important, he has asked for a sequence of flashing lights in at least 2 different colours to light when a master switch is switched on and the system overheats.

Your task is to decide on the components needed to do this and build a prototype which could eventually be used in Berwickshire Electrical.

The completed system can be made up of three separate sub-systems:

- ◆ an input switch unit and sensor
- ◆ a process board with ICs to control the flashing rate
- ◆ a light display with at least four LEDs

Once you have decided on suitable components, you must design and simulate an electronic solution in order to check its operation and finally construct it using appropriate methods.

ADVICE FOR CANDIDATES

The input sub-system

- ◆ There must be at least two inputs, one of which should be an temperature sensor allowing for automatic switch-on when temperature rises

The process sub-system

- ◆ There should be at least 1 flashing system and at least 1 Logic Gate

The output sub-system

- ◆ The output should use at least four LEDs (at least 2 different colours).

Your task is to analyse this problem, then design, construct and test a solution.

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THE TASK

Stage 1: analysing the problem specification (7 marks)

Tick box when
completed

Read the problem description carefully.

1a Create system and sub-system block diagrams for the lighting system. These should clearly show all inputs and outputs, and the logic circuits required.

1b Identify suitable components, including:

- ◆ input device(s)
- ◆ LEDs
- ◆ logic gate ICs

1c Identify all other components required for the task. Complete a bill of materials sheet.

1d Update your record of progress, which should be checked by your assessor.

☐

Stage 2: designing and simulating a solution (7 marks)

2a Demonstrate an YENKA simulation of the solution to your assessor, and keep printouts/screen shots.

2b Produce the component layout drawings for the stripboard section of the construction.

2c Update your record of progress, which should be checked by your assessor.

☐

Stage 3: construction using safe working practices (44 marks)

3a Build a hardwired prototype of the system using appropriate materials and techniques used during the course. You will need to build:

- ◆ the input sub-system
- ◆ the process sub-system
- ◆ the output sub-system
- ◆ the wiring loom

3b Update your record of progress after each stage, which should be checked by your assessor. You may include photographic evidence of the stages of construction.

☐

Stage 4: testing the solution (7 marks)

- 4a Create a test plan, including pre-power-up and functional testing routines.
- 4b Carry out your test plan, keeping a record of the test results on a testing grid.
- 4c Diagnose any faults, and carry out any repairs required.
- 4d Update your record of progress, which should be checked by your assessor. ☐

Stage 5: reporting on the solution (5 marks)

5a Produce a report, which may be written, or in electronic format, or a presentation. Your report must include the following:

- ◆ a report on the tests you carried out, the results of the tests and any changes you made because of the results
- ◆ evidence of your completed solution
- ◆ an evaluation of the completed circuit, explaining how it meets the specification and suggesting how it could be improved
- ◆ a short evaluation of how well you carried out the process of analysis, design, construction and testing of your solution

5b Add your report to your record of progress, which should be checked by your assessor. ☐

You have now completed the assessment.

Check it over to ensure you have completed all sections, and have collected all the required evidence.

If you are sure that you have finished, let your assessor know.

MARKING BREAK DOWN (FOR INFORMATION)

| | | | |
|----------------------------|-------------------------------------|--|---|
| Simulation and Design (14) | Systems/Block Diagram | With no assistance - 4 marks 1 less Per direct intervention 1 less per Error | 4 |
| | Simulation | Complete and functional and fully labelled- 3 marks 1 to 3 Errors - 2 marks Partial functional with 4 or more errors - 1 mark | 3 |
| | Component list | 0 Errors - 3 Marks 1 or 2 Error - 2 Marks 3 or 4 Errors - 1 Marks | 3 |
| | Layout Diagram | 0 Errors, fully annotated with all track cuts - 4 Marks 1 or 2 Error and/or Partial Annotation - 3 Marks 3 or 4 Errors and/or No Annotation - 2 Marks 5 or 6 Errors and/or 2 or more missing Components -1 Mark | 4 |
| | | Test points identified (marks awarded in later section) | |
| Construction (31) | Fully Constricted input subsystem | Layout Fully constructed and fitting all components accurately - 4 marks. | 4 |
| | Fully Constricted Process subsystem | Layout Fully constructed with 1 or 2 errors - 3 marks. | 4 |
| | Fully Constricted Output subsystem | Layout fully constructed but with fitting of components unreliable - 2 marks. Construction partially incomplete - 1 mark | 4 |
| | Quality of soldering | | 3 |
| | Neatness of subsystem Layout | Layout followed and standard conventions used (e.g. Colour Coding) | 3 |
| | Labelling of subsystem | Board functions | 1 |
| | | ICs labelled | 1 |
| | | Swich Functions | 1 |
| | Use of Test Points | Test points inserted at appropriate locations | 2 |
| | | Test points labelled [or annotated on a photo] | 1 |
| | | List of Test points and results | 1 |
| | Safe Working | Holding soldering iron correctly | 1 |
| | | use of stand and sponge | 1 |
| | | Use of eye Protection | 1 |
| | Working Independently | (1 less per direct intervention) | 3 |

| | | | |
|---------------|--|--|---|
| Wiring (13) | Wiring and assembly complete, electrically reliable. | Boards can be turned over with no degradation of function | 1 |
| | | Input, Output, and Process subsystems can be easily detached from each other | |
| | | No dry joints or lifted tracks at wire join | 1 |
| | | All wiring secure | 1 |
| | Neatness of construction. | wiring numbered or colour coded | 1 |
| | | wiring schedule used | 1 |
| | | spiral wrap used | 1 |
| | Working safely. | Holding soldering iron correctly | 1 |
| | | use of stand and sponge | 1 |
| | | not burning oneself or others | 1 |
| | Working independently. | (1 less per direct intervention) | 3 |
| Testing (7) | Test Planning | pre-power up checklist | 1 |
| | | power up check list | 1 |
| | | testing against the specification | 1 |
| | Testing and Repair | completing and recording pre power up checks | 1 |
| | | completing and recording power up checks | 1 |
| | | completing and recording testing against specification checks | 1 |
| | | repairs (or nil) noted | 1 |
| Reporting (5) | Record of Progress and Planning (log) | complete logbook with no gaps | 1 |
| | | accurate record | 1 |
| | | record updated regularly | 1 |
| | Evaluation | what went well | 1 |
| | | what was difficult OR if not functional suggestions on how to fix it if you had time | 1 |

LOGBOOK

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|-------------|--|
| Date: | |
| What I Did: | |
| Next Steps | |

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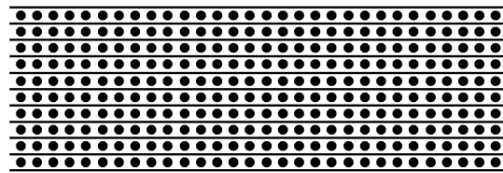
| | |
|-------------|--|
| Date: | |
| What I Did: | |
| Next Steps | |

BLOCK DIAGRAM

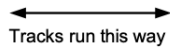
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SIMULATION PRINTOUT

STRIPBOARD PAPER



Actual size stripboard. Hole spacing 0.1" (2.54mm)



Tracks run this way

Tips:

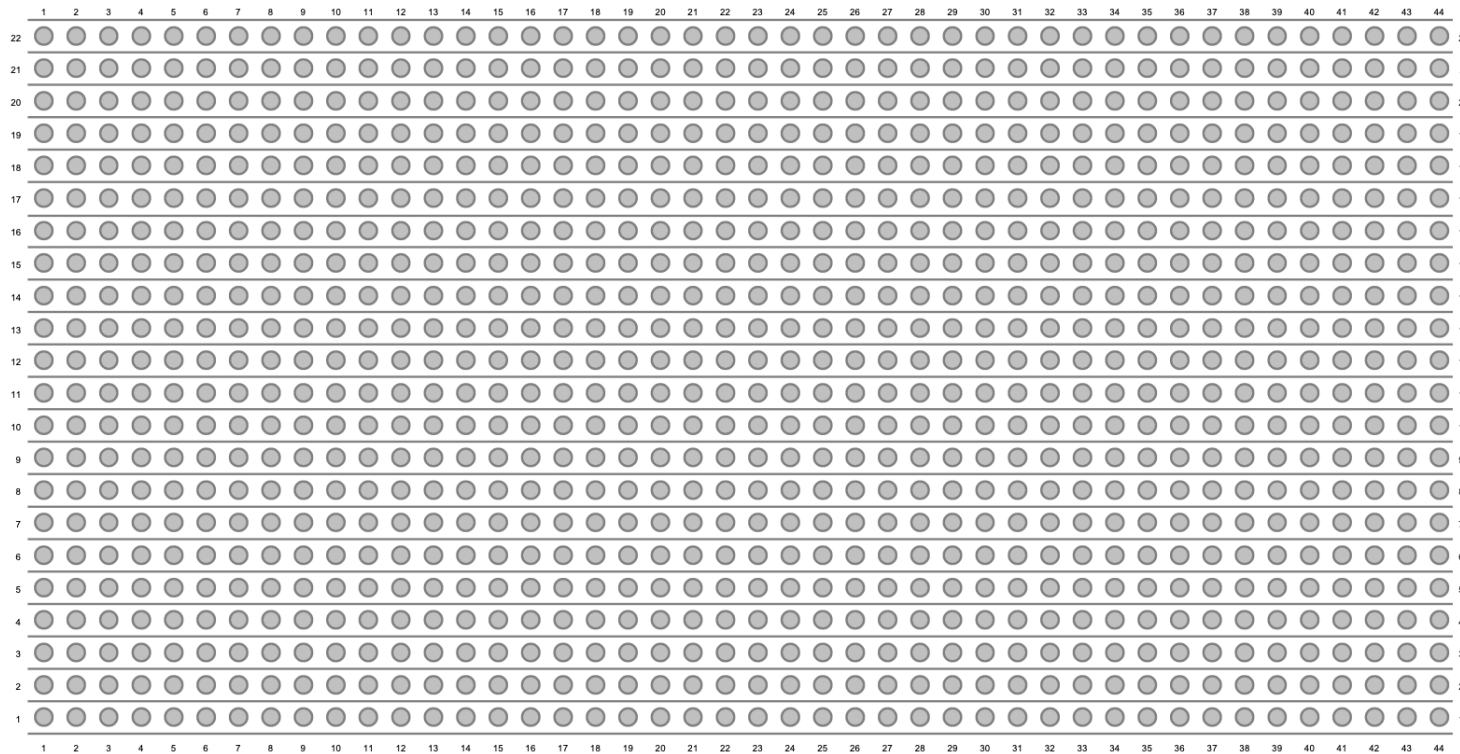
- Mark out the Vs and 0V power lines first, then place the ICs.
- Remember to cut the track between the pins of an IC. Mark the cuts on the diagram with an X.
- Try to make resistors and axial capacitors lay flat on the stripboard. Resistors usually require a gap of 4 holes, capacitors a gap of 8 holes.
- Use the actual size grid on the left to check component spacing.
- Number the pins of the ICs as shown.



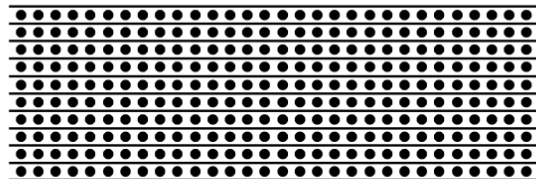
ELECTRONICS IN MECCANO

Stripboard Layout Planning Sheet

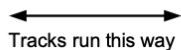
| | |
|--------------|--|
| Project: | |
| Designed by: | |
| Version: | |
| Date: | |
| Notes: | |



Version 3 : 3/02 © 2002 Electronics in Meccano www.eleinmec.com



Actual size stripboard. Hole spacing 0.1" (2.54mm)



Tracks run this way

Tips:

- Mark out the Vs and 0V power lines first, then place the ICs.
- Remember to cut the track between the pins of an IC. Mark the cuts on the diagram with an X.
- Try to make resistors and axial capacitors lay flat on the stripboard. Resistors usually require a gap of 4 holes, capacitors a gap of 8 holes.
- Use the actual size grid on the left to check component spacing.
- Number the pins of the ICs as shown.



ELECTRONICS IN MECCANO

Stripboard Layout Planning Sheet

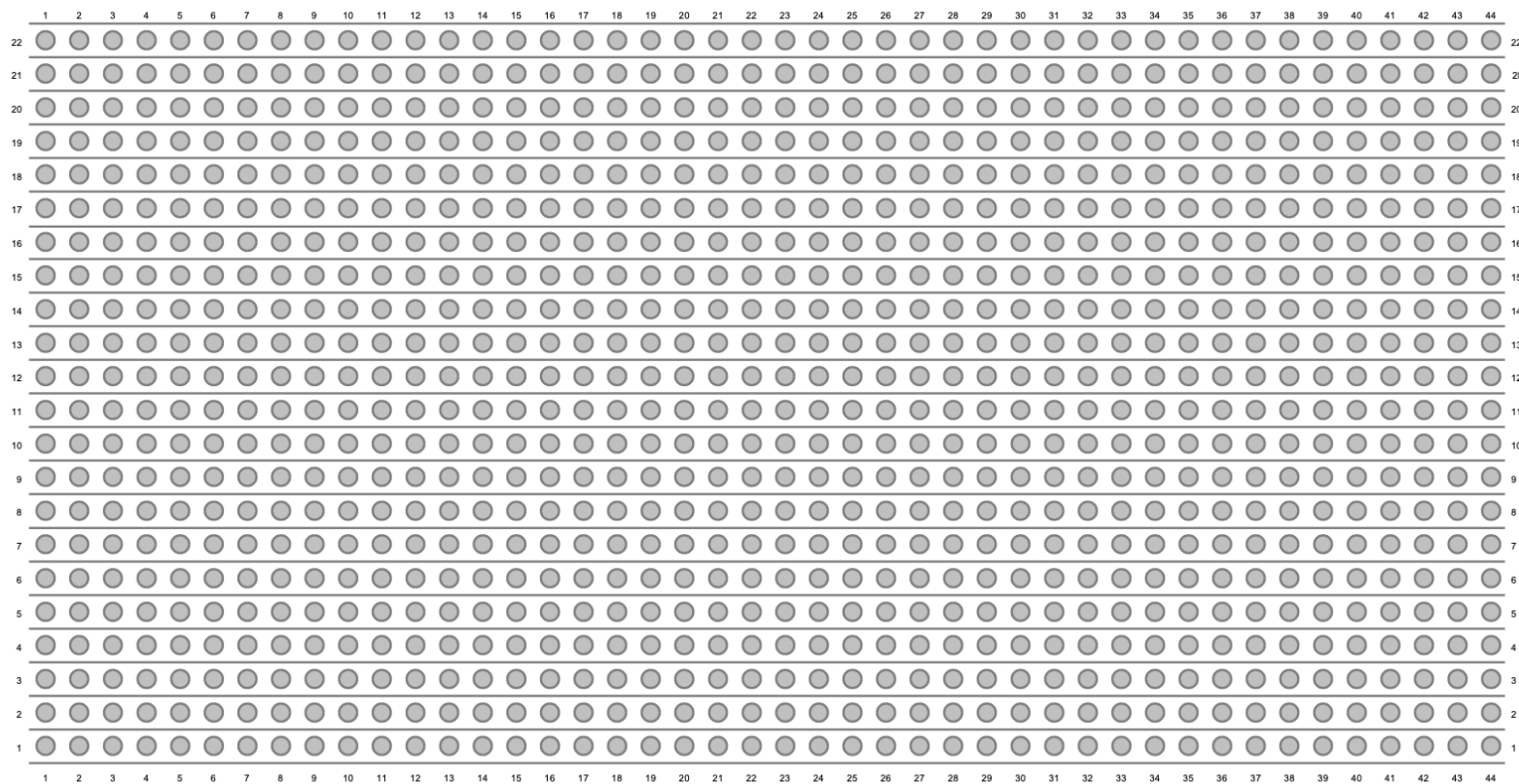
Project:

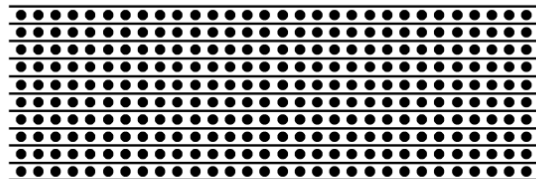
Designed by:

Version:

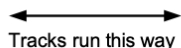
Date:

Notes:





Actual size stripboard. Hole spacing 0.1" (2.54mm)



Tracks run this way

Tips:

- Mark out the Vs and 0V power lines first, then place the ICs.
- Remember to cut the track between the pins of an IC. Mark the cuts on the diagram with an X.
- Try to make resistors and axial capacitors lay flat on the stripboard. Resistors usually require a gap of 4 holes, capacitors a gap of 8 holes.
- Use the actual size grid on the left to check component spacing.
- Number the pins of the ICs as shown.



ELECTRONICS IN MECCANO

Stripboard Layout Planning Sheet

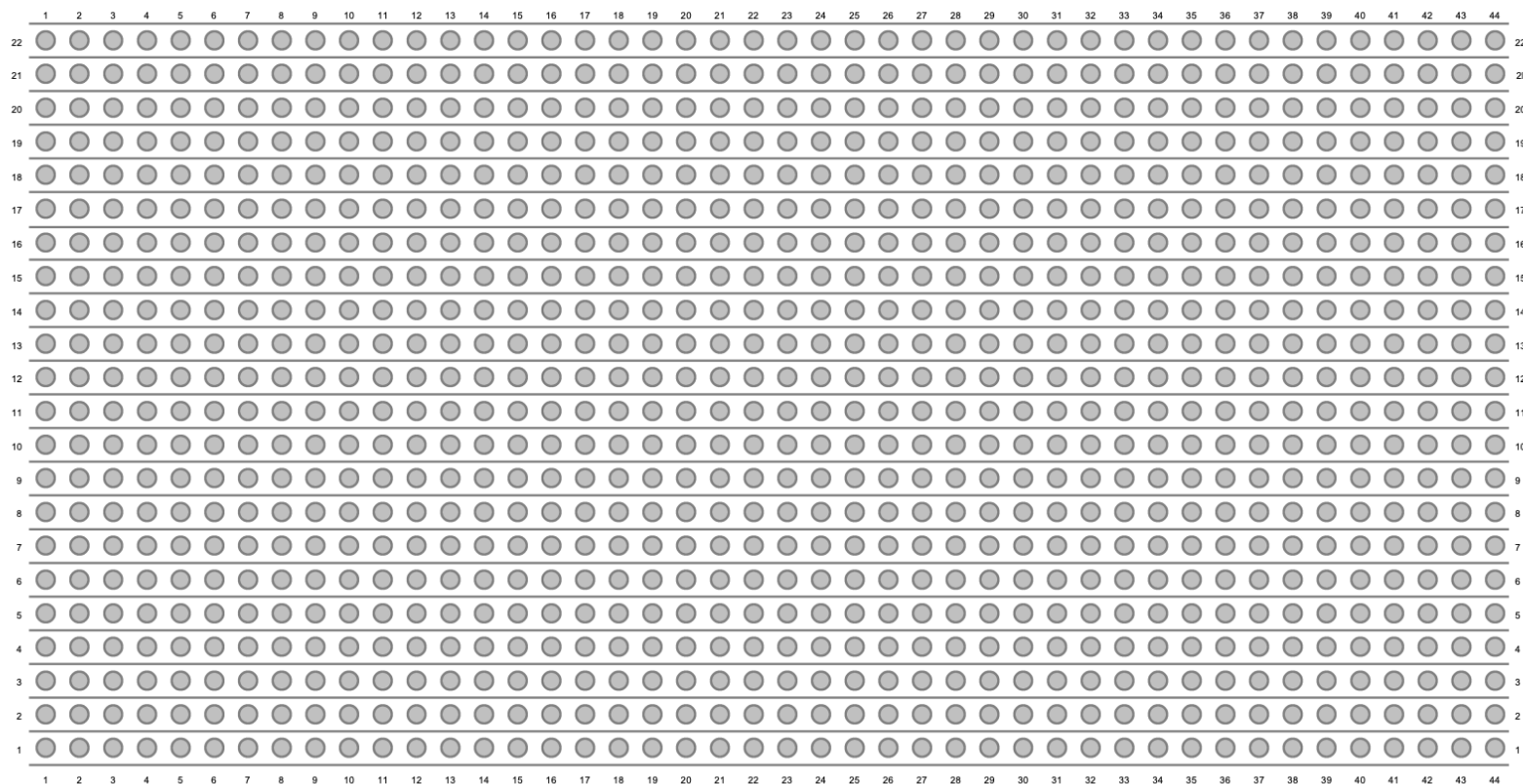
Project:

Designed by:

Version:

Date:

Notes:



TESTING CHECKLISTS

Testing:

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Testing:

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