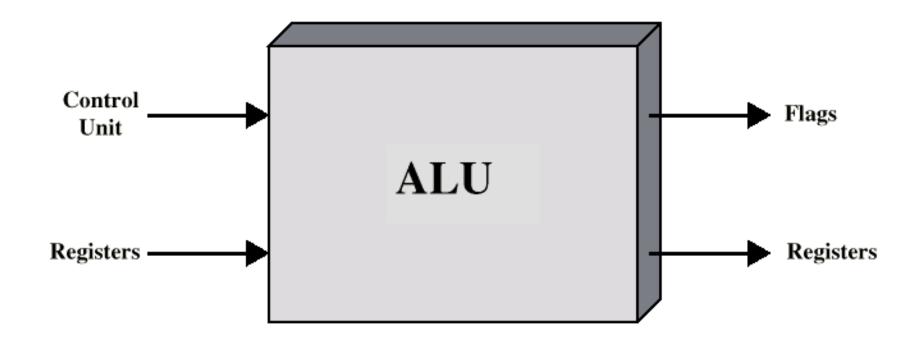
Computer Arithmetic

Arithmetic & Logic Unit

- Does the calculations
- Everything else in the computer is there to service this unit
- Handles integers
- May handle floating point (real) numbers
- May be separate FPU (maths co-processor)
- May be on chip separate FPU (486DX +)

ALU Inputs and Outputs



Conversion Between Lengths

Signed Extension

- Positive number pack with leading zeros
- \bullet +18 = 00010010
- \bullet +18 = 00000000 00010010
- Negative numbers pack with leading ones
- -18 = 10010010
- \bullet -18 = 11111111 10010010
- i.e. pack with MSB (sign bit)

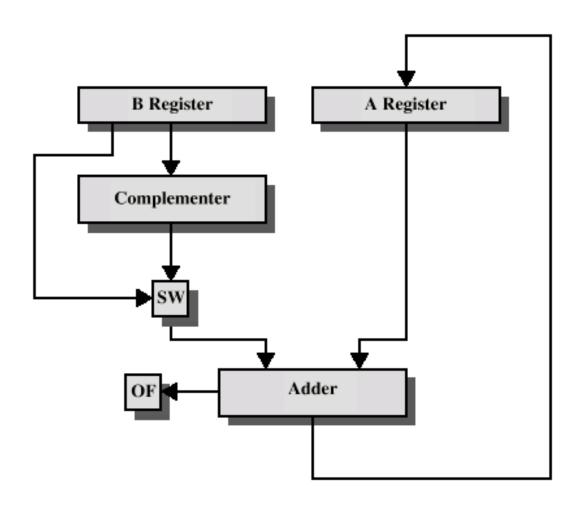
Addition and Subtraction

- Normal binary addition
- Monitor sign bit for overflow
- Take twos compliment of substahend and add to minuend

$$-i.e. a - b = a + (-b)$$

So we only need addition and complement circuits

Hardware for Addition and Subtraction



OF = overflow bit

SW = Switch (select addition or subtraction)

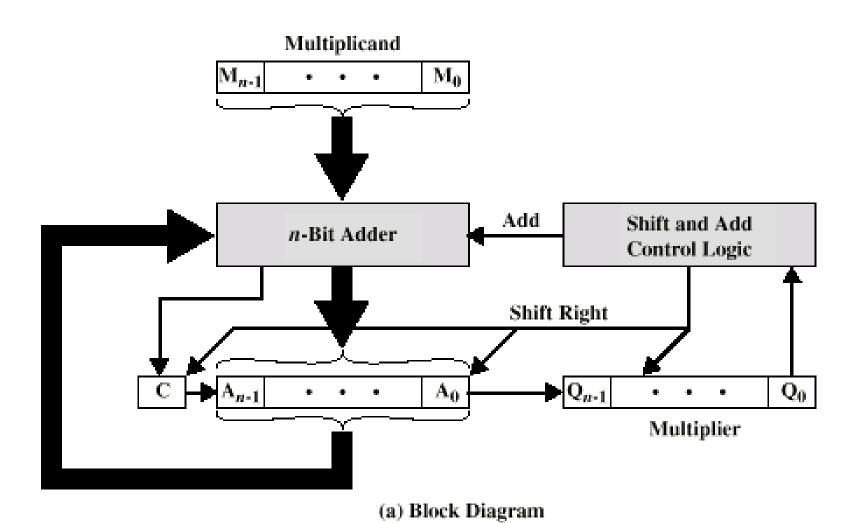
Multiplication

- Complex
- Work out partial product for each digit
- Take care with place value (column)
- Add partial products

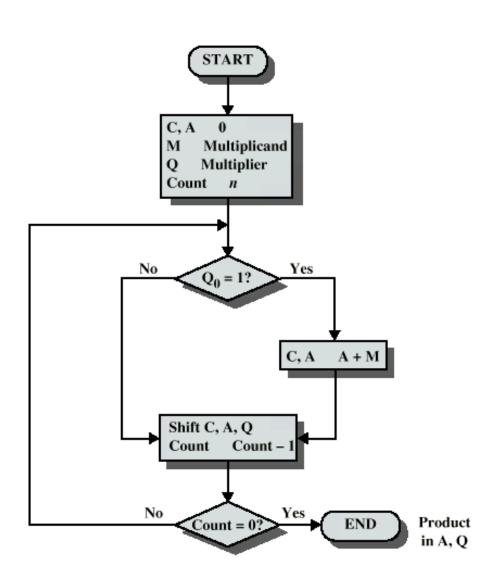
Multiplication Example

- 1011 Multiplicand (11 dec)
- x 1101 Multiplier (13 dec)
- 1011 Partial products
- 0000 Note: if multiplier bit is 1 copy
- 1011 multiplicand (place value)
- 1011 otherwise zero
- 10001111 Product (143 dec)
- Note: need double length result

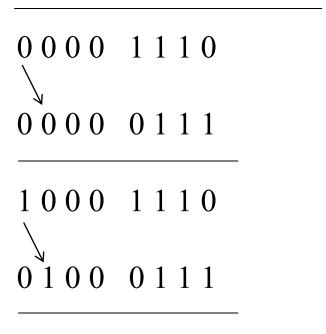
Unsigned Binary Multiplication



Flowchart for Unsigned Binary Multiplication



Simple Right Shift



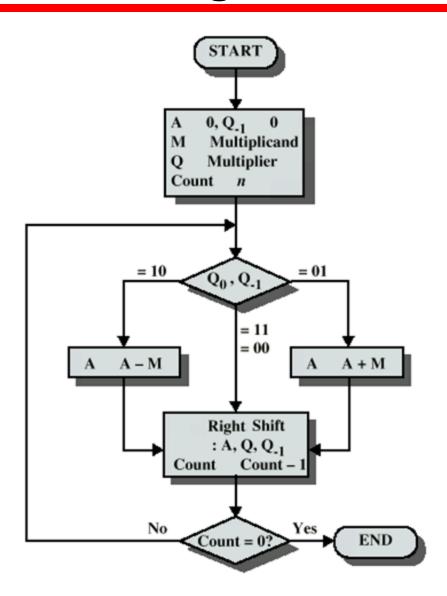
Execution of Example

C 0	A 0000	Q 1101	M 1011	Initial	Values
0	1011	1101	1011	Add	First
	0101	1110	1011	Shift	Cycle
0	0010	1111	1011	Shift }	Second Cycle
0	1101	1111	1011	Add	Third
	0110	1111	1011	Shift	Cycle
1	0001	1111	1011	Add	Fourth
	1000	1111	1011	Shift	Cycle

Multiplying Negative Numbers

- This does not work!
- Solution 1
 - —Convert to positive if required
 - —Multiply as above
 - —If signs were different, negate answer
- Solution 2
 - —Booth's algorithm

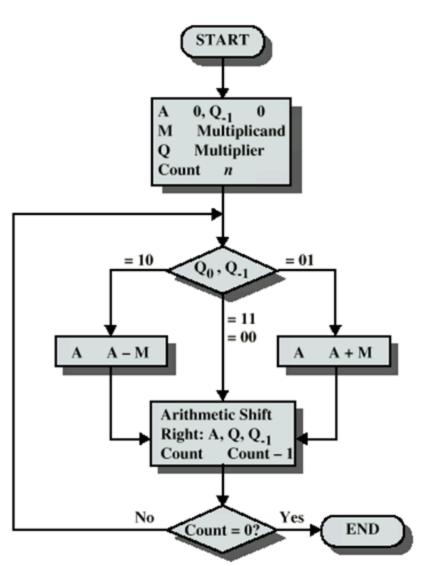
Booth's Algorithm with simple Right Shift



Example of Booth's Algorithm (-4*3)

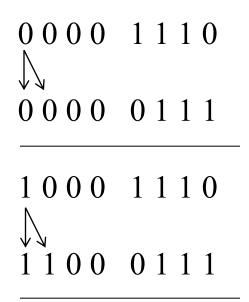
		Мс		Мр								
		-4	*	3								M 1100
		М		Q							-	-M 0100
Constant							Ş			Operation	Мс	: Multiplicand (M)
Counter			Α		Q_3	Q_2	Q_1	Q_0	Q ₋₁	•	Мр	: Multiplier (Q)
4	0	0	0	0	0	0	1	1	0	Initialization	SRS	: Simple Right Shift
	0	1	0	0	0	0	1	1	0	A=A-M	CD	: Counter Decrement
	0	0	1	0	0	0	0	1	1	SRS		
3	0	0	1	0	0	0	0	1	1	CD		START
	0	0	0	1	0	0	0	0	1	SRS		A 0, Q ₁ 0 M Multiplicand Q Multiplier
2	0	0	0	1	0	0	0	0	1	CD		Count n
	1	1	0	1	0	0	0	0	1	A=A+M		= 10 0 = 01
	0	1	1	0	1	0	0	0	0	SRS		$= 10$ $Q_0, Q_{-1} = 01$
1	0	1	1	0	1	0	0	0	0	CD		A A - M = 00 A A + M
	0	0	1	1	0	1	0	0	0	SRS		Right Shift
0	0	0	1	1	0	1	0	0	0	CD		: A, Q, Q ₋₁ Count Count - 1
										STOP		No Count = 0? Yes END

Booth's Algorithm using Arithmetic Right Shift



Use Simple Right Shift OR

Arithmetic Right Shift



Reason: Sign extension in 2's Complement

Note: You can get Answer using both shift..

But simple right shift will need some manipulation in answer in the end

Example of Booth's Algorithm using ARS (7*3)

		Mc 7 M	*	Mp 3 Q								M –M	
Counter			A			(5	-		Operation		Мс	: Multiplicand (M)
					Q_3	Q ₂	Q_1	Q_0	Q ₋₁	operation		Мр	: Multiplier (Q)
4	0	0	0	0	0	0	1	1	0	Initialization]	ARS	: Arithmatic Right Shift
	1	0	0	1	0	0	1	1	0	A= A-M		CD	: Counter Decrement
	1	1	0	0	1	0	0	1	1	ARS		AQ	: Answer
3	1	1	0	0	1	0	0	1	1	CD			START
	1	1	1	0	0	1	0	0	1	ARS			A 0, Q _{.1} 0 M Multiplicand
2	1	1	1	0	0	1	0	0	1	CD			M Multiplicand Q Multiplier Count n
	0	1	0	1	0	1	0	0	1	A= A+M	_		
	0	0	1	0	1	0	1	0	0	ARS			$=10$ Q_0, Q_{-1} $=01$
1	0	0	1	0	1	0	1	0	0	CD			= 11
	0	0	0	1	0	1	0	1	0	ARS		A .	A - M A A + M
0	0	0	0	1	0	1	0	1	0	CD			Arithmetic Shift Right: A, Q, Q, 1 Count Count - 1
										STOP			No Count = 0? Yes END

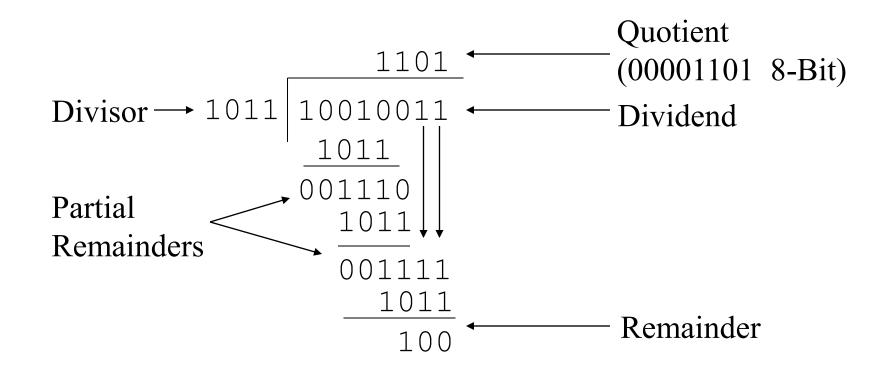
Example of Booth's Algorithm using ARS (-7*3)

Counter A		1001 0111		M –M							Mp 3 Q	*	Mc -7 M		
Counter		Multiplicand (M)	:	Мс	Operation			ζ	(_
0 1 1 1 0 0 1 1 1 0 A=A-M CD : Counter Decrement 0 0 1 1 1 1 0 0 0 1 1 ARS 0 0 0 1 1 1 1 0 0 0 1 ARS 2 0 0 0 1 1 1 1 0 0 1 1 CD 1 0 1 0 1 1 0 1 1 0 0 A=A+M 1 1 0 0 1 0 1 1 0 0 A=A+M 1 1 1 0 1 0 1 1 0 0 CD		Multiplier (Q)	:	Мр		Q ₋₁	Q_0	Q_1	Q_2	Q_3		A			Counter
O O O O O O O O O O		Arithmatic Right Shift	:	ARS	Initialization	0	1	1	0	0	0	0	0	0	4
3 0 0 1 1 1 0 0 0 1 1 CD 0 0 0 0 1 1 1 1 0 0 0 1 ARS 2 0 0 0 1 1 1 0 0 1 1 CD 1 0 1 0 1 1 0 0 1 A=A+M 1 1 0 1 0 1 0 1 1 0 0 CD		Counter Decrement	:	CD	A=A-M	0	1	1	0	0	1	1	1	0	
0 0 0 1 1 1 0 0 1 ARS 2 0 0 0 1 1 1 0 0 1 CD 1 0 1 0 1 0 1 1 0 0 ARS 1 1 1 0 1 0 1 0 1 1 0 0 CD		Answer	:	AQ	ARS	1	1	0	0	1	1	1	0	0	
2 0 0 0 1 1 1 0 0 1 CD 1 0 1 0 1 1 0 0 1 A=A+M 1 1 0 1 0 1 0 1 1 0 0 CD		START			CD	1	1	0	0	1	1	1	0	0	3
2 0 0 0 1 1 1 0 0 1 CD 1 0 1 0 1 1 0 0 1 A=A+M 1 1 0 1 0 1 0 0 ARS		A 0, Q ₋₁ 0			ARS	1	0	0	1	1	1	0	0	0	
1 1 0 1 0 1 1 0 0 ARS 1 1 1 0 1 0 1 1 0 0 CD		Q Multiplier			CD	1	0	0	1	1	1	0	0	0	2
1 1 1 0 1 0 1 1 0 0 CD					A=A+M	1	0	0	1	1	0	1	0	1	
A A - M		$= 10$ $Q_0, Q_{-1} = 01$			ARS	0	0	1	1	0	1	0	1	1	
		-00			CD	0	0	1	1	0	1	0	1	1	1
	1	A A + M			ARS	0	1	1	0	1	0	1	1	1	
0 1 1 1 0 1 0 1 1 0 CD Arithmetic Shift Right: A, Q, Q, 1 Count Count 1		Arithmetic Shift Right: A, Q, Q ₋₁			CD	0	1	1	0	1	0	1	1	1	0
STOP STOP		Count Count - 1			STOP										

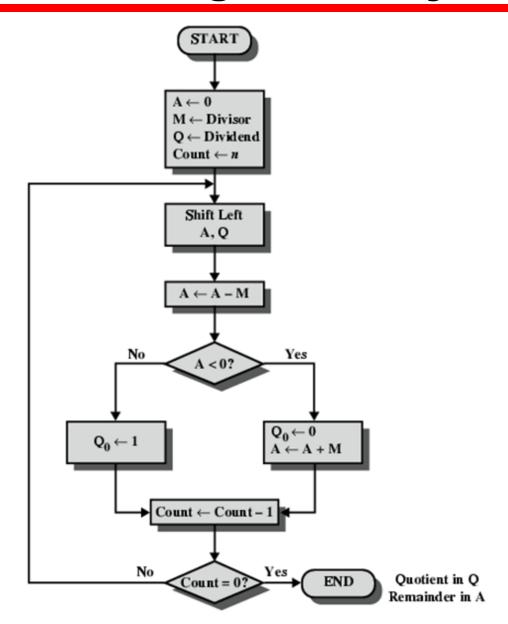
Division

- More complex than multiplication
- Negative numbers are really bad!
- Based on long division

Division of Unsigned Binary Integers



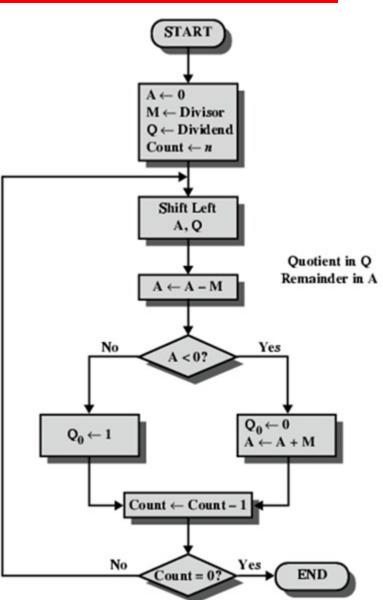
Flowchart for Unsigned Binary Division



Binary Division: Example

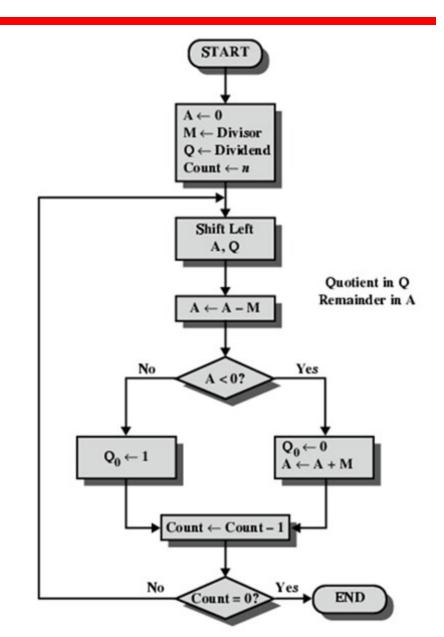
Dividend (Q) = 11, Devisor(M) = 3

n	M	A	Q	Operation	
4	0011	0000	1011	initialize	
	0011	0001	011	shift left AQ	
	0011	1110	011_	A=A-M (Using 2's Compl)	
	0011	0001	0110	Q[0]=0 and	
				Restore A i.e. A=A+M	
3	0011	0010	110_	shift left AQ	
	0011	1111	110	A=A-M	1 – –
	0011	0010	1100	Q[0]=0, Restore A	1 1
2	0011	0101	100	shift left AQ	Q ₀ ←
	0011	0010	100	A=A-M	V ₀ (-
	0011	0010	$100\overline{1}$	Q[0]=1	
1	0011	0101	001	shift left AQ	-
	0011	0010	001	A=A-M	
	0011	0010	0011	Q[0]=1	



Problem

- 1. 2/2
- 2. 4/2



Division of signed numbers

Use previously taught division algorithm and adjust sign later

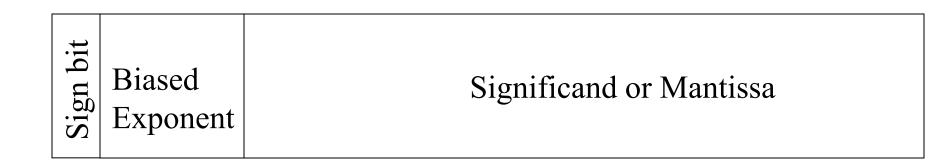
Real Numbers

- Numbers with fractions
- Could be done in pure binary

$$-1001.1010 = 2^4 + 2^0 + 2^{-1} + 2^{-3} = 9.625$$

- Where is the binary point?
- Fixed?
 - —Very limited
- Moving?
 - —How do you show where it is?

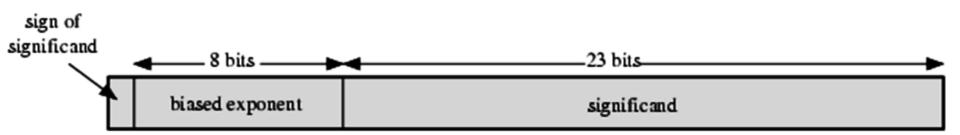
Floating Point



- +/- .significand x 2^{exponent}
- Misnomer
- Point is actually fixed between sign bit and body of mantissa
- Exponent indicates place value (point position)

Floating Point Examples

(a) Format



(b) Examples

Signs for Floating Point

- Mantissa is stored in 2s compliment
- Exponent is in excess or biased notation
 - -e.g. Excess (bias) 128 means
 - —8 bit exponent field
 - —Pure value range 0-255
 - —Subtract 128 to get correct value
 - —Range -128 to +127

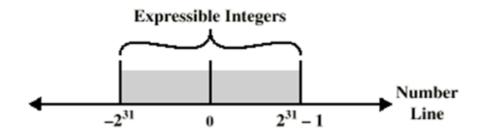
Normalization

- FP numbers are usually normalized
- i.e. exponent is adjusted so that leading bit (MSB) of mantissa is 1
- Since it is always 1 there is no need to store it
- (c.f. Scientific notation where numbers are normalized to give a single digit before the decimal point
- e.g. 3.123 x 10³)

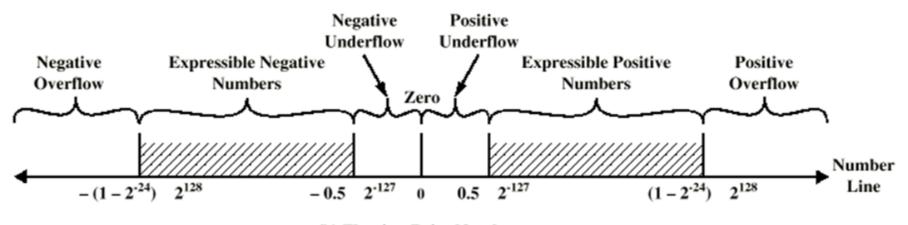
FP Ranges

- For a 32 bit number
 - —8 bit exponent
 - $-+/-2^{256} \approx 1.5 \times 10^{77}$
- Accuracy
 - —The effect of changing lsb of mantissa
 - -23 bit mantissa $2^{-23} \approx 1.2 \times 10^{-7}$
 - —About 6 decimal places

Expressible Numbers

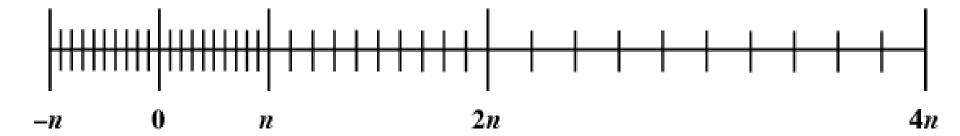


(a) Twos Complement Integers



(b) Floating-Point Numbers

Density of Floating Point Numbers



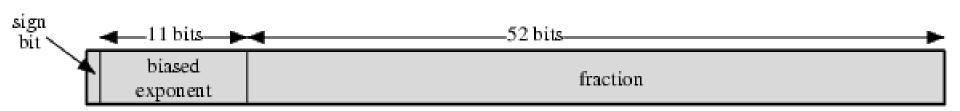
IEEE 754

- Standard for floating point storage
- 32 and 64 bit standards
- 8 and 11 bit exponent respectively
- Extended formats (both mantissa and exponent) for intermediate results

IEEE 754 Formats



(a) Single format

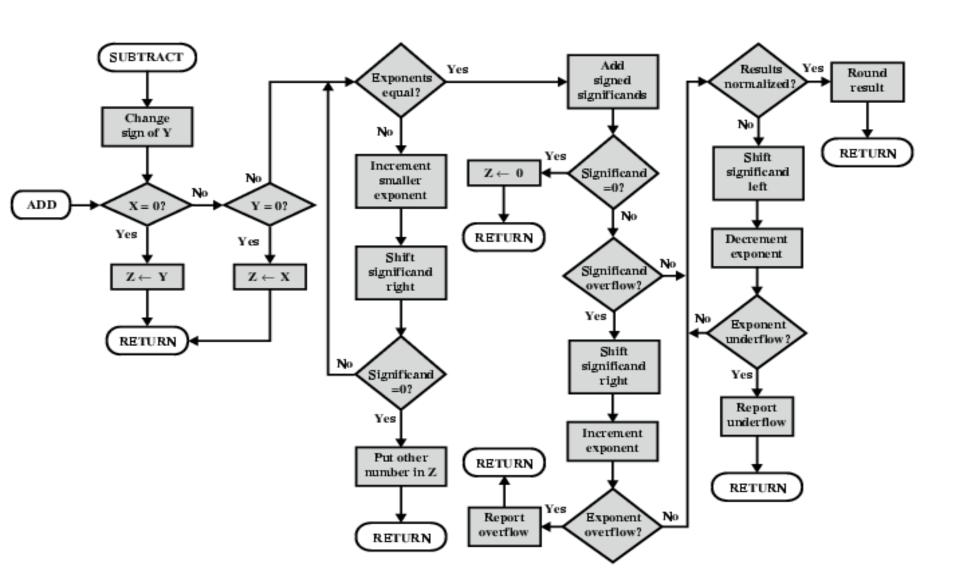


(b) Double format

FP Arithmetic +/-

- Check for zeros
- Align significands (adjusting exponents)
- Add or subtract significands
- Normalize result

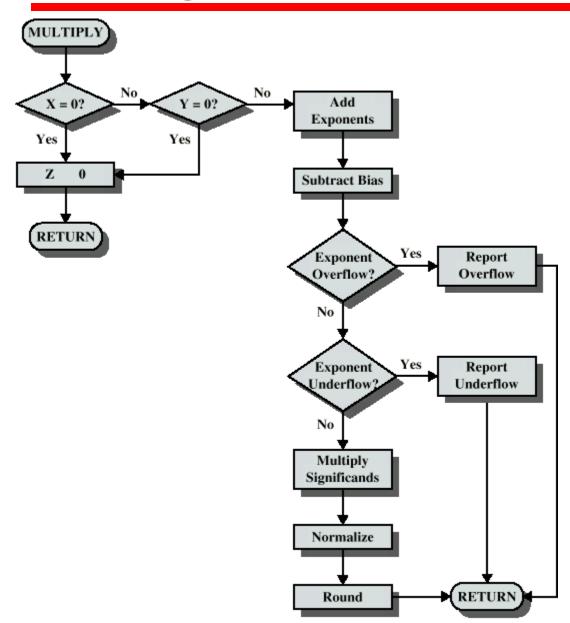
FP Addition & Subtraction Flowchart



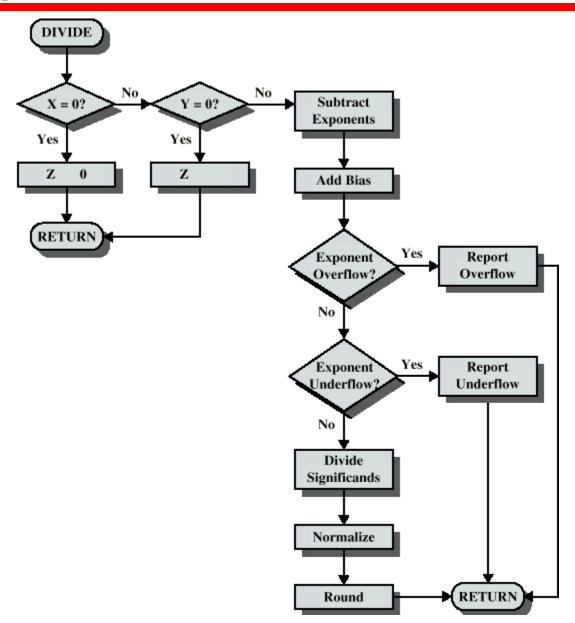
FP Arithmetic x/÷

- Check for zero
- Add/subtract exponents
- Multiply/divide significands (watch sign)
- Normalize
- Round
- All intermediate results should be in double length storage

Floating Point Multiplication



Floating Point Division



Required Reading

- William Stallings Chapter 9
- IEEE 754 on IEEE Web site