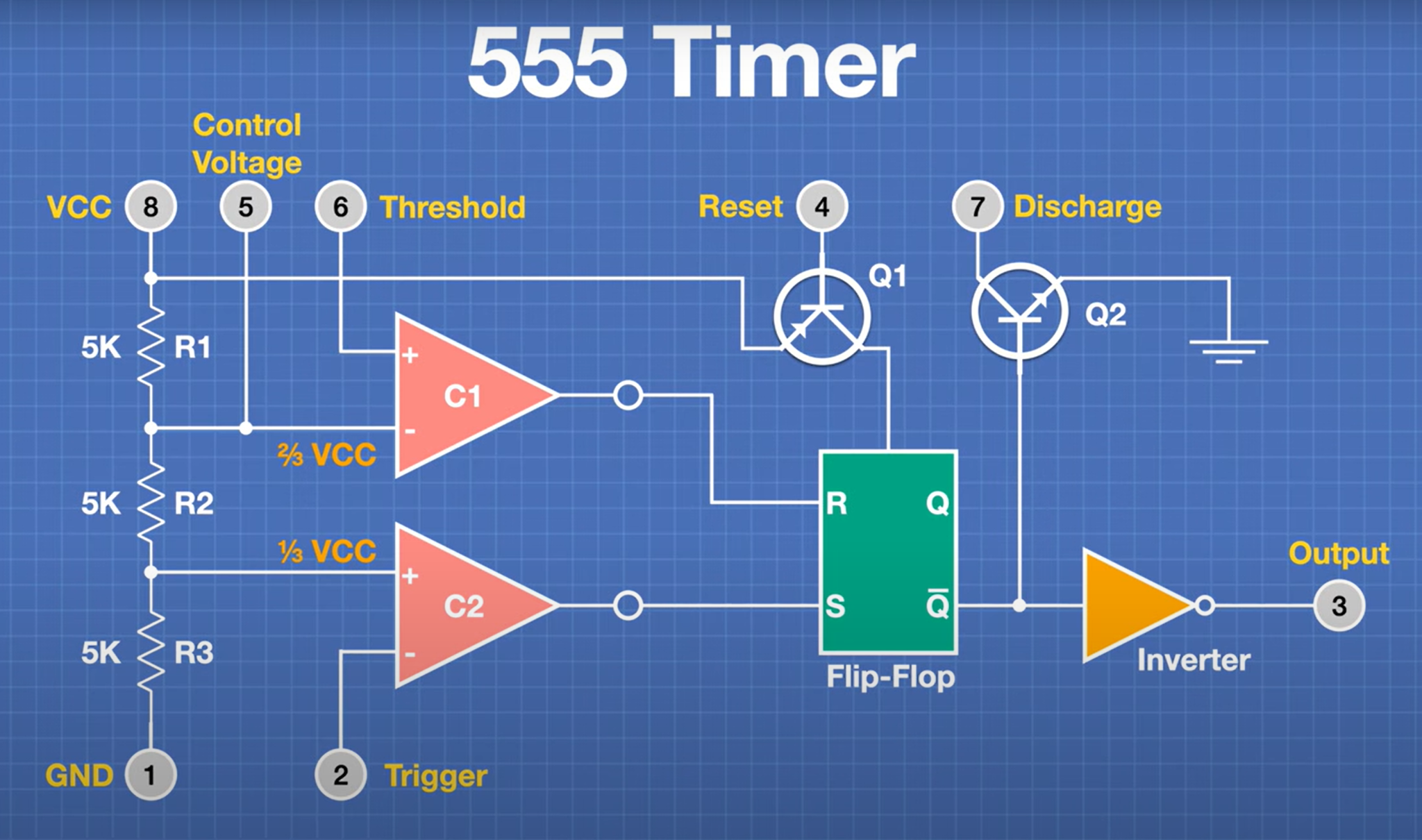
**Task-2: Designing a PWM Generator using 555 Timer at two frequencies**

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23EC10068

**Objective:** To design a PWM generator using a 555 Timer IC at two specified frequencies (490Hz, 980Hz)

**555 Timer IC:** The 555 timer is an integrated circuit that can be used to create pulses, delays, etc.



**Components:**

1. **Comparator:** If the voltage at the positive pin of the comparator is higher than that at the negative pin, it returns a logic HIGH. Else if the voltage at the positive pin of the comparator is lesser than that at the negative pin, it returns a logic LOW.
2. **Flip-Flop:** The SR Flip-Flop takes in two inputs, SET (S) and RESET (R). The output Q is HIGH when R is LOW and S is HIGH. When both R and S are HIGH, the state of Q cannot be determined. In the other cases, Q is LOW.
3. **Transistors:** The two transistors used are used as a switch.

**Truth Table:**

| **Threshold** | **Trigger** | **R** | **S** | **Q** | **NOT Q** |
| --- | --- | --- | --- | --- | --- |
| LOW | LOW | LOW | HIGH | HIGH | LOW |
| LOW | HIGH | LOW | LOW | previous state | previous state |
| HIGH | HIGH | HIGH | LOW | LOW | HIGH |
| HIGH | LOW | HIGH | HIGH | - | - |

**Working of the circuit:**

Initially, when the circuit is just turned on, the capacitor Ct is fully uncharged. Hence the output of C1 is LOW and C2 is HIGH. This implies that Q = HIGH and Q’ = LOW.

As Q’ is LOW, the transistor connected to the discharge pin is in an OFF condition. Thus, the capacitor Ct is charged. As the capacitor is charged, the voltage at the TRIGGER and THRESHOLD pins start increasing.

When the voltage at the pins just crosses Vcc/3, the output of C1 would be LOW and C2 would be LOW. As both RESET and SET are LOW, the output Q remains the same as the previous state, i.e. Q = HIGH and Q’ = LOW.

When the voltage at the pins just crosses 2Vcc/3, both TRIGGER and THRESHOLD would be at a higher potential. Thus, the output of C1 is HIGH and C2 is LOW. As RESET is HIGH and SET is LOW, the output Q = LOW / Q’ = HIGH. As Q’ is HIGH, the transistor turns to an ON state and the capacitor is discharged through the transistor and the voltage of the pins will gradually decrease to 2Vcc/3.

When the voltage of the capacitance is just lesser than 2Vcc/3, C1 would be LOW and C2 would be HIGH. Hence, as RESET and SET are both LOW, the state will remain as the previously existing one, i.e. Q = LOW and Q’ = HIGH.

Once the pins reduce to a voltage of Vcc/3, C1 would give an output of LOW and C2 would give HIGH. Hence, the output Q becomes HIGH again and as Q’ is LOW, the transistor switches to the OFF condition and the capacitor starts charging again.

**Calculations:**

The charge on the capacitor changes as follows:

0 —> 2CV/3 —> CV/3 —> 2CV/3 …

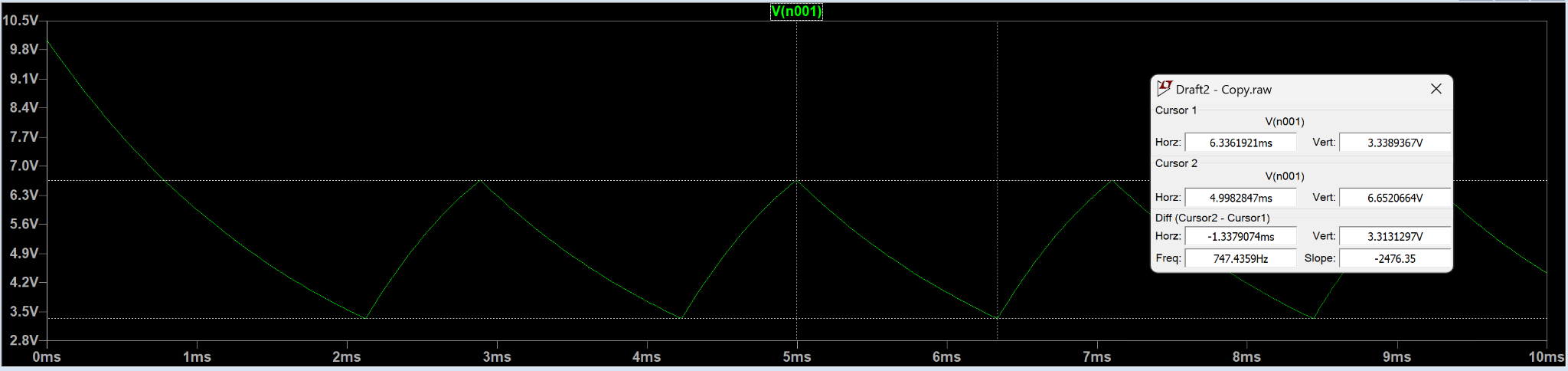
Initially when the circuit is turned on, the capacitor contains a net charge of 0. It first charges to 2CV/3 and then discharges to CV/3. After which, it charges back to 2CV/3 and the cycle continues. When the **capacitor charges**, the output Q corresponds to **HIGH**, while when the **capacitor discharges**, the output Q corresponds to **LOW**.

1. **LOW Time:** The low time of the cycle occurs when the charge is discharged from the capacitor from 2CV/3 to CV/3.

* Thus, q(t) = (2CV/3) x e-t/T1, where T1 is the time constant of the circuit
* Putting q(t) = CV/3, **tLOW = T1(ln2)**

1. **HIGH Time:** The high time of the cycle occurs when the charge is charged from the capacitor from CV/3 to 2CV/3.

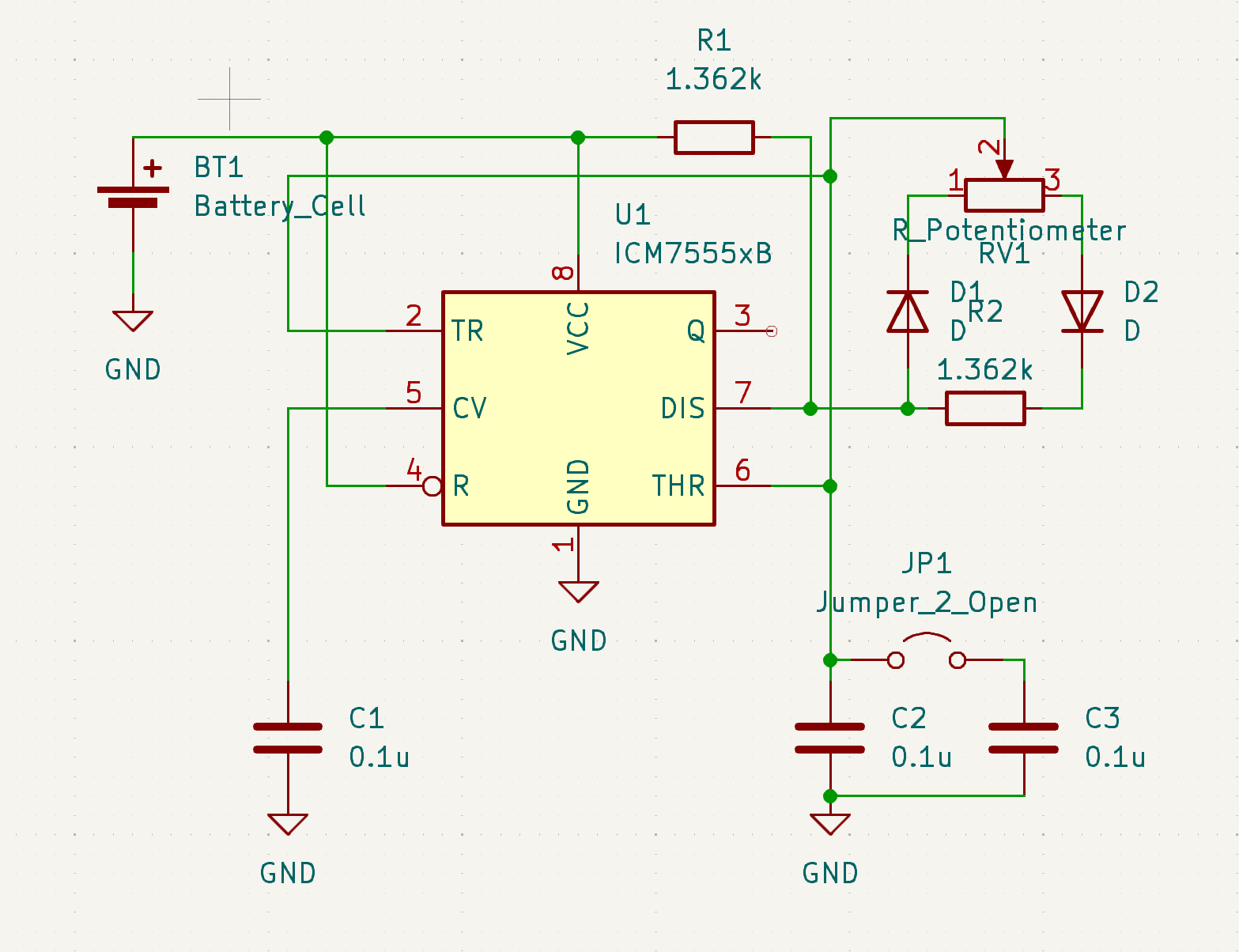
* Thus, q(t) = CV(1 - (⅔)x e-t/T2) , where T2 is the time constant of the circuit
* Putting q(t) = 2CV/3, **tHIGH = T2(ln2)**



When V = 10V, as shown in the graph above, the maximum and minimum potentials correspond to 2V/3 (6.67V) and V/3 (3.33V).

**Note that these calculations are correct assuming the diodes to be ideal.**

**Circuit Schematic:**

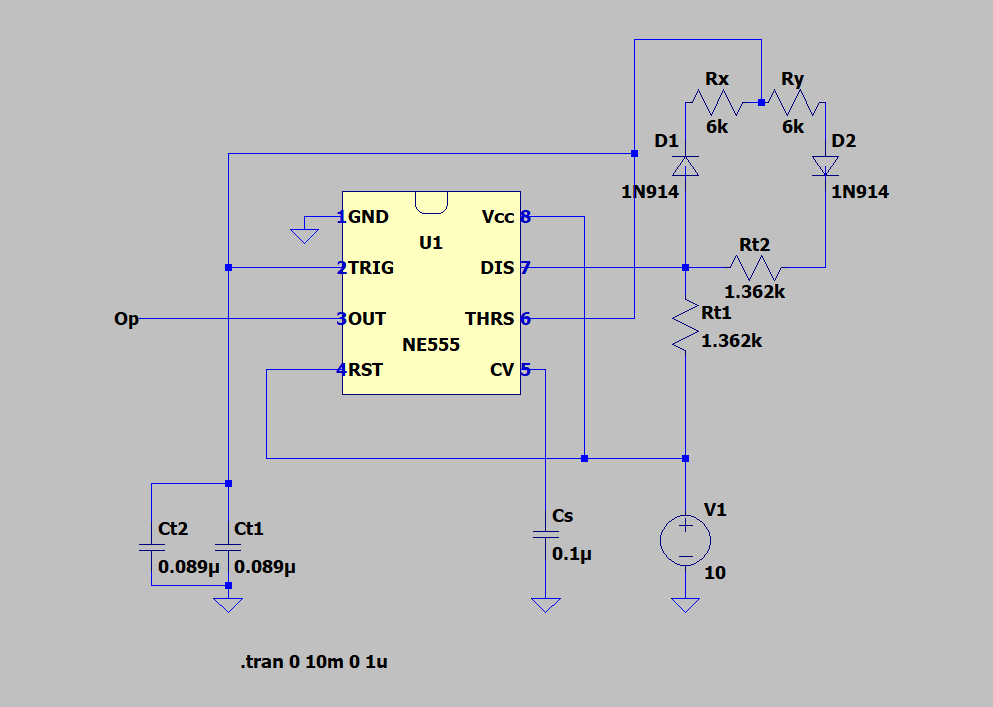


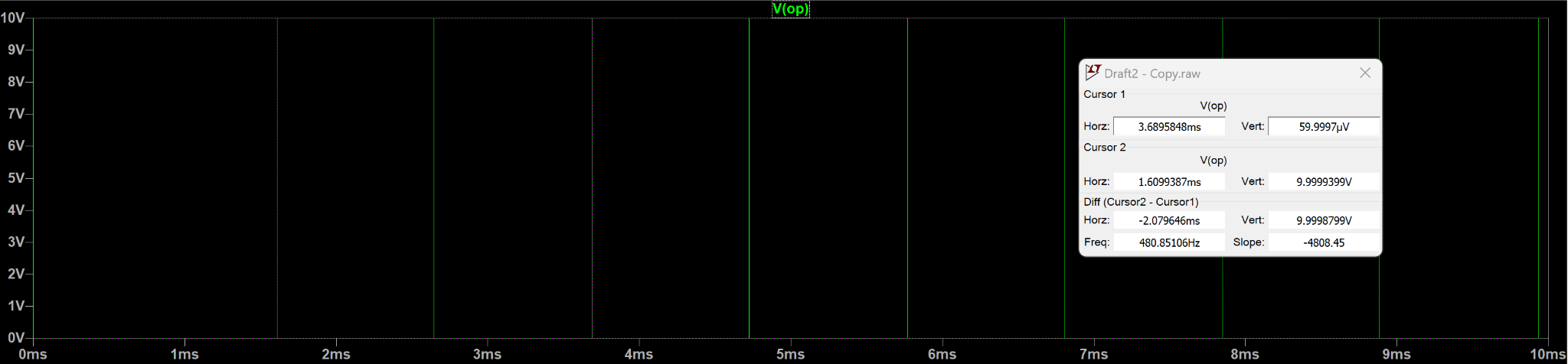
**The link below contains the schematics and PCB layouts I made for the task.**

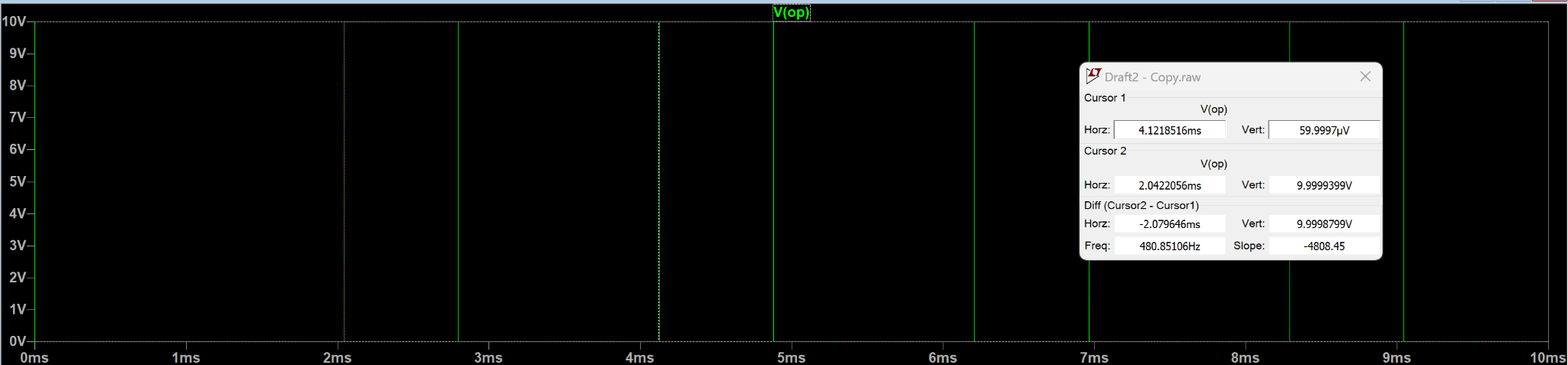
[Task-2](https://drive.google.com/drive/folders/1spYkEWWHwJom_PVyDvGPrEbl7C4A3Fct?usp=sharing)

**Simulation Results:**

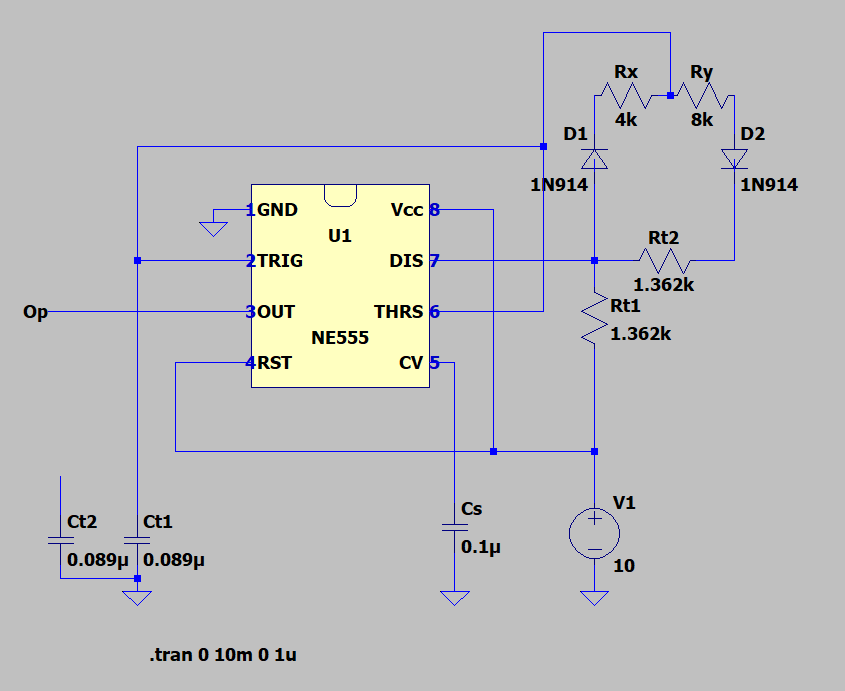
**480Hz:** Connecting the two capacitances in parallel

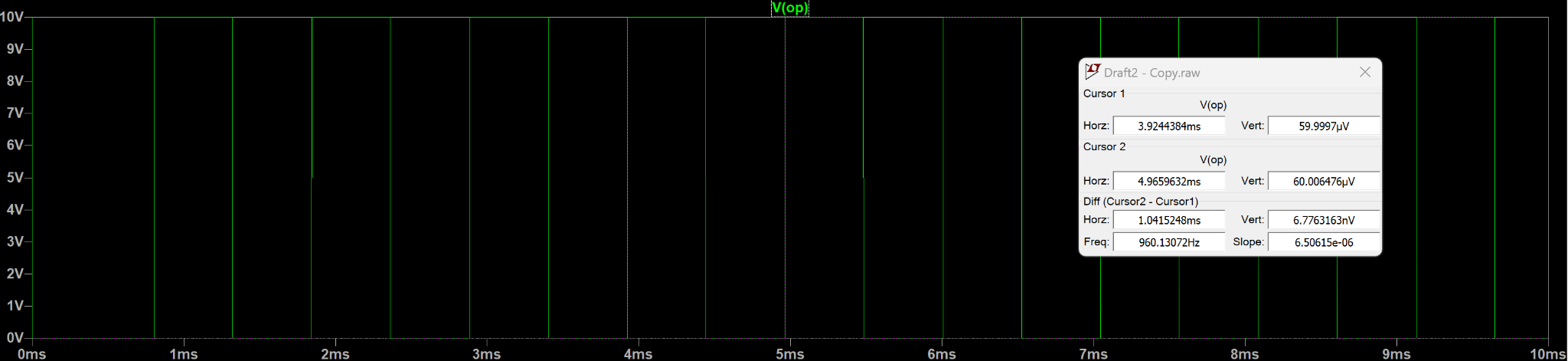


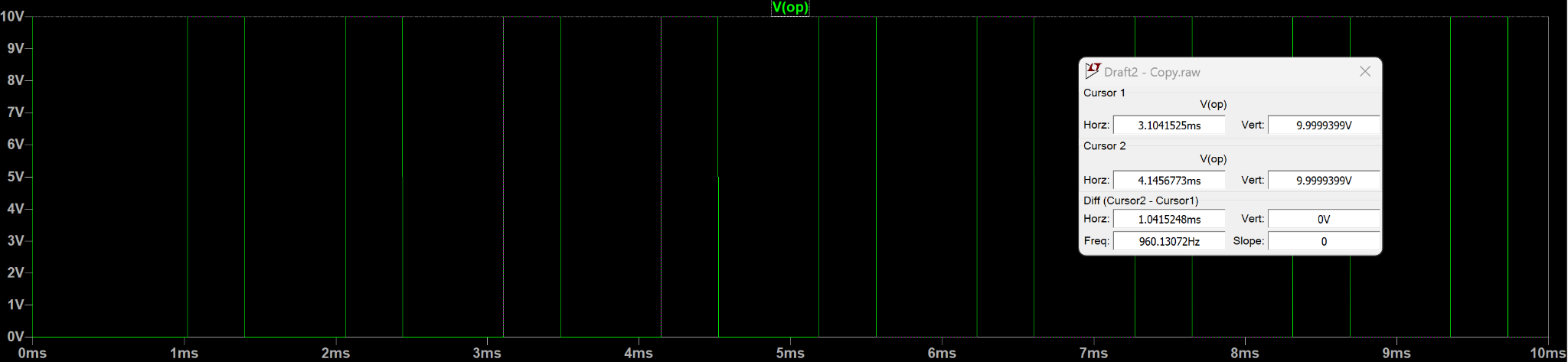
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**960Hz:** Connecting only one capacitance







**Difficulties / Problems Faced:**

Initially when I connected two resistances in the general Astable state connections. I got the following to be the low and high times of the signal:

**tHIGH = (R1+R2)(ln2)(Ct), tLOW = (R2)(ln2)(Ct)**

Hence the net time period **T= (R1+2R2)(ln2)(Ct).**

To switch between the two frequencies, I used an external switch to change the value of the capacitance Ct by using the switch to connect another capacitance in parallel to the first one. This however keeps the duty cycle same as the ratio between tHIGH and tLOW was same even after changing the capacitance.

To alter the duty cycle, it was evident that the resistances had to be changed, but changing the resistances would cause the frequency to be altered unless the net change of R1+2R2 equals zero.

Hence, I used a diode connection to make it such that the low and high times of the signal are:

**tHIGH = (R1+Rx)(ln2)(Ct), tLOW = (R2+Ry)(ln2)(Ct)**

Where Rx+Ry equals a constant resistance R, and the resistances Rx and Ry are varied by the rheostat. Thus, the net time period **T= (R1+R2+R)(ln2)(Ct)** which is constant in the given circuit. As Rx and Ry can be altered, the ratio between tHIGH and tLOW can vary, and hence the duty cycle can be changed accordingly.

Another issue I faced was with the potential drop caused by the diodes. When I ran the simulation, the results were slightly different from what I calculated. Hence, I had to adjust the value of the capacitance accordingly to get the desired frequency.