USB hardware and PCB guidelines using STM32 MCUs

Introduction

STM32 microcontrollers include a group of products embedding a USB (Universal Serial Bus) peripheral (see the table below for applicable products). Full-speed and high-speed operations are provided through embedded and/or external PHYs (physical layers of the open system interconnection model).

This application note gives an overview of the USB peripherals implemented on STM32 MCUs. It also provides hardware guidelines for PCB design, to ensure electrical compliance with the USB standards.

For more details, refer to USB or OTG sections in the product reference manual.

Table 1. Applicable products

Type	Reference	Series, lines, part numbers
Microcontrollers	Complete series	STM32F2 Series, STM32L1 Series, STM32L4+ Series
	Complete lines	STM32F102, STM32F103, STM32F105/107, STM32F373, STM32F401, STM32F405/415, STM32F407/417, STM32F411, STM32F412, STM32F413/423, STM32F427/437, STM32F429/439, STM32F446, STM32F469/479, STM32F7x2, STM32F7x3, STM32L0x2, STM32L0x3, STM32L4x2, STM32L4x3, STM32L4x5, STM32L4x6, STM32H743/753, STM32H750 Value line
	STM32F04xxx	STM32F042C4, STM32F042C6, STM32F042F4, STM32F042F6, STM32F042G4, STM32F042G6, STM32F042K4, STM32F042K6, STM32F042T4, STM32F042T6, STM32F048C6, STM32F048G6, STM32F048T6
	STM32F072xx	STM32F072C8, STM32F072CB, STM32F072R8, STM32F072RB, STM32F072V8, STM32F072VB
	STM32F078xx	STM32F078CB, STM32F078RB, STM32F078VB
	STM32F070xx	STM32F070C6, STM32F070CB, STM32F070F6, STM32F070RB
	STM32F302x6	STM32F302C6, STM32F302K6, STM32F302R6
	STM32F302x8	STM32F302C8, STM32F302K8, STM32F302R8
	STM32F302xB	STM32F302CB, STM32F302RB, STM32F302VB
	STM32F302xC	STM32F302CC, STM32F302RC, STM32F302VC
	STM32F302xD	STM32F302CD, STM32F302RD, STM32F302VD, STM32F302ZD
	STM32F302xE	STM32F302RE, STM32F302VE, STM32F302ZE
	STM32F303xB	STM32F303CB, STM32F303RB, STM32F303VB
	STM32F303xC	STM32F303CC, STM32F303RC, STM32F303VC
	STM32F303xD	STM32F303CD, STM32F303RD, STM32F303VD, STM32F303ZD
	STM32F303xE	STM32F303RE, STM32F303VE, STM32F303ZE
	STM32F74xxx	STM32F745IE, STM32F745IG, STM32F745VE, STM32F745VG, STM32F745ZE, STM32F745ZG, STM32F746BE, STM32F746BG, STM32F746IE, STM32F746IG, STM32F746NE, STM32F746NG, STM32F746VE, STM32F746VG, STM32F746ZE, STM32F746ZG
	STM32F756xx	STM32F756BG, STM32F756IG, STM32F756NG, STM32F756VG, STM32F756ZG
	STM32F76xxx	STM32F765BI, STM32F765IG, STM32F765II, STM32F765NG, STM32F765NI, STM32F765VG, STM32F765VI, STM32F765ZG, STM32F765ZI, STM32F767BG, STM32F767BI, STM32F767IG, STM32F767II, STM32F767NG, STM32F767NI, STM32F767VG, STM32F767VI, STM32F767ZG, STM32F767ZI, STM32F768AI, STM32F769AG, STM32F769AI, STM32F769BG, STM32F769BI, STM32F769IG, STM32F769II, STM32F769NG, STM32F769NI, STM32F769SL
	STM32F77xxx	STM32F777BI, STM32F777II, STM32F777NI, STM32F777VI, STM32F777ZI, STM32F778AI, STM32F779AI, STM32F779BI, STM32F779II, STM32F779NI

1 General information

This document applies to STM32 microcontrollers which are based on Arm® cores.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Table 2. Abbreviations and acronyms

Acronym	Description
ADP	Attach detection protocol
BCP	Battery charging detection
EMI	Electromagnetic interference
ESD	Electrostatic discharge
FS	Full-speed
HBM	Human body model
HS	High-speed
IEC	International electrotechnical commission
LPM	Link power management
LS	Low-speed
MCU	Microcontroller unit or microcontroller
OTG	On-the-go
PCB	Printed circuit board
PHY	Physical layer
SOF	Start of frame
ULPI	UTMI + low-pin interface
USB	Universal Serial Bus
UTMI	USB 2.0 transceiver macrocell interface

References

- System Level ESD-expanded, JEDEC, September 2013.
- Improve System ESD Protection While Lowering On-Chip ESD Protection, www.mobiledevdesign.com, February 2009.
- USB 2.0 specification, revision 2.0, April 2000, available at www.usb.org.
- On The Go and Embedded Host Supplement to the USB revision 2.0 specification, revision 2.0, July 2012 available at www.usb.org.
- High Speed USB Platform Design Guidelines, available at www.usb.org.

2 USB on STM32 products

Each device with USB support embeds at least one of the following interfaces:

- A: USB 2.0 FS device interface
- B: USB 2.0 OTG FS, that is, USB 2.0 FS device/host/OTG controller with on-chip FS PHY
- C: USB 2.0 OTG HS, that is, USB 2.0 FS/HS device/host/OTG controller, integrating the transceivers for full-speed operation, and featuring an ULPI for high-speed operation: an external PHY device connected to the ULPI is required.
- D: USB 2.0 OTG HS controller with embedded on-chip HS PHYs

The table below lists the STM32 devices supporting a USB, and describes which USB peripheral is implemented in each of them.

Table 3. USB implementation in STM32 devices

Series, lines, or references		Supported USB(1)				Size of dedicated packet buffer SRAM	Dedicated V_{DDUSB}	Embedded pull-up resistor on USB_DP line
		A	B	C	D			
STM32F0 Series	STM32F04x, STM32F072, STM32F078, STM32F070x6/B	X	-	-	-	1 Kbyte	No	Yes
STM32F1 Series	STM32F102 line, STM32F103 line	X	-	-	-	512 bytes	No	-(2)
	STM32F105/107 line	-	X	-	-	1.25 Kbytes	No	Yes
STM32F2 Series		-	X	-	-	1.25 Kbytes	No	Yes
		-	-	X	-	4 Kbytes	No	Yes
STM32F3 Series	STM32F302xB/C, STM32F303xB/C, STM32F373 line	X	-	-	-	512 bytes	No	-(2)
	STM32F302x6/8, STM32F302xD/E, STM32F303xD/E	X	-	-	-	1 Kbyte	No	-(2)
STM32F4 Series(3)	STM32F405/415 line, STM32F407/417 line, STM32F427/437 line, STM32F429/439 line, STM32F401 line, STM32F411 line	-	X	-	-	1.25 Kbytes	No	Yes
		-	-	X	-	4 Kbytes	No	Yes
	STM32F446 line, STM32F469/479 line, STM32F412 line, STM32F413/423 line	-	X	-	-	1.25 Kbytes	Yes	Yes
		-	-	X	-	4 Kbytes	Yes	Yes
STM32F7 Series	STM32F74x, STM32F756, STM32F76x, STM32F77x, STM32F7x2 line	-	X	-	-	1.25 Kbytes	Yes	Yes
		-	-	X	-	4 Kbytes	Yes	Yes
	STM32F7x3 line	-	X	-	-	1.25 Kbytes	Yes	Yes
		-	-	-	X	4 Kbytes	Yes	Yes
STM32L0 Series	STM32L0x2 line, STM32L0x3 line	X	-	-	-	1 Kbyte	Yes	Yes
STM32L1 Series		X	-	-	-	512 bytes	No	Yes
STM32L4 Series	STM32L4x2 line, STM32L4x3 line	X	-	-	-	1 Kbyte	Yes	Yes

Series, lines, or references		Supported USB[1]				Size of dedicated packet buffer SRAM	Dedicated V_{DDUSB}	Embedded pull-up resistor on USB_DP line
		A	B	C	D			
STM32L4 Series	STM32L4x5 line, STM32L4x6 line	-	X	-	-	1.25 Kbytes	Yes	Yes
STM32L4+ Series		-	X	-	-	1.25 Kbytes	Yes	Yes
STM32H7 Series	STM32H743/753 line, STM32H750 Value line	-	X[4]	X	-	4 Kbytes	Yes[5]	Yes

1. *X: supported.*
2. *To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin must be pulled up to a voltage in the 3.0 to 3.6 V range with a 1.5 kΩ resistor.*
3. *STM32F401/411/412/413/423 devices support only FS mode.*
4. *USB 2.0 OTG HS device/host/OTG peripheral, supporting only full-speed operations.*
5. *Available through VDD50USB and VDD33USB pins.*

2.1 USB implementation on STM32 products

Table 4. USB implementation on STM32 mainstream products

Feature[1]	STM32F070x6/B	STM32F072 STM32F078 STM32F04x	STM32F102 STM32F103	STM32F105/107	STM32F302xB/C STM32F303xB/C STM32F373	STM32F302x6/8 STM32F302xD/E STM32F303xD/E
	USB 2.0 FS device interface			USB OTG FS	USB 2.0 FS device interface	
Crystal-less USB	-	X	-	-	-	
Number of endpoints	8			4[2]	8	
Host mode channels	-			8	-	
Size of dedicated packet buffer SRAM	1 Kbyte[3]		512 bytes[4]	1.25 Kbytes[5]	512 bytes[5]	1 Kbytes[3]
Pull-up resistor on USB_DP line	Embedded		1.5 kΩ resistor must be added	Embedded	1.5 kΩ resistor must be added	
LPM	X		-			X
BCD	X		-			
ADP	-					

1. *X: supported.*
2. *Bidirectional, including EP0.*
3. *When the CAN peripheral is used, only the first 768 bytes are available to the USB. The last 256 bytes are used by the CAN.*
4. *The USB and CAN share a dedicated 512 bytes SRAM. They can then be used in the same application but not at the same time.*
5. *The dedicated SRAM is used exclusively by the USB endpoints (not shared with any other peripheral).*

Table 5. USB implementation on STM32 high-performance products

Feature[1]	STM32F401 STM32F411		STM32F2x5/2x7 STM32F405/415 STM32F407/417 STM32F427/437 STM32F429/439		STM32F412 STM32F413/423		STM32F446 STM32F469 STM32F479 STM32F74x STM32F756 STM32F76x STM32F77x STM32F7x2 STM32F730R/V STM32F750		STM32F7x3 STM32F730Z/I		STM32H743/753 STM32H750	
	OTG FS	OTG HS	OTG FS	OTG HS	OTG FS	OTG HS	OTG FS	OTG HS	OTG FS	OTG HS	OTG FS	OTG HS
Crystal-less USB	-	-	-	-	-	-	-	-	-	-	X	X
Bidirectional endpoints (including EP0)	4	-	4	6	6	-	6	9	6	9	9	9
Host mode channels	8	-	8	12	12	-	12	16	12	16	16	16
Size of dedicated packet buffer SRAM (Kbytes)[2]	1.25	-	1.25	4	1.25	-	1.25	4	1.25	4	4	4
ULPI available to primary I/Os via muxing	-	-	-	X	-	-	-	X	-	-	-	X
Integrated PHY	FS[3]	-	FS[3]	FS[3]	FS[3]	-	FS[3]	FS[3]	FS[3]	HS[4]	FS[3]	FS[3]
LPM	-	-	-	-	X	-	X	X	X	X	X	X
BCD	-	-	-	-	X	-	-	-	X	-	X	X
ADP	-	-	-	-	-	-	-	-	-	-	-	-

1. *X: supported.*
2. *The dedicated SRAM is used exclusively by the USB endpoints (not shared with any other peripheral).*
3. *Internal FS OTG PHY support.*
4. *Internal HS OTG PHY support.*

Table 6. USB implementation on STM32 ultra-low-power products

Feature[1]	STM32L0x2 STM32L0x3	STM32L1xx	STM32L4x2 STM32L4x3	STM32L4x5, STM32L4x6 STM32L4Rx, STM32L4Sx
	USB 2.0 FS device interface			USB OTG FS
Crystal-less USB	X	-	X	X[2]
Number of endpoints	8			6 (bidirectional)
Host mode channels	-			12
Size of dedicated packet buffer SRAM[3]	1 Kbyte			1.25 Kbytes (with advanced FIFO control)
pull up resistor on USB_DP line	X			X
LPM	X			X
BCD	X			X
ADP	-			X

1. *X: supported.*
2. *Except for STM32L47x/L48x devices.*
3. *The dedicated SRAM is used exclusively by the USB endpoints (not shared with any other peripheral).*

2.2 Supported USB speeds

In Host mode, the USB OTG_FS supports full- and low-speed transfers, while in device mode it only supports full-speed transfers.

Table 7. Supported OTG_FS speeds

Mode(1)	FS (12 Mbit/s)	LS (1.5 Mbit/s)
Host	X	X
Device	X	-

1. *X: supported.*

In Host mode, the USB OTG_HS supports high-, full-, and low-speed transfers, while in device mode, it only supports high- and full-speed transfers.

Table 8. Supported OTG_FS speeds

Mode(1)	HS (480 Mbit/s)	FS (12 Mbit/s)	LS (1.5 Mbit/s)
Host	X	X	X
Device	X	X	-

1. *X: supported.*

2.3 Protection against ESD and EMI

Protection against ESD and EMI is needed. The system must comply with both the JESD22-A114D (also known as HBM) and the IEC 61000-4-2 standards.

The HBM requires that the USB pins of the component device be tolerant up to 2 kV discharge, this is the case for STM32 MCUs. Refer to the figure and the table below for JESD22-A114D standard test waveform and class levels. For more details, refer to the document *System Level ESD-expanded* available at www.jedec.org.

Figure 1. JESD22-A114D standard test waveform

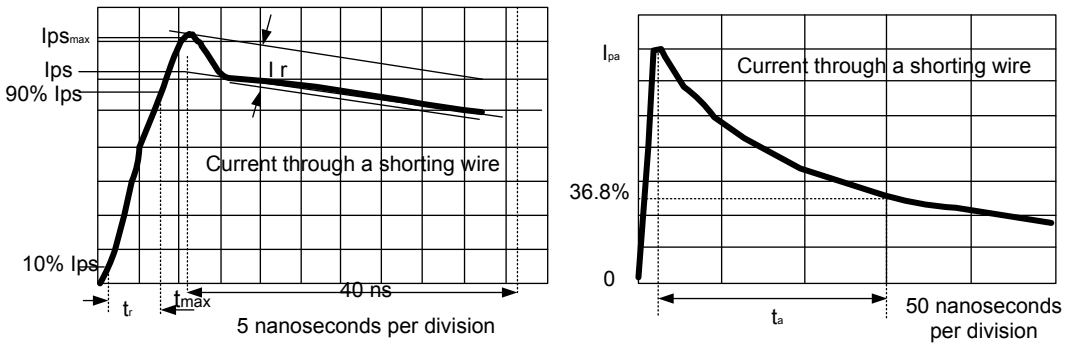


Table 9. JESD22-A114D standard class levels

Class	Voltage range	Current range
Class 0	V < 250 V	I < 0.17 A
Class 1A	250 V < V < 500 V	0.17 A < I < 0.33 A
Class 1B	500 V < V < 1000 V	0.33 A < I < 0.67 A
Class 1C	1 kV < V < 2 kV	0.67 A < I < 1.33 A
Class 2	2 kV < V < 4 kV	1.33 A < I < 2.67 A
Class 3A	1 kV < V < 8 kV	2.67 A < I < 5.33 A
Class 3B	V > 8 kV	I > 5.33 A

The system must also comply with the IEC 61000-4-2 standard on USB lines when they are connected to a receptacle. This standard is fairly different from the HBM standard. Refer to the image and the table below for IEC 61000-4-2 standard test waveform and class levels.

Figure 2. IEC 61000-4-2 standard waveform

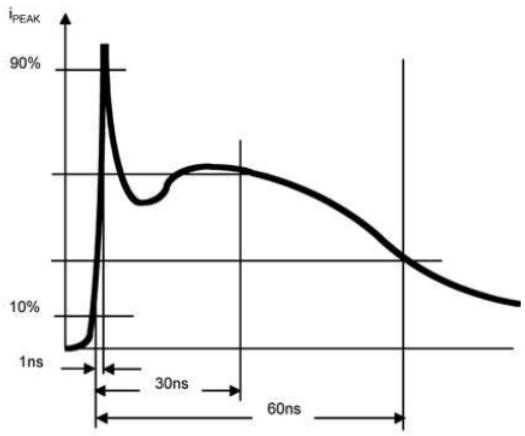


Table 10. IEC 61000-4-2 standard class levels

Level	Contact	Air	Peak current (A)
	Indicated voltage (kV)		
1	2	3	7.5
2	4	4	15
3	6	8	22.5
4	8	15	30

To see the difference between the current pulses applied in the two tests, compare the two figures presented above.

To improve the protection against high ESD surges (and then to meet the conditions requested by the standards), dedicated components have to be placed as close as possible to the receptacle (see the table below).

Table 11. ESD protection

Interface	Protection	
	Low price	Low area on PCB
USB FS	USBLC6-2SC6 (+ ESDA7P60-1U1M for VBUS)	USBLC6-2P6 (+ ESDA7P60-1U1M for VBUS)
USB FS OTG	USBLC6-4SC6	DSILC6-4P6
USB HS	ECMF02-2AMX6 (+ ESDA7P60-1U1M for 5 V VBUS)	
USB HS OTG ECMF02	ECMF02-2AMX6 (+ ESDA7P60-1U1M for 5 V VBUS + ESDALC6V1-1U2 for ID)	

2.4 Clock

The FS USB device/OTG requires a precise 48 MHz clock. This frequency can be generated from the internal main PLL, or by the internal 48 MHz oscillator.

In the first case, the clock source must use an HSE crystal oscillator, in the second case, the synchronization for the oscillator can be taken from:

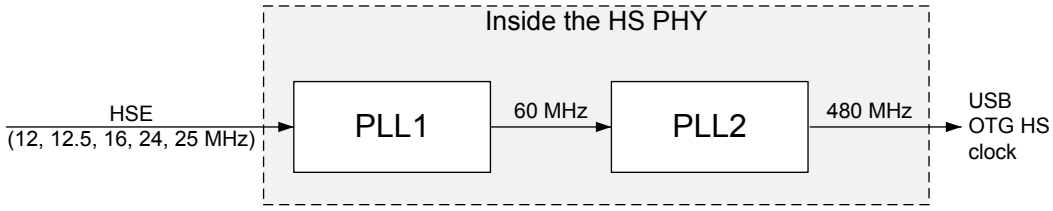
- The USB data stream itself (SOF signalization), no external resonator/ crystal is needed (this feature is only available for devices embedding a crystal-less USB 2.0 FS device interface), or
- The internal 48 MHz oscillator trimmed on LSE (not accurate enough for a USB host).
- MSI and LSE only for STM32L47x/L48x devices.

If HS operation is required, the OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output (provided from the HS PHY: HSE is not mandatory in this case).

As stated on the following figure, for STM32F7x3xx devices the USB HS PHY includes two embedded PLLs:

- PLL1: has as clock source the HSE clock. The supported values are: 12, 12.5, 16, 24 and 25 MHz. The PLL1 outputs the 60 MHz used as input for the PLL2.
- PLL2: outputs the high speed (480 MHz) clock.

Figure 3. HS PHY PLLs on STM32F7x3 devices



Note: The AHB frequency has to be higher than 14.2 MHz to guarantee a correct operation for the USB OTG FS peripheral, and higher than 30 MHz for the USB OTG HS peripheral.

2.5 Power

For USB transceivers, the operating voltage ranges between 3.0 and 3.6 V. This voltage is obtained from one of the following:

- V_{DD}: standard external power supply for the STM32MCU I/Os
- V_{DDUSB}: a dedicated independent power supply for USB. This power supply can be connected either to V_{DD} or to an external independent power supply for USB transceivers.

Consequently, the microcontroller can be powered with the minimum specified supply voltage, while an independent power supply 3.3 V can be connected to V_{DDUSB}.

When the V_{DDUSB} is connected to a separated power supply, it is independent from V_{DD} or V_{DDA}, but it must be the last supply to be provided and the first to be removed.

Some important points to notice are listed below:

- The USB full-speed transceiver functionality is ensured down to 2.7 V. The USB full-speed electrical characteristics are degraded when V_{DD} ranges between 2.7 and 3.0 V
- V_{DDUSB} is not available on all STM32 devices. Refer to the "Dedicated VDDUSB" column in Table 3. USB implementation in STM32 devices to check whether this feature is available on a specific MCU.
- The V_{DDUSB} pin must be connected to two external decoupling capacitors (100 nF ceramic + 1 µF tantalum or ceramic)
- Some devices, when in high-pin-count packages, feature a dedicated VDDUSB pin. When assembled in low-pin-count packages, these devices have only the VDD pin to ensure the USB functionality.
- On STM32F7x3xx devices, the USB HS PHY subsystem uses an additional power supply pin: VDD12OTGHS pin is the output of the HS PHY regulator (1.2 V). An external capacitor (2.2 µF) must be connected to the VDD12OTGHS pin.
- On STM32H7x3 devices, $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via a USB internal regulator. This is used to support a V_{DD} supply different from 3.3 V. The USB regulator can be bypassed to supply $V_{DD33USB}$ directly when V_{DD} = 3.3 V.

2.6 VBUS sensing detection

Based on the USB specification, a USB device must use VBUS sensing detection. When the device detects the host presence, it connects its pull-up resistor to either D+ or D- data signal. This allows the host to detect the device presence on the bus.

There are two cases:

- The USB device is bus-powered. VBUS sensing is not mandatory (USB is always connected when the device is powered)
- The device is self-powered. VBUS sensing is mandatory.

Pin PA9, a five V-tolerant pin, is natively dedicated to VBUS sensing. The absolute maximum ratings table of the datasheet indicates that the five V-tolerant pin voltage cannot exceed VDD + 4 V. The user must avoid the situation when the MCU is not powered, and a 5 V VBUS is connected to PA9: this violates the condition on absolute maximum ratings, and can result in permanent damages to the device.

For this purpose, it is mandatory to reduce the voltage on PA9 below 4 V. Additionally, the internal VBUS detection block within the OTG peripheral has a current consumption, as mentioned in the STM32 datasheets: *“When the VBUS sensing feature is enabled, PA9 must be left at their default state (floating input), not as an alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.”.*

For a reliable and safe VBUS detection, the use of a voltage divider is recommended to guarantee absolute maximum ratings. In this case, the total resistance between VBUS and GND must be high to minimize the DC current. The basic GPIO input levels (VIL, VIH) can now be used with the resistor divider.

Note: For the VIL/VIH calculation, all GPIOs are powered by the main I/O supply V_{DD}. The V_{DDUSB} is dedicated in some MCUs to the USB signals.

The recommended resistor divider values for VBUS detection are the following:

- For V_{DD} in 3.0-3.6 V range: 82 kΩ (to GND), 33 kΩ (to VBUS).
- For V_{DD} in 1.8-2.0 V range: 68 kΩ (to GND), 82 kΩ (to VBUS).

Resistor values have been assessed assuming a ± 0.1 % tolerance. They are checked against VIL/VIH across the different STM32 families, in order to guarantee switching when V_{BUS} is between 0.8 and 3.67 V.

3 Hardware guidelines for USB implementation

This section describes the hardware requirements for correct operation of the USB peripheral.

3.1 USB FS upstream port

In peripheral mode, the V_{BUS} power is always provided through the cable. The USB FS impedance driver is always managed internally to avoid the need to add external serial resistors on the data line path.

According to the USB specification, there are two main use cases:

- Self-powered applications: platforms providing their own power supply and acting as an upstream port on the cable insertion. Not allowed, under any condition, to draw any current from the USB interface.
- Bus-powered applications: a platform supplied only through VBUS and acting as an upstream port.

3.1.1 USB FS upstream port in self-powered applications

To optimize the power consumption on self-powered platforms, only a USB PHY and a controller must be started on the VBUS detection.

It is recommended to implement a resistor bridge (refer to Section 2.6 for more details). It is also recommended to use an ESD protection device and to place it as close as possible to the USB connector.

To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin must be pulled up with a 1.5 kΩ resistor to a voltage in the 3.0 to 3.6 V range.

In several STM32 MCUs, the pull-up resistor is already implemented. The user must add this resistor in other STM32 MCUs (refer to the 'Embedded pull-up resistor on USB_DP line' column in Table 3).

Figure 4. USB FS upstream port with embedded pull-up resistor in self-powered applications

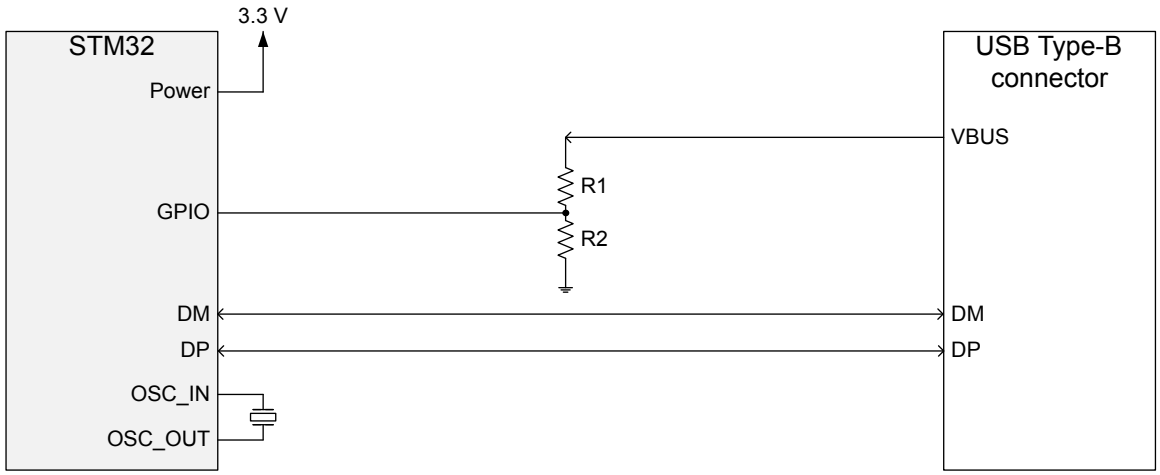
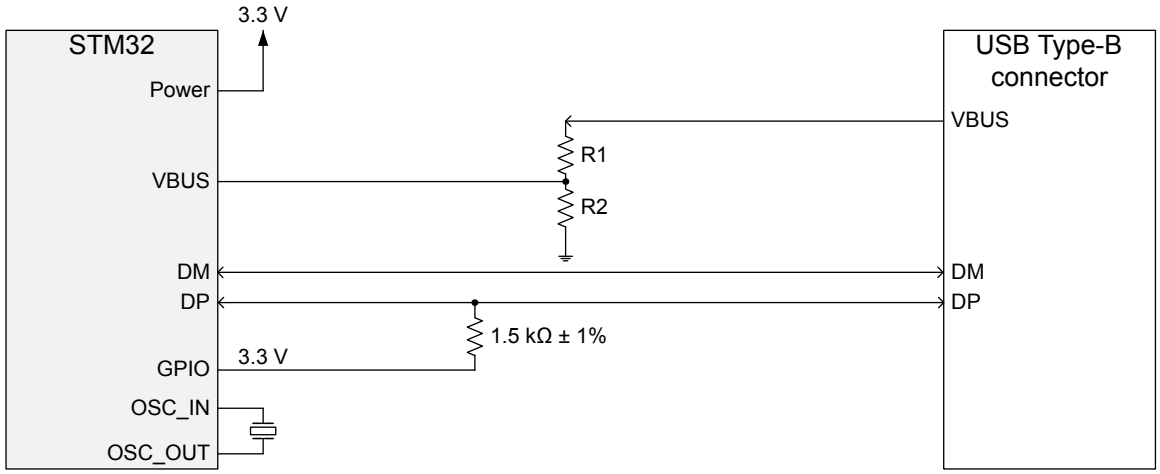


Figure 5. **USB FS upstream port without embedded pull-up resistor in self-powered applications**



A DP pull-up must be connected only when VBUS is plugged. A GPIO from the MCU is used to drive it after the VBUS detection.

3.1.2 USB FS upstream port in bus-powered applications

A bus-powered application is an application where the supply comes exclusively from VBUS. In order to keep the host alive and the VBUS available, both the PHY and the controller must always be active.

It is recommended to use an external low-dropout regulator (LDO) to lower the input supply of the MCU (LDO39050PU33R or an equivalent component can be used), and to place the ESD protection chip (if used) as close as possible to the USB connector.

Figure 6. **USB FS upstream port with embedded pull-up resistor in bus-powered applications**

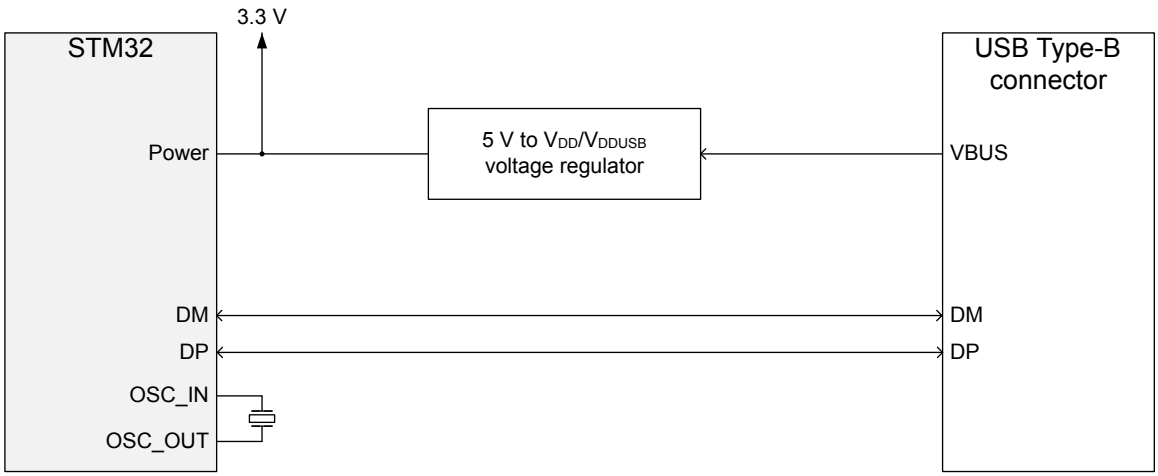
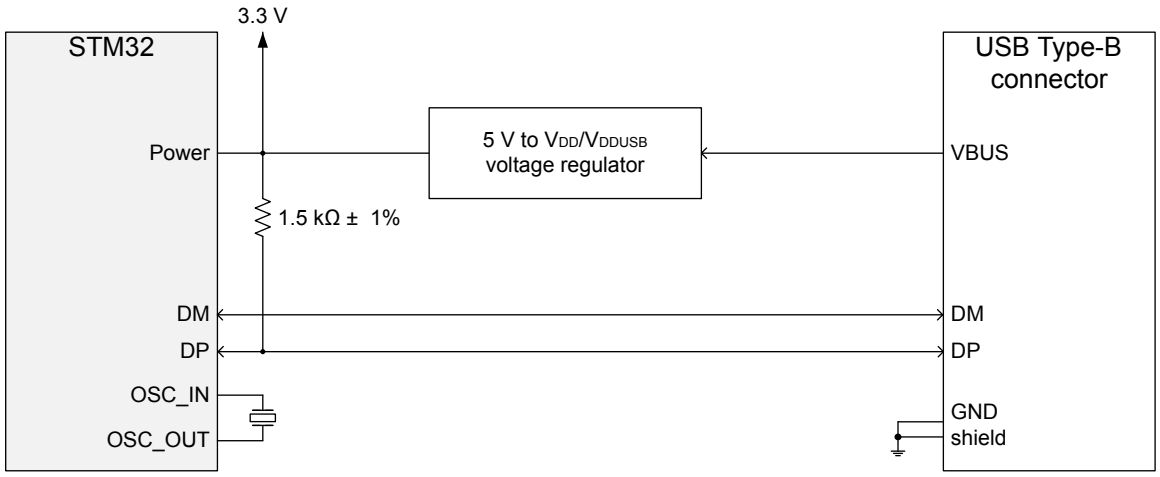


Figure 7. **USB FS upstream port without embedded pull-up resistor in bus-powered applications**



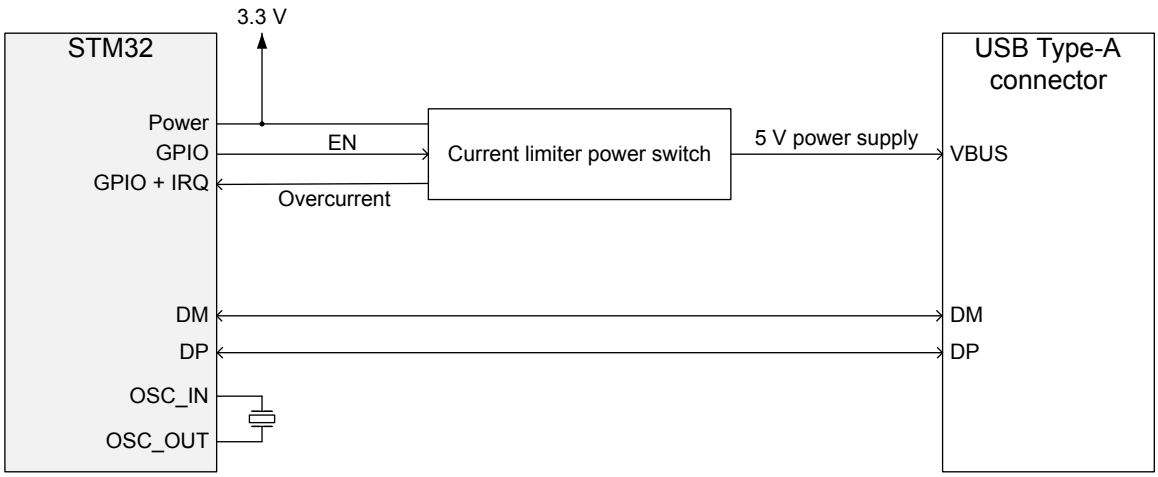
3.2 USB FS downstream port

This section describes the implementation for the USB FS downstream port, available on all the STM32 microcontrollers supporting host connection.

As required by the USB specification, if a VBUS overload occurs, it must be indicated to the user. The information regarding a VBUS overload is provided to the STM32 device via a switch with overcurrent protection (STMPS2151STR or equivalent)., as shown in the figure below.

The ESD protection chip, if used, has to be placed as close as possible to the USB connector.

Figure 8. **USB FS downstream implementation**



3.3 OTG applications through embedded PHY

The USB OTG products address scenarios that allow portable devices and non-PC hosts to have the following enhancements:

- targeted host capability to communicate with a list of selected USB peripherals
- support for direct connections between OTG devices
- power saving features to preserve battery life
- a new pin on connector, named ID, identifies the USB power role

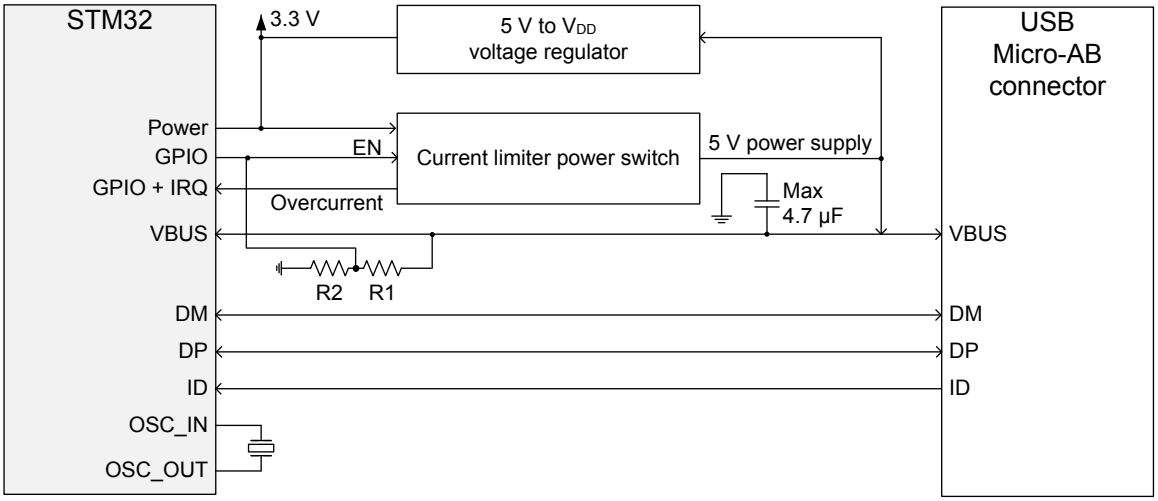
Consequently, the OTG platforms must include:

- an STM32 MCU supporting the OTG feature
- a Micro-AB connector: the USB role is identified through the ID pin
- a VBUS generation when the OTG device acts as a downstream facing port
- a VBUS current overflow, both monitoring and acting as a downstream facing port

Regarding the figure that is presented below:

- The OTG specification requires the use of a capacitor (maximum value 4.7 µF) on VBUS.
- The ESD protection chip, if used, must be placed as close as possible to the USB connector.
- A power switch (such as STMPS2151STR) is required.
- When an over-current is detected, the information is sent to the STM32 software, which alerts the user about the issue (it is recommended to route VBUS far from DP/DM).
- The STM32 must always be supplied when the platform is connected as device to a host (in case of dead battery support, voltage on PA9 must be reduced as explained in Section 2.6).

Figure 9. OTG schematic implementation (dual-mode)



Additional considerations:

- An external voltage regulator is only needed when building a VBUS powered device.
- The current limiter is required only if the application has to support a VBUS powered device. A basic power switch can be used if 5 V supply is available on the application board.
- The ID pin is required in dual role only.
- The same application can be developed using the OTG HS in FS mode to achieve enhanced performance thanks to the large Rx/Tx FIFO and to a dedicated DMA controller.

3.4 OTG_HS PHY connected through ULPI

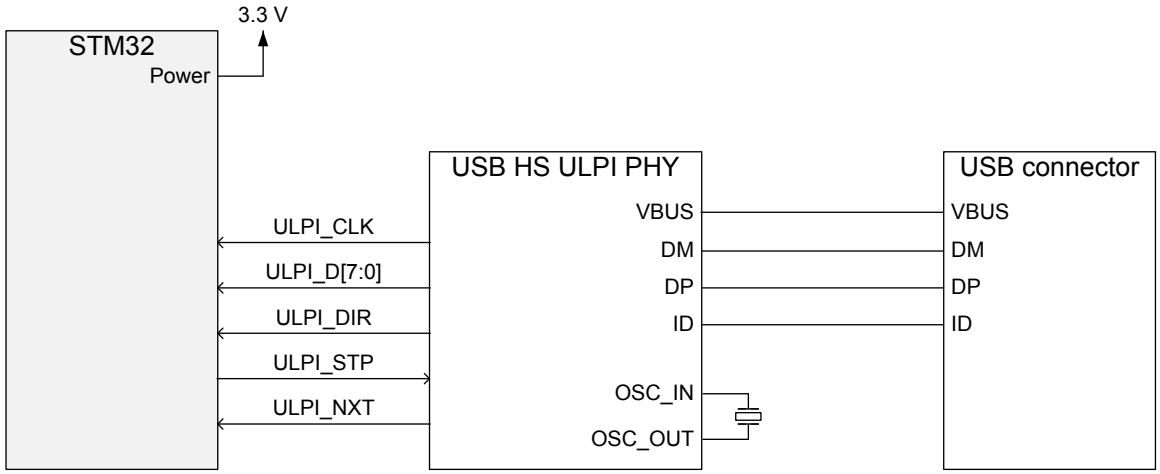
The USB standards propose routing guidelines for high-speed USB platforms in the *High Speed USB Platform Design Guidelines* document available on USB-IF website.

Note: For a full speed driver that is part of an high speed driver, the impedance is 45 Ω ± 10%.

Recommendations:

- Because the ULPI PHY is master of an ULPI CLK, a crystal oscillator is required to guarantee clock precision for the ULPI sampling and for the USB HS data sampling.
- The OTG specification requires a capacitor (maximum value 4.7 µF) on VBUS.
- The ESD protection chip, if used, has to be placed as close as possible to the USB connector.

Figure 10. USB HS via ULPI interface



3.4.1 External USB HS PHYs compatible via ULPI interface

The following table lists some external USB HS PHYs compatible through the ULPI interface.

Table 12. Compatible USB HS PHY

USB HS PHY	Tested on	
	Board	MCU
ISP1705AET	STM3240G-Eval	STM32F407
	STM3241G-Eval	STM32F417
	STM3221G-Eval	STM32F207
	STM3220G-Eval	STM32F217
USB3300-EZK	STM32779I-Eval	STM32F777
	STM32769I-Eval	STM32F769
	STM32756G-Eval	STM32F756
	STM32746G-Eval	STM32F746
	STM32479I-Eval	STM32F479
	STM32F446E-Eval	STM32F446
	STM32F439I-Eval	STM32F439
	STM32F429I-Eval	STM32F429
USB3320C-EZK	STM32H753I-Eval	STM32H753
	STM32H743I-Eval	STM32H743
	STM32F769I-Disco	STM32F769
	STM32F746G-Disco	STM32F746

3.5 USB applications through the embedded OTG HS PHY

To operate USB HS on STM32F7x3 devices there is no need to connect an external HS PHY via ULPI, as they already include an internal HS USB PHY.

There are some other recommendations in addition to those detailed for the embedded USB FS PHY:

- An external capacitor of 2.2 µF must be connected on the VDD12OTGHS pin.
- The HS PHY has an OTG_HS_REXT pin needed for calibration, this pin must be connected to GND via an external precision resistor (3 KΩ ± 1%).

3.6 STM32 on USB-IF integrators list

The list of the STM32 devices with certified USB peripherals is available on www.usb.org. The table below summarizes the certified USB peripherals by STM32 device.

Table 13. Certified USB peripherals

STM32 device	Certified category	Speed(s)	TID
STM32F072	Peripheral	LS/FS	40001561
STM32F103	Peripheral	LS/FS	40000455
STM32F105	Peripheral	LS/FS	40001571
STM32F205/7	Peripheral	LS/FS	40001366
STM32F205/7	Peripheral	HS	40001365
STM32F207	Embedded host	FS	120000252
STM32F207	Embedded host	HS	120000251
STM32F303	Peripheral	LS/FS	40001494
STM32F373	Peripheral	LS/FS	40001496
STM32F405/7	Peripheral	HS	40001393
STM32F405/7	Peripheral	LS/FS	40001394
STM32F407	Embedded host	HS	120000253
STM32F407	Embedded host	FS	120000256
STM32F723	Peripheral	HS	40001777
STM32F723	Embedded host	FS	120000703
STM32F723	Embedded host	HS	120000702
STM32F723	Peripheral	LS/FS	40001776
STM32L053	Peripheral	LS/FS	40001612
STM32L152	Peripheral	LS/FS	10730015
STM32L476, STM32L476ZGT6U	Peripheral	LS/FS	40001658
STM32L476, STM32L476ZGT6U	Embedded host	FS	120000348

4 FAQs (frequently asked questions)

Q: What is the minimum operating voltage for USB?

A: The USB, including its internal transceiver, is functional only for $V_{DD}/V_{DDUSB} \geq 2.7$-V. However, to be compliant with USB specification, a minimum of 3.0 V is needed. Below 2.7-V, the functionality of the internal transceiver is not ensured over the whole temperature range.

Q: The datasheet says that the USB transceiver functionality is ensured down to 2.7 V, but the full-speed electrical characteristics are degraded in 2.7 to 3.0 V voltage range. What is the meaning of this sentence?

A: When the USB operating voltage is below 3.0 V, ST guarantees that the PLL generates correctly the 48 MHz, and that the analog transceivers are functional: the USB is correctly operating.

However, the electrical signals are not compliant with the USB2.0 full-speed specification, and, consequently, some tests needed to get the USB certification (such as the eye diagram test) do not pass. In other words, the USB is operational, but the customer cannot get the USB certification.

Refer to www.usb.org for more details about the electrical requirements needed to be compliant with the USB specification.

Q: The pull up resistor on D+ line must always be added for the STM32 acting as a full speed device?

A: A full-speed device uses a pull-up resistor attached to D+ to specify itself as a full-speed device (and to indicate its speed). The pull-up resistor at the device end is also used by the host or hub to detect the presence of a device connected to its port. Without a pull-up resistor, the USB assumes there is nothing connected to the bus.

On some STM32 microcontrollers the pull-up resistor is already embedded. Otherwise, the customer needs to add it. Refer to *Embedded pull-up resistor on USB_DP* line in Table 3 to know if this resistor is integrated on the used STM32 MCU.

Q: In order to manage the VBUS sensing for USB device, are there any recommendations for the resistor bridge values?

A: Resistor bridge values must be chosen with respect to the following conditions:

- Voltage must be lower than 4 V.
- Voltage must be higher than $0.7 \times V_{DD}$.
- A 200 µA typical current consumption is tolerated.

Refer to "*Management of VBUS sensing for USB device design*" shared on http://community.st.com.

Q: Can the external clock source (HSE bypass mode) be used for the USB clock source?

A: Yes, this is possible. HSE ON with an external crystal or HSE in bypass mode are required, but HSI cannot be used.

Q: Can we use two USB ports simultaneously (when they are available)?

A: Yes, this is feasible.

Q: Is it possible to connect more than one device to the same USB port configured as host?

A: No, hub operation is not supported.

Q: Can the STM32 USB FS peripheral be used to make a USB LS device?

A: No, only full-speed transfers are supported in device mode. Refer to Section 2.2 for more details.

Q: According to the USB specification (FS driver characteristics), when the full-speed driver is/is not part of a high-speed capable transceiver, the impedance of each of the drivers must be in the range 40.5 to 49.5 Ω/28 to 44 Ω, respectively. Are the STM32 devices embedding these matching resistors?

A: Yes. On the internal USB PHYs, the matching output impedance is already embedded in the pad transceiver and is in line with the USB specification. No external resistors are needed.

Q: Is it possible to use the USB peripheral when the operating voltage V_{DD} on the MCU is below 2.7 V?

A: This is possible only if a VDDUSB pin is available to power the USB block. In this case, the microcontroller can be powered with the minimum specified supply voltage, while an independent 3.3 V power supply can be connected to V_{DDUSB}.

5 Conclusion

This application note helps STM32 MCUs users to correctly design their USB applications.

All aspects described inside this document, and specifically requirements described in Section 3 , are mandatory for correct operation of the USB peripheral on STM32 MCUs, and for ensuring its electrical compliance with the USB standard.

Revision history

Table 14. **Document revision history**

Date	Version	Changes
10-Aug-2016	1	Initial release.
24-Nov-2016	2	Document classification updated from public to ST Restricted.
27-Apr-2018	3	• Document classification changed from ST Restricted to Public. • Scope extended to all STM32 microcontrollers. • Updated Introduction and Section 3: Hardware guidelines for USB implementation and its subsections. • Added Section 1: List of abbreviations and acronyms, Section 2: USB on STM32 products and its subsections, Section 4: FAQs and Section 6: Conclusion. • Updated all figures in Section 3: Hardware guidelines for USB implementation. • Removed former Table 1: Applicable products, Section 1: Layout guidelines for USB FS devices, Section 1.1: PCB track impedance and routing on FS data lines, Section 4: Hardware guideline for OTG product implementation and Section 5: OTG USB high speed PHY connected to STM32 through the ULPI link.
18-Dec-2018	4	Added Table 1. Applicable products Updated: • Section 1 General information • Table 3. USB implementation in STM32 devices • Section 2.1 USB implementation on STM32 products and all its tables • Section 2.4 Clock • Section 3.1.1 USB FS upstream port in self-powered applications • Section 3.1.2 USB FS upstream port in bus-powered applications • Section 3.2 USB FS downstream port • Section 4 FAQs (frequently asked questions) • Section 6 Conclusion • All figures in the document
30-May-2022	5	Updated: • Section 2.6 VBUS sensing detection • STM32F105/107 in Table 4. USB implementation on STM32 mainstream products • Figure 4. USB FS upstream port with embedded pull-up resistor in self-powered applications • Figure 9. OTG schematic implementation (dual-mode) • References integrated in Section 1 General information

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