

# SDRAM CONTROLLER

## DESIGN

EE 5313

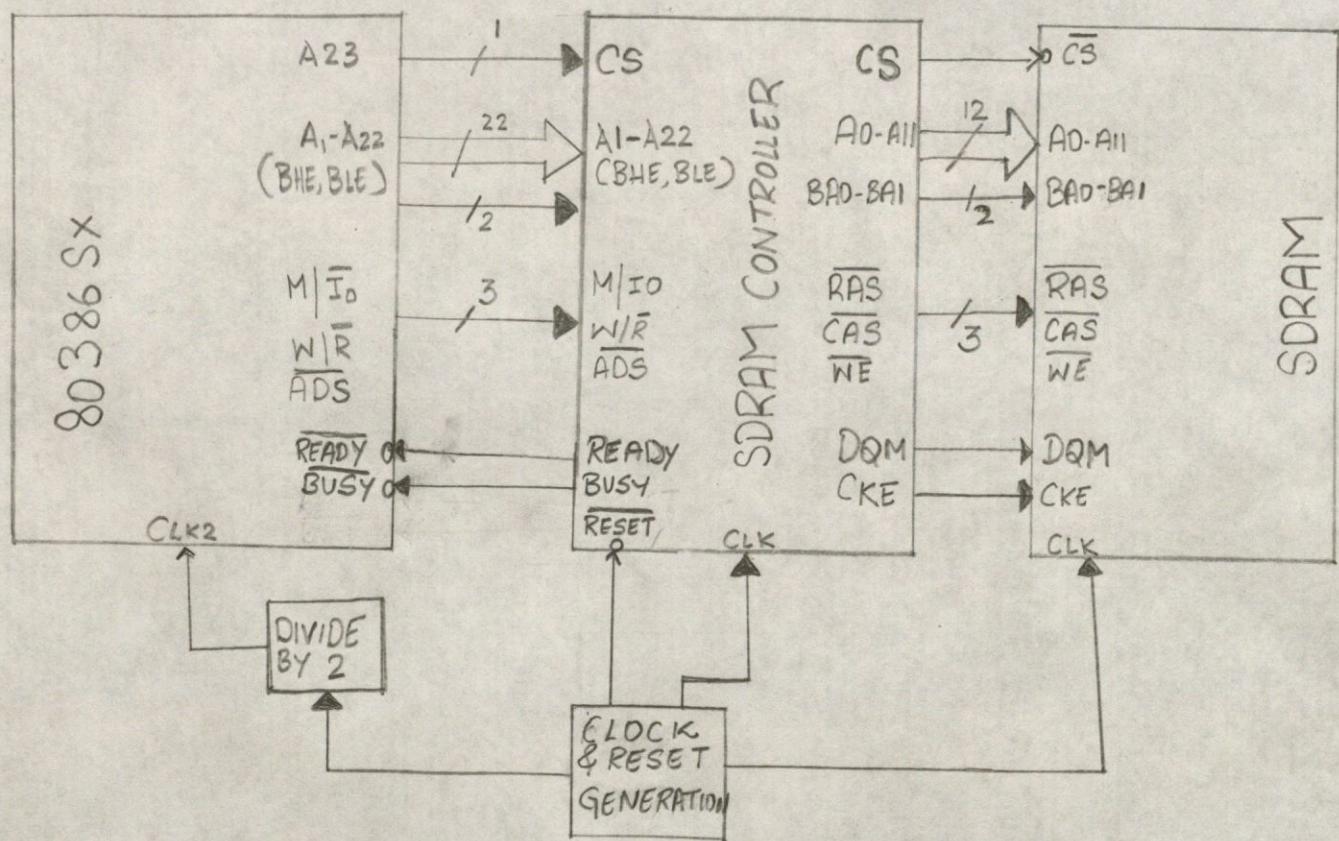
BY :-

(1). HEMANI SHAH  
(1001165860)

(2). RAJATH SHIVANANDA  
(1001096626)

(3). REKHA TATTAMANGALAM RAJAN  
(1001164021)

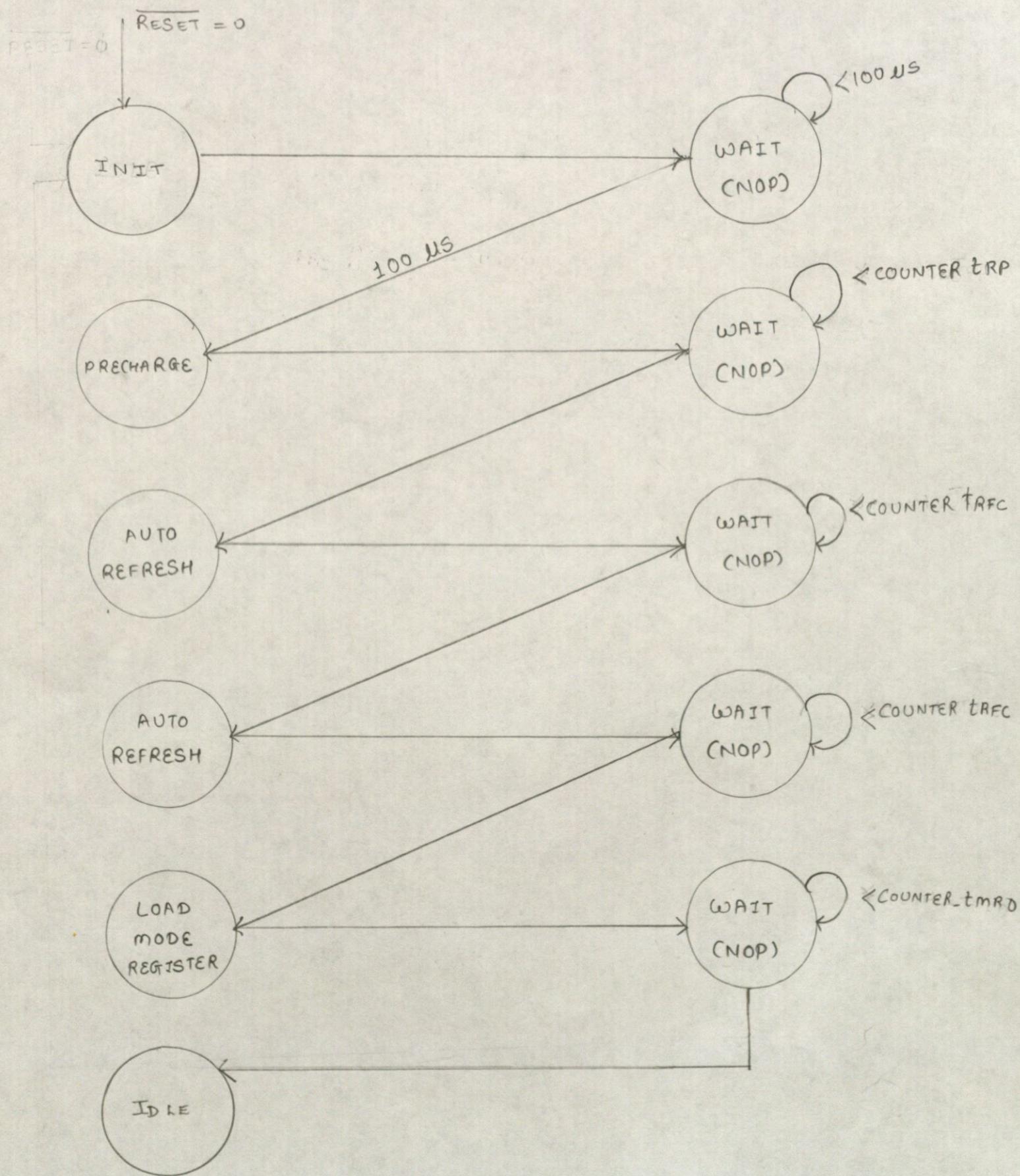
# INTERFACING DIAGRAM



The Figure shows the overall block diagram of the scope of our project where the basic system and interface blocks between the processor, the SDRAM controller, and the SDRAM are shown.

The clock source is a 133 MHz clock which is directly used to clock the SDRAM controller and the SDRAM. The clock source is divided by 2 to clock the processor at 66.5 MHz.

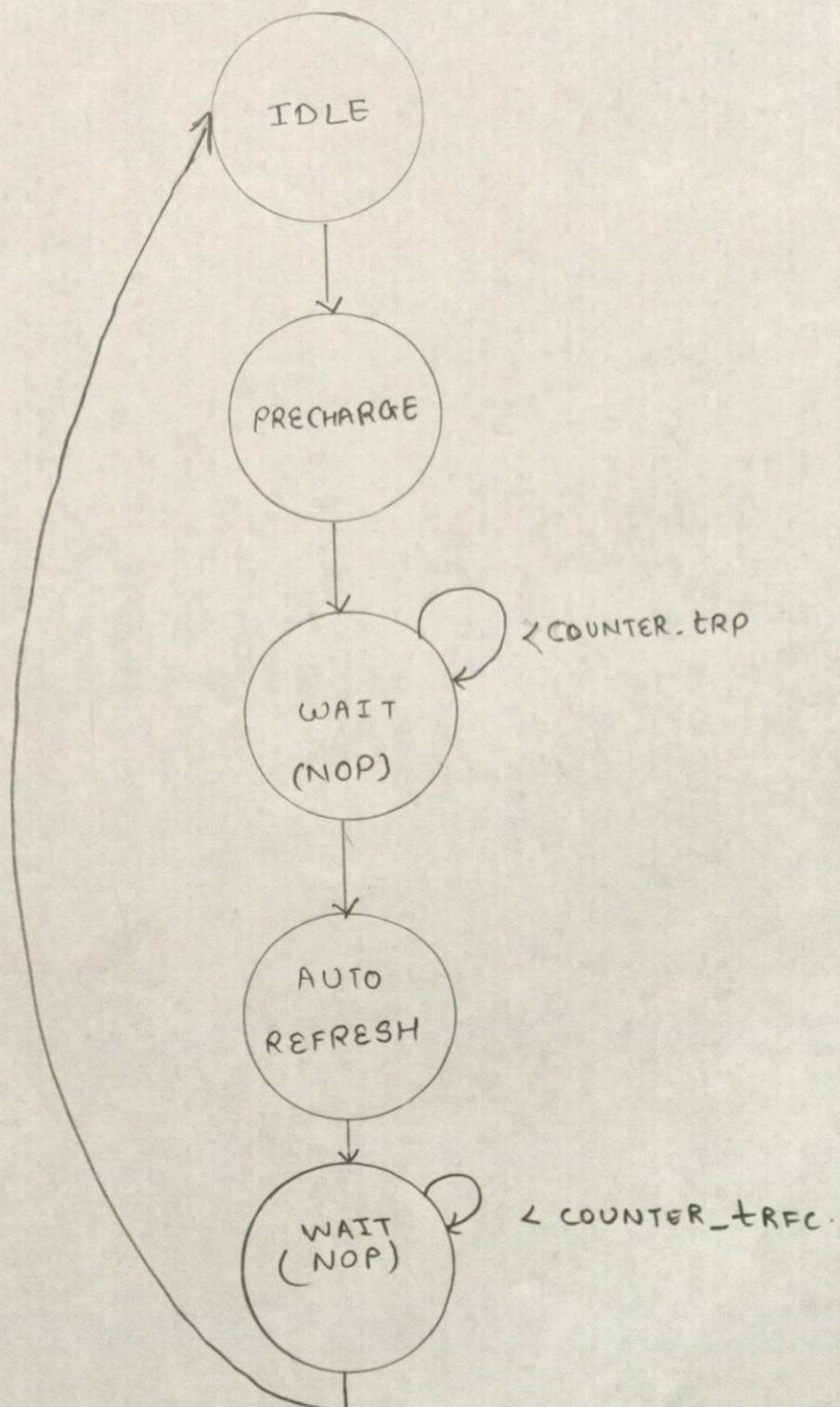
## STATE DIAGRAM FOR INITIALIZATION



## STATE TRANSITION TABLE FOR INITIALIZATION

Current State	Input	Next State
X	RESET = 0	INIT
INIT	CLK Stable	NOP
NOP	counter 100 != 0	NOP
NOP	counter 100 = 0, CS = 1	Precharge
precharge	$\overline{RAS} = 0, \overline{CAS} = 1, \overline{WE} = 0$ $CS = 0$	NOP
NOP	counter - tRP != 0	NOP
NOP	counter - tRP = 0, CS = 1	Auto-Refresh1
Auto-Refresh1	$\overline{RAS} = 0, \overline{CAS} = 0, \overline{WE} = 1$	NOP
NOP	counter - tRFC != 0	NOP
NOP	counter - tRFC = 0	Auto-Refresh2
Auto-Refresh2	$\overline{RAS} = 0, \overline{CAS} = 0, \overline{WE} = 1$	NOP
NOP	counter tRFC != 0	NOP
NOP	counter tRFC = 0	Load mode Register
Load mode Register	Next - clock	NOP
NOP	Counter tmRD != 0	NOP
NOP	Counter tmRD = 0	IDLE

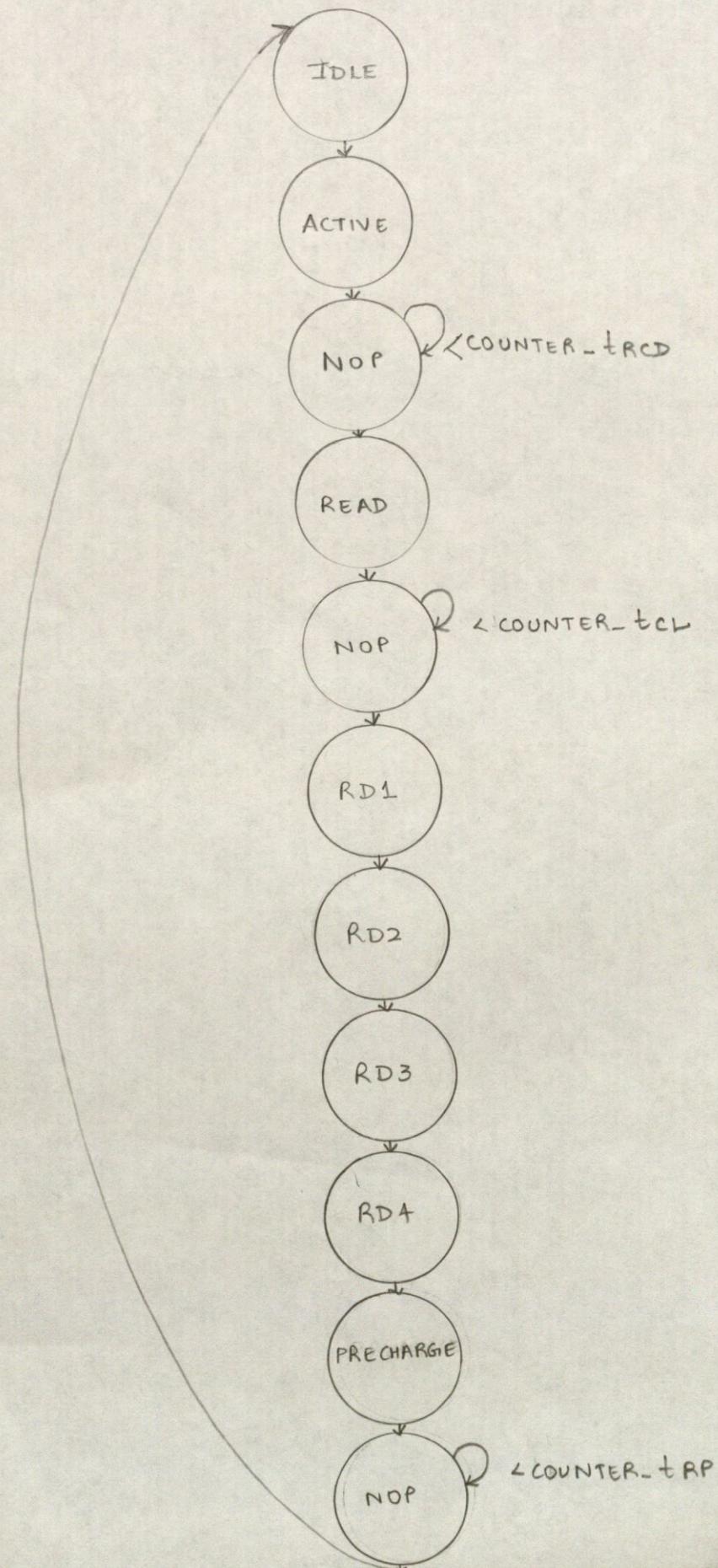
## STATE DIAGRAM FOR AUTO REFRESH



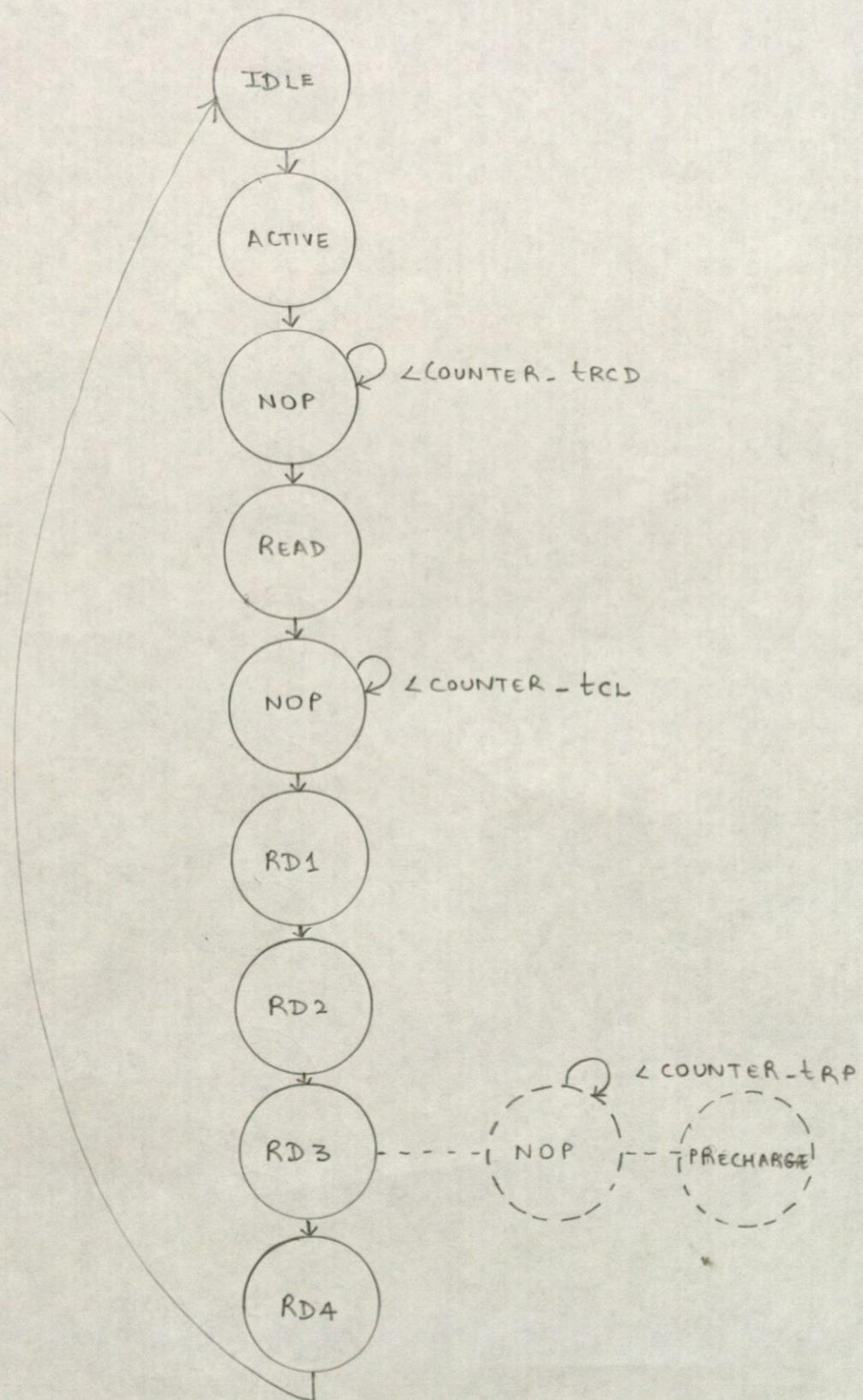
## STATE TRANSITION TABLE FOR AUTO REFRESH

CURRENT STATE	INPUT	NEXT STATE
IDLE	REFRESH REQUEST = 1	precharge
precharge	$\overline{RAS} = 0, \overline{CAS} = 1, \overline{WE} = 0, \overline{CS} = 0$	NOP
NOP	counter - tRP != 0	NOP
NOP	counter - tRP = 0, $\overline{CS} = 1$	Auto Refresh
Auto Refresh	$\overline{RAS} = 0, \overline{CAS} = 0, \overline{WE} = 1, \overline{CS} = 0$	IDLE

STATE DIAGRAM FOR READ CYCLE  
WITH MANUAL PRECHARGE



STATE DIAGRAM FOR READ CYCLE  
WITH AUTO PRECHARGE



STATE TRANSITION TABLE FOR READ CYCLE  
WITH MANUAL RECHARGE

CURRENT STATE	INPUT	NEXT STATE
INIT	$\overline{G} = 0, \overline{RD} = 0, \overline{CD} = 1,$ $\overline{WE} = 1$	ACTIVE
ACTIVE	ACTIVE COMMAND, $\overline{G} = 0,$ $RD = 0, \overline{CD} = 1, \overline{WE} = 0$	READY
READY	COUNTER, $LD = 0$	READY
READY	$\overline{RD} = 0, \text{COMMAND}, RD = 0$ $\overline{G} = 0, \overline{RD} = 1, \overline{CD} = 0,$ $\overline{WE} = 1, RD = 0$	READY
READY	READ COMMAND, $\overline{G} = 0, \overline{RD} = 1, \overline{CD} = 1,$ $\overline{WE} = 1$	READY
READY	COUNTER, $RD = 0$	READY
READY	COUNTER, $RD = 0$	READY
RD1	BURST 1	RD2
RD2	BURST 2	RD3
RD3	BURST 3	RD4
RD4	READY COMMAND, $\overline{G} = 0, \overline{RD} = 0, \overline{CD} = 1,$ $\overline{WE} = 1, \text{BURST } 4$	RECHARGE
RECHARGE	$\overline{G} = 1, \overline{RD} = 1, \overline{CD} = 1,$ $\overline{WE} = 1$	READY
READY	COUNTER, $RD = 0$	READY
READY	COUNTER, $RD = 0$	READY

STATE TRANSITION TABLE FOR READ CYCLE  
WITH AUTO PRECHARGE

CURRENT STATE	INPUT	NEXT STATE
IDLE	$\overline{CS} = 0, \overline{RAS} = 0, \overline{CAS} = 1,$ $\overline{WE} = 1$	ACTIVE
ACTIVE	ACTIVE COMMAND, $\overline{CS} = 0,$ $\overline{RAS} = 1, \overline{CAS} = 1, \overline{WE} = 1$	NOP
NOP	COUNTER_TRC = 0	NOP
NOP	$\overline{MRDC} = 0, \text{COUNTER\_TRCD}=0$ $\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 0,$ $\overline{WE} = 1, A10 = 1$	READ
READ	READ COMMAND, $\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 1,$ $\overline{WE} = 1$	NOP
NOP	COUNTER_TCL = 0	NOP
NOP	COUNTER_TCL = 0	RD1
RD1	BURST 1	RD2
RD2	BURST 2	RD3
RD3	BURST 3	RD4
RD4	BURST 4	IDLE

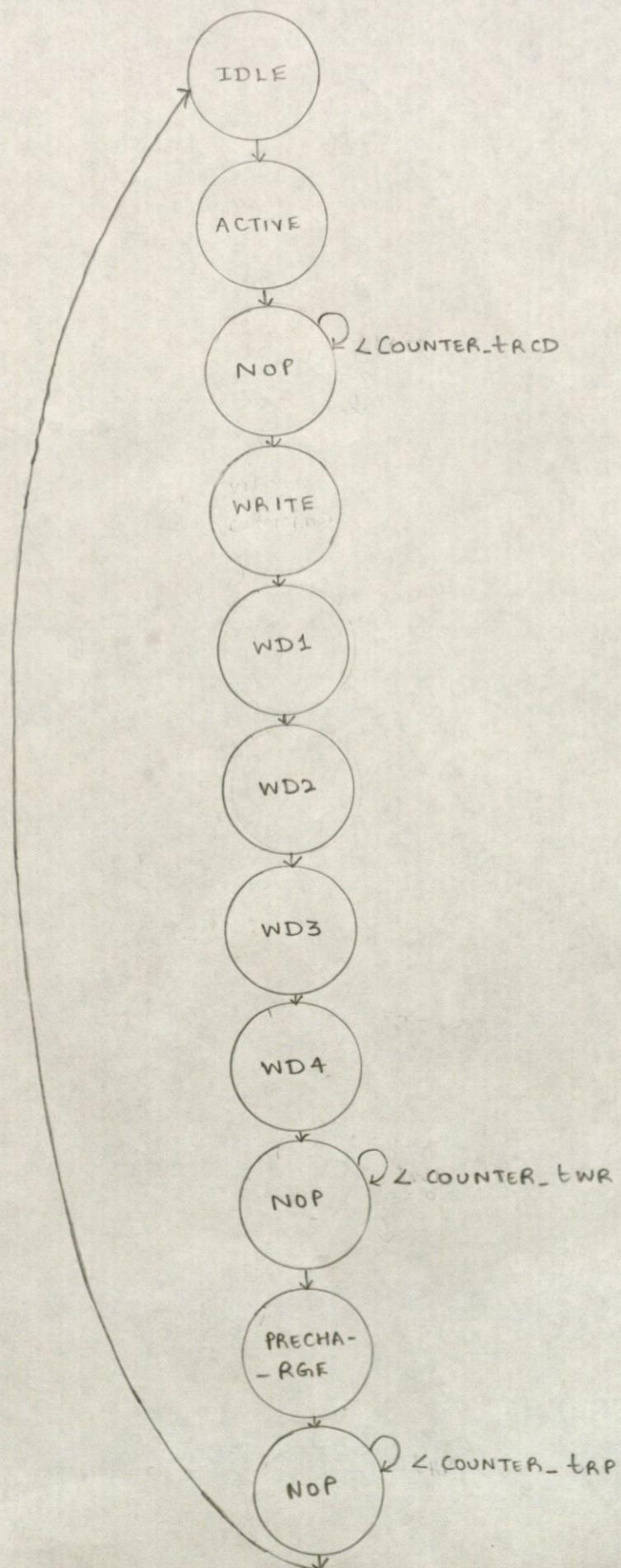
STATE TRANSITION TABLE FOR READ CYCLE  
WITH MANUAL PRECHARGE

CURRENT STATE	INPUT	NEXT STATE
IDLE	$\overline{CS} = 0, \overline{RAS} = 0, \overline{CAS} = 1,$ $\overline{WE} = 1$	ACTIVE
ACTIVE	ACTIVE COMMAND, $\overline{CS} = 0,$ $\overline{RAS} = 1, \overline{CAS} = 1, \overline{WE} = 1$	NOP
NOP	COUNTER-T <sub>RCD</sub> ≠ 0	NOP
NOP	$\overline{MRDC} = 0, \text{COUNTER\_tRCD} = 0$ $\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 0,$ $\overline{WE} = 1, A10 = 0$	READ
READ	READ COMMAND, $\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 1,$ $\overline{WE} = 1$	NOP
NOP	COUNTER-t <sub>CL</sub> ≠ 0	NOP
NOP	COUNTER-t <sub>CL</sub> = 0	RD1
RD1	BURST 1	RD2
RD2	BURST 2	RD3
RD3	BURST 3	RD4
RD4	PRECHARGE COMMAND, $\overline{CS} = 0, \overline{RAS} = 0, \overline{CAS} = 1,$ $\overline{WE} = 1, \text{BURST 4}$	PRECHARGE
PRECHARGE	$\overline{CS} = 1, \overline{RAS} = 1, \overline{CAS} = 1,$ $\overline{WE} = 1$	NOP
NOP	COUNTER-t <sub>RP</sub> ≠ 0	NOP
NOP	COUNTER-t <sub>RP</sub> = 0	IDLE

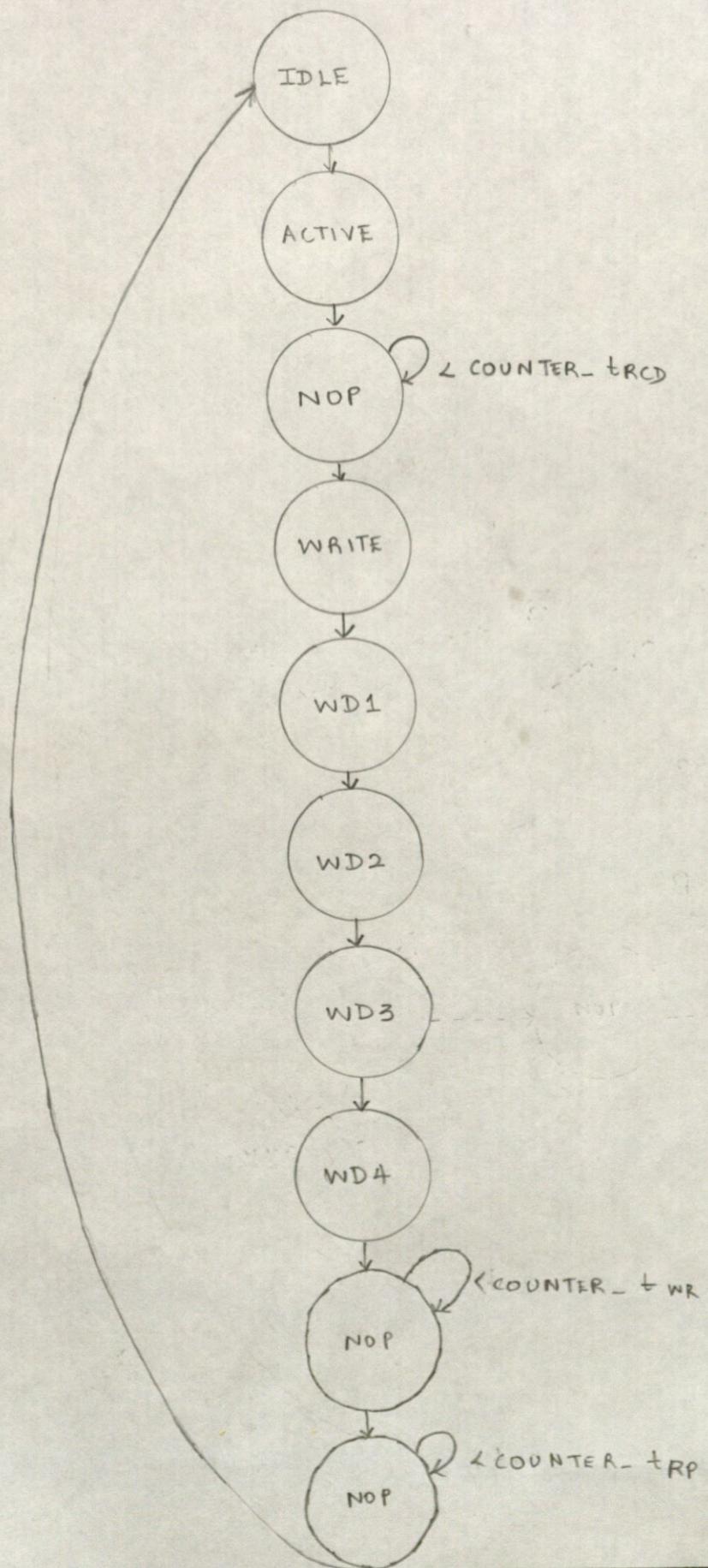
(3)

# STATE DIAGRAM FOR WRITE CYCLE

WITH MANUAL PRECHARGE



STATE DIAGRAM FOR WRITE CYCLE  
WITH AUTO PRECHARGE



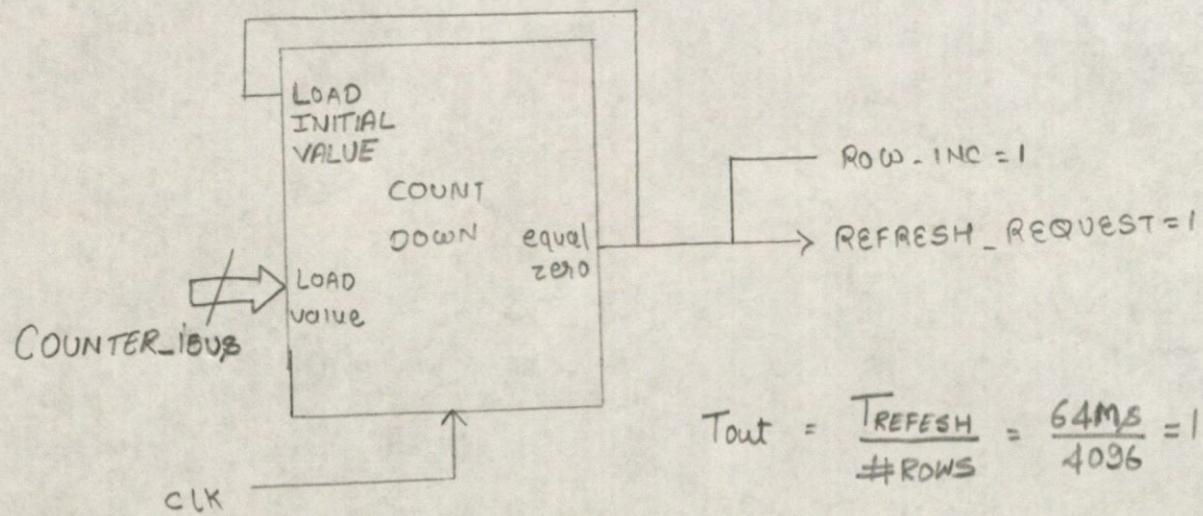
STATE TRANSITION TABLE FOR WRITE CYCLE  
WITH MANUAL PRECHARGE

CURRENT STATE	INPUT	NEXT STATE
IDLE	$\overline{CS} = 0, \overline{RAS} = 0, \overline{CAS} = 1,$ $\overline{WE} = 1$	ACTIVE
ACTIVE	$\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 1,$ $\overline{WE} = 1$ , ACTIVE COMMAND	NOP
NOP	COUNTER\_tRCD ≠ 0	NOP
NOP	$\overline{MWTC} = 0, \text{COUNTER\_tRCD} = 0$ $\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 0,$ $\overline{WE} = 0, A10 = 0$	WRITE
WRITE	WRITE COMMAND	WD1
WD1	BURST 1	WD2
WD2	BURST 2	WD3
WD3	BURST 3	WD4
WD4	$\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 1,$ $\overline{WE} = 1$ , BURST4.	NOP
NOP	COUNTER\_tWR ≠ 0	NOP
NOP	COUNTER\_tWR = 0, PRECHARGE COMMAND, $\overline{CS} = 0, \overline{RAS} = 0, \overline{CAS} = 1,$ $\overline{WE} = 0$	PRECHARGE
PRECHARGE	$\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 1,$ $\overline{WE} = 1$	NOP
NOP	COUNTER\_tRP ≠ 0	NOP
NOP	COUNTER\_tRP = 0	IDLE

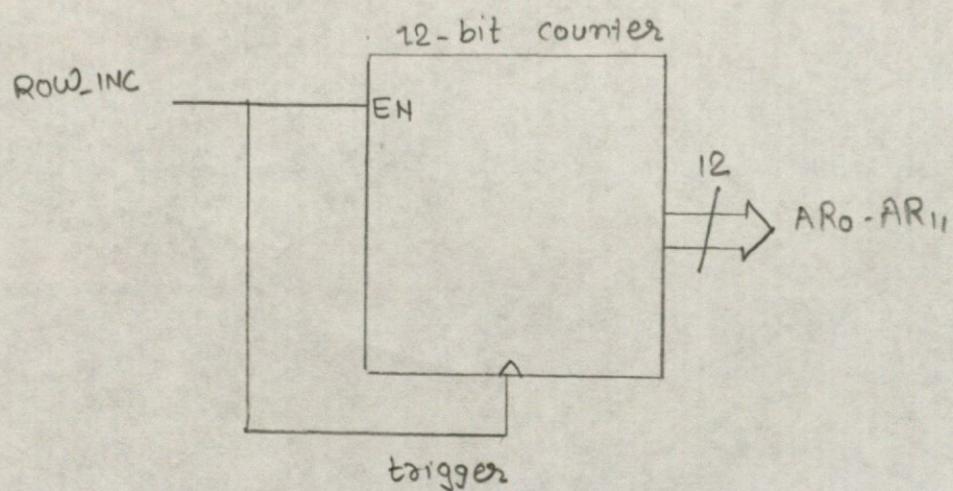
STATE TRANSITION TABLE FOR WRITE CYCLE  
WITH AUTO PRECHARGE

CURRENT STATE	INPUT	NEXT STATE
IDLE	$\overline{CS} = 0, \overline{RAS} = 0, \overline{CAS} = 1$ $\overline{WE} = 1$	ACTIVE
ACTIVE	$\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 1,$ $\overline{WE} = 1$ , ACTIVE COMMAND	NOP
NOP	COUNTER_TRCQ ≠ 0	NOP
NOP	$\overline{MWTC} = 0, \text{COUNTER\_TRCD} = 0,$ $A10 = 1, \overline{CS} = 0, \overline{RAS} = 1,$ $\overline{CAS} = 0, \overline{WE} = 0$	WRITE
WRITE	WRITE COMMAND	WD1
WD1	BURST 1	WD2
WD2	BURST 2	WD3
WD3	BURST 3	WD4
WD4	$\overline{CS} = 0, \overline{RAS} = 1, \overline{CAS} = 1$ $\overline{WE} = 1$ , BURST 4	NOP
NOP	COUNTER_TWQ ≠ 0	NOP
NOP	COUNTER_TWR = 0	NOP
NOP	COUNTER_TRP ≠ 0	NOP
NOP	COUNTER_TRP = 0	IDLE

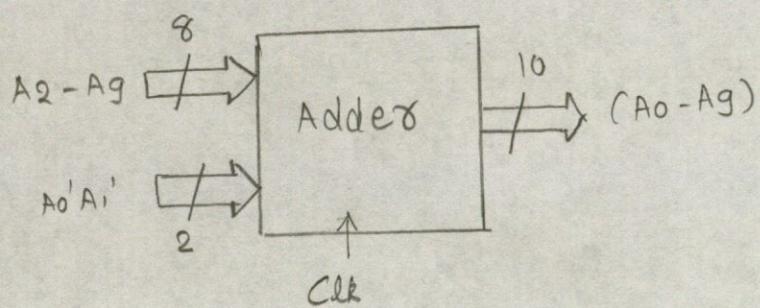
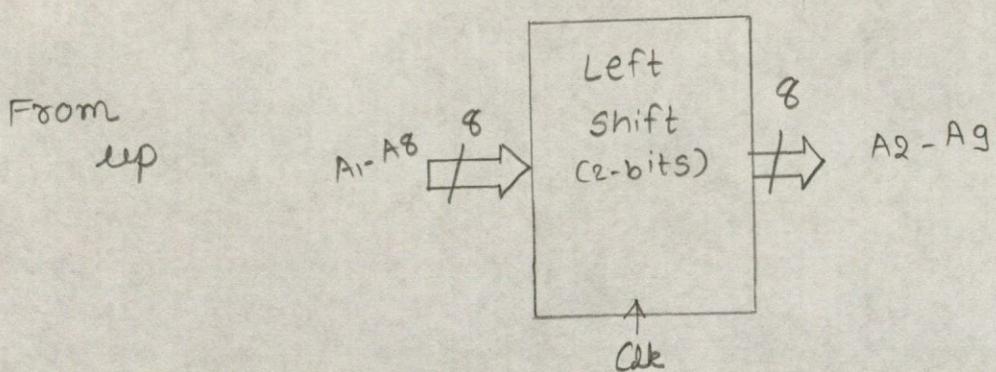
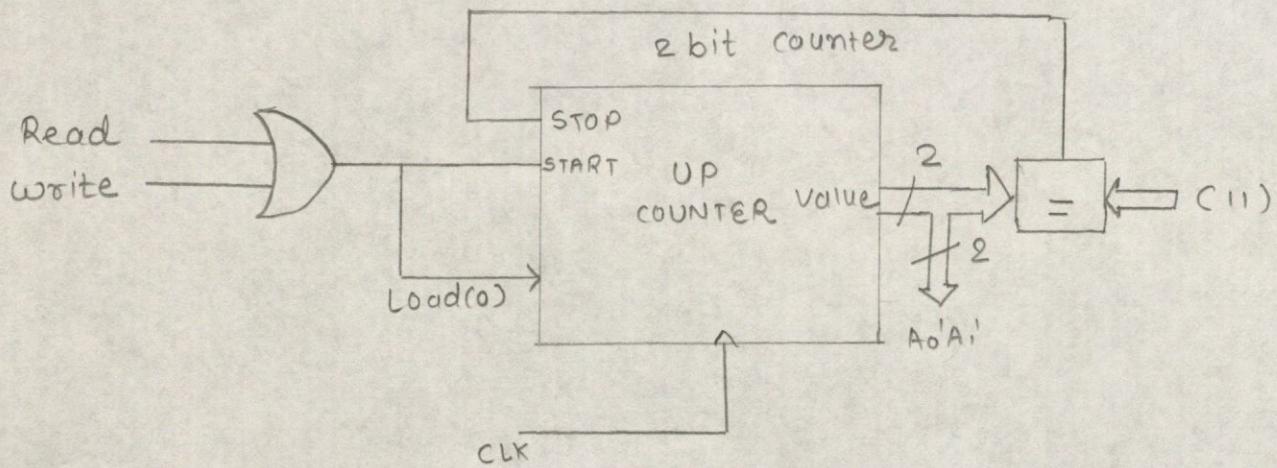
## REFRESH LOGIC



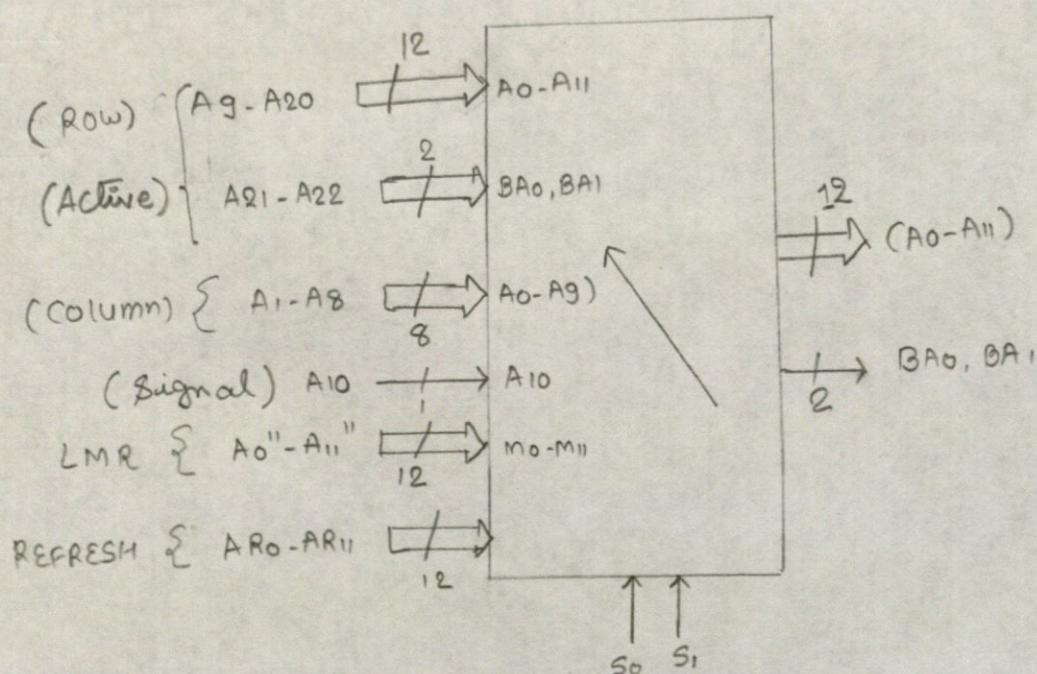
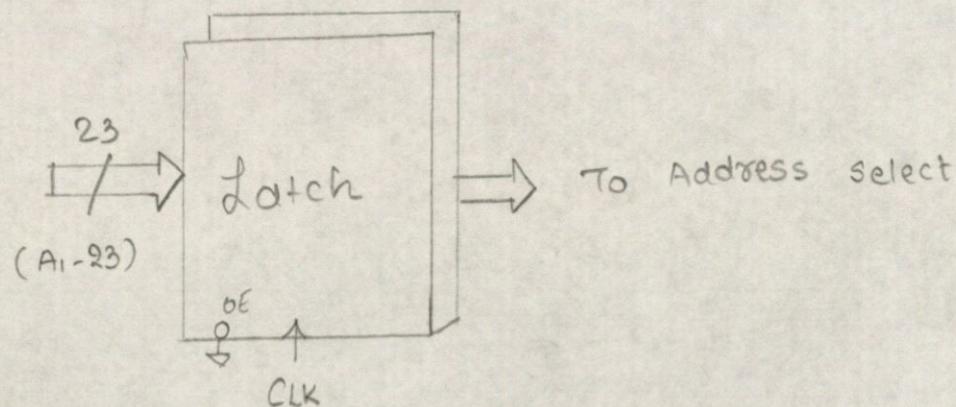
$$T_{out} = \frac{T_{REFRESH}}{\#ROWS} = \frac{64\text{MS}}{4096} = 15.625\text{MS}$$



## COLUMN ADDRESS GENERATION

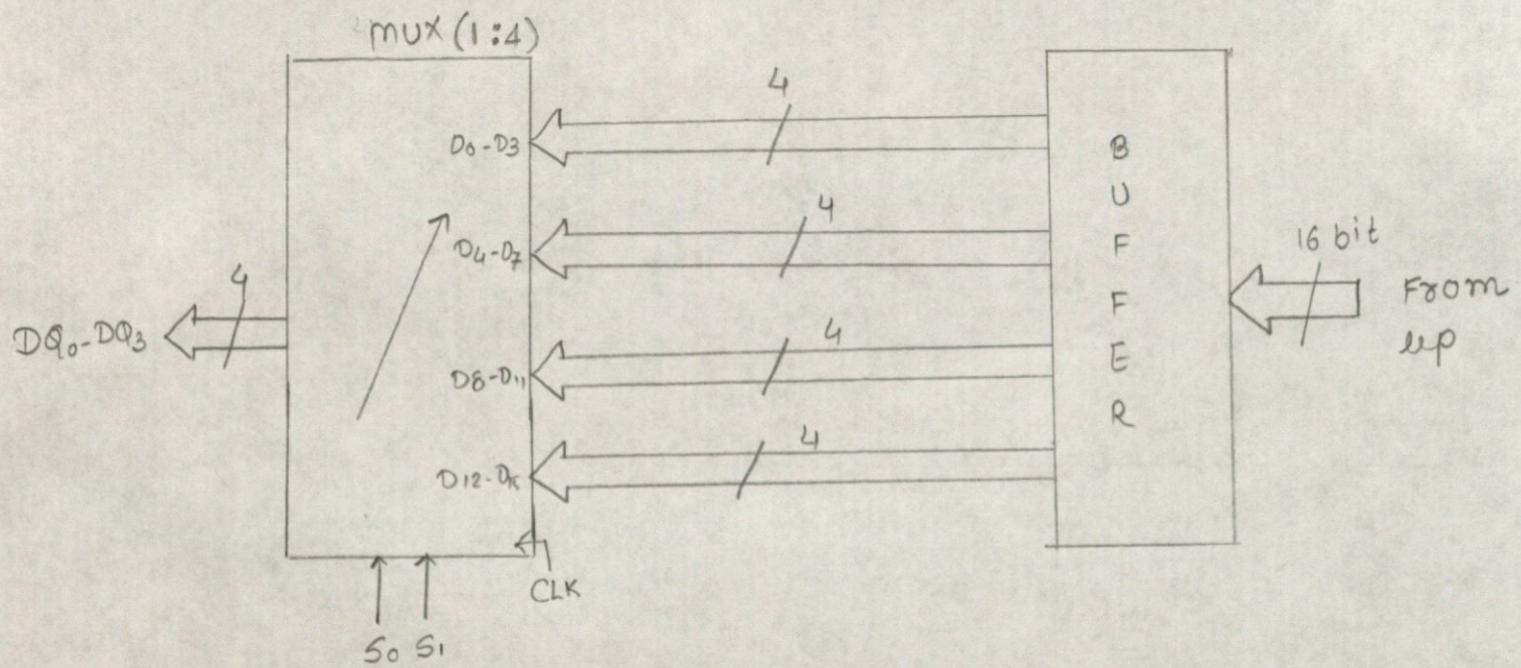


## ADDRESS SELECTION



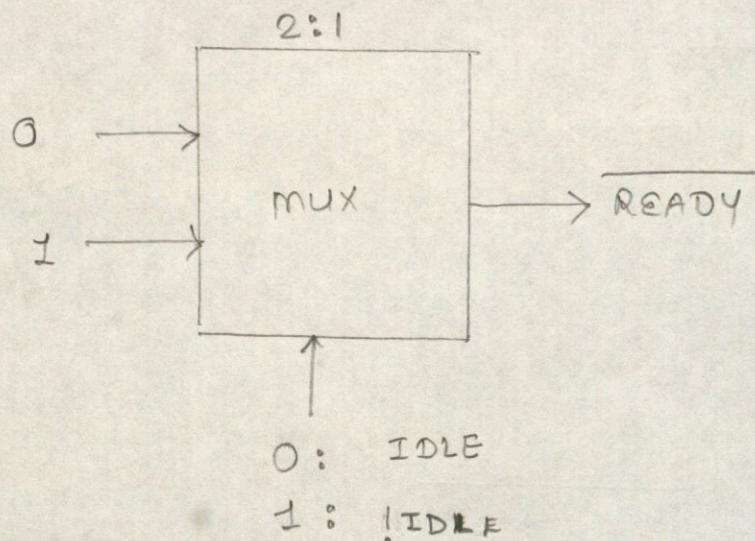
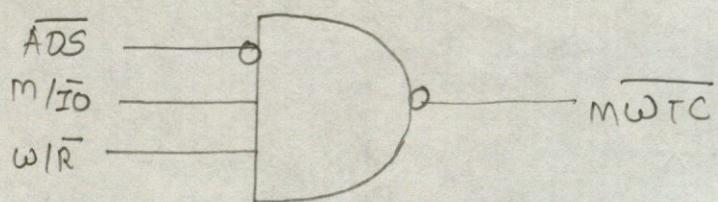
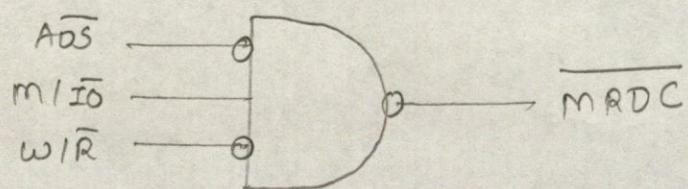
S <sub>0</sub>	S <sub>1</sub>	STATE
0	0	ACTIVE
0	1	READ / WRITE
1	0	LOAD MODE REGISTER
1	1	REFRESH

## WRITE TO MEMORY

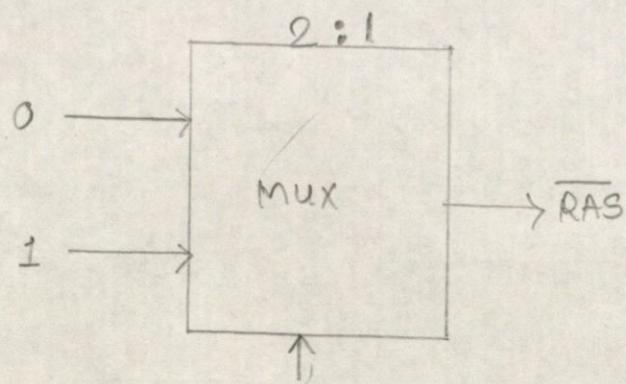


$S_0$	$S_1$	Data
0	0	$D_0 - D_3$
0	1	$D_4 - D_7$
1	0	$D_8 - D_{11}$
1	1	$D_{12} - D_{15}$

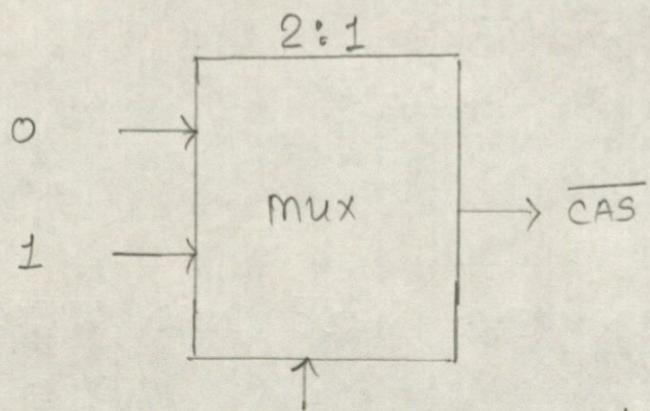
## READY STATE GENERATION

SIGNAL GENERATION FOR  $\overline{\text{MRDC}}$  AND  $\overline{\text{MWTC}}$ 

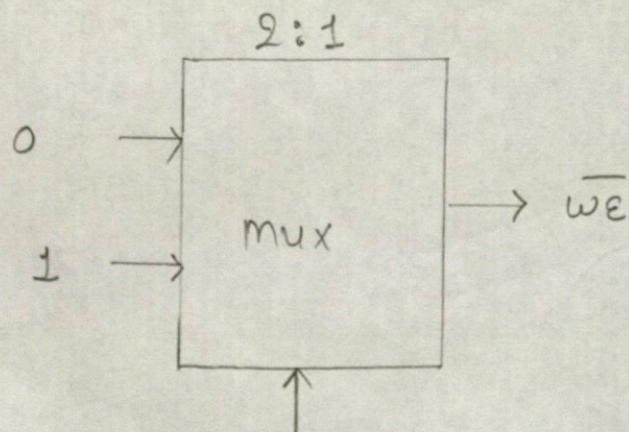
## RAS , CAS AND WE GENERATION



0 : STATE (ACTIVE / PRECHARGE / AUTOREFRESH / LMR)  
1 : STATE (NOP / READ / WRITE)

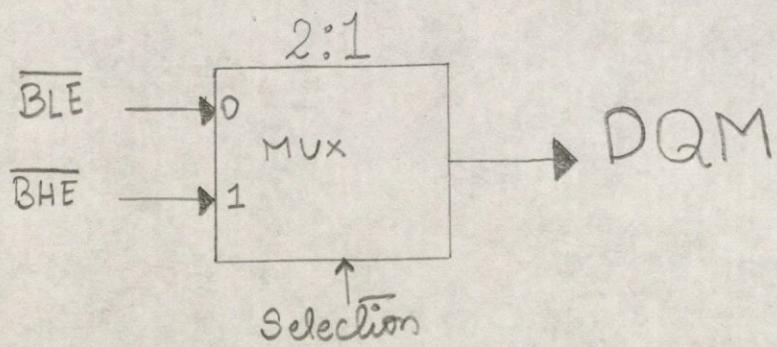


0 : STATE (READ / WRITE / AUTOREFRESH / LMR)  
1 : STATE (NOP / ACTIVE / PRECHARGE)



0 : STATE (WRITE / PRECHARGE / LMR)  
1 : STATE (NOP / ACTIVE / READ / AUTOREFRESH)

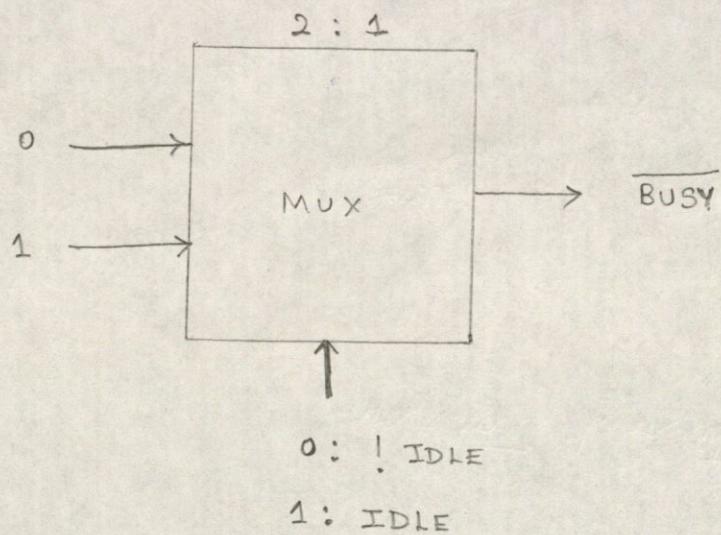
## DQM LOGIC



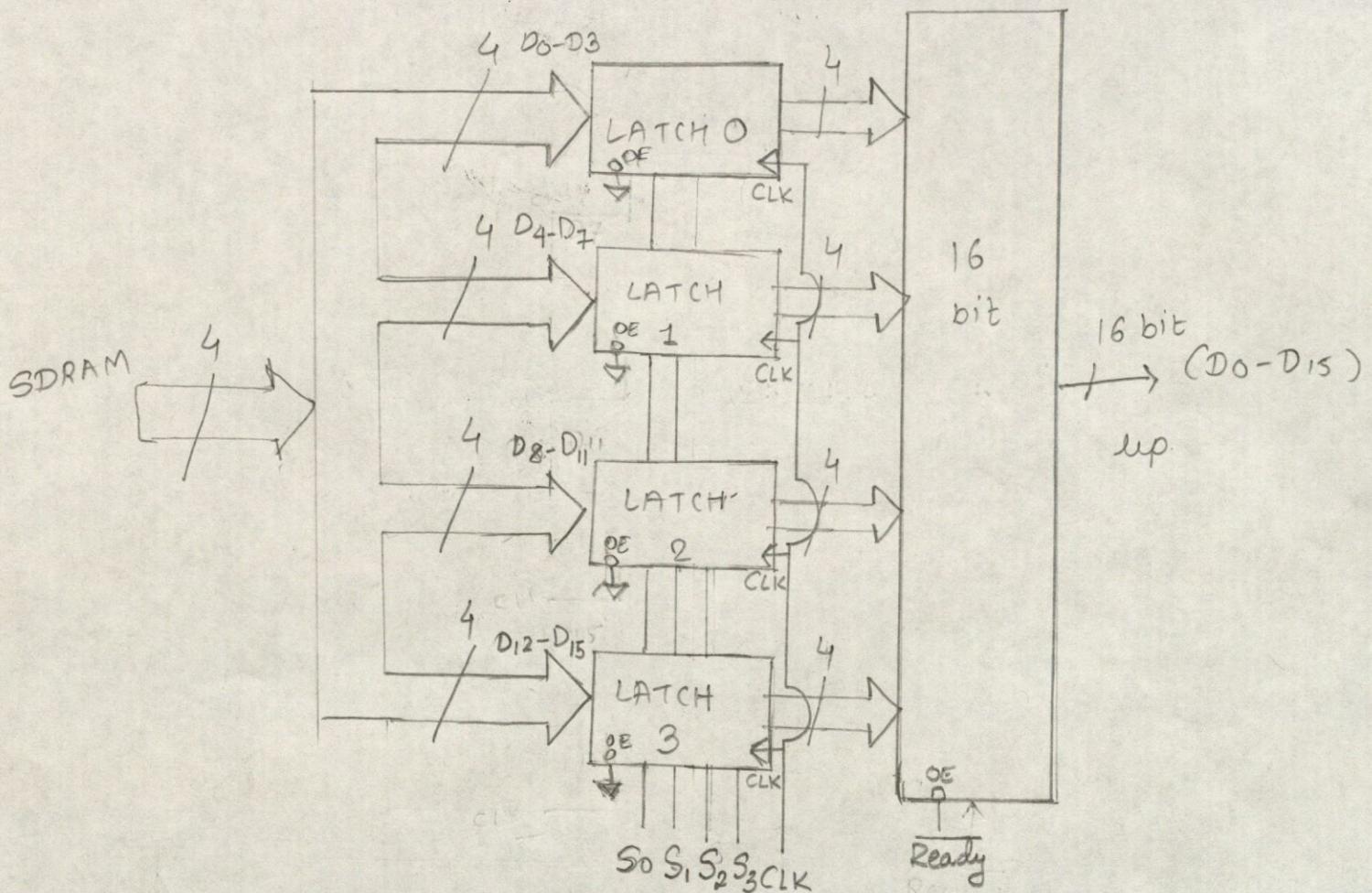
0	State = RDO RDI WD0 WD1
1	State = RD2 RD3 WD2 WD3

(16)

## BUSY LOGIC

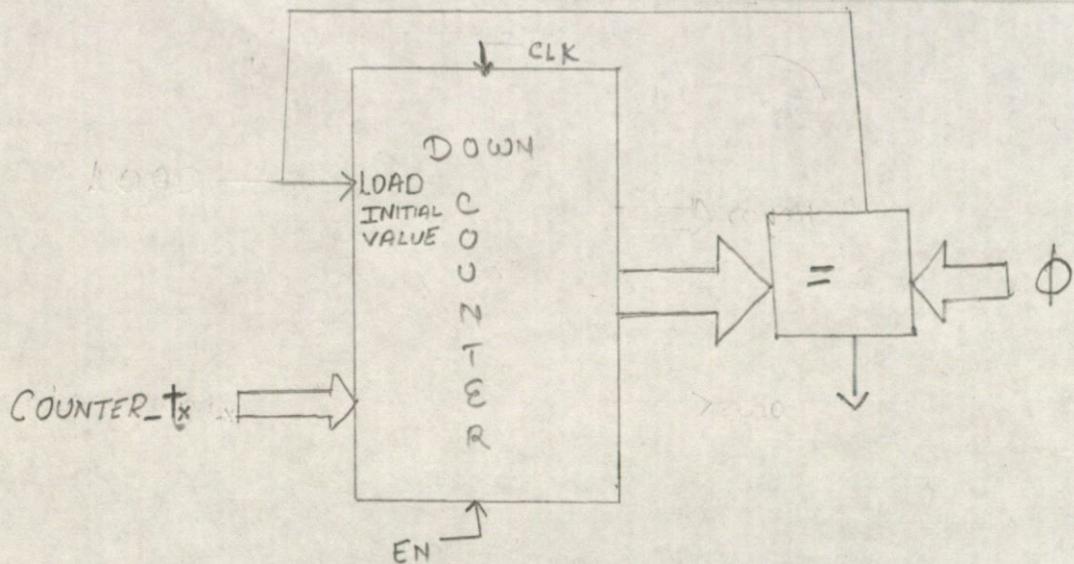


## READ FROM MEMORY



SL No	Selection	State
1.	$S_0$	RD1
2.	$S_1$	RD2
3.	$S_2$	RD3
4.	$S_3$	RD4

## COUNTER DESIGN



Taking  $f = 183 \text{ MHz}$

$$T = \frac{1}{f} = 7.5 \text{ ns}$$

(1). Initialization count =  $\frac{100 \times 10^{-6}}{7.5 \times 10^{-9}} = (13333)_{10} = (3415)_{16}$   
(COUNTER-INIT) for 100 ns

(2). Auto Refresh =  $\frac{64 \times 10^{-3}}{4096} = 15.625 \text{ ns/row}$   
for each row

Auto Refresh count =  $\frac{15.625 \times 10^{-6}}{7.5 \times 10^{-9}} = (2083)_{10} = (0823)_{16}$   
(COUNTER-ISUS)

(3). Precharge time = 15 ns  
(COUNTER-tRP)  
 Precharge count =  $\frac{15 \times 10^{-9}}{7.5 \times 10^{-9}} = (2)_{10} = (02)_{16}$

(4). Auto Refresh time tRFC = 66 ns  
(COUNTER-tRFC)  
 Auto Refresh count =  $\frac{66 \times 10^{-9}}{7.5 \times 10^{-9}} = 8.8 \approx 9 = (09)_{16}$

(5). Active to Read or write Delay tRCD = 15 ns  
(COUNTER-tRCD)  
 tRCD count =  $\frac{15 \times 10^{-9}}{7.5 \times 10^{-9}} = (2)_{10} = (02)_{16}$

(6). Load mode Register command Activate

(COUNTER-tLMRD)

$$t_{MRD} = 2 \times \text{CLK}$$

$$= 2 \times 7.5 \times 10^{-9} = 15 \text{ ns}$$

$$\text{Count} = \frac{15 \times 10^{-9}}{7.5 \times 10^{-9}} = (02)_{10} = (02)_H$$

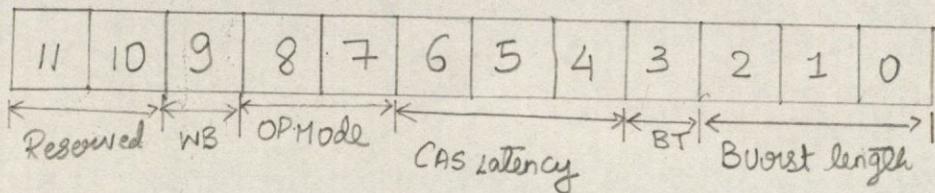
(7). CL=2 (2x7.5)

(COUNTER-tCL)

$$CL \text{ count} = \frac{15 \text{ ms}}{7.5 \times 10^{-9}} = (02)_{10} = (02)_H$$

SL NO	NAME OF THE COUNTER	COUNTER VALUE
1.	COUNTER_INIT	(3415) <sub>H</sub>
2.	COUNTER_trp	(02) <sub>H</sub>
3.	COUNTER_trfc	(09) <sub>H</sub>
4.	COUNTER_trcd	(02) <sub>H</sub>
5.	COUNTER_tLMRD	(02) <sub>H</sub>
6.	COUNTER_tcr	(02) <sub>H</sub>
7.	COUNTER-15us	(0823) <sub>H</sub>

# LOAD MODE REGISTER



Burst Length - 010 (4-burst length)

Burst Type - 0 (sequential)

CAS latency - 010 (2-CAS latency)

OP Mode - 00 (Standard operation)

WB - 0 (Programmed Burst Length)

Reserved - 00

Load\_Mode\_Register = 0x022 (0000 0010 0010)<sub>2</sub>