To be able to synthesize and implement the project the following settings should be checked:

Synthesis:

- Strategy: Flow_AlternativeRoutability

Implementation:

- Strategy: Performance_ExtraTimingOpt
- Opt Design More Options: -muxf_remap -carry_remap -dsp_register_opt -aggressive_remap -resynth_remap -resynth_seq_area

Note: Only the Integration Projekt can be synthesized and implemented. If you try to synthesize or implement the other projects, it will fail or be incorrect.

To synthesize and implement the Integration Project the following steps must be followed:

- Reset the output Products of the Block Design
- Generate the output Products of the Block Design
- Check if some IP`s still need to be upgraded. If so, do that
- Synthesize
- Implement
- If the WNS (Worst Negative Slack-Time) is below 0.5ns then something went wrong with your Setup. Check your Settings and try again.
- If WNS is greater than 0.5ns you can generate a .bit and .bin file

To upload the project to the FPGA, a bin file must be created (bin file check box in the settings).

The CPU must be uploaded to the spi-flash memory on the board to work.

Not every testbench is inside the main project (Integration). Specialized testbenches are inside the specific projects that are also included in the .zip file.

To use the debugger, simply start it with the correct "COM" port selected in the debugger program code. Also make sure that the CPU is connected to the PC. Also, the debugger will not work if the CPU is not booted from spi-flash memory.