IEEE RTCSA 2022 Technical Program

Time	Aug. 23 (Tue)	Time	Aug. 24 (Wed)	Time	Aug. 25 (Thur)
08:45 09:00	Opening				
09:00 10:00	Live Keynote 1:	09:00 10:00		09:00 10:00	
10:00 10:30	Break	10:00 10:40	Keynote 2	10:00 10:30	
10:30 12:00	Session 1: Best Paper Candidates	10:40 10:50	Break	10:30 12:00	Sessions 6a, 6b: Purely Online Presentations
		10:50 11:30	Keynote 3		
12:00 13:30	Lunch	11:30 13:45	Banquet		
13:30 15:30	Session 2a: Real-time Systems (I) Session 2b: IoT, CPS, and Emerging Applications Track (I)	13:45 15:15	Session 4: Invited Papers		
15:00 15:30	Break	15:15 15:30	Break		
15:30 17:30	Session 3a: Real-time Systems (II) Session 3b: Embedded Systems Track (I)	15:30 17:00	Session 5a: Embedded Systems Track (II) Session 5b: IoT, CPS, and Emerging Applications Track (II)		
17:30 ~	Welcome Reception				

Keynote Speeches

Live Keynote 1 (Aug. 23, 09:00–10:00)

Title: Rethinking of Computing - Memory-Centric or In-Memory Computing
Speaker: Tei-Wei Kuo, National Taiwan University

Abstract

Flash memory opens a window of opportunities to a new world of computing over 20 years ago. Since then, storage devices gain their momentum in performance, energy, and even access behaviors. With over 1000 times in performance improvement over storage in recent years, there is another wave of adventure in removing traditional I/O bottlenecks in computer designs. In this talk, I shall first address the opportunities of new system architectures in computing. In particular, hybrid modules of DRAM and non-volatile memory (NVM) and all NVM-based main memory will be considered. I would also comment on a joint management framework of host/CPU and a hybrid memory module to break down the great memory wall by bridging the process information gap between host/CPU and a hybrid memory module. I will then present some solutions in neuromorphic computing which empower memory chips to own new capabilities in computing. In particular, I shall address challenges in in-memory computing in application co-designs and show how to utilize special characteristics of non-volatile memory in deep learning.

Biography

Prof. Kuo received his B.S.E. and Ph.D. degrees in Computer Science from National Taiwan University and University of Texas at Austin in 1986 and 1994, respectively. He is now Distinguished Professor of Department of Computer Science and Information Engineering of National Taiwan University, where he was an Interim President (2017.10–2019.01) and an Executive Vice President for Academics and Research (2016.08–2019.01). Between August 2019 and July 2022, Prof. Kuo took a leave to join City University of Hong Kong as Lee Shau Kee Chair Professor of Information Engineering, Advisor to President (Information Technology), and Founding Dean of College of Engineering. His research interest includes embedded systems, non-volatile-memory software designs, neuromorphic computing, and real-time systems.

Dr. Kuo is Fellow of ACM, IEEE, and US National Academy of Inventors. He is also a Member of European Academy of Sciences and Arts. He is Vice Chair of ACM SIGAPP and Chair of ACM SIGBED Award Committee. Prof. Kuo received numerous awards and recognition, including Humboldt Research Award (2021) from Alexander von Humboldt Foundation (Germany), Outstanding Technical Achievement and Leadership Award (2017) from IEEE Technical Committee on Real-Time Systems, and Distinguished Leadership Award (2017) from IEEE Technical Committee on Cyber-Physical Systems. Prof. Kuo is the founding Editor-in-Chief of ACM Transactions on Cyber-Physical Systems (2015–2021) and a program committee member of many top conferences. He has over 300 technical papers published in international journals and conferences and received many best paper awards, including the Best Paper Award from ACM/IEEE CODES+ISSS 2019 and ACM HotStorage 2021.

Live Keynote 2 (Aug. 24, 10:00–10:40)

Title: Challenges and Opportunities of Next-Generation Enterprise SSD Storage
Speaker: K.S. Pua, Phison Electronics Corp.

Abstract

Data is driving the transformation of the world, including the Internet of Everything, AI, and high-speed computing technologies. All of which are driving the digital transformation of all industries, and assisting humans and enterprises to make faster and more accurate decisions through data analysis and artificial intelligence. In such a transformation process, data storage and reading and writing behaviors play a very important role; for example, the computing results of artificial intelligence come from the collection of big data, the foundation of cloud services comes from the construction of data centers, and the server environment for high-speed computing comes from the matching stable and high-speed enterprise-level storage architecture. What kind of challenges and opportunities will enterprise SSDs face due to the transformation of these digital technologies? Welcome to join the keynote speech of K.S. Pua, CEO of Phison, to explore the latest enterprise SSD technologies and development trends.

Biography

KS Pua is the Founder, Chairman and CEO of Phison Electronics. He was born in a farming community Sekinchan in Selangor, Malaysia in 1974. At the age of 19, went to Taiwan with just US$4,000 in his pocket. With no relatives to help him, his only dream was to study hard, graduated from National Chiao Tung University (NCTU) in Hsinchu, Taiwan in 1997 and earned Master's from NCTU in 1999. Mr. Pua and his four friends founded Phison Electronics Corp. in Taiwan. He designed and produced the world's first single chip USB flash controller with other founders. Under his lead, the company has become a global leader in NAND Flash controller IC and storage solutions.

As an entrepreneur, Mr. Pua is a successful high-teck entrepreneur and the recipient of the Ten Outstanding Young Malaysian Awards , and received Outstanding Young Entrepreneur Award, Outstanding Young Manager Award and The President Award of National Management Excellence Award from the Government. He was elected as Fellow of Chinese Society for Management Of Technology in 2009. In 2010, Phison enjoyed turnover of US$1.06 billion, and had become the largest market of flash-memory related products in Asia-Pacific area and was named 65th in U.S. magazine Bloomberg Businessweek's Tech 100. From 2015 to present, production value of Phison were ranked 3rd of IC Design Houses in Taiwan IC design industry.

Phison Electronics Corporation

Established in 2000 and headquartered in Hsinchu, Taiwan, Phison Electronics Corp. is a global leader in NAND Flash controller IC and storage solutions. The name Phi-son comes from "Five-Persons" since there were five founders who started the company as fresh graduates. In 2000, Phison developed world's first single-chip USB flash drive controller, and successfully launched the USB-based product called Pen Drive. The term Pen Drive had since become symbolic in the realms of flash memory. For 20 years, Phison created of a wide range of innovative solutions over SSD, eMMC, UFS, SD and USB interfaces. Moreover, Phison provides system integration and total solution services across consumer, industrial and enterprise markets. As an active member in industry standards, Phison is on the Board of Directors for SDA, ONFI, UFSA and a contributor for JEDEC, PCI-SIG, MIPI, NVMe and IEEE-SA.

Live Keynote 3 (Aug. 24, 10:40–11:30)

Title: Overview of Arm Confidential Compute Architecture
Speaker: David Hsu, ARM Inc.

Abstract

Confidential Computing is the protection of data in use, by performing computation within a trustworthy hardware-backed secure environment. This protection shields code and data from observation or modification by privileged software and hardware agents. In this talk, we will describe how the Arm Confidential Compute Architecture (Arm CCA) enables confidential computing in an Arm compute platform.

Biography

David Hsu is FAE Director of Arm, leading FAE team of Taiwan for closer collaboration and communications internally and externally to accomplish partners and customers solutions. He has over 20 years of professional experience in the semiconductor industry. David Hsu joined Arm in 2011 as a CPU FAE as well as responsible for product marketing and sales project management and then left in 2017. After then, he joined Intelligo, a start-up invested by MediaTek, leading the business development team to explore opportunities in Japan, Korea, and US. In 2019 David was recruited by Arm again as FAE director to drive Arm's IP solutions adoption. In addition to Arm, David worked at Faraday, Alpha Imaging Technology (MediaTek subsidiary) and BenQ, focusing on IC design work ranging from architecture definition, RTL coding, front-end/back-end implementation to IC verification and testing. He has rich experience in pre-sales strategy set-up and sales enablement. David received a master's degree in Computer Science and Engineering at National Chiao Tung University.

Arm Inc.

Arm is the leading technology provider of processor IP, offering the widest range of processors to address the performance, power, and cost requirements of every device. Arm CPUs and NPUs include Cortex-A, Cortex-M, Cortex-R, Neoverse, Ethos and SecurCore.

Detailed Technical Program

DAY 1

Session 1: Best Paper Candidates

Session: Chair: Chao Wang (National Taiwan Normal University)

1. (Real-time Systems Track)
   A Concurrency Framework for Priority-Aware Intercomponent Requests in CAmkES on seL4
   Marion Sudvarg (Washington University in St. Louis) and Chris Gill (Washington University in St. Louis)
2. (Embedded Systems Track)
   Statistical Hypothesis Testing of Controller Implementations Under Timing Uncertainties
   Bineet Ghosh (The University of North Carolina at Chapel Hill), Clara Hobbs (The University of North Carolina at Chapel Hill), Shengjie Xu (The University of North Carolina at Chapel Hill), Parasara Sridhar Duggirala (The University of North Carolina at Chapel Hill), Jim Anderson (The University of North Carolina at Chapel Hill), P. S. Thiagarajan (None) and Samarjit Chakraborty (The University of North Carolina at Chapel Hill)
3. (IoT, CPS, and Emerging Applications Track)
   Agnostic Hardware-Accelerated Operating System for Low-End IoT
   Miguel Silva (Centro ALGORITMI, Universidade do Minho), Tiago Gomes (Centro ALGORITMI, Universidade do Minho) and Sandro Pinto (Centro ALGORITMI, Universidade do Minho)

Session 2a: Real-time Systems Track (I)

Session: Chair: Chao Wang (National Taiwan Normal University)

1. Anytime-Lidar: Deadline-aware 3D Object Detection
   Ahmet Soyyigit (University of Kansas), Shuochao Yao (George Mason University) and Heechul Yun (The University of Kansas)
2. IP Core for Cache and Memory Thrashing
   Michal Dobeš (Honeywell Aerospace), Pavel Zaykov (Honeywell Aerospace), Larry Miller (Honeywell Aerospace), Pavel Badin (Honeywell Aerospace) and Srivatsan Varadarajan (Honeywell Aerospace)
3. Analyzing Fixed Task Priority Based Memory Centric Scheduler for the 3-Phase Task Model
   Jatin Arora (CISTER Research Centre, ISEP, Porto), Syed Aftab Rashid (CISTER Research Centre, ISEP and VORTEX CoLab, Porto), Cláudio Maia (CISTER Research Centre, ISEP, Porto) and Eduardo Tovar (CISTER Research Centre, ISEP, Porto)

Session 2b: IoT, CPS, and Emerging Applications Track (I)

Session: Chair: Po-Chun Huang (National Taipei University of Technology)

1. An Open-World Time-Series Sensing Framework for Embedded Edge Devices
   Abdulrahman Bukhari (University of California - Riverside), Seyedmehdi Hosseinimotlagh (University of California - Riverside) and Hyoseung Kim (University of California - Riverside)
2. Distributed Successive Packet Scheduling for Multi-Channel Real-Time Wireless Networks

Dawei Shen (Northeastern University), Tianyu Zhang (Northeastern University), Jiachen Wang (University of Connecticut), Qingxu Deng (Northeastern University), Song Han (University of Connecticut) and Xiaobo Sharon Hu (University of Notre Dame)

3. QoS Guaranteed Resource Allocation for Coexisting eMBB and URLLC Traffic in 5G Industrial Networks
   Dawei Shen (Northeastern University), Tianyu Zhang (Northeastern University), Jiachen Wang (University of Connecticut), Qingxu Deng (Northeastern University), Song Han (University of Connecticut) and Xiaobo Sharon Hu (University of Notre Dame)

Session 3a: Real-time Systems Track (II)

Session: Chair: Chung-Wei Lin (National Taiwan University)

1. The Role of Causality in a Formal Definition of Timing Anomalies
   Benjamin Binder (Université Paris-Saclay, CEA, List), Mihail Asavoae (Université Paris-Saclay, CEA, List), Florian Brandner (LTCI, Télécom Paris, Institut Polytechnique de Paris), Belgacem Ben Hedia (Université Paris-Saclay, CEA, List) and Mathieu Jan (Université Paris-Saclay, CEA, List)
2. Building Time-Triggered Schedules for typed-DAG Tasks with alternative implementations
   Zahaf Houssam Eddine (University of Nantes) and Nicola Capodieci (University of Modena and Reggio Emilia)

Session 3b: Embedded Systems Track (I)

Session: Chair: Tony Tan (National Taiwan University)

1. Exploiting Binary Equilibrium for Efficient LDPC Decoding in 3D NAND Flash
   Hsiang-Sen Hsu (National Yang Ming Chiao Tung University) and Li-Pin Chang (National Yang Ming Chiao Tung University)
2. DeepPicarMicro: Applying TinyML to Autonomous Cyber Physical Systems
   Michael Bechtel (University of Kansas), Qitao Weng (University of Kansas) and Heechul Yun (The University of Kansas)
3. DVFS Virtualization for Energy Minimization of Mixed-Criticality Dual-OS Platforms
   Takumi Komori (Nagoya University), Yutaka Masuda (Nagoya University) and Tohru Ishihara (Nagoya University)

DAY 2

Session 4: Invited Papers

Session Chair: Shih-Hao Hung (National Taiwan University)

1. Performance Acceleration of Secure Machine Learning Computations for Edge Applications
   Zi-Jie Lin (National Taiwan University), Chuan-Chi Wang (National Taiwan University), Chia-Heng Tu (National Cheng Kung University) and Shih-Hao Hung (National Taiwan University).
2. Segment-Level FP-Scheduling in FreeRTOS
   Robin Edmaier (TU Dortmund University), Jian-Jia Chen (TU Dortmund University) and Niklas Ueter (TU Dortmund University).

Session 5a: Embedded Systems Track (II)

Session: Chair: Tseng-Yi Chen (National Central University)

1. IPDeN: Real-Time deflection-based NoC with in-order flits delivery
   Yilian Ribot González (CISTER Research Centre, ISEP), Geoffrey Nelissen (TU Eindhoven) and Eduardo Tovar (CISTER Research Centre, ISEP)
2. Scalable and Bounded-time Decisions on Edge Device Network using Eclipse Zenoh
   Chi-Sheng Shih (National Taiwan University), Hsiang-Jui Lin (National Taiwan University), Yuyuan Yuan (National Taiwan University), Yi-Hung Kuo (National Taiwan University) and Wen-Yew Liang (ZettaScale Technology Inc.)
3. Design Methodology for Deep Out-of-Distribution Detectors in Real-Time Cyber-Physical Systems
   Michael Yuhas (Nanyang Technological University), Daniel Jun Xian Ng (Nanyang Technological University) and Arvind Easwaran (Nanyang Technological University)

Session 5b: IoT, CPS, and Emerging Applications Track (II)

Session: Chair: Chung-Wei Lin (National Taiwan University)

1. Segment-Level FP-Scheduling in FreeRTOS
   Robin Edmaier (TU Dortmund University), Jian-Jia Chen (TU Dortmund University) and Niklas Ueter (TU Dortmund University)
2. Enabling Real-time AI Inference on Mobile Devices via GPU-CPU Collaborative Execution
   Hao Li (Hong Kong Baptist University), Joseph Ng (Hong Kong Baptist University) and Tarek Abdelzaher (University of Illinois at Urbana-Champaign)
3. Energy-Adaptive Real-time Sensing for Batteryless Devices
   Mohsen Karimi (University of California Riverside), Yidi Wang (University of California Riverside) and Hyoseung Kim (University of California Riverside)

DAY 3

(Special notice: Due to the schedule, Sessions 6b will start after Session 6a.)

Session 6a: Short Paper Session (Embedded Systems Track)

Session: Chair: Po-Chun Huang (National Taipei University of Technology)

1. Controlling High-Performance Platform Uncertainties with Timing Diversity
   Robin Hapka (Techniche Universität Braunschweig - Institute of Computer and Network Engineering), Anika Christmann (Techniche Universität Braunschweig - Institute of Computer and Network Engineering) and Rolf Ernst (Techniche Universität Braunschweig - Institute of Computer and Network Engineering)
2. QoS-MAN: A Novel QoS Mapping Algorithm for TSN-5G Flows
   Zenepe Satka (Mälardalen University), Mohammad Ashjaei (Mälardalen University), Hossein Fotouhi (Mälardalen University), Masoud Daneshtalab (Mälardalen University), Mikael Sjödin (Mälardalen University) and Saad Mubeen (Mälardalen University)

Session 6b: Short Paper Session (Real Time Systems Track)

Session: Chair: Po-Chun Huang (National Taipei University of Technology)

1. Using Trace Data for Run-Time Optimization of Parallel Execution in Real-Time Multi-Core Systems
   Florian Schade (Karlsruhe Institute of Technology), Timo Sandmann (Karlsruhe Institute of Technology), Jürgen Becker (Karlsruhe Institute of Technology) and Henrik Theiling (SYSGO GmbH)