## **Richy Teas**

# https://richyteas.herokuapp.com

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## **EDUCATION:**

University of California, Irvine

June 2016

Bachelor of Science, Computer Science and Engineering

#### **WORK EXPERIENCE:**

## Software Developer Intern @ Kappboom Inc.

July 2014 - September 2014

- Wrote backend software with Ruby/Rails to expose RESTful APIs to application clients
- Developed Android applications with Java and Eclipse, interfacing with web apps
- Worked with Linux, Angular.js, Node.js, JQuery, CSS3, MySQL, and MongoDB

### **Private Tutor**

June 2013 - September 2013

Tutored intro to Java and C++ to community college students

#### PROJECTS:

## **Unity Game Project** (Currently in-progress):

- Developing 2D arcade shooting game with Unity
- Designed & implemented player tracking, allowing enemies to fire accurate shots to player
- Using GIMP to create and design (all original) sprites/art assets

## **Portfolio Website** (https://richyteas.herokuapp.com):

- Developed SPA website using Angular.js and consuming Github's api
- Developed backend with Rails, implementing Google's reCAPTCHA

# Senior Project (3D Modelling Quadcopter):

- Designed and implemented 3D modelling algorithm using vertices scanned by laser
- Created backend website for storing 3D vertices data

#### OTHER SKILLS AND EXPERIENCE:

#### Java

- Recreated data structures & created simulations using input text data
- Worked with team to create a rouge game using the Slick2D library

## Ruby/Rails

Created mock-up twitter website and used front-end web languages such as ¡Query and JavaScript

## C# (ASP.NET)

Developed ASP MVC application to manage patient medical data with Entity Framework 6

## Embedded Systems (C/C++)

- Developed a functional digital watch with time, date, timer, countdown, alarm, and settings
- Created a sound equalizer by manipulating LP, HP, and BP filters to manipulate amp/dB of frequencies

## Matlab

- Generated textures using sample data images and image stitching techniques
- Generated sinusoidal data and samples for processing and analysis

## Verilog and VHDL

Designed components to function as a fully functional MIPS processor with pipelining