Ion Electrospray Thruster Assembly (IETA)
Command Interface

Rev 11, 8-26-2014

F. J. LaRosa, Espace, Inc.

Electrical Interface

The IETA Thruster Assembly is controlled using a SPI interface, and also supports a serial interface for testing situations that require wireless control or long cable runs. The interface signals are shown in Table 1.

Table 1. J3 Pin Assignments.

Signal	Direction	Description
RST/	IN	Reset Input, active low
INT/	OUT	Interrupt Output, currently unused
CS/	IN	SPI Chip Select input, active low
SCK	IN	SPI Serial Clock
MOSI	IN	SPI data input
MISO	OUT	SPI data output, tri-state
RX	IN	Serial port input
TX	OUT	Serial port output

The thruster assembly can be controlled via the SPI or serial port interface, as selected by a “UART_SEL” jumper on the HV board. When UART_SEL is shorted, the serial port is used. When left open, the SPI interface is used. Also, a special command via the serial port, forces the unit into Serial mode.

Control/Status – SPI (Serial Peripheral Bus) Interface

The SPI Control/Status interface follows the conventions for the Serial Peripheral Interface (SPI) standard. The signals, shown in Figure 1, include an active low Chip Select (CS/), a gated Serial Clock (SCK), a Master-Out-Slave-In (MOSI) data line and a Master-In-Slave-Out (MISO) data line.

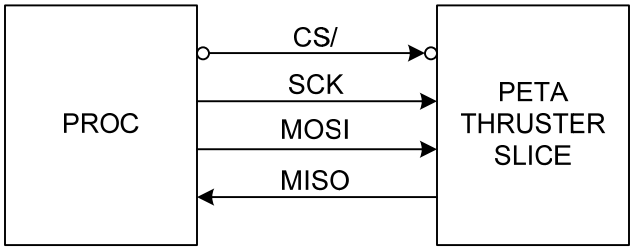

Figure 1. Serial Peripheral Interface (SPI) Signals.

The serial interface will operate at any clock speed up to 2MHz, as set by SCK from the Master. 1MHz has been extensively tested, and is used as an example here to derive the timings shown below (see Figure 2). The CS/ line is driven low, and the MSB of the command word is presented on the MOSI line at the same time. Data is changed on the falling edge of the gated SCK, and is sampled at the slave on the rising edge. The command word is 24 bits in length. Response data for read cycles is 16 bits, and the MSB of the read data begins after 8 SCK cycles. During the first 8 SCK cycles, the MISO line is 0. In SPI terms, CPOL=0 and CPHA=0.

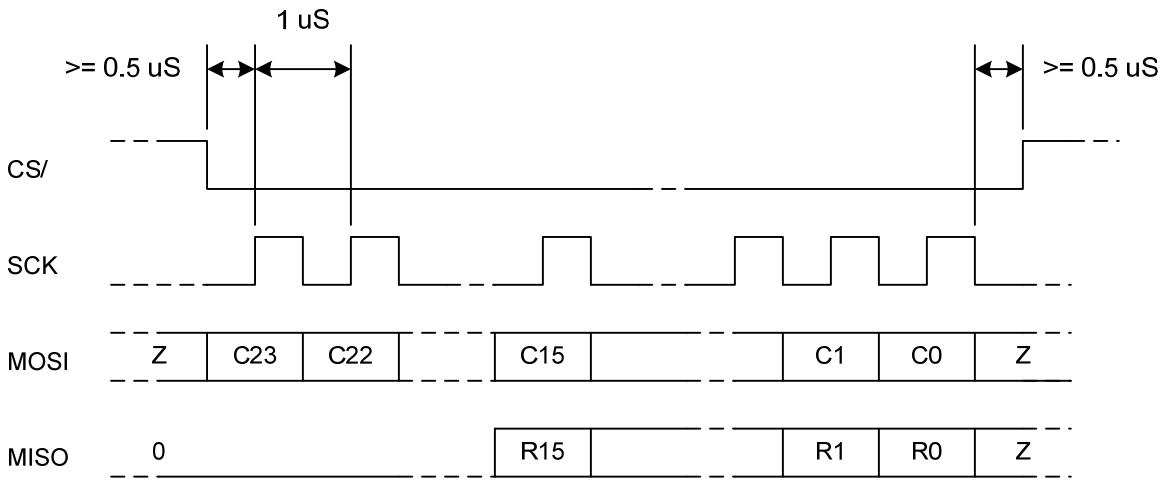

Figure 2. SPI Timing.

Functional Interface – SPI Port

The command word has the format shown in Figure 3. The order of transmission is MSB to LSB. The first 7 bits (23:17) comprise the register address (see Table 2). The next bit (16) is the Read-not-Write (RNW) bit. A '0' signifies a Write cycle, and a '1' signifies a read cycle. The last 16 bits are the data to write to the addressed register.

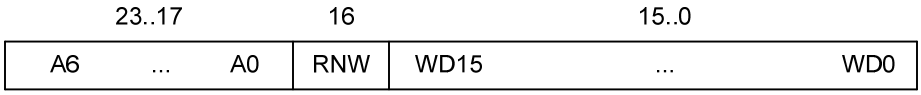

Figure 3. SPI Command Word.

When the RNW bit is set to '1', a Read cycle is initiated. For a read, bits 15 to 0 of the command word are irrelevant and can be set to '0', but the SCK line continues to toggle to read out the 16 response bits from the slave (see Figure 4).

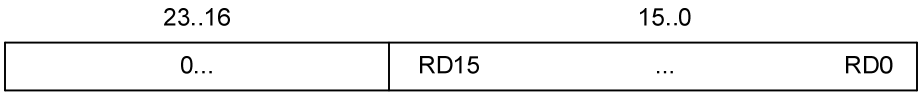

Figure 4. SPI Response Data Format.

A summary of commands (registers) is shown in Table 2. The SETUP command allows a choice between manual thrusting and batch mode thrusting.

Functional Interface – Serial Port

The UART interface runs at 115.2kbps, with 1 Start bit and 1 Stop bit, and no flow control. For a write command, three bytes are sent to the assembly, as shown in Figure 5. The RNW bit in Byte 0 is set to 0.

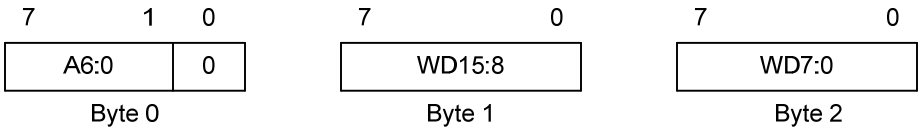

Figure 5. Serial Port Write Command Format.

The order of the 24 total bits of data matches that for the SPI interface (Figure 3). As each byte is received by the assembly, it is echoed back via the TX line. These bytes can be ignored or used for verification.

For a Read, only the command byte with RNW bit set to 1 is sent to the assembly. Upon receipt, the command byte is echoed on the TX line, followed by two response bytes: MSByte followed by LSByte, as shown in Figure 6.

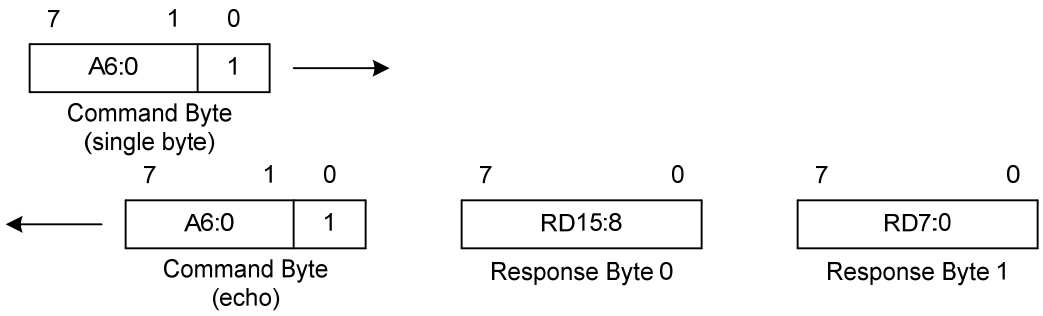

Figure 6. Serial Port Read Command Format.

Table 2. IETA EM Thruster Assembly Commands.

ADDRESS	W/R	REGISTER	DESCRIPTION
0x00	WR	Setup	Bit 0: 1 = closed loop voltage control Bit 1: 1 = thrust timeout enable Bit 2: 1 = auto polarity reverse enable Bit 3: 1 = batch mode enable Bit 4: 1 = controller gain scheduler enable
0x01	-	(unused)	
0x02	WR	HVDAC	Manual supply range setting (Setup bit 1 = 0) Range 0 to 0x3FF
0x03	WR	Thrust Gap Time	Gap time during which thrust switches are disabled before new thrust command is engaged, or when reversing polarity in Auto Reverse mode. Range 0 (1mS) to FF (256mS). (See Thrust Reverse Time register).
0x04	WR	Thrust Timeout	Timeout time in 10mS increments. Range 0 (10 mS) to FFFF (655.36 S , or 11 minutes).
0x05	WR	Thrust Reverse Time	In Auto Reverse mode, this is the total time the thrusters are enabled before a gap time is inserted. Range 0 (1mS) toFFFF (65,536mS). The total reversal period is [reverse_time_reg+1] + [gap_time_reg+1] (See Thrust Gap Time register).
0x06	WR	(reserved)	
0x07	WR	Thrust Register	Bitwise Thruster Enable/Disable register (see Figure 7)
0x08	WR	HV Setpoint	HV_Set_register * 4.096 * 455.05 / 65536 Theoretical max = 1864V Hardware limit (comparator) = 1745V
0x09	WR	(reserved)	
0x0A	WR	(reserved)	
0x0B	WR	(reserved)	
0x0C	WR	Test Register	16 bit test register to test writes/reads
0x0D	WR	Status	Bit 0: reserved Bit 1: batch executing (0 = ready) Bits 2-5: unused Bit 6: HV_Diff (HVCOM – GND over limit) Bit 7: unused Bit 8: HV_Over (HV+ supply over limit Bit 9: HV_Under (HV- supply over limit) Bit 10: I_Limit (Input current over limit) Bit 11: limits_OK (Bits 6, 8, 9 & 10 are all OFF) Bits 12, 13: reserved

			Bit 14: thruster load > 0 (at last one on) Bit 15: uart_sel_n (0 = ser port enabled)
0x0E	R	FPGA Revision Reg Low	DDRR, Hex-encoded Day/ Rev#
0x0F	R	FPGA revision Reg High	YYMM, Hex-encoded Year/Month
0x10	R	ADC0	+3.3V supply voltage
0x11	R	ADC1	+HK, positive HV supply
0x12	R	ADC2	-HK, negative HV supply
0x13	R	ADC3	+BUS, raw bus voltage
0x14	R	ADC4	IS, primary side current
0x15	R	ADC5	+5V supply voltage
0x16	R	ADC6	TS1, temperature sensor 1
0x17	R	ADC7	TS2, temperature sensor 2
0x18	-	(unused)	
0x19	-	(unused)	
0x1A	WR	Controller Gain	HV Controller gain. Range 0 to FF
0x1B	WR	HVDAC Limit	Limit over which HVDAC write will be ignored (see HVDAC register).
0x1C	WR	HV Setpoint Limit	Limit over which HV_Set write will be ignored (see HV Setpoint register).
0x1D	WR	(reserved)	
0x1E	-	(unused)	
0x1F	-	(unused)	
0x20	W	Batch thrust vector address set	(see Batch Mode section)
0x21	W	Batch thrust vector write port	(see Batch Mode section)
0x22	W	Batch Command Write port	(see Batch Mode section)
0x23	WR	HV_DIFF set	Sets the limit for |HVCOM – GND| Limit = HV_DIFF_reg * 4.096 * 455.05 / 4096
0x24	WR	(reserved)	
0x25	WR	(reserved)	
0x26	WR	Auto Period Set	Sets the period range for the HV controller. 16-bit register. Period Set reg = Max period (uS) * 50 / 16 Example: 10,000uS * 50 / 16 = 31,250 (0x7A12) Note: resulting min period = Max_period/1024. Min period equates to max voltage
0x27	WR	Auto Pulse Width Set	Sets the pulse used for voltage control. 8-bit register. Pulse width reg = Pulse width (uS) * 50 Max FF = 5.12 uS
0x28	R	Auto Period Read	Read only register returns the period currently being used by the controller. It will be in the range set by the Auto Period Set register.
0x29	R	Auto Pulse Width Read	Read only register returns the pulse width currently being used by the controller (will be the

			same value as AutoPulse Width set register).
0x30	W	Serial Port force	Only used via the serial port. Writing the value 0xCAFE to this register forces the command interface to switch to the serial port. This is a debug “backdoor” entry. Writing any other value does nothing. Resetting or power cycling the unit restores SPI operation.

Thrust Register

In manual thrust mode, each Thrust command (register 5) is executed immediately upon receipt. Timing is under manual control of the host processor. The Manual Thrust command has the format shown in Figure 7.

To enable Thruster 0 with positive polarity, set P0 to 1. For Thruster 0 negative polarity, set N0 to 1. There is a P/N bit pair for each thruster. Setting both P and N for a thruster to 0 disables thrust. P and N may not both be set to 1, and when this is the case, that thruster will be disabled.

BIT:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH:	N7	N6	N5	N4	N3	N2	N1	N0	P7	P6	P5	P4	P3	P2	P1	P0

Figure 7. Manual Thrust Command Format.

Any thrust command causes a gap (all thrusters disabled) to be inserted before the new command is engaged. The gap is set by register 0x03.

If Auto Polarity Reverse mode is enabled (see register 0x00), all thruster channels are polarity switched in sync. Any new thrust command also causes a forced gap right when the command is received, in additional to ongoing automatic gap insertions. Also, since polarity is handled automatically, the use of positive and negative bits in the command are irrelevant. For example, sending a command of 0x0001 has the same effect as sending 0x0100. For simplicity, one can just use bits 7:0, as if all commands are positive values.

Batch Thrust Mode

In batch thrust mode, thrust sequences can be executed by storing thrust enable vectors and durations in the Thrust Enable Memory, thrust commands in the Thrust Command Stack, and writing to the Control register to initiate a sequence. The Control register and memories are shown in Figure 8. The lowest level is the Thrust Enable Memory, which is a 256-deep memory storing 8-bit thrust enable patterns with 8-bit thrust durations. The thrust enable bits are defined as

Thrust Enable Memory Bit	Description
15	Enable for Thruster 7
14	Enable for Thruster 6
13	Enable for Thruster 5
12	Enable for Thruster 4
11	Enable for Thruster 3

10	Enable for Thruster 2
9	Enable for Thruster 1
8	Enable for Thruster 0

Note that in Batch mode, thrust polarity reversal is handled automatically by the hardware. Bits 7:0 set the duration, in 0.1 Second increments, associated with the enable pattern. The maximum value of 0xFF produces a duration of 25.5S.

The next level up is the Thrust Command Stack. A value stored in this memory points to a starting address in the Thrust Enable Memory. The bits are defined as

Command Stack Bits	Width (bits)	Description
15:12	4	Forms upper nibble of Thrust Enable memory address
11:8	4	Length of pattern in Thrust Enable memory to execute
7:0	8	Repeat Count (number of times to execute this command)

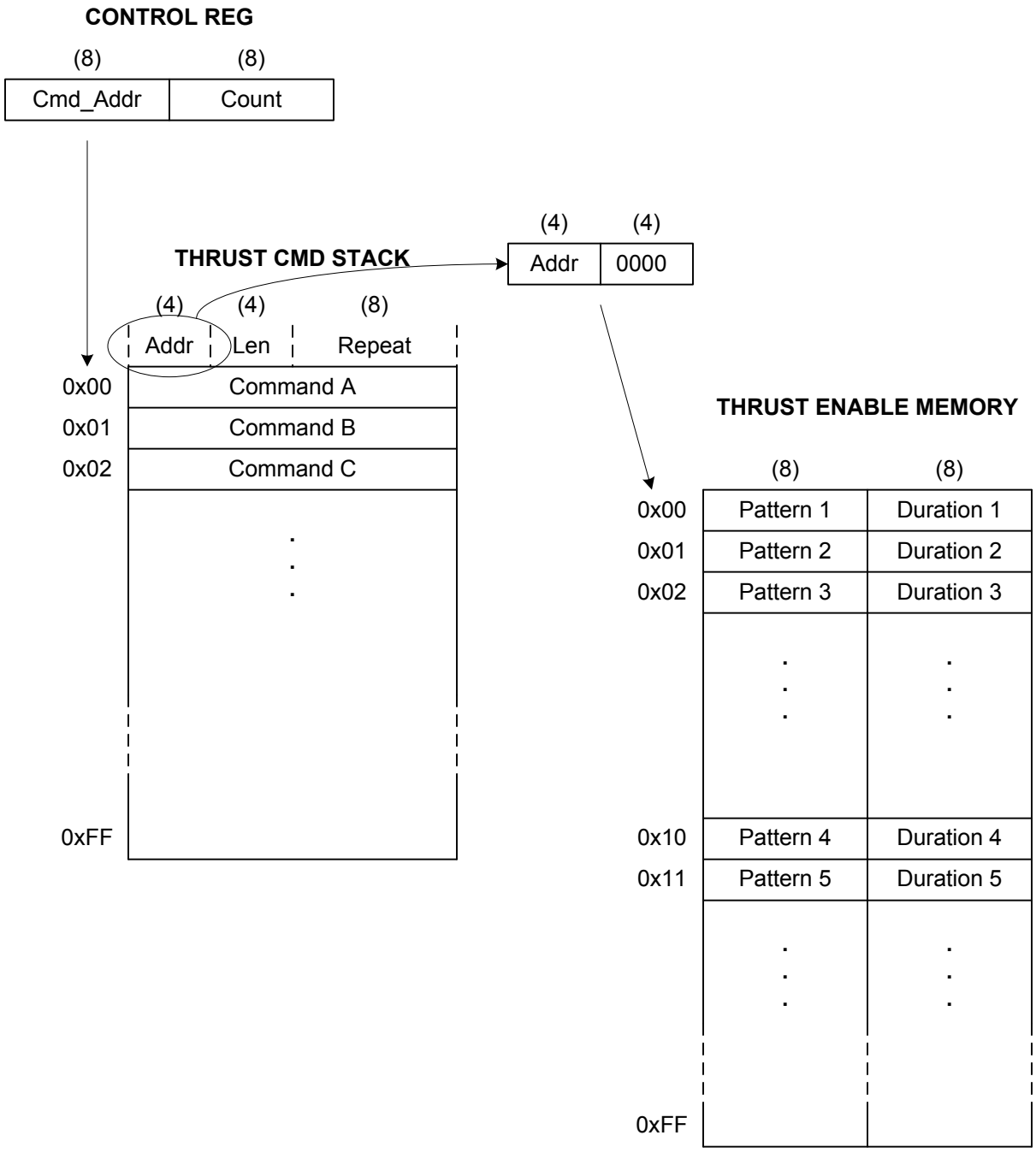

Figure 8. Batch Mode Control Register and Memories.

The top level is the Control Register, which is used to initiate a command sequence. The upper 8 bits set the address in the Command Stack at which to begin execution. The lower 8 bits set the number of contiguous Command Stack locations to execute. Writing all zeros to this register cause all execution to stop, and all thrusters to be disabled.

Thrust Enable Memory is accessed by first loading an address pointer into the Thrust Enable Memory Address register and then performing a series of writes (or reads). The Thruster Slice auto-increments the address pointer after each write or read cycle. The address pointer is 8 bits. The memory is logically subdivided into 16 equal blocks at address 0x00, 0x10, 0x20, up to 0xF0. These blocks are executed by commands stored in the Thrust Command Stack. The Length field in a Thrust Command Stack memory location may be greater than 16, allowing execution to span more than one block in the Thrust Enable memory.

The stack is access by means of the Thrust Command Stack Address pointer and the Thrust Command Stack Access register, with auto-increment. The stack is 256 deep.

Reading ADC Channels

Each ADC channel has its own calculation necessary to produce a meaningful housekeeping measurement. These are provided in Table 3 for Rev 3 units and Table 4 for Rev 4.

Table 3. ADC Channel Calculations for Rev 3.

Channel	Description	Calculation	Units
ADC0	+3.3V supply voltage	V_+3.3V = Reading*(2.5/4096) * 2	V
ADC1	+HK, positive HV supply	V_+HK = Reading*(2.5/4096) *650.35	V
ADC2	-HK, negative HV supply	V_-HK =- Reading*(2.5/4096) *650.35	V
ADC3	+BUS, raw bus voltage	V_+bus = Reading*(2.5/4096) * 5.5455	V
ADC4	IS, primary side current	I_is = Reading*(2.5/4096)	A
ADC5	+5V supply voltage	V_+5V = Reading*(2.5/4096) * 2	V
ADC6	TS1, temperature sensor 1	T1 = (Reading*(2.5/4096) – 0.5) * 100	Deg. C
ADC7	TS2, temperature sensor 2	T2 = (Reading*(2.5/4096) – 0.5) * 100	Deg. C

Table 4. ADC Channel Calculations for Rev 4.

Channel	Description	Calculation	Units
ADC0	+3.3V supply voltage	V_+3.3V = Reading*(4.096/4096)	V
ADC1	+HK, positive HV supply	V_+HK = Reading*(4.096/4096) * 455.55	V
ADC2	-HK, negative HV supply	V_-HK =- Reading*(4.096/4096) * 454.55	V
ADC3	+BUS, raw bus voltage	V_+bus = Reading*(4.096/4096) * 3.564	V
ADC4	IS, primary side current	I_is = Reading*(4.096/4096)	A
ADC5	+5V supply voltage	V_+5V = Reading*(4.096/4096) * 2	V
ADC6	TS1, temperature sensor 1	T1 = (Reading*(4.096/4096) – 0.5) * 100	Deg. C
ADC7	TS2, temperature sensor 2	T2 = (Reading*(4.096/4096) – 0.5) * 100	Deg. C