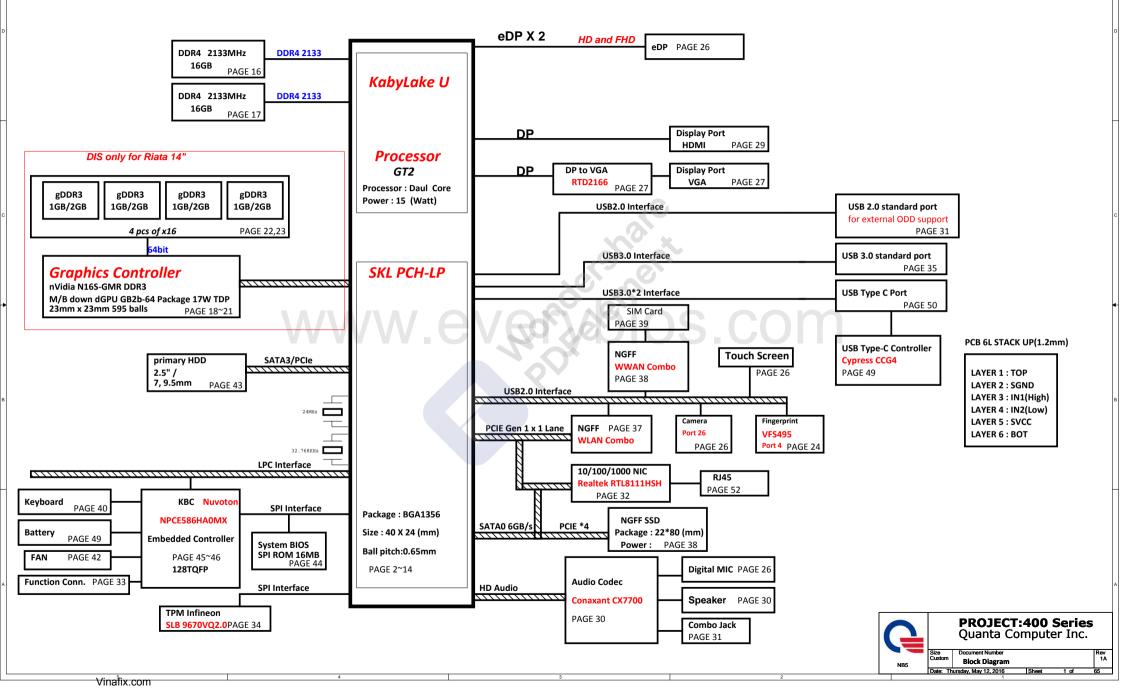
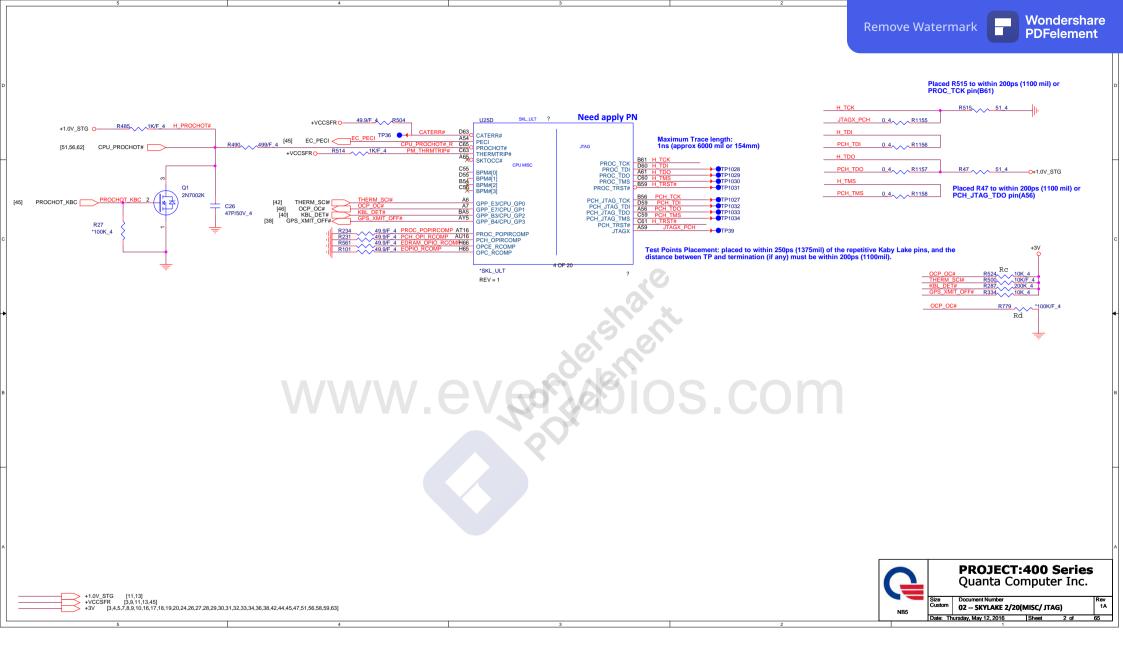
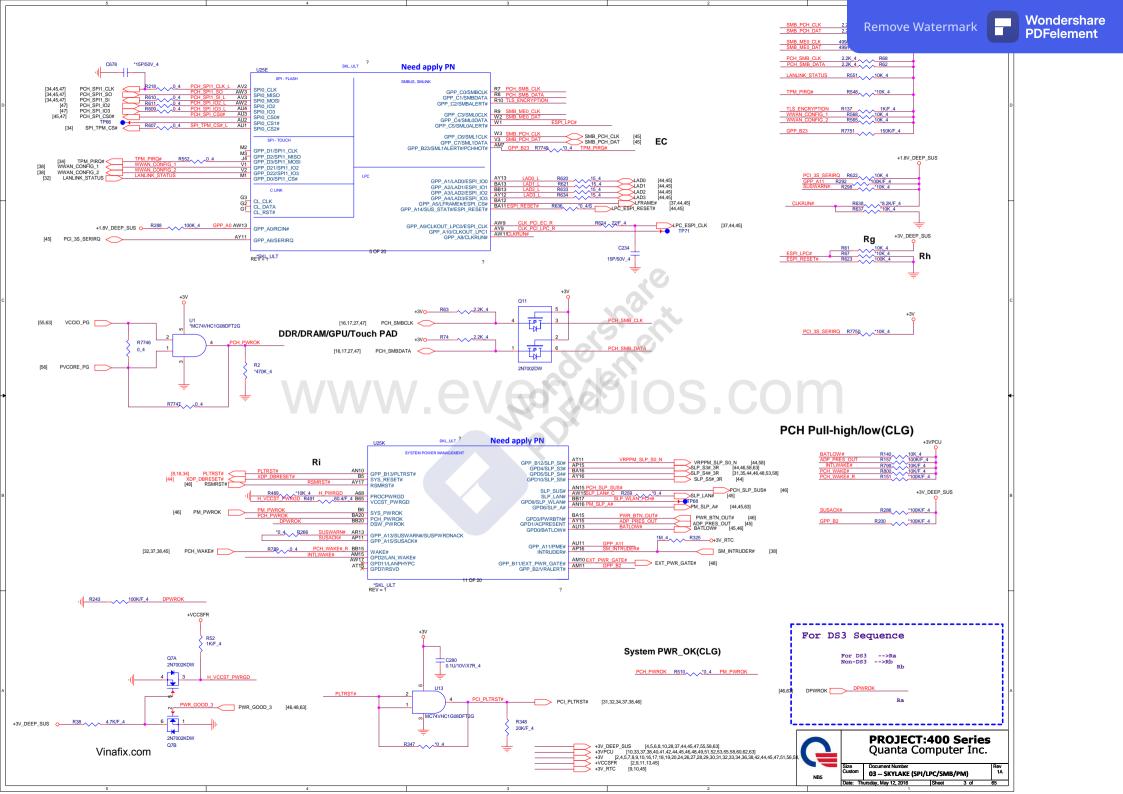
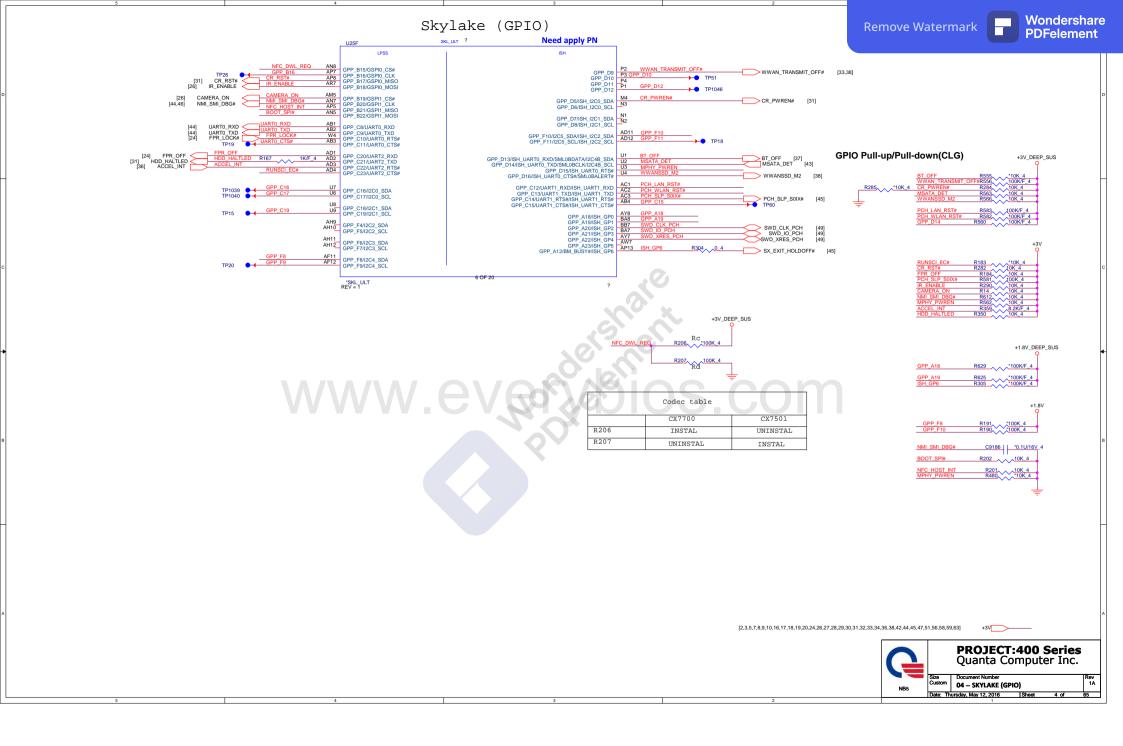
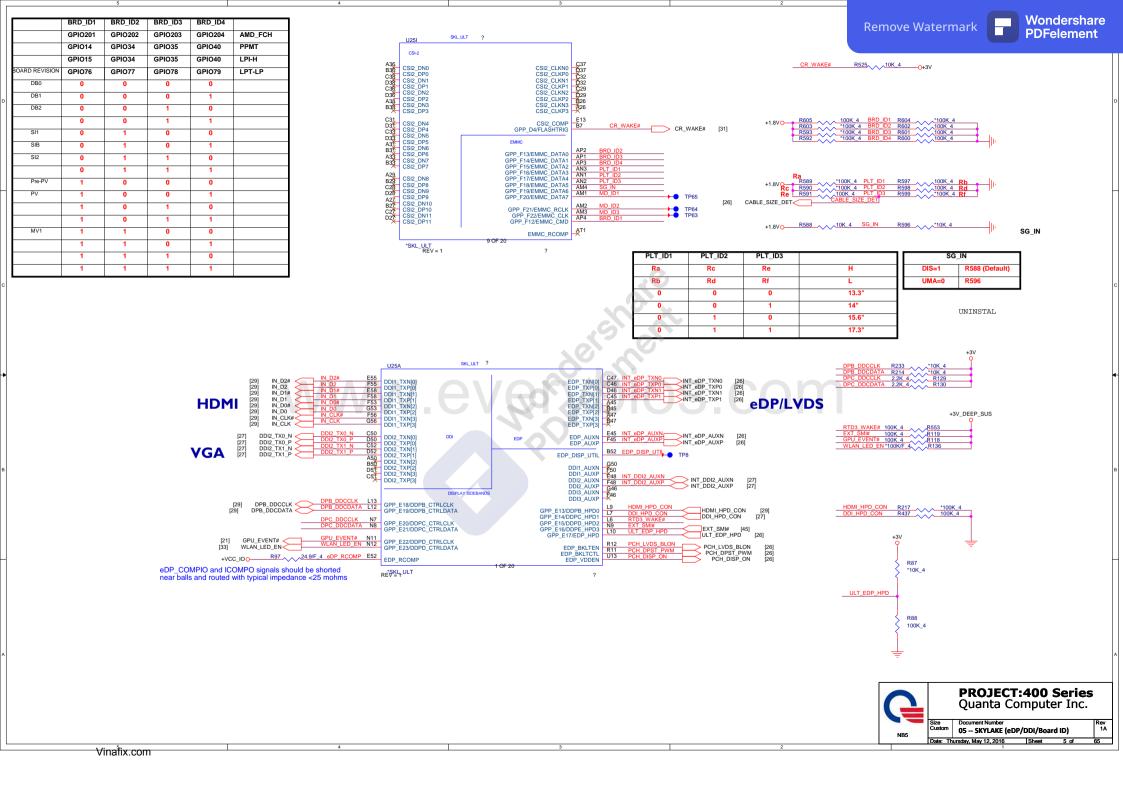
Reilly 13"/Rourke 14" KabyLake -U (UMA/DIS) Sentiments

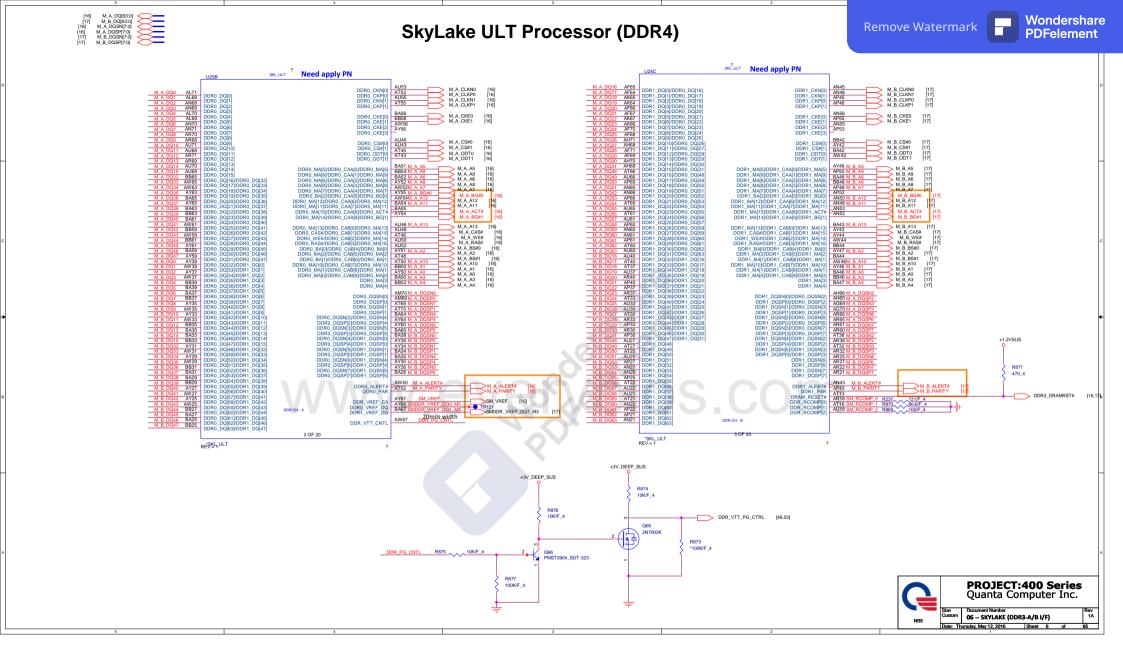


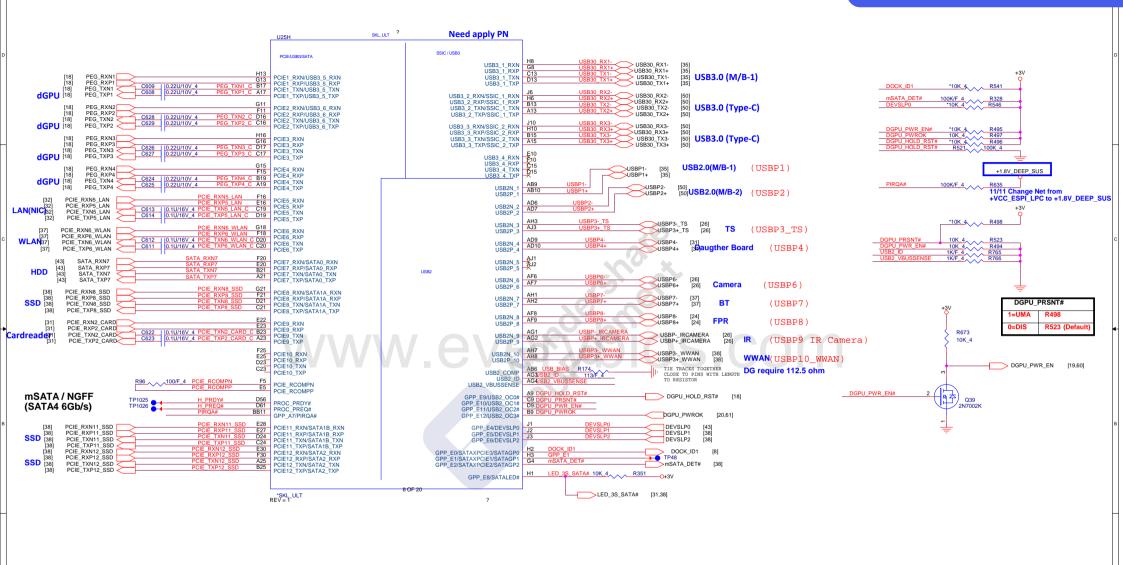






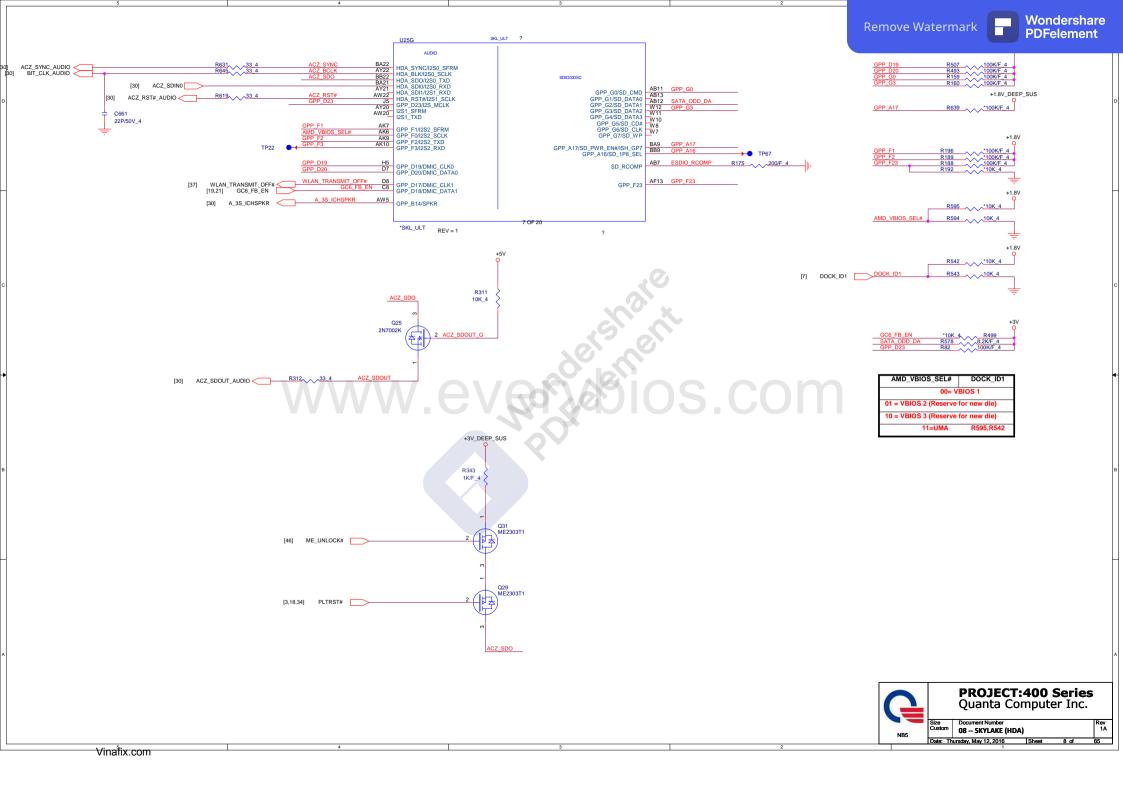


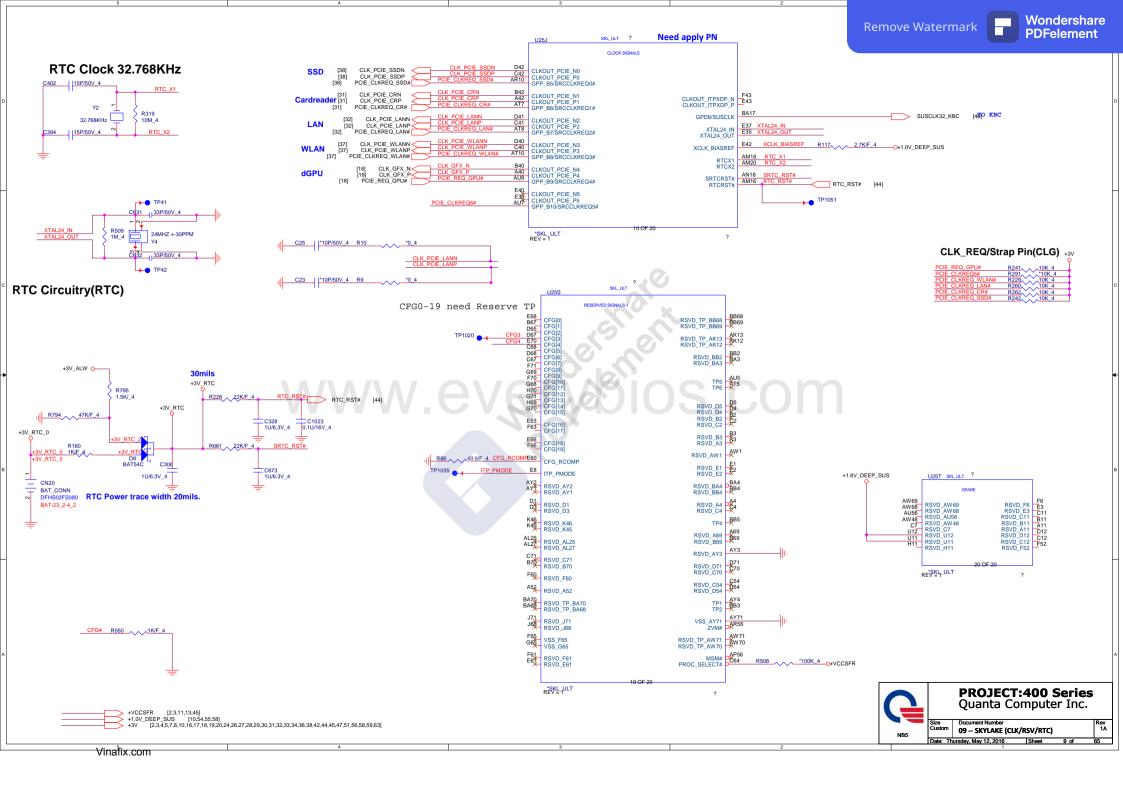


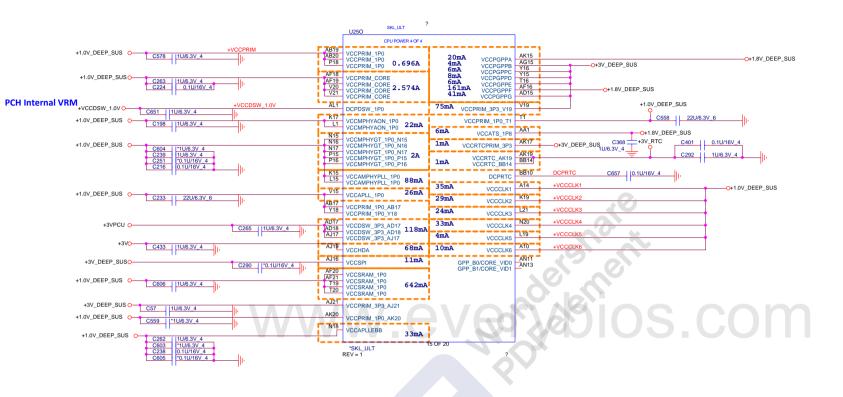


[2,3,4,5,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63] +3V_DEEP_SUS







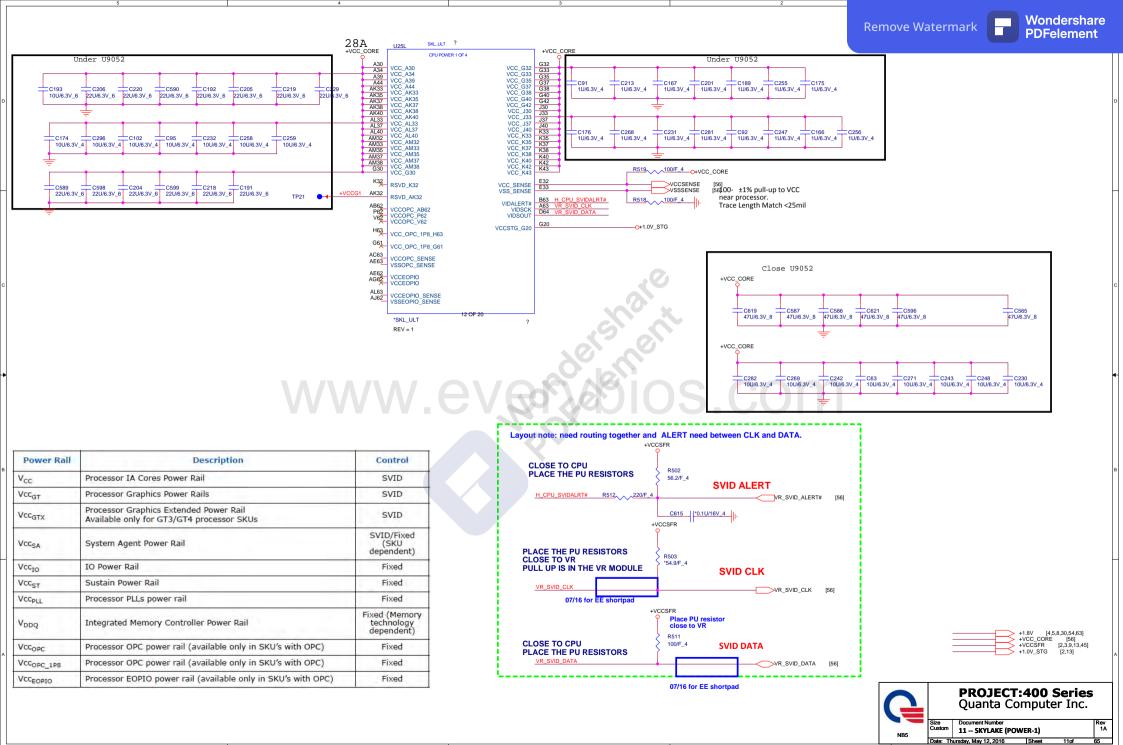




**- 3V DEEP SUS | 3,4,5,6,8,28,37,4,4,5,47,55,58,63) **-3VPCLI | 33,337,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] **-1,3V DEEP SUS | (8,45,5,6,8) **-1,3V C, PRM | 2,3,4,5,7,8,9,16,17,18,19,20,24,6,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63] **-1,3V DEEP SUS | (3,47,89,45,5,46,3) PROJECT:400 Series
Quanta Computer Inc.

Size Document Number
10 - SKYLAKE (PCH POWER)
Date: Thursday, May 12, 2016 | Sheet 10 of

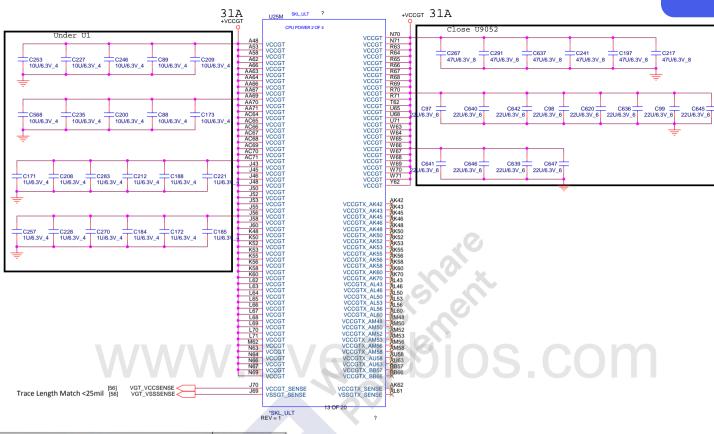
Rev 1A





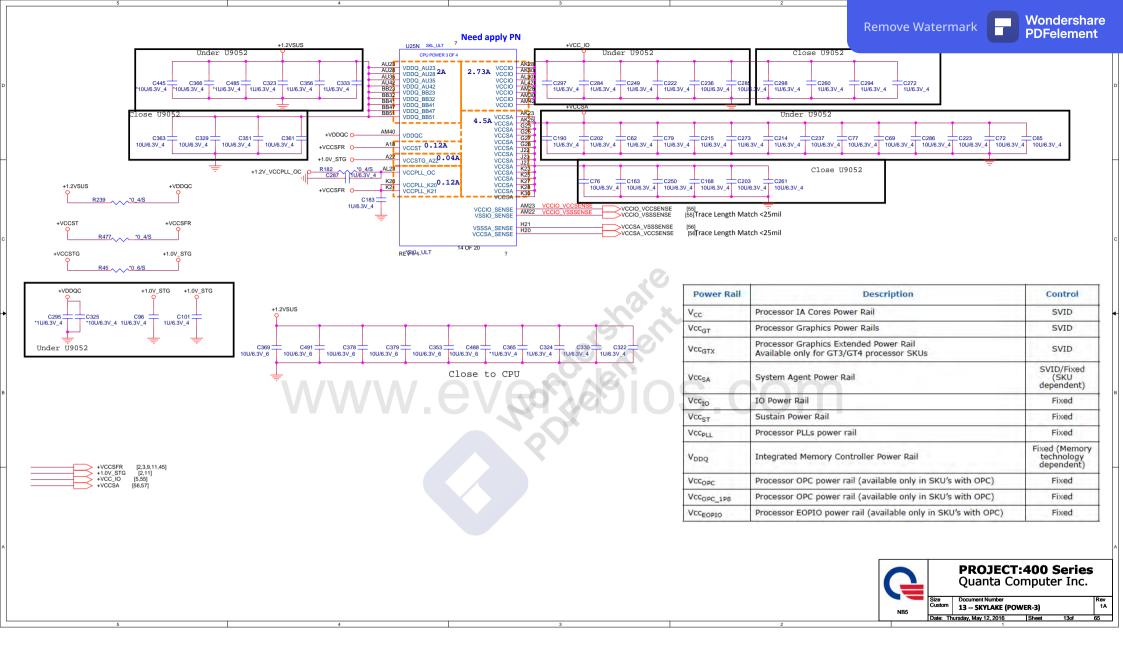
47U/6.3V_8

47U/6.3V_8



Power Rail	Description	Control	
V _{cc}	Processor IA Cores Power Rail	SVID	
Vcc _{GT}	Processor Graphics Power Rails	SVID	
Vcc _{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID	
Vcc _{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)	
Vcc _{IO}	IO Power Rail	Fixed	
Vcc _{ST}	Sustain Power Rail	Fixed	
Vcc _{pLL}	Processor PLLs power rail	Fixed	
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)	
Vcc _{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed	
Vcc _{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed	
Vcc _{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed	

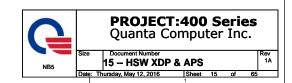
PROJECT:400 Series Quanta Computer Inc. Rev 1A 12 -- SKYLAKE (POWER-2) NB5 Date: Thursday, May 12, 2016

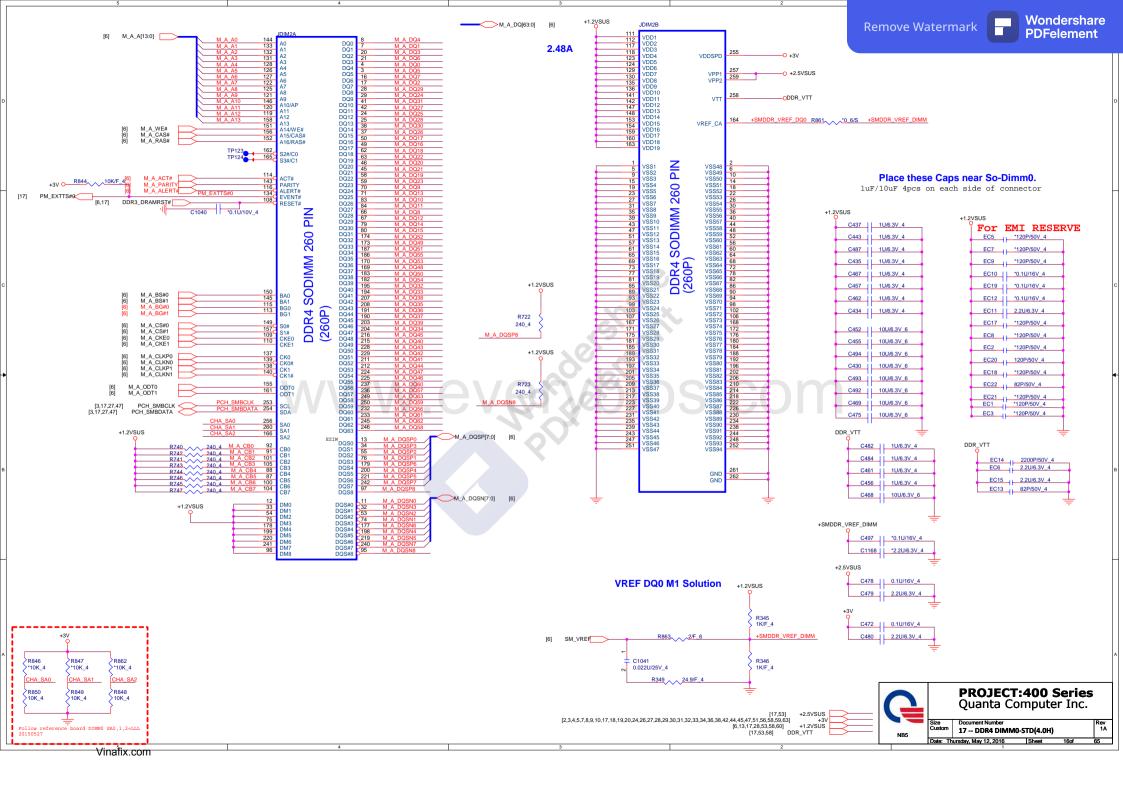


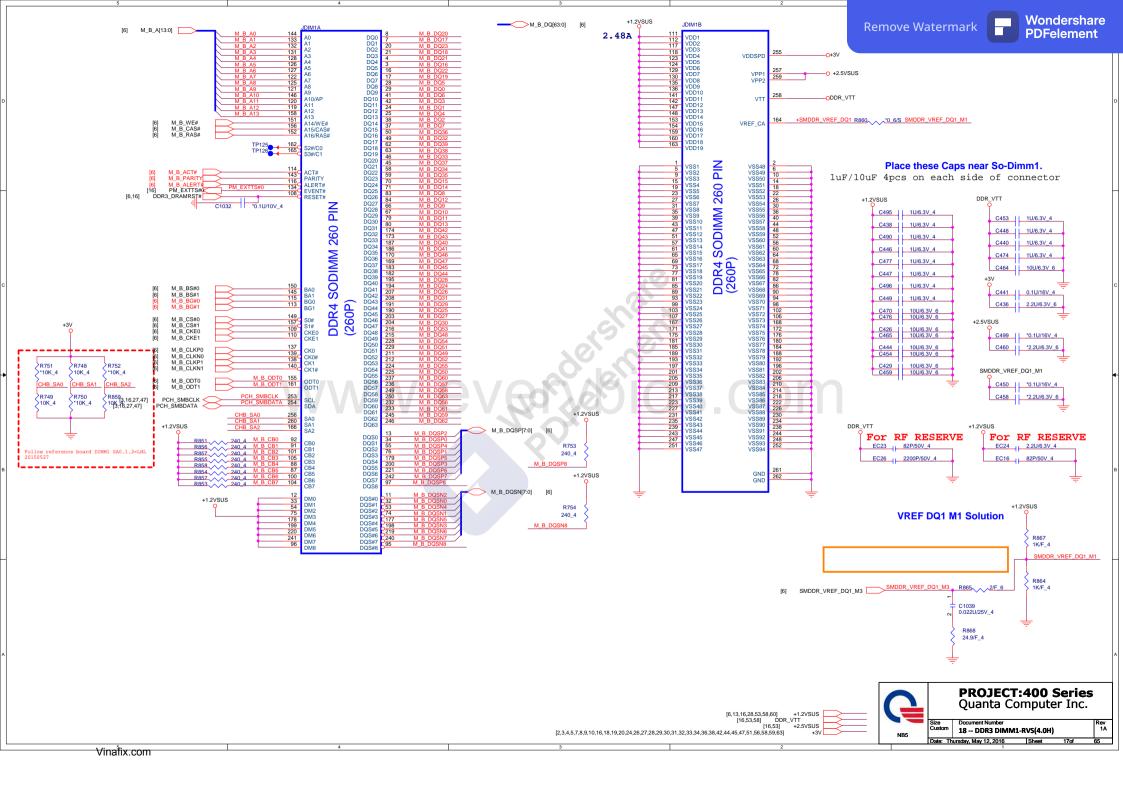


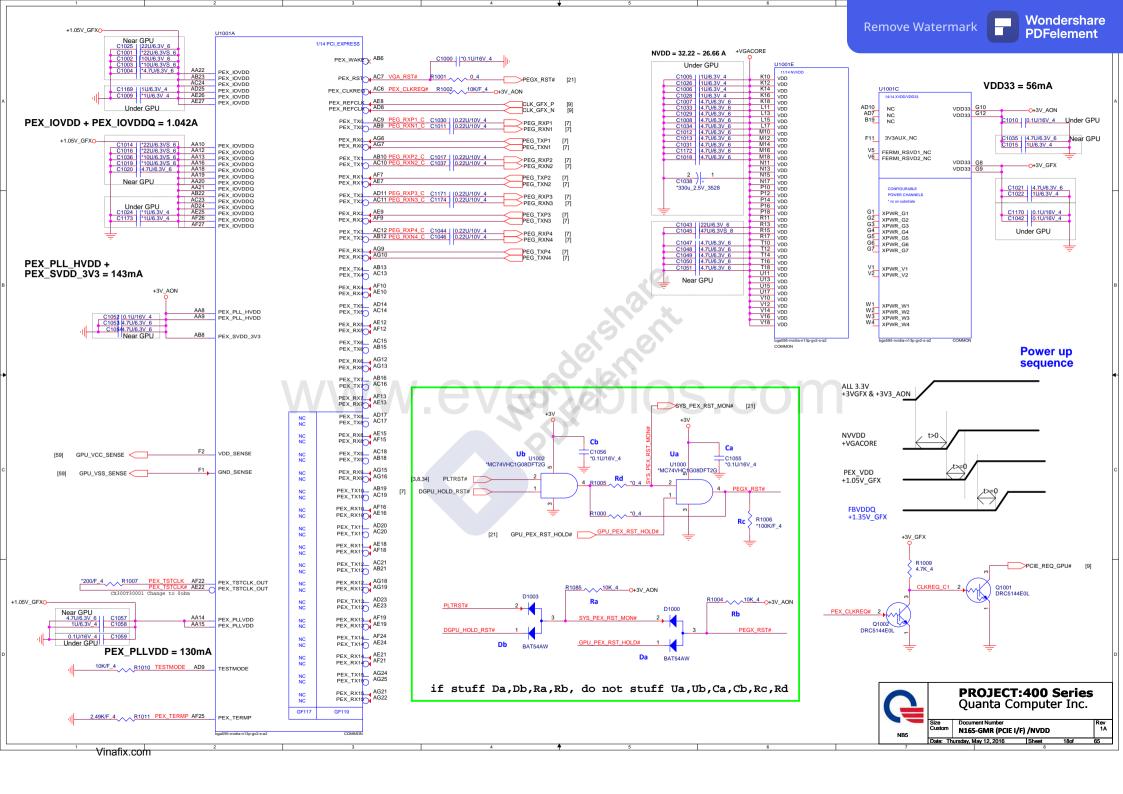


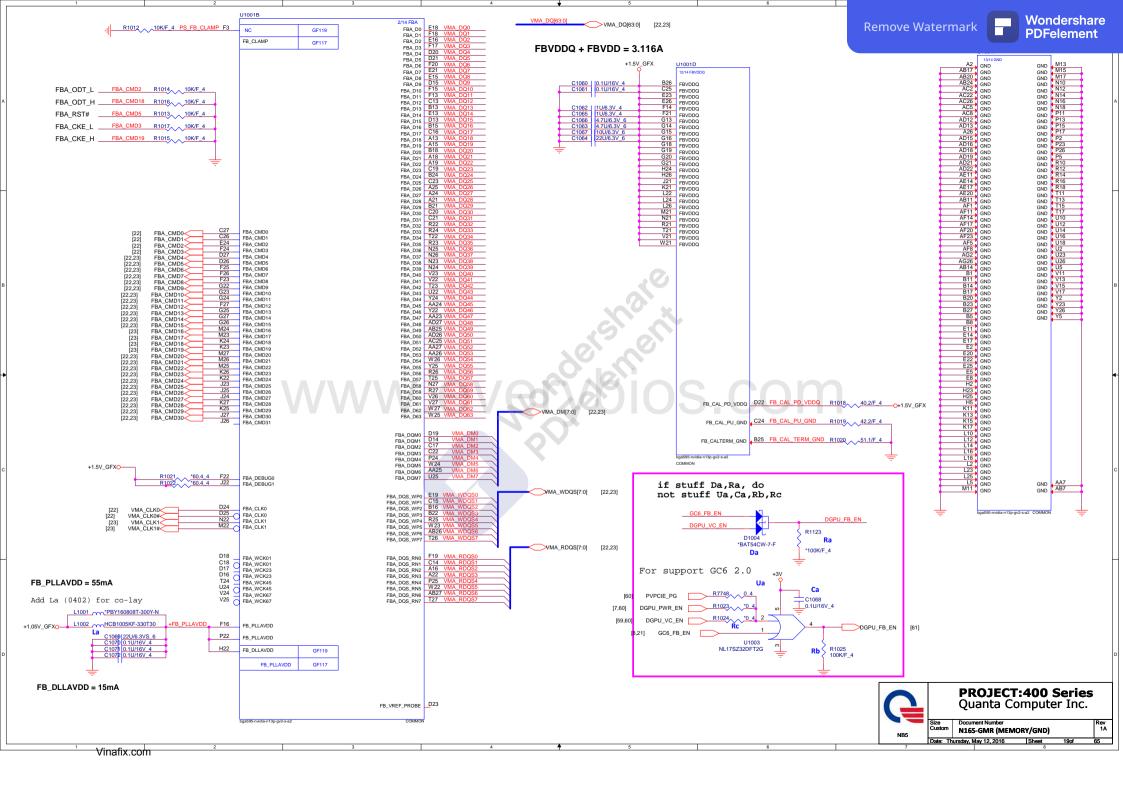
www.everlesios.com

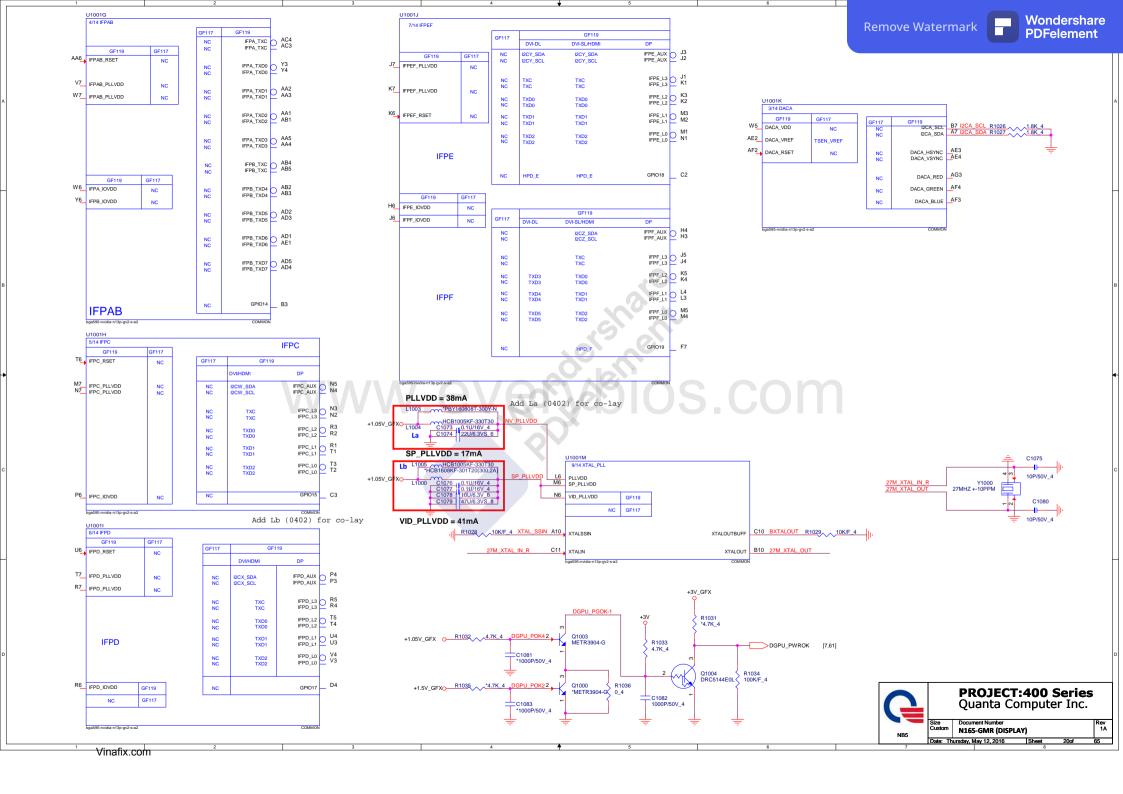


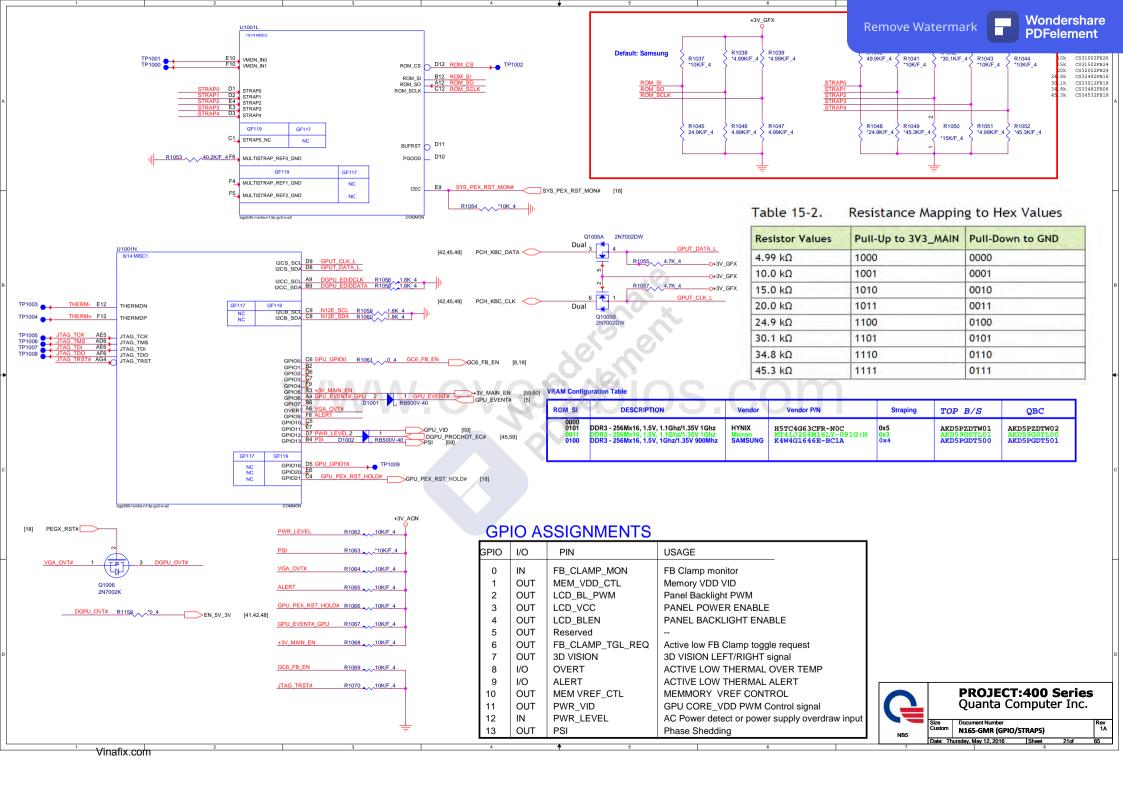


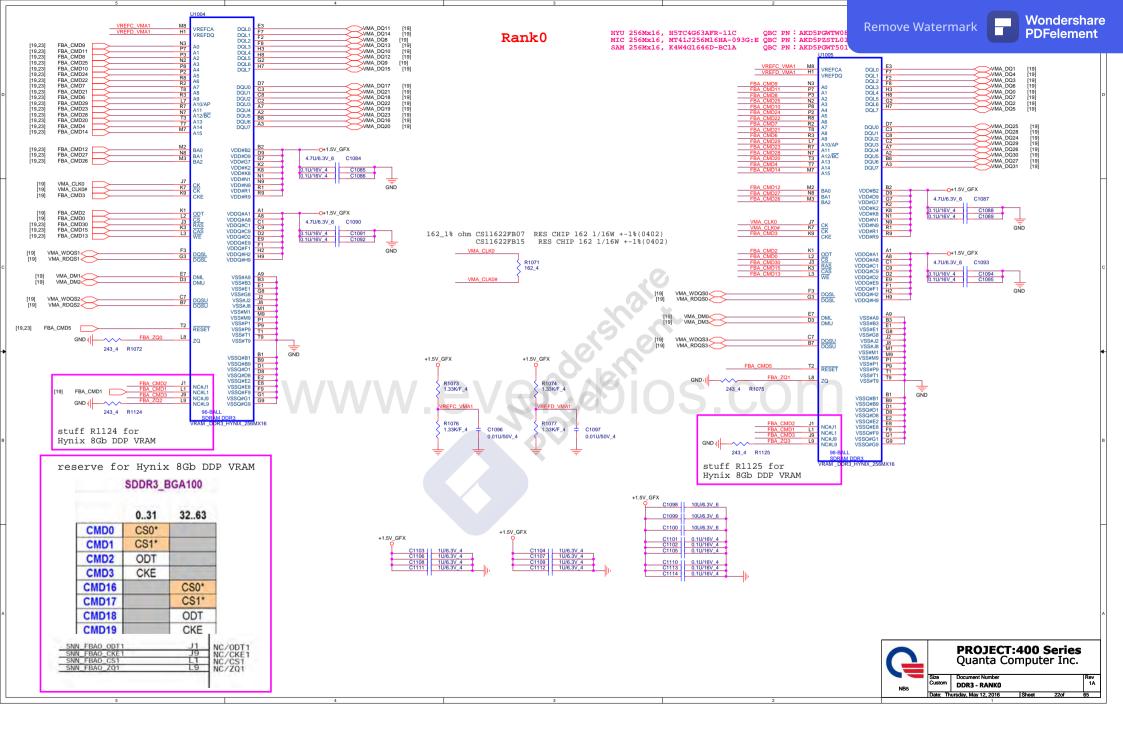


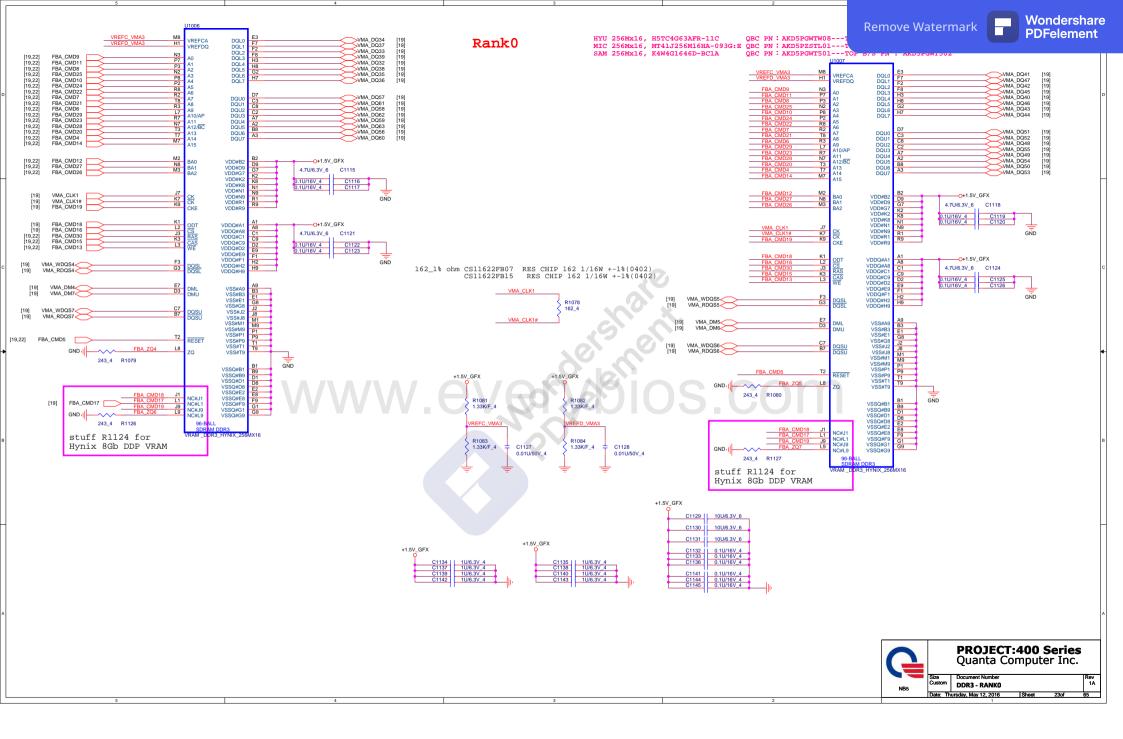


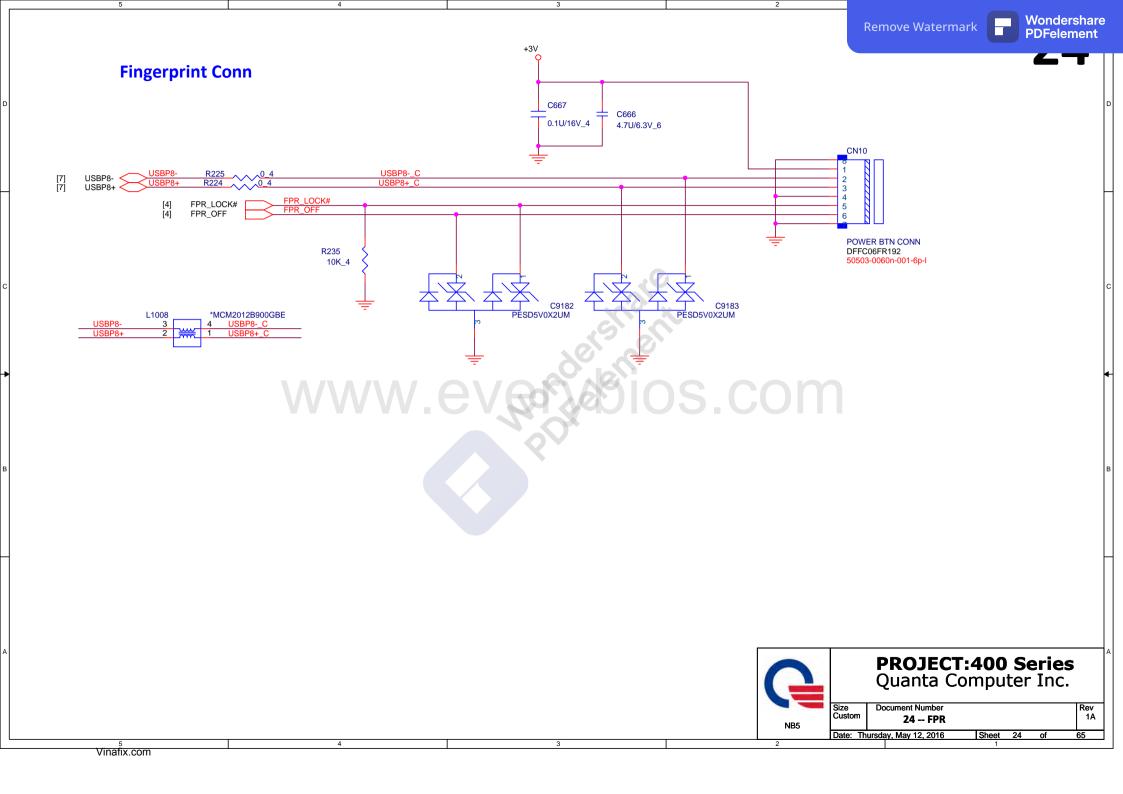






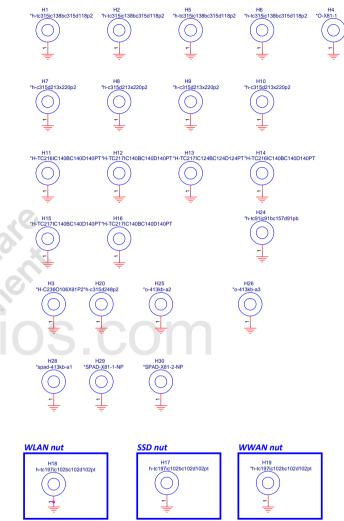


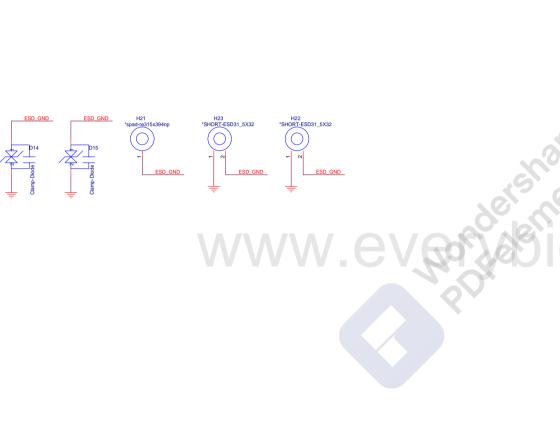


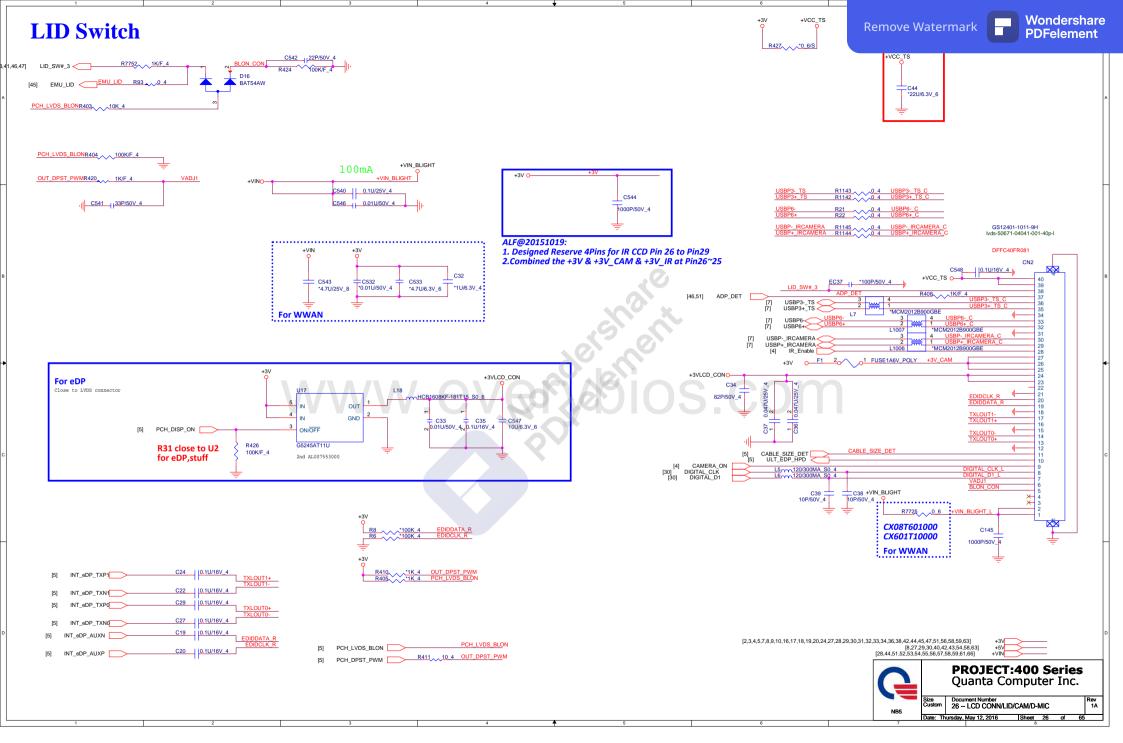


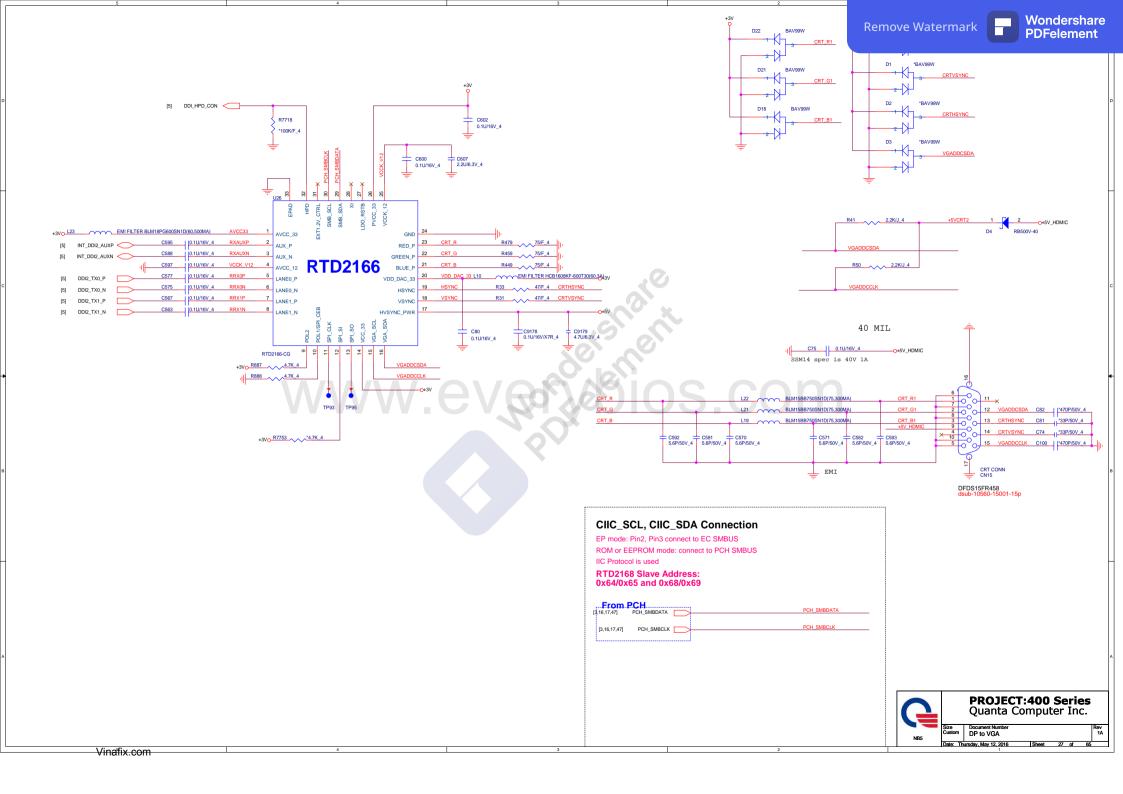


Hole

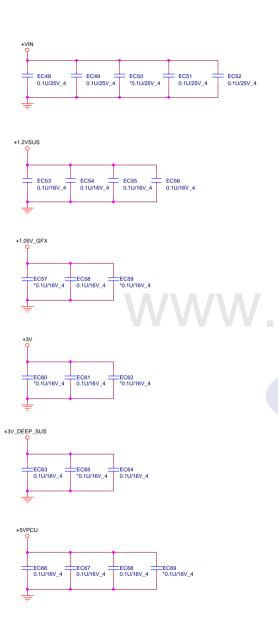




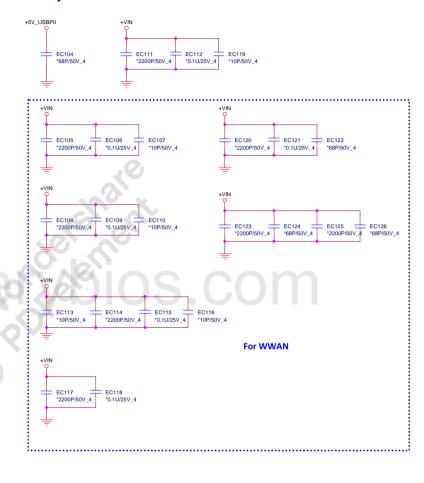


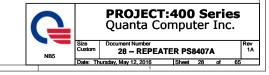


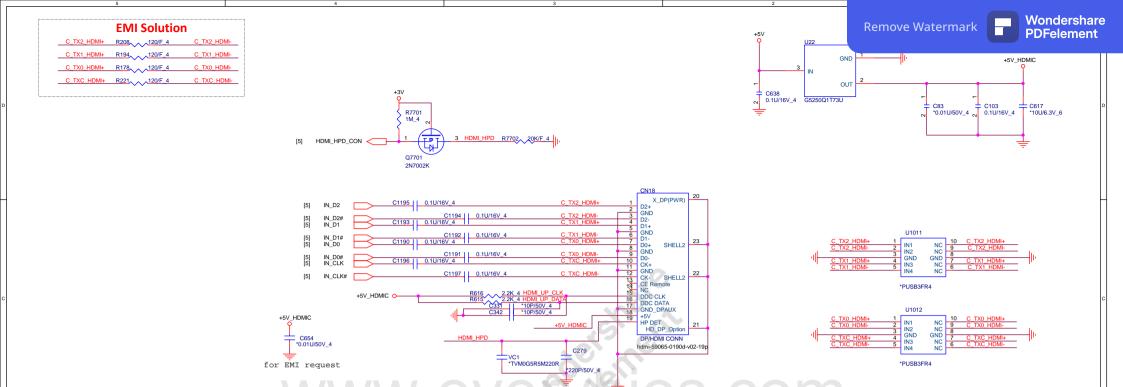
EMI CAP

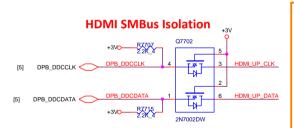


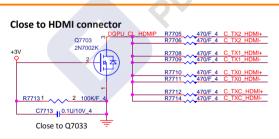
RF Cap

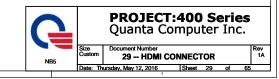


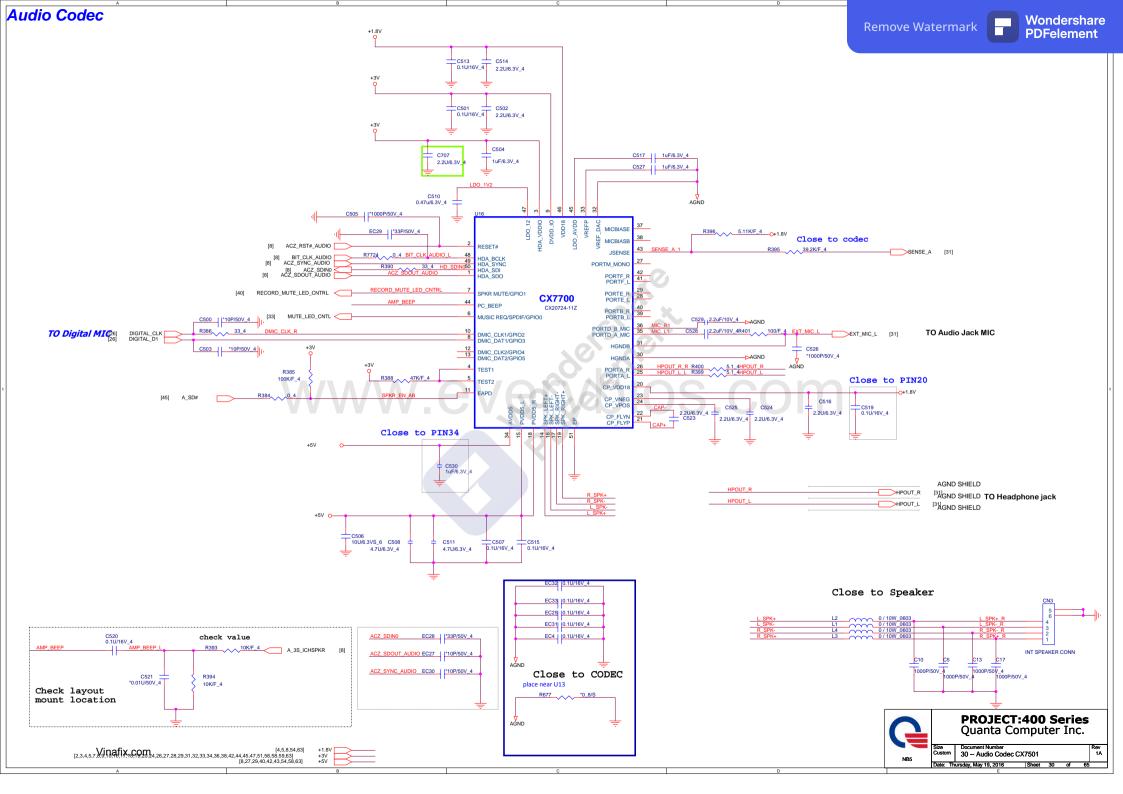




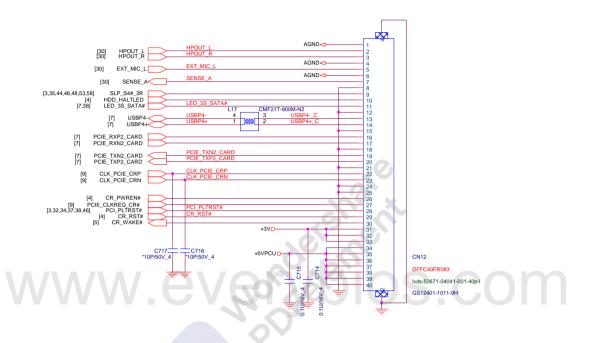




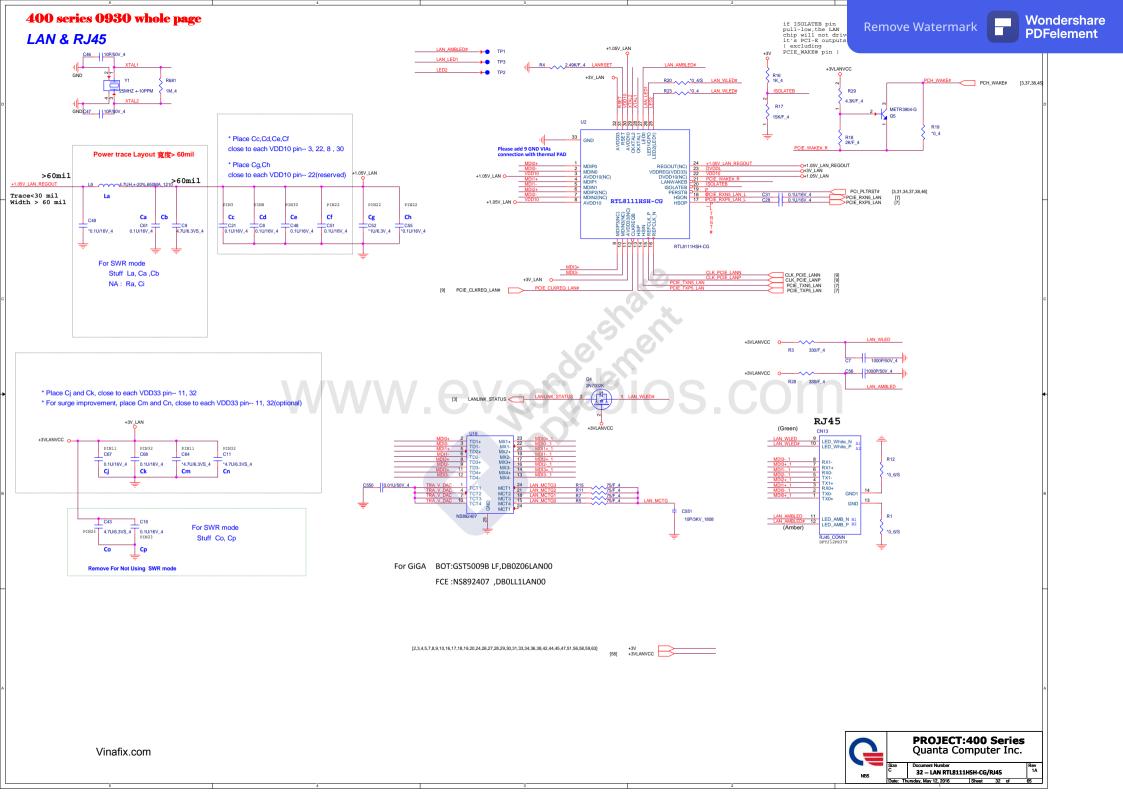


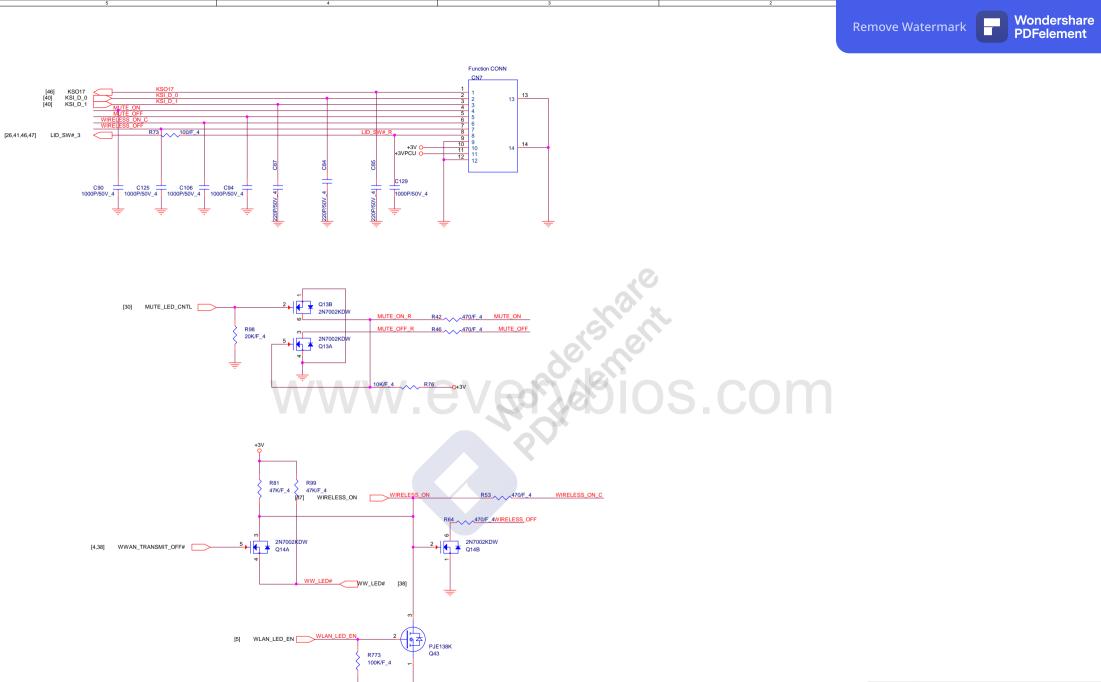


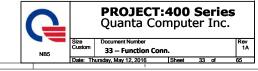
USB/Card Reader/Headphone_Mic Combo Jack Daugther Board Connector

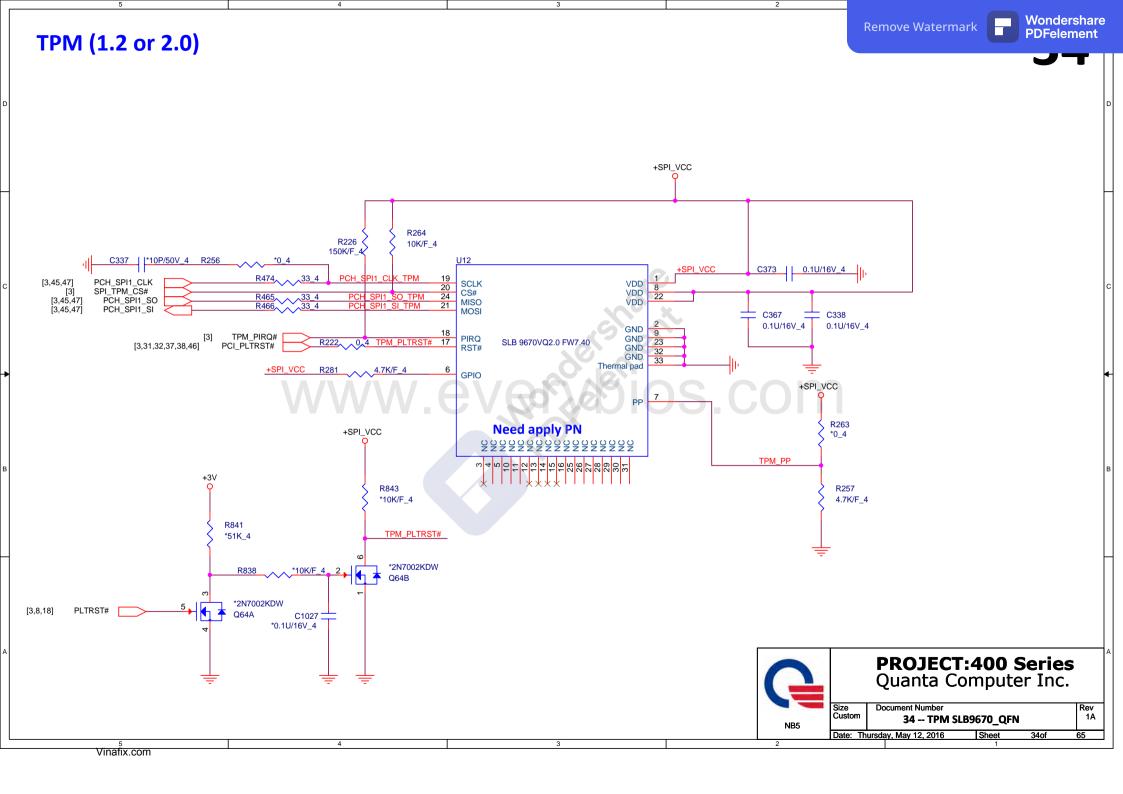




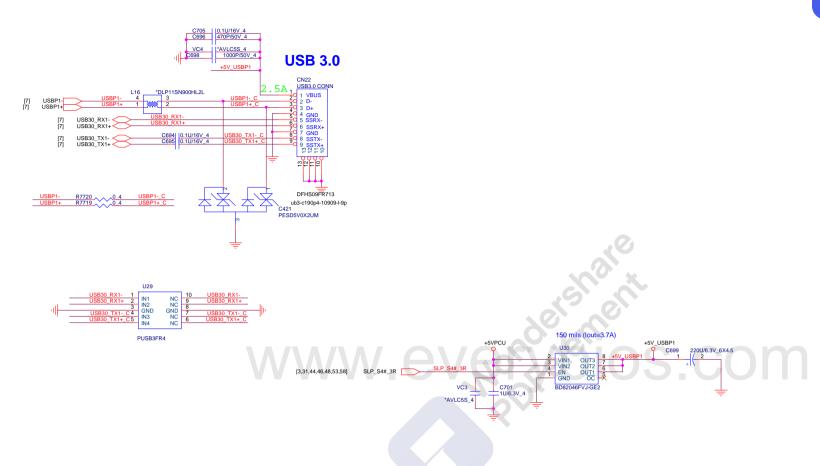












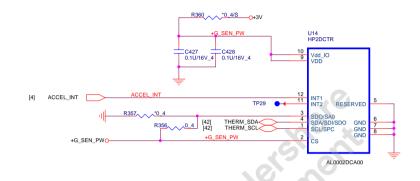
[28,31,44,49,50,51,52,53,54,56,57,58,59,60,61,63] [3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] +5VPCU +3VPCU



PROJECT:400 Series Quanta Computer Inc.

Size Custom	Document Number 35 USB3.0 x2				Rev 1A
Date: Tu	esday, May 17, 2016	Sheet	35	of	65
	1				

Accelerometer Sensor





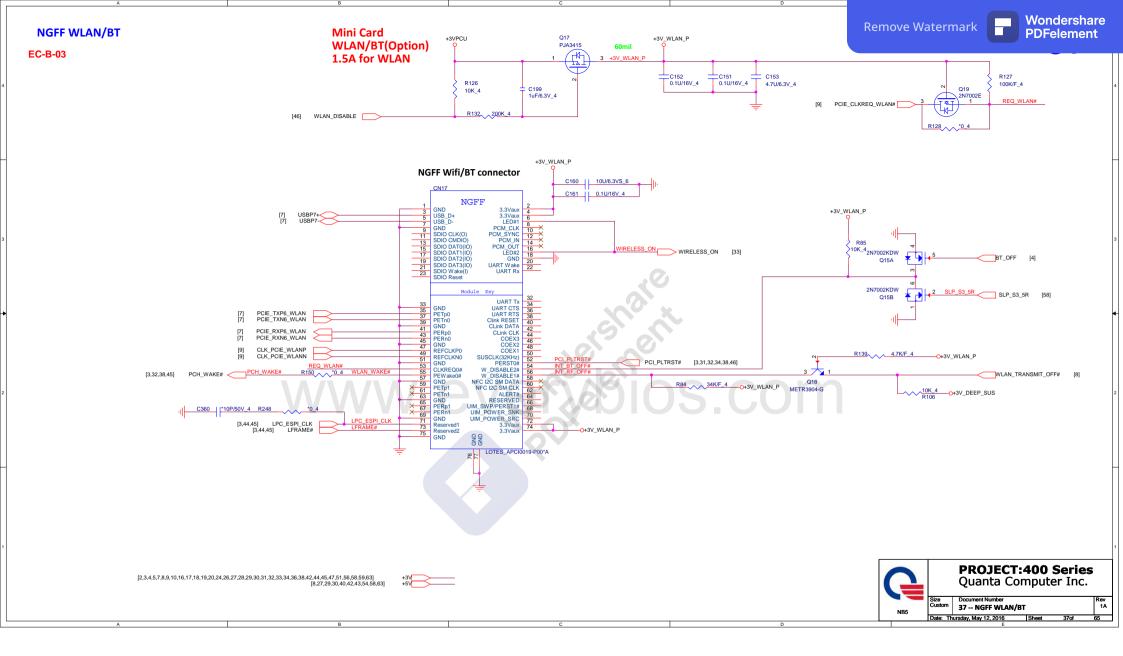
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,38,42,44,45,47,51,56,58,59,63]

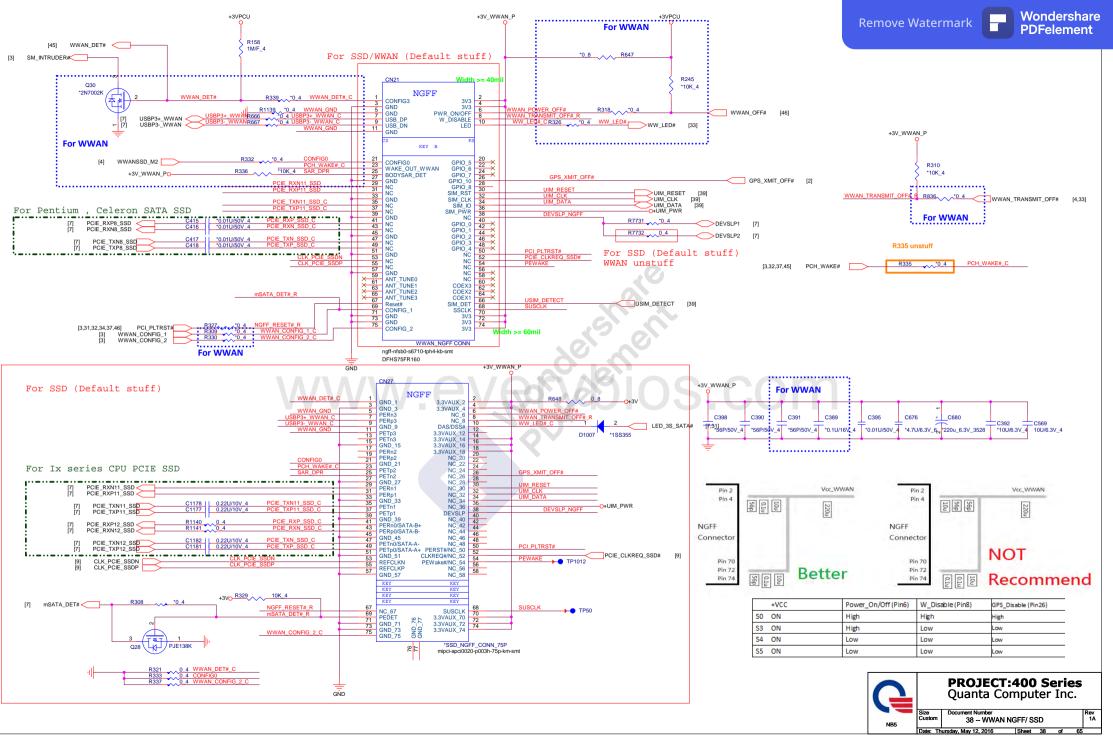
[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63]



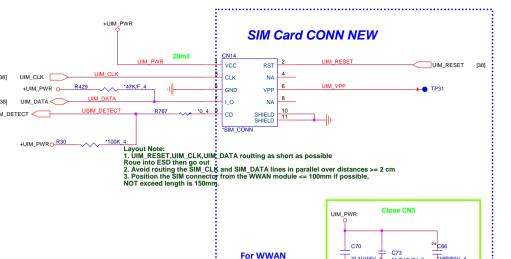


PROJECT:400 Series Quanta Computer Inc.





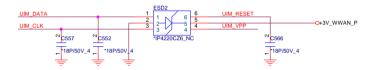




*0.1U/16V_4

.....

*4.7U/6.3V 6



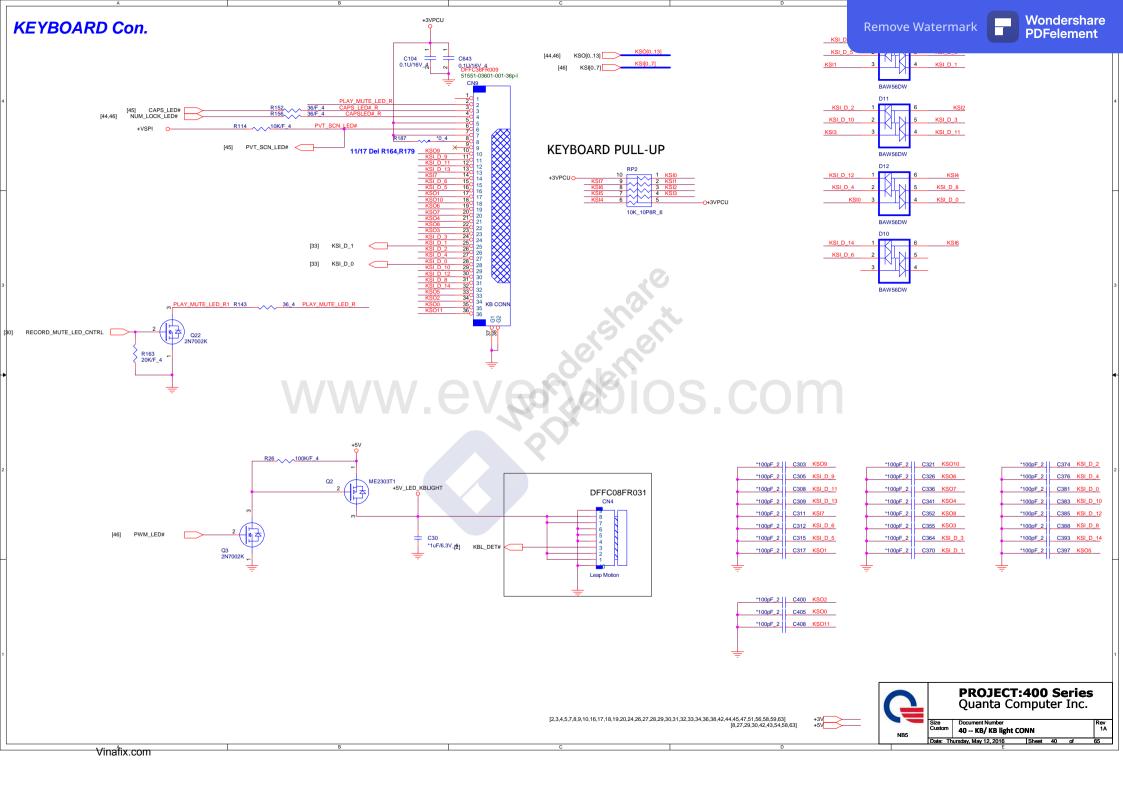
Trace Length and Routing

- Special attention should be paid to SIM traces (UIM CLK, UIM DATA and UIM RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues. Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM CLK and UIM DATA should be 20 mils. Static signals such as UIM RST can be routed between UIM CLK and UIM DATA to conserve space if needed.√
- . It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM CLK, UIM DATA and any other high-speed switching
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

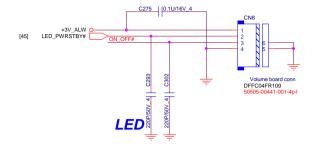
SIM Power ₽

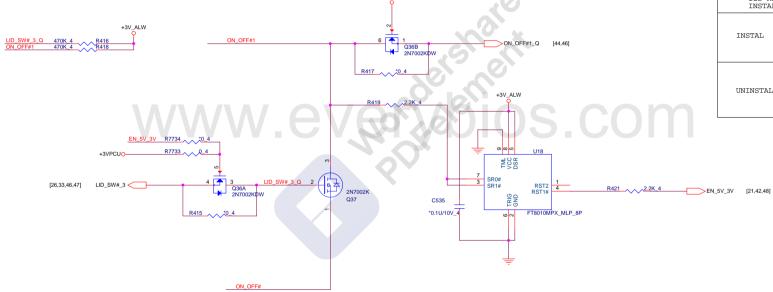
- The UIM PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM PWR supply and locate near the SIM connector.





Power Botton Connector





12S RESET MODE INSTAL FOR DB0				
INSTAL	R10702 R10704 R10701 U9068	R581		
UNINSTAL	R10754 Q7080	R10755 Q7081		

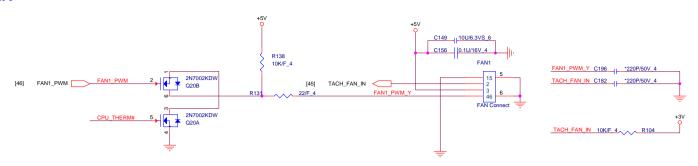




PROJECT:400 Series Quanta Computer Inc.

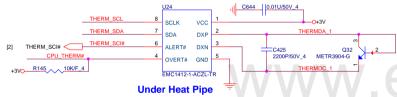
Rev 1A 41 -- Power Button/ HW Reset Date: Thursday, May 12, 2016





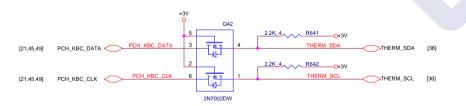
Thermal sensor

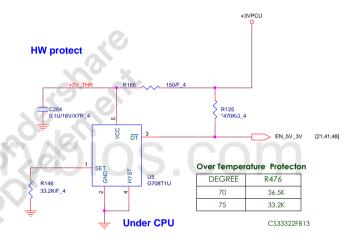




2nd:AL000431014 TMP431ADGKR

Main: AL000781012 G781P8(98h)





RSET (K OHM) = $0.0012T^2 - 0.9308T + 96.147$

[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,44,45,47,51,56,58,59,63] [9,41,48,51,52,58,62,63]





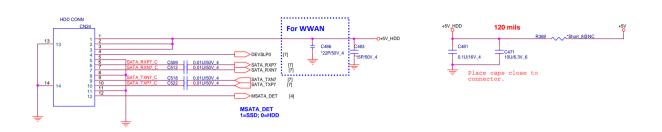
PROJECT:400 Series Quanta Computer Inc.

42-- FAN and Thermal IC Date: Thursday, May 19, 2016 | Sheet 42 of

Vinafix.com

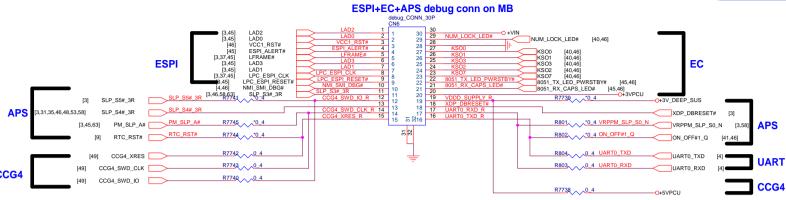
SATA-HDD



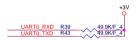


www.eversios.com







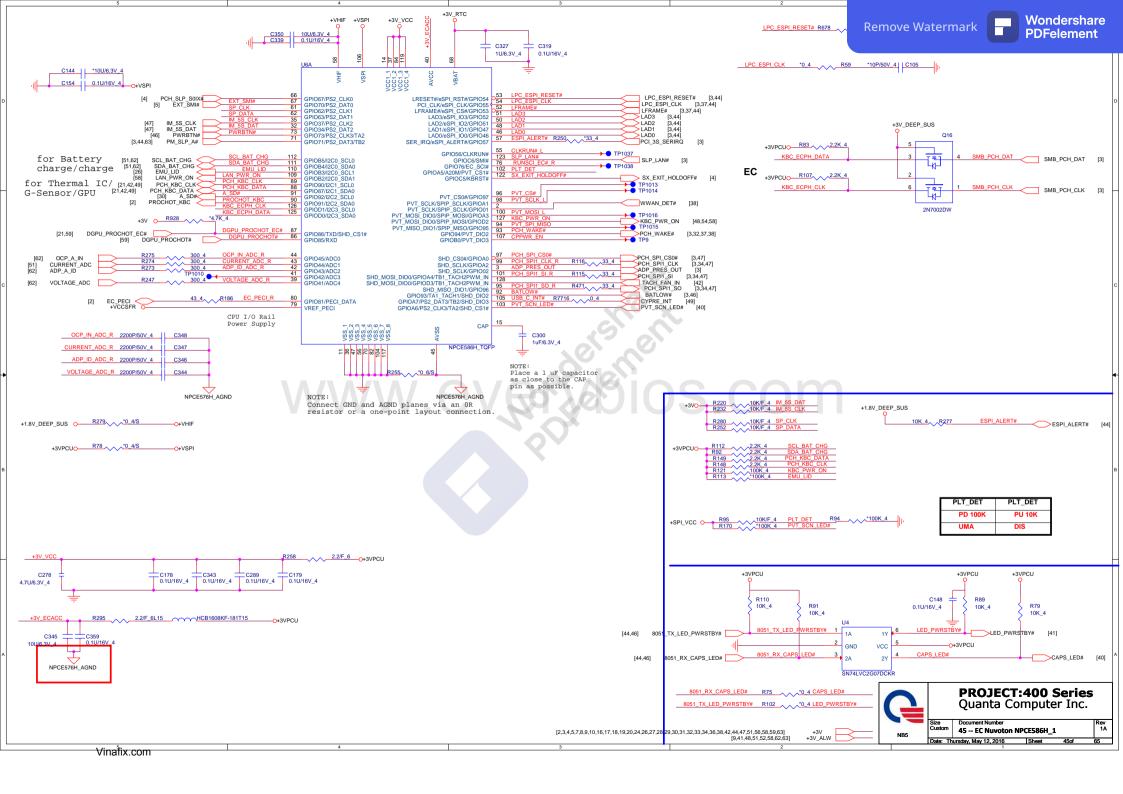


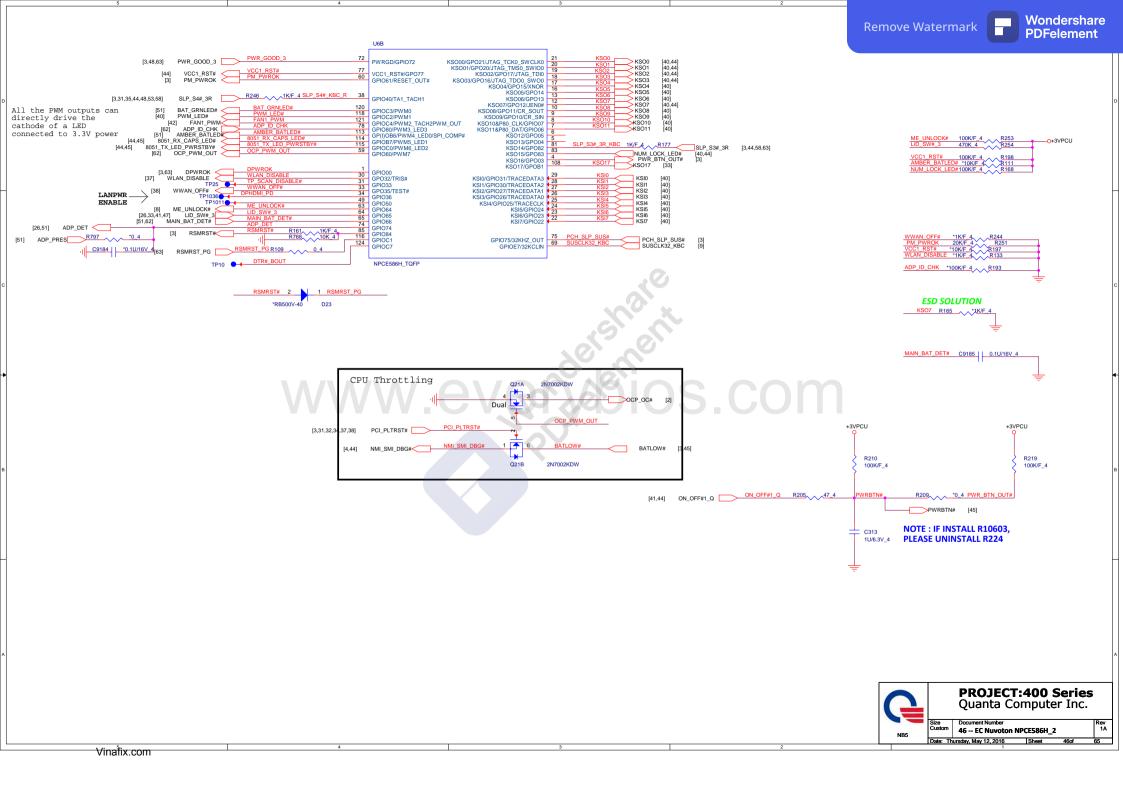
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R771	INSTAL	UNINSTAL
R769	UNINSTAL	INSTAL
R770	INSTAL	UNINSTAL

LPC & ESPI TABLE				
		LPC MODE	ESPI MODE	
R658	Ra	INSTAL	UNINSTAL	
R646	Rb	INSTAL	UNINSTAL	
R659	Rc	INSTAL	UNINSTAL	
R656	Rd	INSTAL	UNINSTAL	
R649	Re	INSTAL	UNINSTAL	
R657	Rf	INSTAL	UNINSTAL	
R249	Rg	INSTAL	UNINSTAL	
R147	Rh	INSTAL	UNINSTAL	
R120	Ri	INSTAL	UNINSTAL	
R276	Rj	INSTAL	UNINSTAL	
R678	Rk	UNINSTAL	INSTAL	

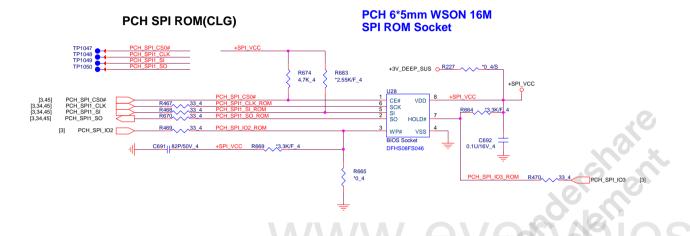
R538 10K 4 XDP_DBRESET#

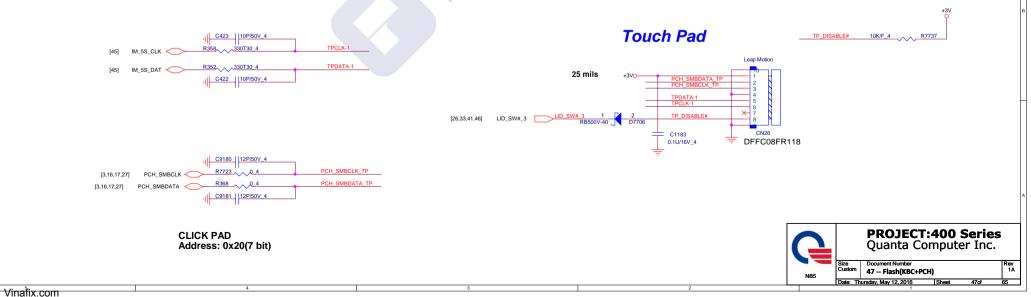


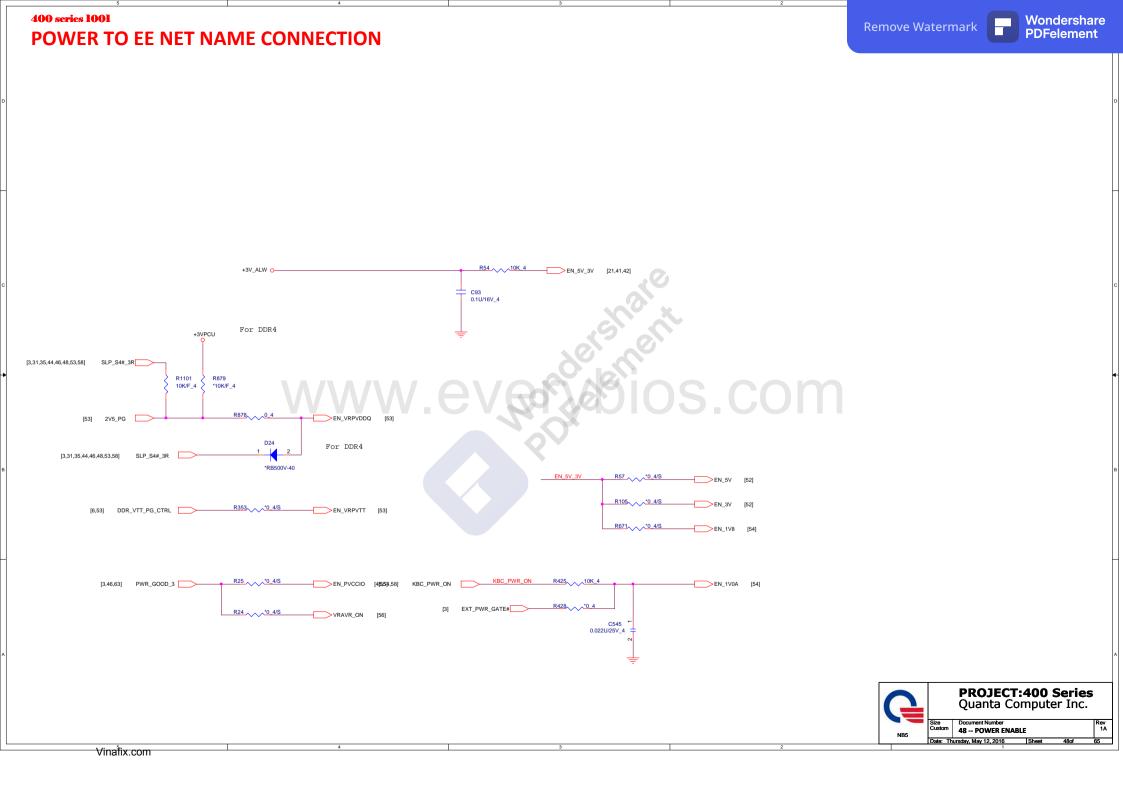


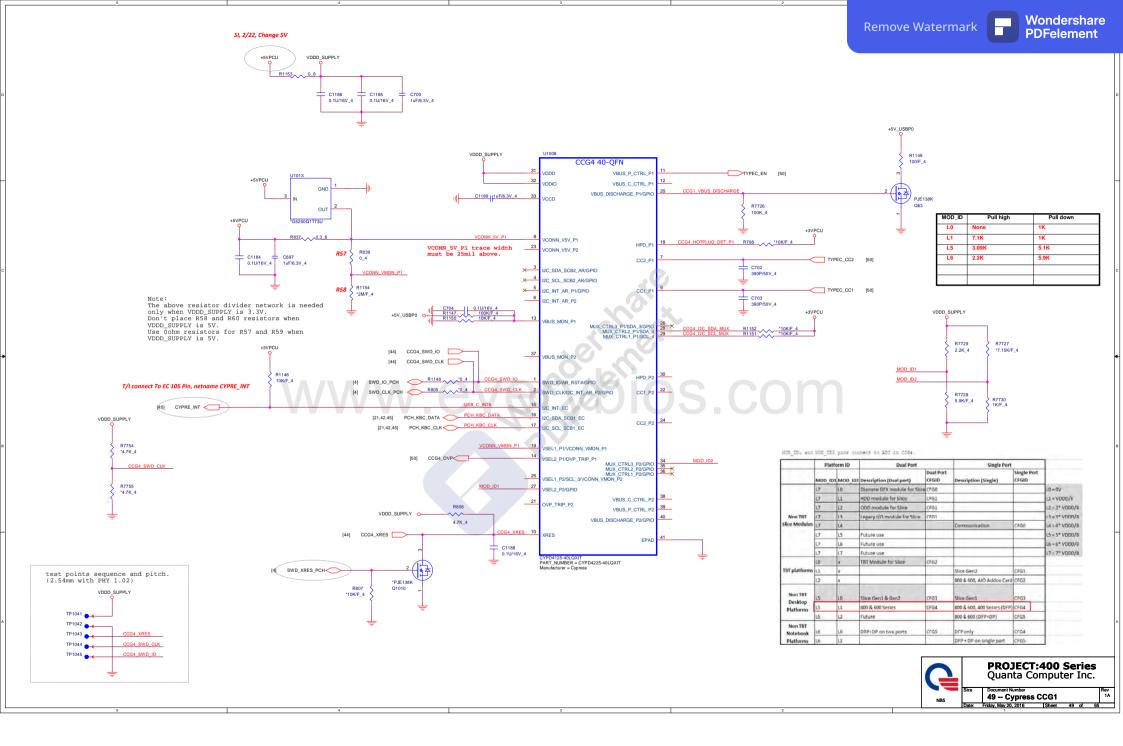


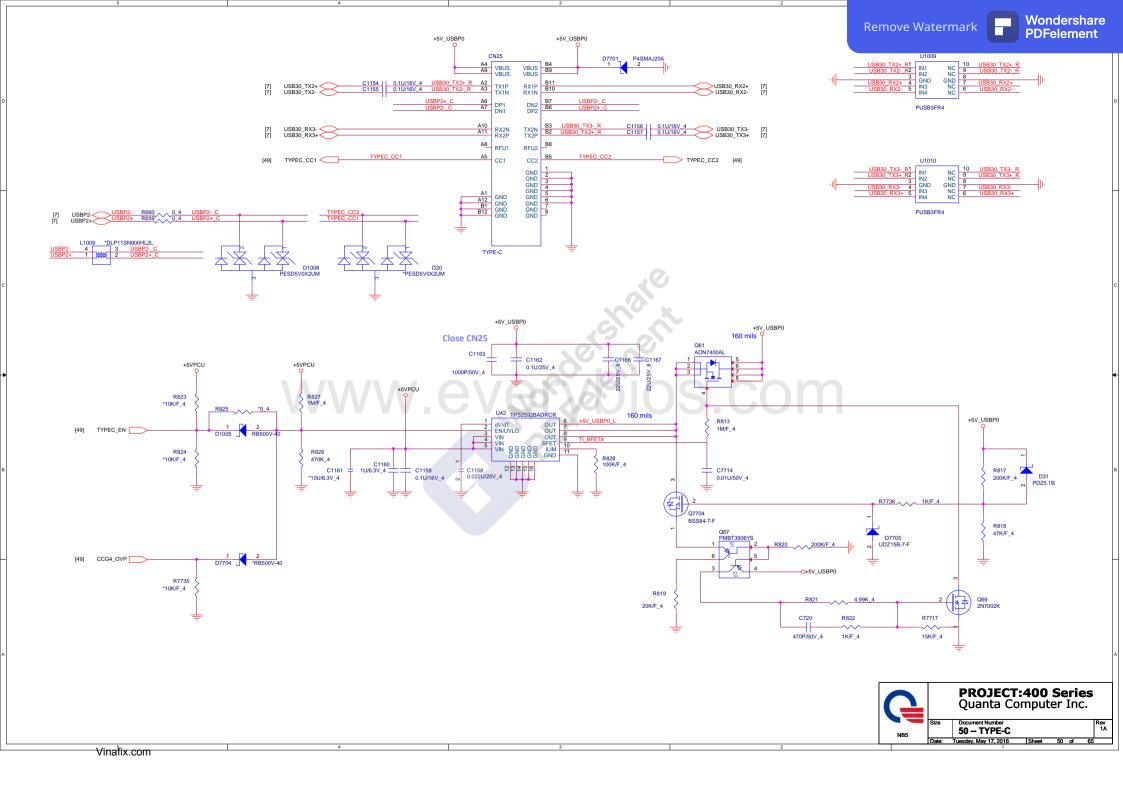
Vender	Size	P/N
GD	128MB	AKE2DF0KQ00
Winbond	128MB	AKE3DZNKN00
Socket		DFHS08FS046

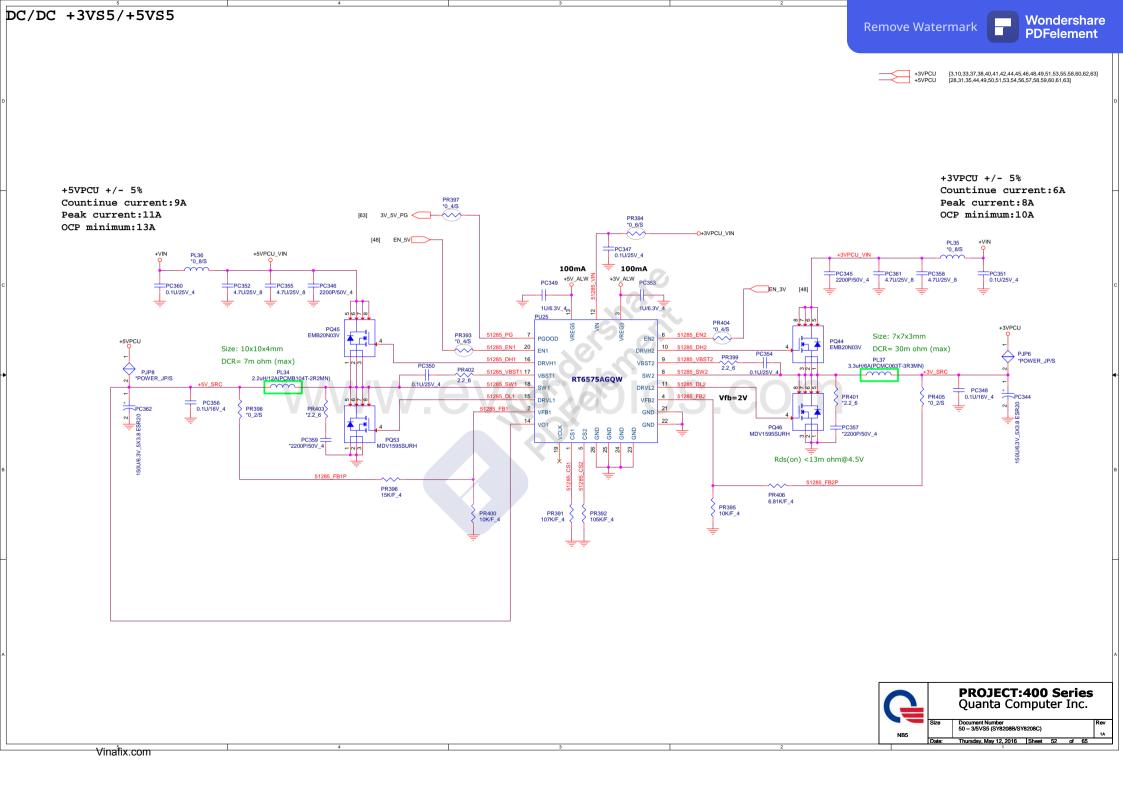


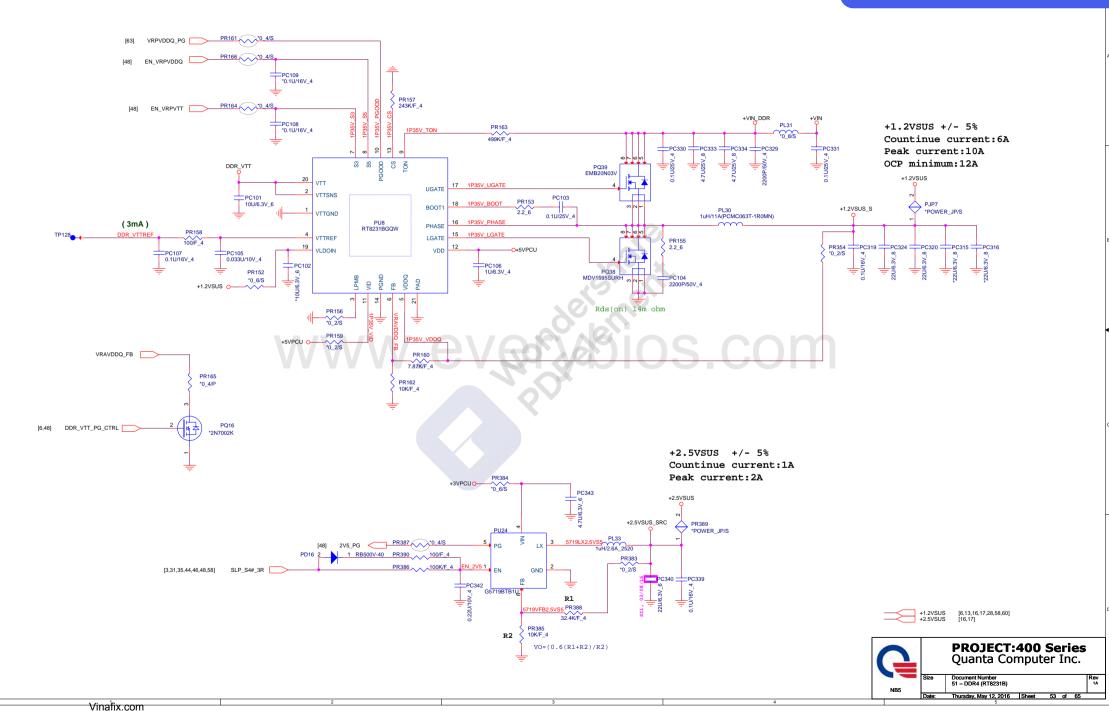




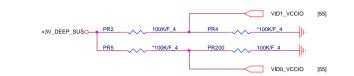


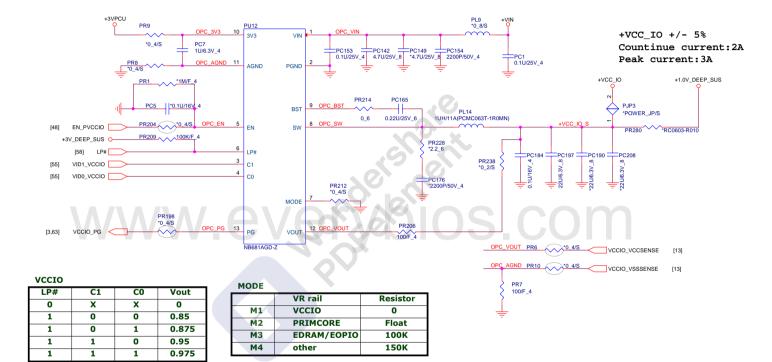


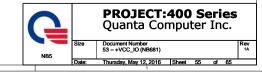




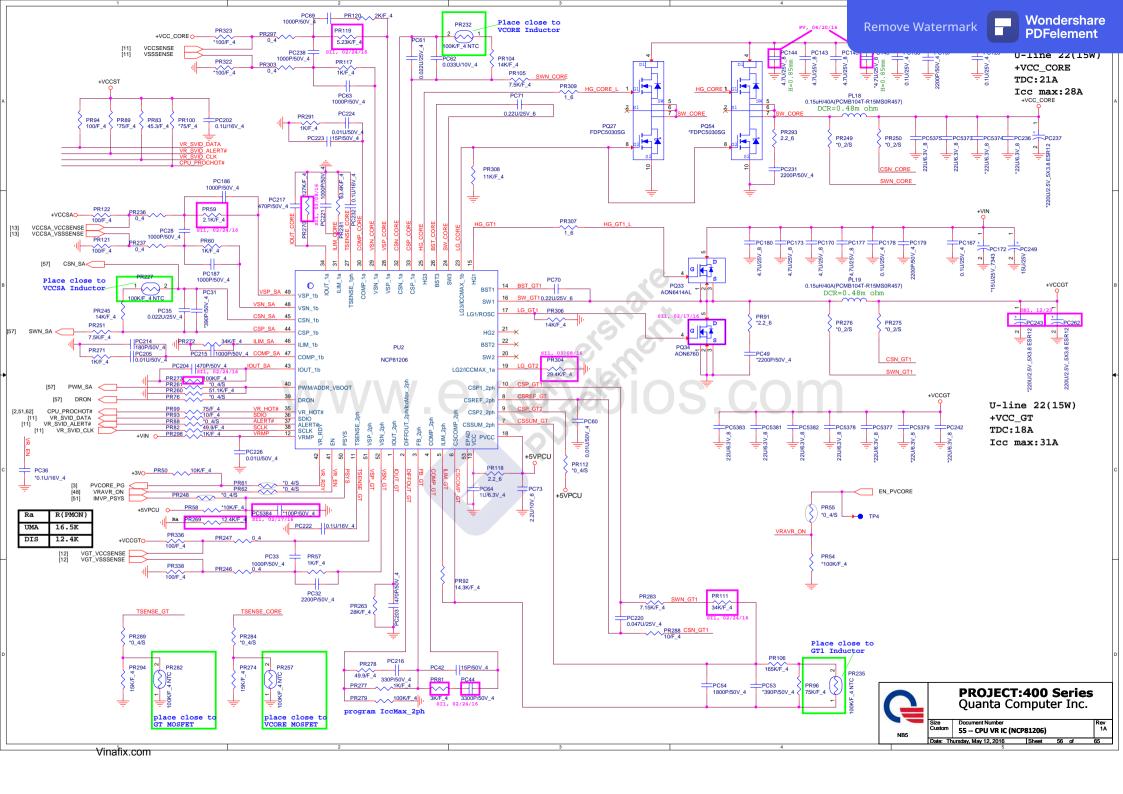
Vinafix.com





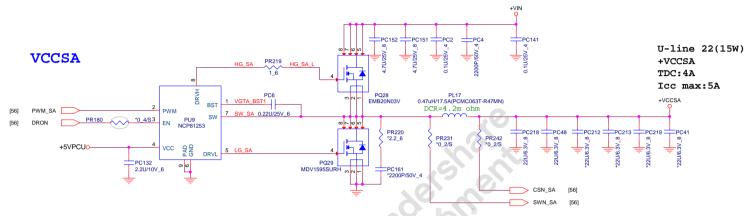


[26,28,44,51,52,53,54,56,57,58,59,61,66] +VIN [9,41,48,51,52,58,62,63] +3V_ALW +VCC_IO

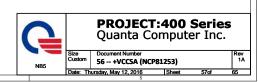


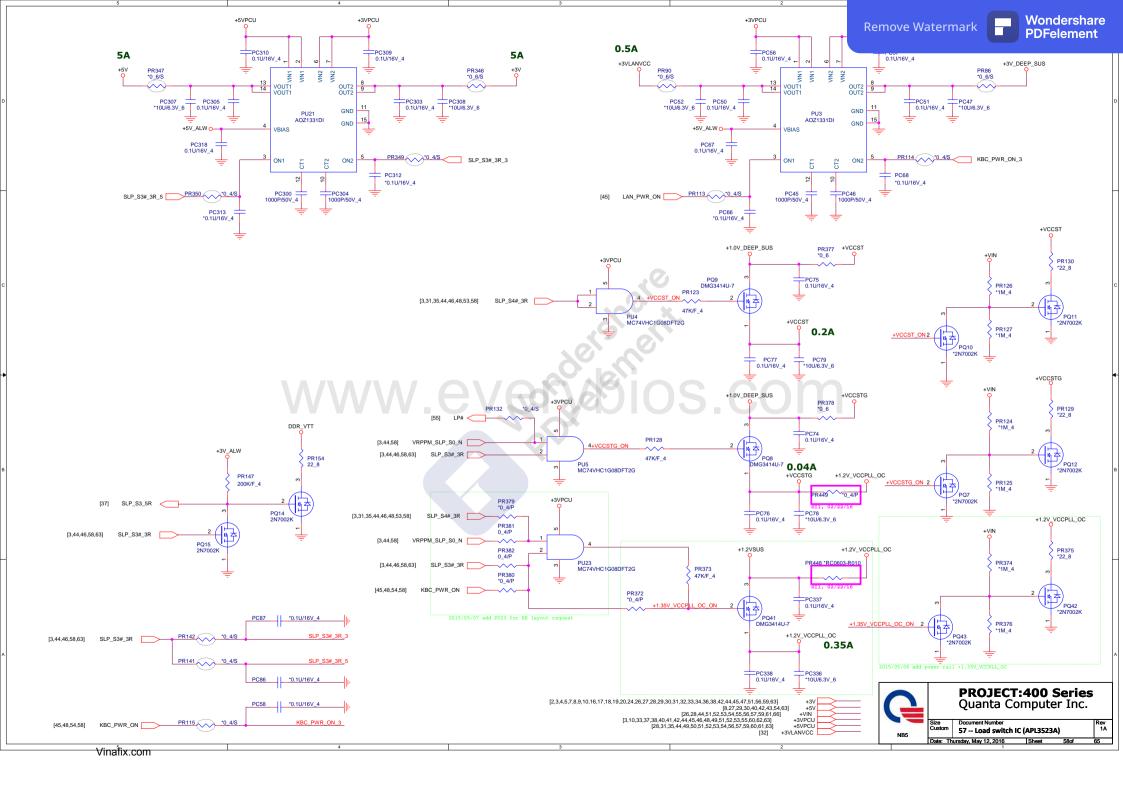


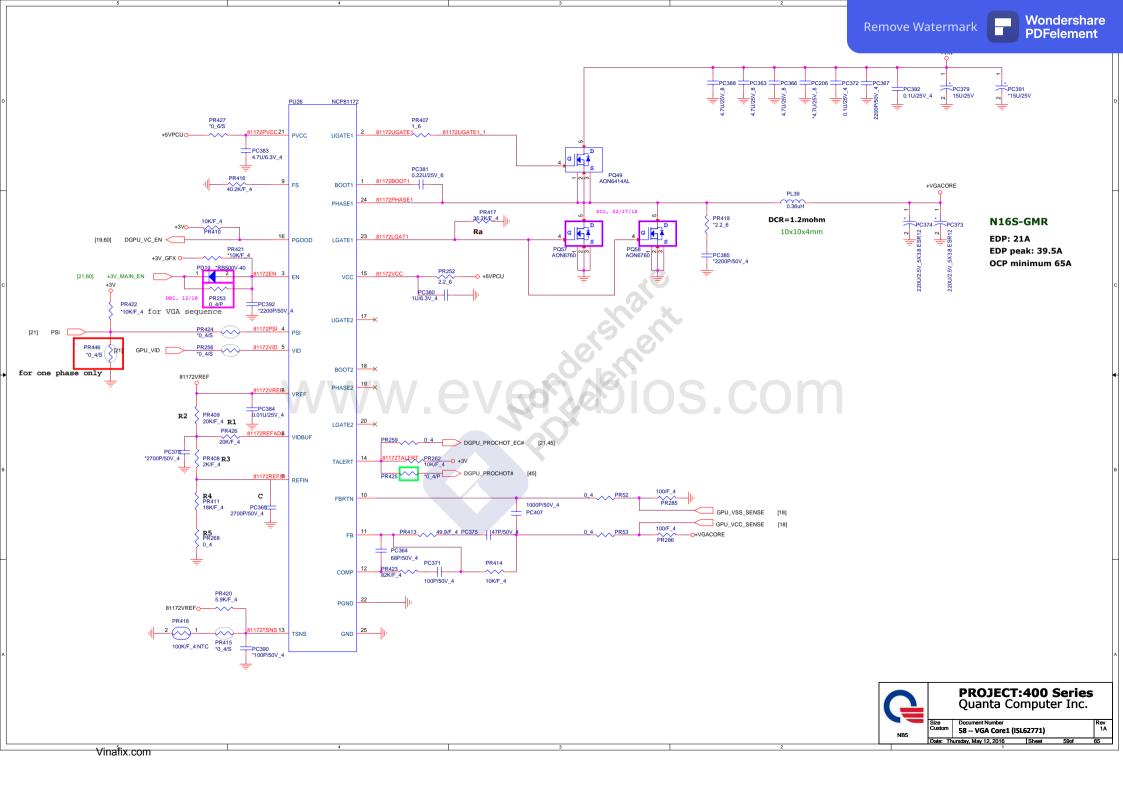




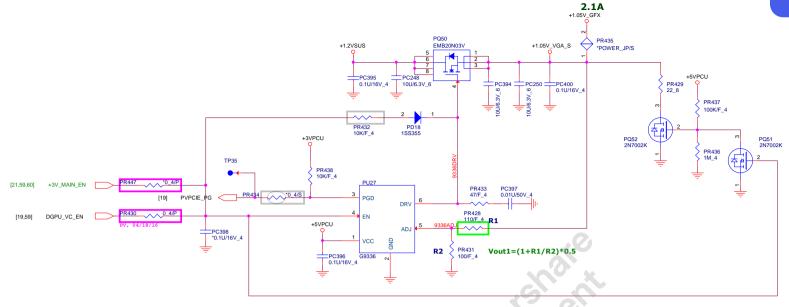
www.everagios.com

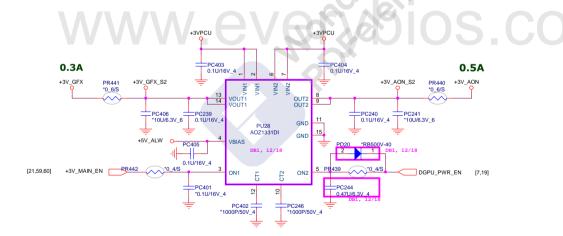


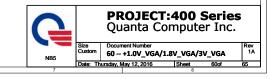


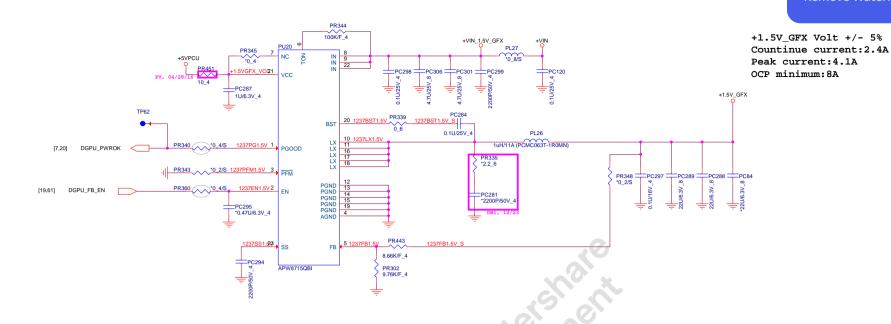


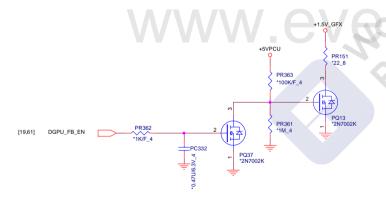




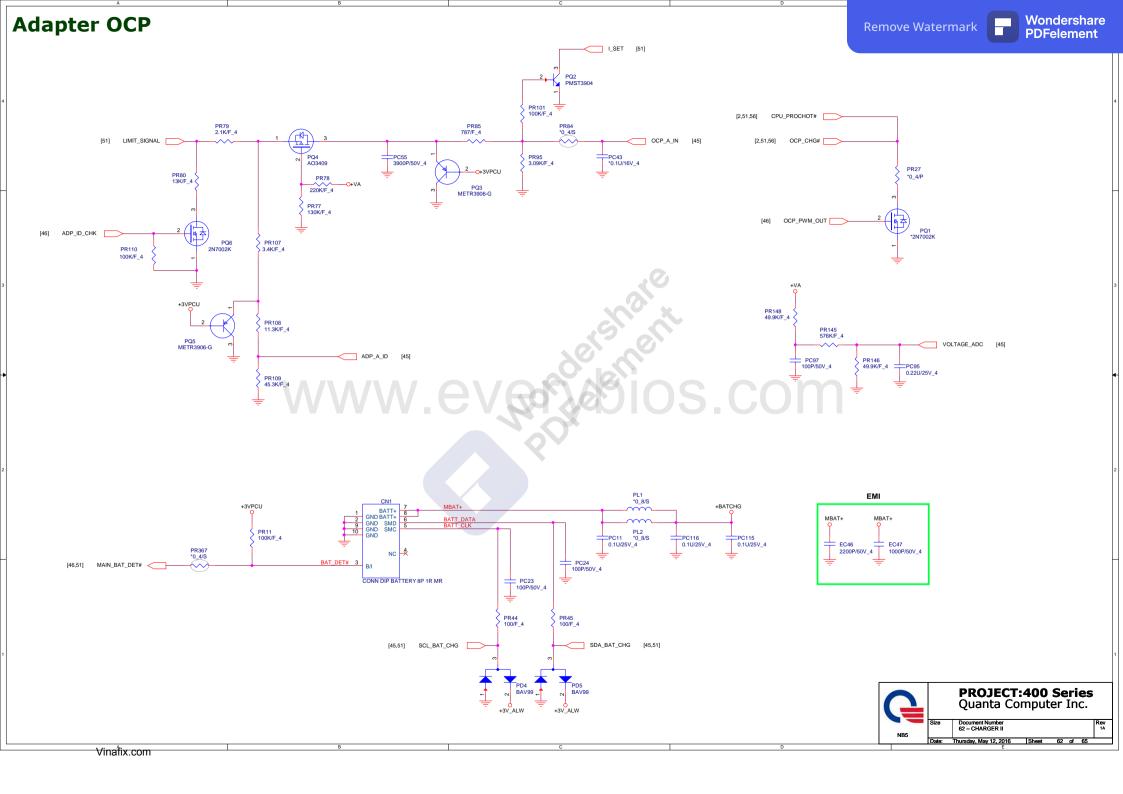












POK CKT

PM SLP S4# = SUSON PM_SLP_S3# = MAINON PR194 +V5S = +5V[3,55] VCCIO_PG +V3S = +3V 10K/F_4 +V0.75S =+0.75V_DDR_VTT PR97 115K/F_4 PR46 76.8K/F_4 PR311 51.1K/F 4 -O+3V_DEEP_SUS PR87 41.2K/F_4 PR318 28K/F_4 +1.8VO--O+1.8V_DEEP_SUS +3V AIW 3.3K/F_4 SI1, 02/17/16 1V8A_PG [54] PR98 3.3K/F_4 PR33 57.6K/F_4 PR305 3.3K/F_4 VRPVDDQ_PG PR32 31.6K/F_4 1V0A_PG [54] PR36 10K/F_4 PR296 10K/F_4 PR301 *3.3K/F_4 [3,44,46,58] SLP_S3#_3R PC17 PR102 3.3K/F_4 1 2 1000P/50V_4 VCC_PRIM_PG [54] PM_SLP_A# [3,44,45] PR48 = 18.7K/F_4 PR313 22.6K/F_4 PC18 PC245 0.22U/25V_4 3300P/50V_4 +5VPCU PU14B AS393MTR-G1 PR290 1M/F_4 PR41 1M/F_4 PR47 20K/F 4 PR295 20K/F_4 -O+3V_DEEP_SUS [3,46,48] PWR_GOOD_3 RSMRST_PG [46] PC88 *0.01U/50V_4 +3VPCU +3V_ALW PR140 100K/F 4

TC7SZ07FU

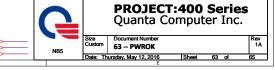
[52] 3V_5V_PG PR139 100/F

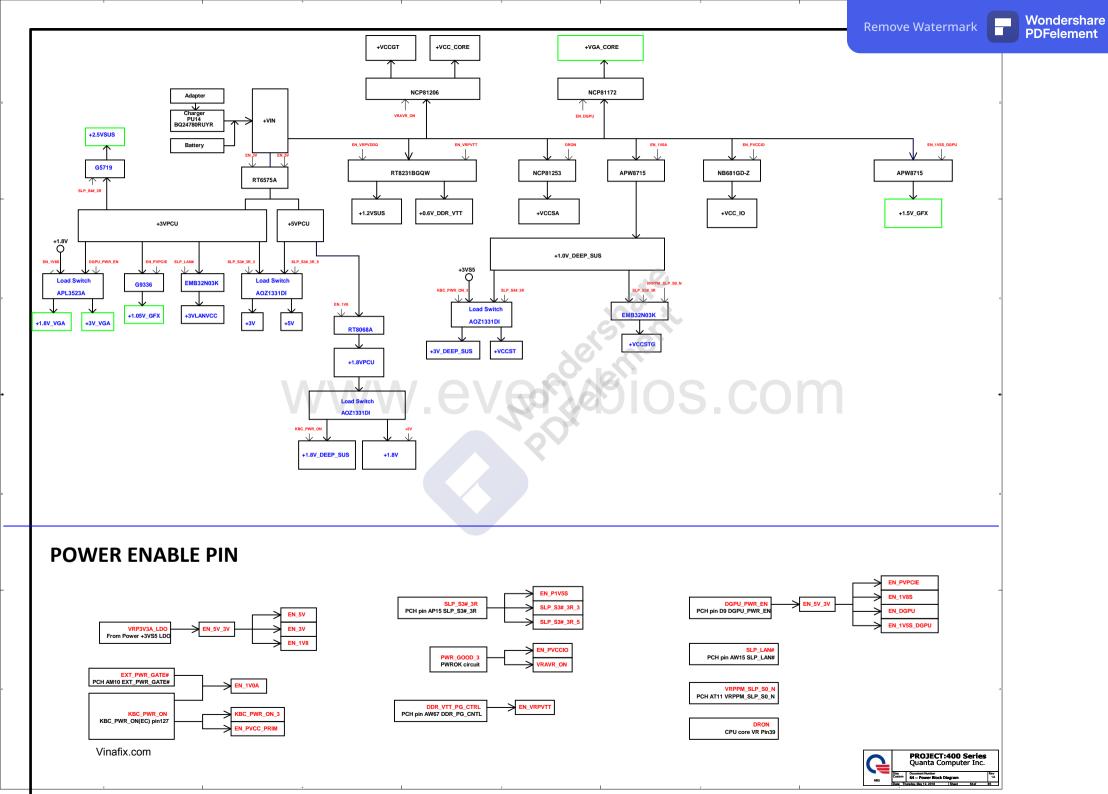
PC85 1U/6.3V_4 PR138 10K/F_4 O+3VPCU

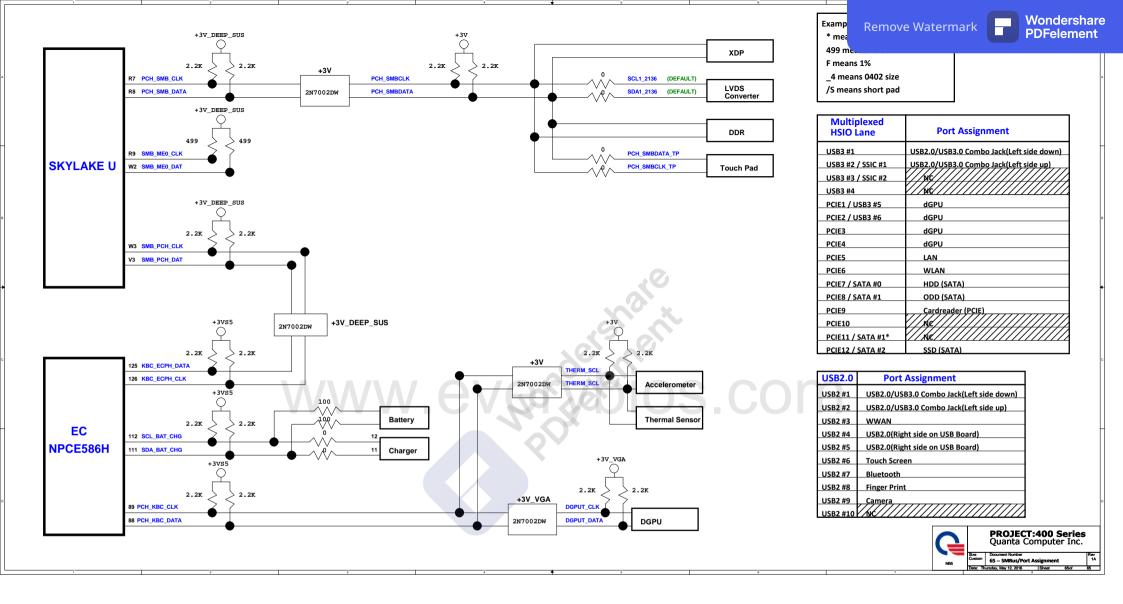
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59] [8,27,29,30,40,24,35,44,58] [8,41,48,51,52,56,62] *3

> DPWROK

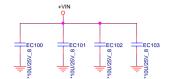
+3V_ALW











www.everlagios.com

