ClockConfigure online generates code not supported in the IDE

R rtek1000 - General Member, Oct 17, 2025 | 0 32 5

Hello,

I'm trying to create a program to operate with ADC and UART, but I'm still stuck on the Clock.

ClockConfigure online generates code not supported in the IDE

IC: M452LD3AE

Code:

```
CLK->PCLKDIV = (CLK_PCLKDIV_APB0DIV_DIV1 | CLK_PCLKDIV_APB1DIV_DIV1);
```

Errors:

> ../User/main.c:192:10: error: 'CLK_T' has no member named 'PCLKDIV'; did you mean 'CLKDIV0'?
> 192 | CLK->PCLKDIV = (CLK_PCLKDIV_APB0DIV_DIV1 | CLK_PCLKDIV_APB1DIV_DIV1);
> | ^~~~~~~
> | CLKDIV0
> ../User/main.c:192:21: error: 'CLK_PCLKDIV_APB0DIV_DIV1' undeclared (first use in this function)
> 192 | CLK->PCLKDIV = (CLK_PCLKDIV_APB0DIV_DIV1 | CLK_PCLKDIV_APB1DIV_DIV1);
> | ^~~~~~~~~~~~~~~~~~~~~~~~~
> ../User/main.c:192:21: note: each undeclared identifier is reported only once for each function it appears in
> ../User/main.c:192:48: error: 'CLK_PCLKDIV_APB1DIV_DIV1' undeclared (first use in this function)
> 192 | CLK->PCLKDIV = (CLK_PCLKDIV_APB0DIV_DIV1 | CLK_PCLKDIV_APB1DIV_DIV1);

Is there any file (manual) that can help me know what the right reference is?

0

Reply

If you want to use ADC, you could use this sample code directly.

https://github.com/OpenNuvoton/M451BSP/blob/master/SampleCode/StdDriver/EADC_SWTRG_Trigger/main.c

In addition, the correct code is as below:

CLK->CLKSEL0 = CLK->CLKSEL0 & (~CLK_CLKSEL0_PCLK0SEL_Msk) | CLK_CLKSEL0_PCLK0SEL_HCLK_DIV2

CLK->CLKSEL0 = CLK->CLKSEL0 & (~CLK_CLKSEL0_PCLK1SEL_Msk) | CLK_CLKSEL0_PCLK1SEL_HCLK_DIV2

C chhuang16
Replied Oct 19, 2025

1

Hello, I've managed to make some progress based on the GPIO_OutputInput example using the internal clock.

- I managed to get a pin to blink.
- I managed to get UART1 to send data.

But I'm having trouble getting the external clock to work.

- Note: the example is pre-configured for an external clock with a 12MHz crystal. But I need to configure it for 16MHz and only clock input. It's not a crystal, but an external oscillator that delivers the signal only to the XT1_IN pin. The XT1_OUT pin is left unused.

I made some modifications to the files:

system_M451Series.h (Original):

```
#define __HSI       (12000000UL)    /*!< PLL default output is 72MHz */
#define __HXT       (12000000UL)    /*!< External Crystal Clock Frequency     */
```

system_M451Series.h (New):

```
#define __HSI       (16000000UL)    /*!< PLL default output is 72MHz */
#define __HXT       (16000000UL)    /*!< External Crystal Clock Frequency     */
```

ckl.h Original (12MHz):

#define CLK_PLLCTL_72MHz_HXT (CLK_PLLCTL_PLLSRC_HXT | CLK_PLLCTL_NR(2) | CLK_PLLCTL_NF(48) | CLK_PLLCTL_NO_4) /*!< Predefined PLLCTL setting for 72MHz PLL output with HXT(12MHz X'tal) */

ckl.h New (16MHz):

#define CLK_PLLCTL_72MHz_HXT (CLK_PLLCTL_PLLSRC_HXT | CLK_PLLCTL_NR(2) | CLK_PLLCTL_NF(36) | CLK_PLLCTL_NO_4) /*!< Predefined PLLCTL setting for 72MHz PLL output with HXT(16MHz X'tal) */

The code compiles without error, but processing hangs at this part:

```
/* Wait for HXT clock ready */
CLK_WaitClockReady(CLK_STATUS_HXTSTB_Msk);
```

Perhaps I need to configure the use of only the XT1_IN input pin.

Could you help me configure this external clock part?

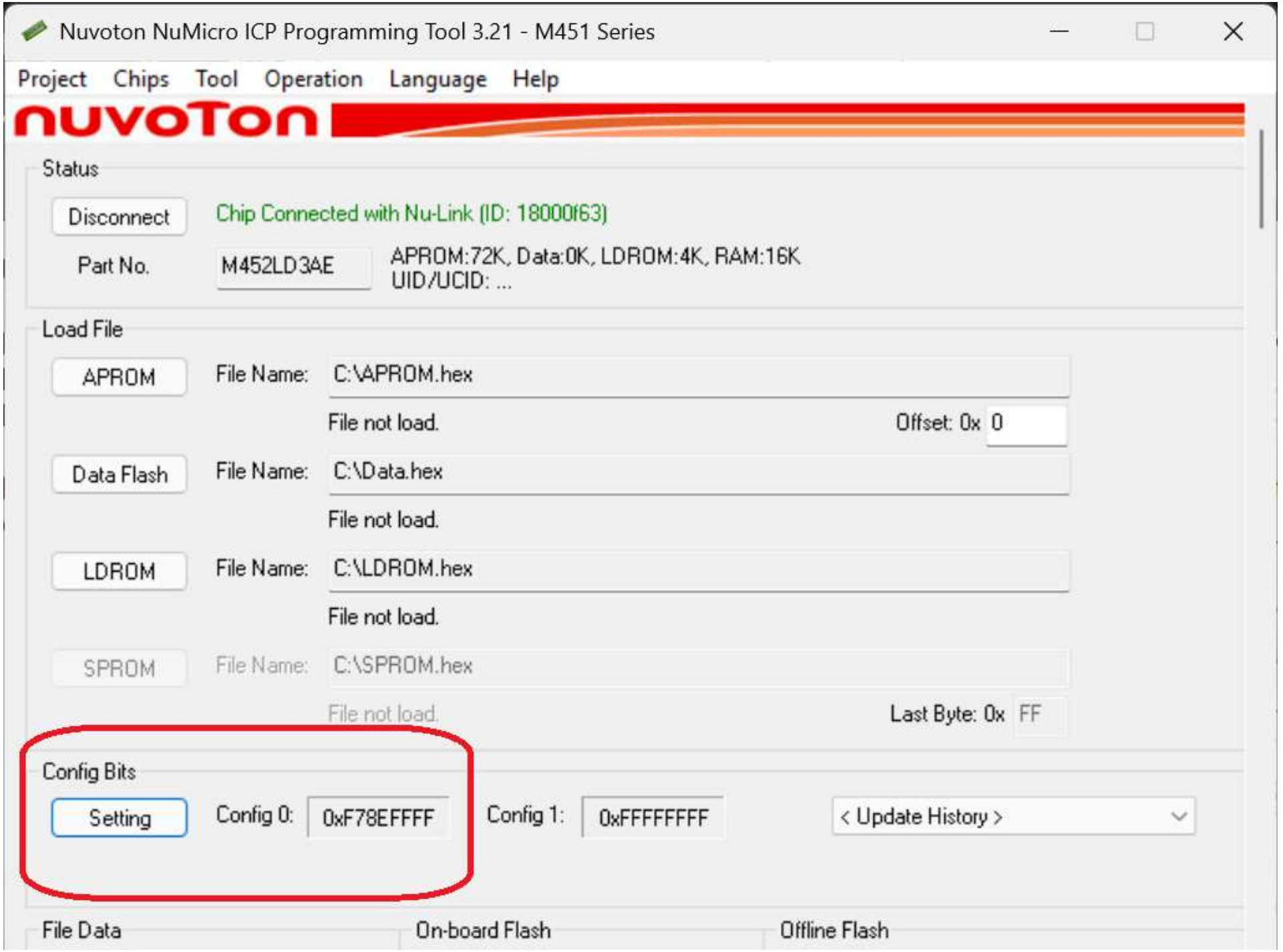
R rtek1000
Replied Oct 22, 2025

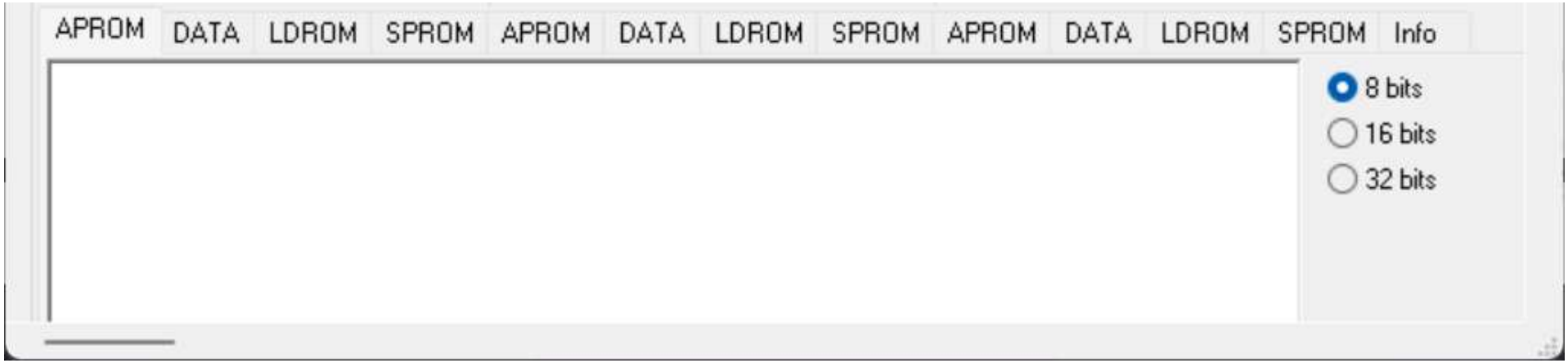
0

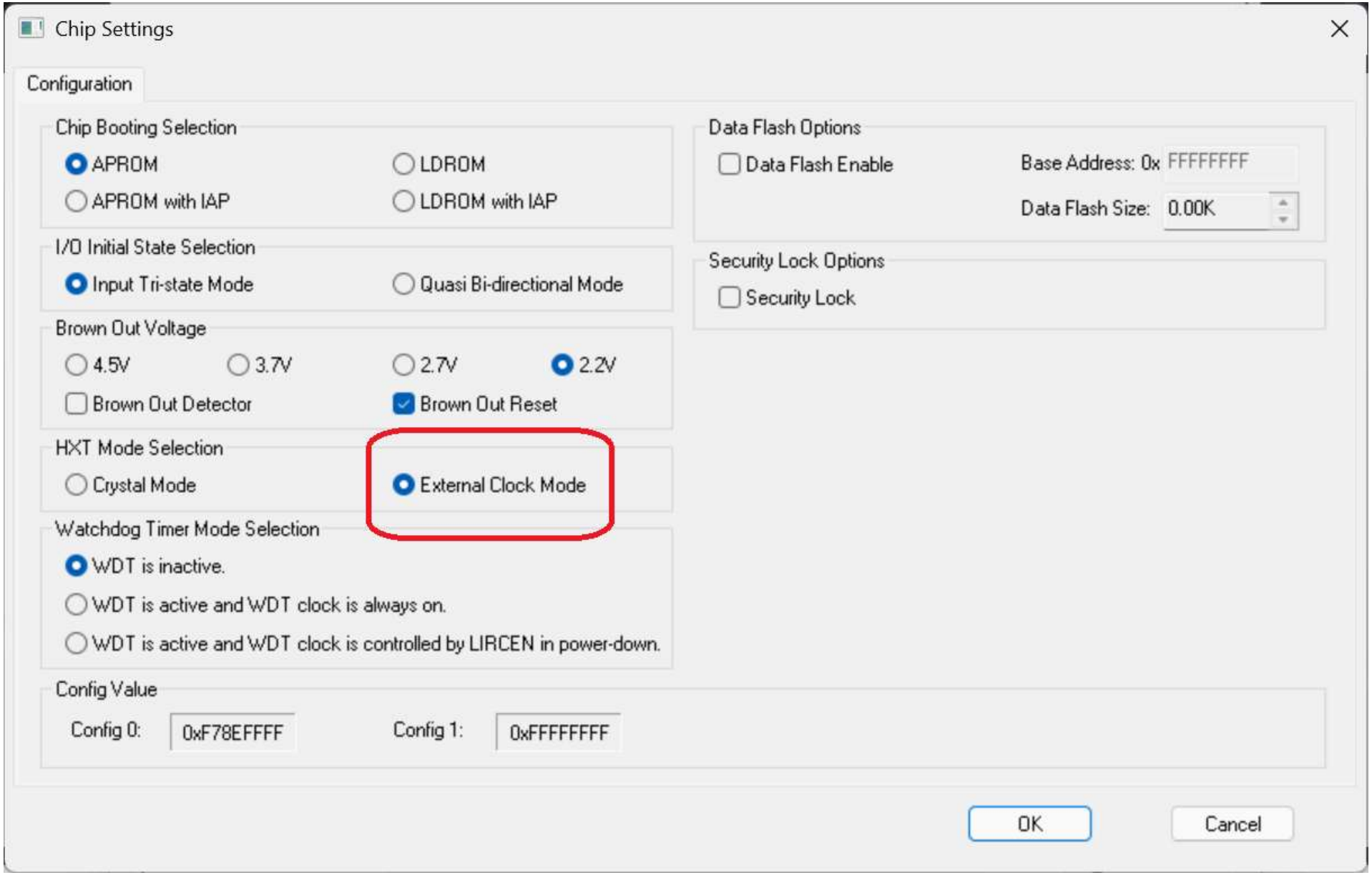
I found a setting in the ICP programming tool for the Config_0 register: HXT Mode Selection. Even though I left it set to External Clock Mode, it still doesn't work. Configuration 0 was confirmed via command line:

>nulink.exe -r CFG0

> >>> Start to read CFG.
> 0%
> Config 0: 0xF78EFFFF
> 100%
> >>> Read CFG finish.
>
> ********** Execute operation ending **********


Nuvoton NuMicro ICP Programming Tool 3.21 - M451 Series
Project
Chips
Tool
Operation
Language
Help
nuvoTon
Status
Disconnect
Chip Connected with Nu-Link (ID: 18000f63)
Part No.
M452LD3AE
APROM:72K, Data:0K, LDROM:4K, RAM:16K
UID/UCID: ...
Load File
APROM
File Name:
C:\APROM.hex
File not load.
Offset: 0x 0
Data Flash
File Name:
C:\Data.hex
File not load.
LDROM
File Name:
C:\LDROM.hex
File not load.
SPROM
File Name:
C:\SPROM.hex
File not load.
Last Byte: 0x FF
Config Bits
Setting
Config 0:
0xF78EFFFF
Config 1:
0xFFFFFFFF
< Update History >
File Data
On-board Flash
Offline Flash


APROM
DATA
LDROM
SPROM
APROM
DATA
LDROM
SPROM
APROM
DATA
LDROM
SPROM
Info
8 bits
16 bits
32 bits



R rtek1000
Replied Oct 22, 2025

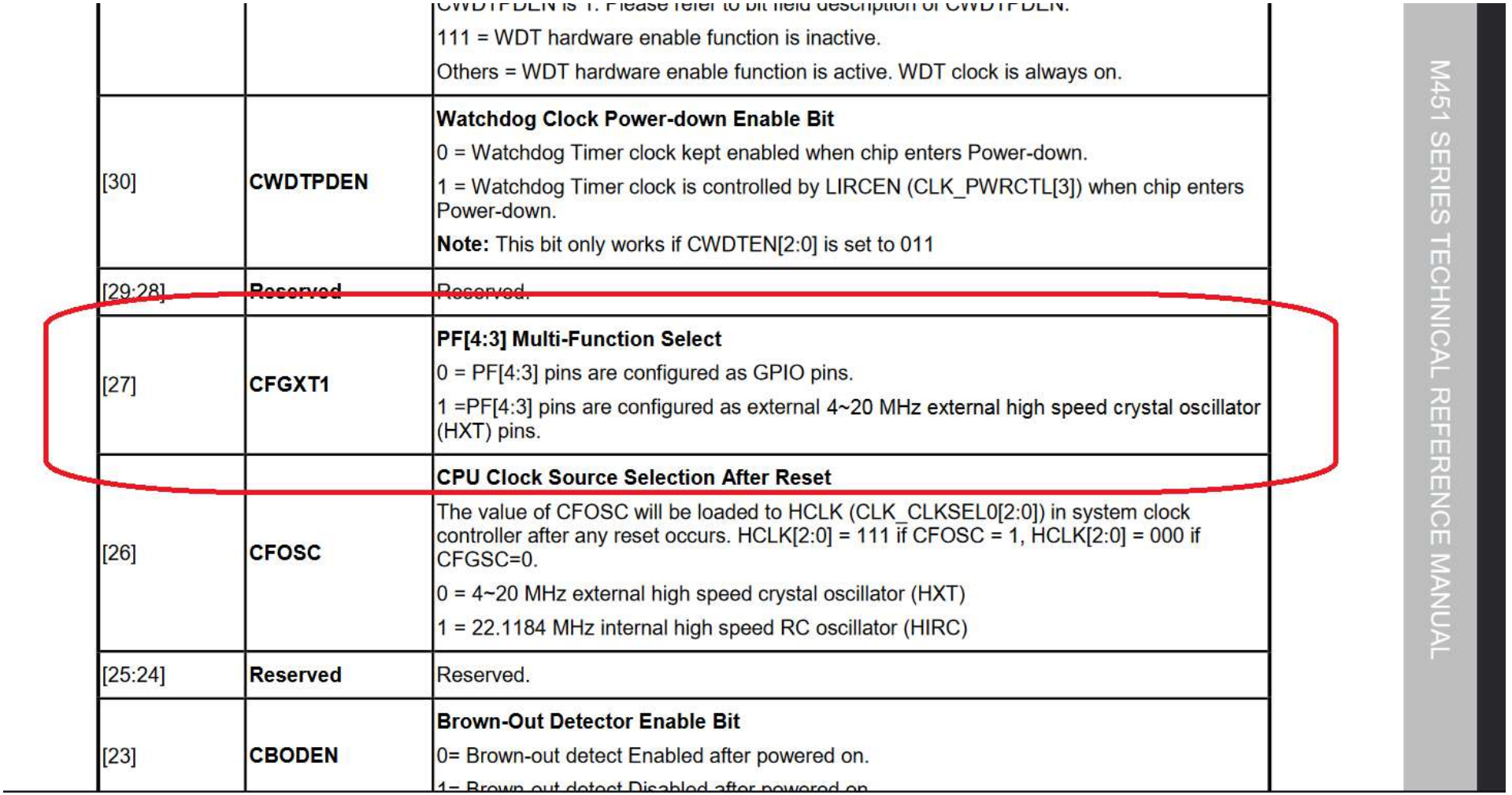
0

Ok, I understood what was happening. The first time I tried to program the M452, I had left the wrong bit selected.

Contrary to what the ICP program led me to believe, this BIT27 setting is not for using an external oscillator (value 0), but rather for using the crystal pins for general use.

By leaving the setting at 1, the program no longer froze at the line mentioned above.

Thank you.



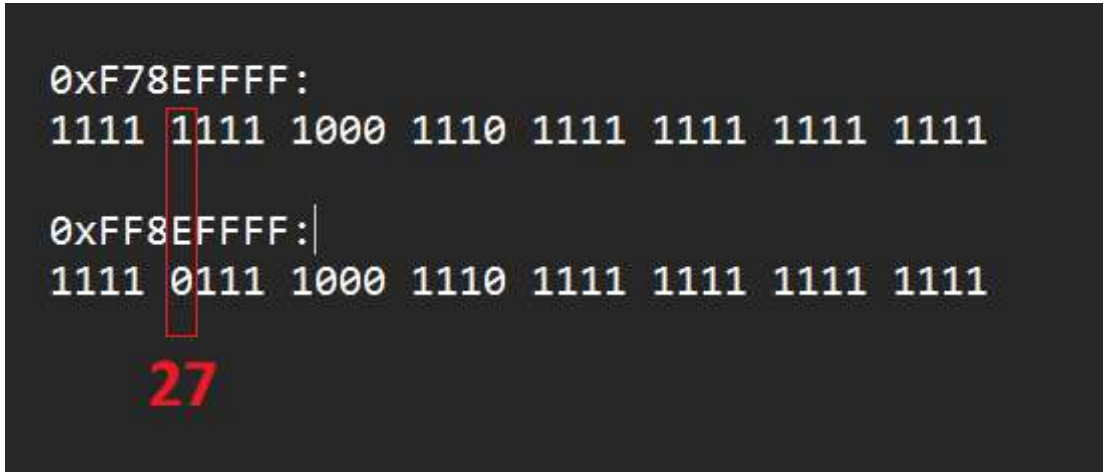
		CWDTPDEN is 1. Please refer to bit field description of CWDTPDEN. 111 = WDT hardware enable function is inactive. Others = WDT hardware enable function is active. WDT clock is always on.
[30]	**CWDTPDEN**	**Watchdog Clock Power-down Enable Bit** 0 = Watchdog Timer clock kept enabled when chip enters Power-down. 1 = Watchdog Timer clock is controlled by LIRCEN (CLK_PWRCTL[3]) when chip enters Power-down. **Note:** This bit only works if CWDTEN[2:0] is set to 011
[29:28]	**Reserved**	Reserved.
[27]	**CFGXT1**	**PF[4:3] Multi-Function Select** 0 = PF[4:3] pins are configured as GPIO pins. 1 =PF[4:3] pins are configured as external 4~20 MHz external high speed crystal oscillator (HXT) pins.
[26]	**CFOSC**	**CPU Clock Source Selection After Reset** The value of CFOSC will be loaded to HCLK (CLK_CLKSEL0[2:0]) in system clock controller after any reset occurs. HCLK[2:0] = 111 if CFOSC = 1, HCLK[2:0] = 000 if CFGSC=0. 0 = 4~20 MHz external high speed crystal oscillator (HXT) 1 = 22.1184 MHz internal high speed RC oscillator (HIRC)
[25:24]	**Reserved**	Reserved.
[23]	**CBODEN**	**Brown-Out Detector Enable Bit** 0= Brown-out detect Enabled after powered on. 1= Brown-out detect Disabled after powered on

M451 SERIES TECHNICAL REFERENCE MANUAL

>nulink.exe -r CFG0

> >>> Start to read CFG.
> 0%
> Config 0: 0xFF8EFFFF

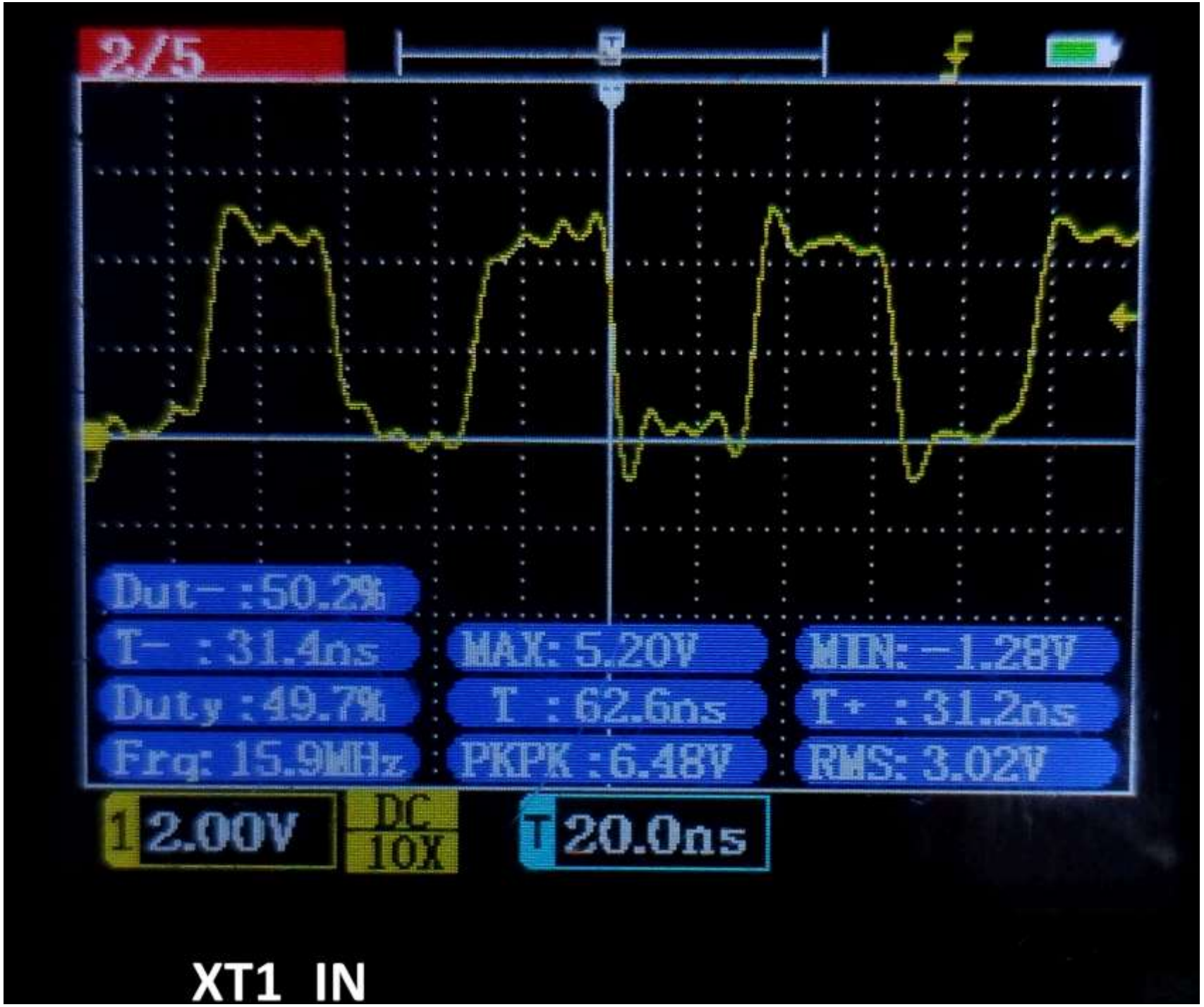
> 100%
> >>> Read CFG finish.
>
> ********** Execute operation ending **********

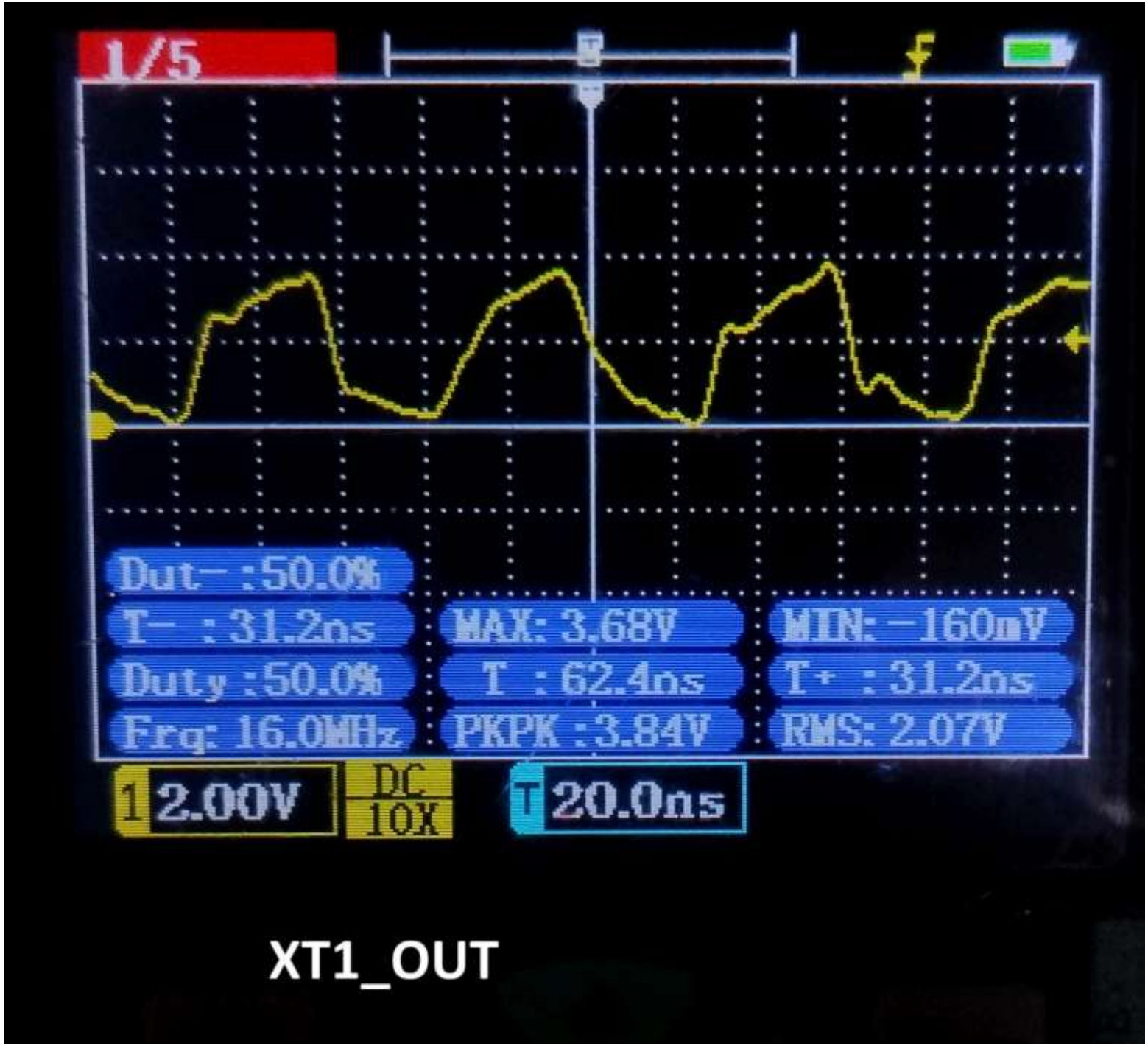


R rtek1000
Replied Oct 22, 2025

0

Note: When bit 27 was set to 0, the XT1_OUT pin did not output a signal. And with bit 27 set to 1, the XT1_OUT pin displayed a 16MHz signal (weaker than the signal input to the XT1_IN pin, because in the board circuit the signal comes from a 16MHz oscillator and passes through a TTL IC used as a buffer before reaching the XT1_IN pin):


2/5
Dut- :50.2%
T- :31.4ns
MAX: 5.20V
MIN: -1.28V
Duty :49.7%
T :62.6ns
T+ :31.2ns
Frq: 15.9MHz
PKPK :6.48V
RMS: 3.02V
1 2.00V
DC
10X
T 20.0ns
XT1 IN


1/5
Dut- :50.0%
T- :31.2ns
MAX: 3.68V
MIN: -160mV
Duty :50.0%
T :62.4ns
T+ :31.2ns
Frq: 16.0MHz
PKPK :3.84V
RMS: 2.07V
1 2.00V
DC
10X
T 20.0ns
XT1_OUT

R

rtek1000
Replied Oct 22, 2025

0

Reply