

SIMULATION OF CMOS CIRCUIT

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ABSTRACT

In this section of the lab, the goal is to build and simulate a CMOS circuit that can achieve the following logic expression $W = (A+B+C) + (D+E+F)$. Using the LT spice software, the desired circuit is built with the help of a truth table. Once that was done, we examine the output, and a screen capture was completed.

OBJECTIVE

The objective is to build and simulate a CMOS circuit that can achieve the following logic expression $W = (A+B+C) + (D+E+F)$.

PROCEDURE

The first step in this lab was to open the LT spice software and build the circuit according to the logic expression given in the question. Key to this gate circuit's elegant design is the complementary use of both P- and N-channel. The second step was to create a truth table shown below using the logic expression $W = (A+B+C) + (D+E+F)$.

A	B	C	D	E	F	W
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	1
0	0	0	1	0	0	1
0	1	1	0	0	0	1
1	0	0	0	0	0	1

Using the truth table and the LT spice application, a circuit was able to be connected as shown in Figure 1 below. For the OR gate, the NMOS and PMOS transistors are connected in parallel and series respectively.

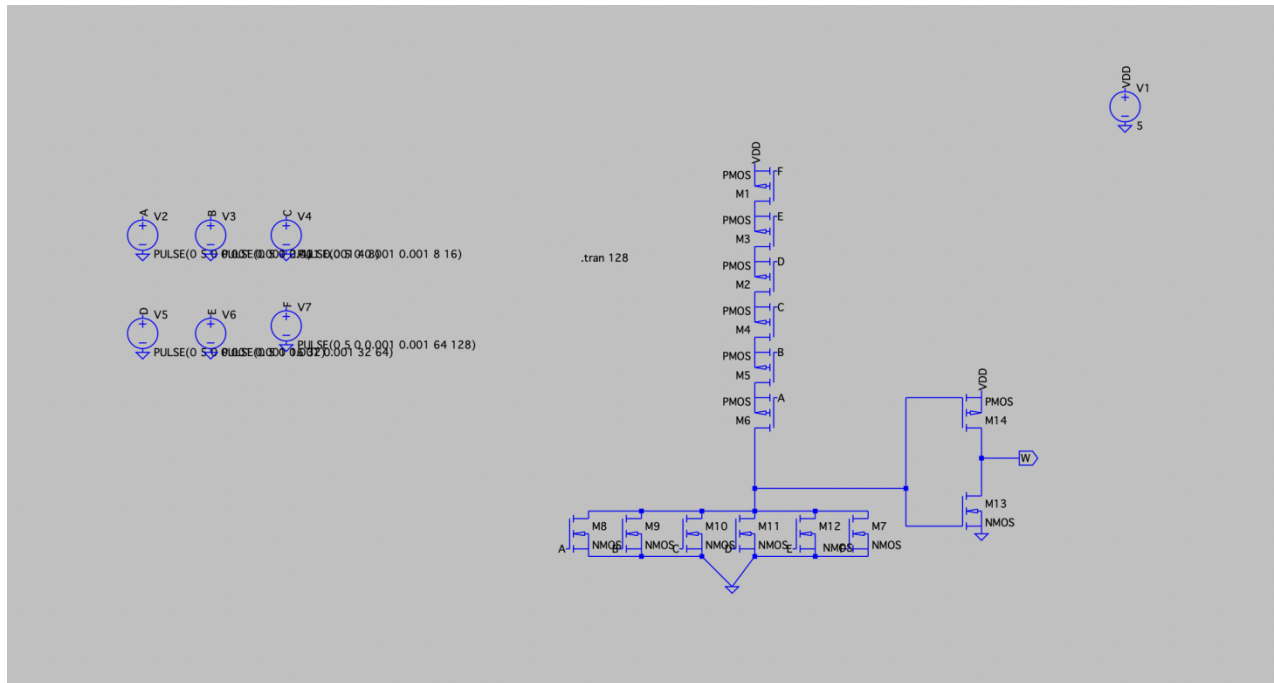
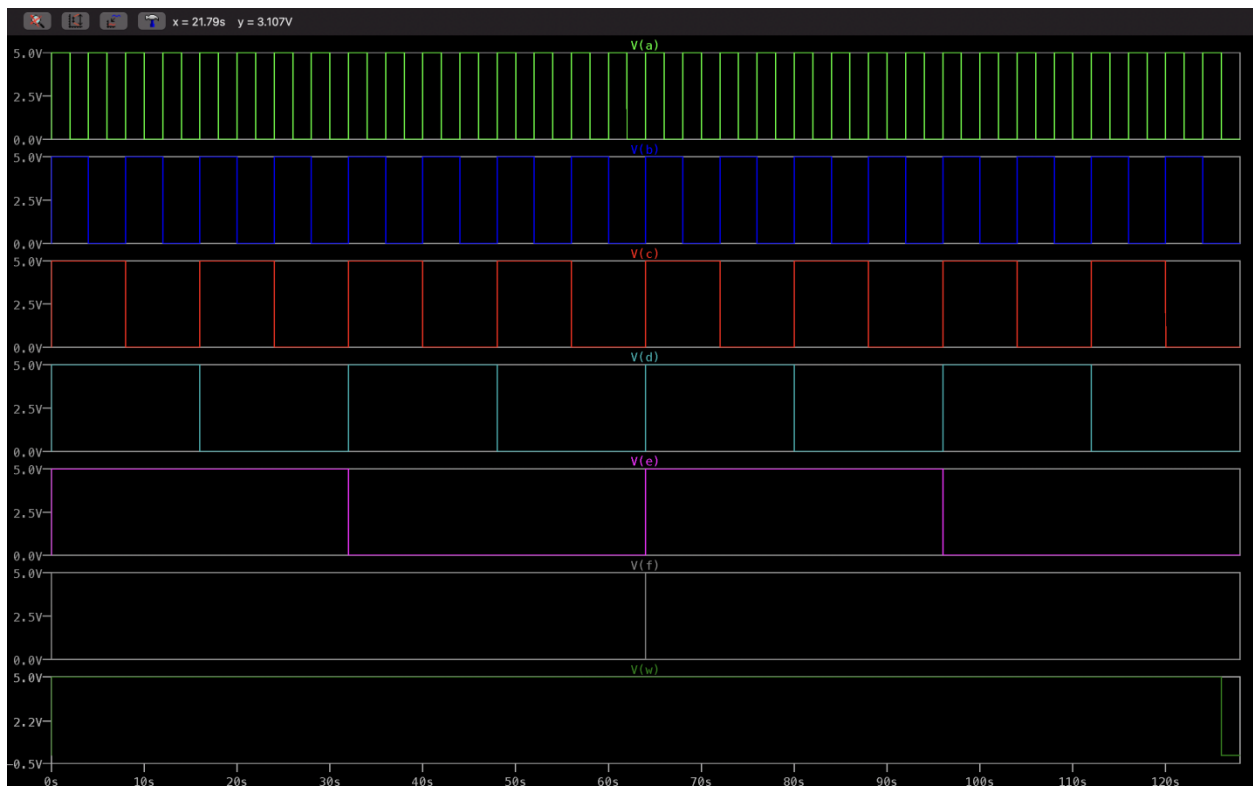


Figure 1 : CMOS circuit

After running the circuit successfully, a graph was created and is pictured in Figure 3 below.



CONCLUSION

A CMOS circuit with the following logic expression $W = (A+B+C) + (D+E+F)$ is built and simulated using the LT spice software. From the results above, we observe that all the output values from the truth table result in 1 except for the first input. Hence, the graph remains stagnant for the same while it is different for the rest of the input values.

MATERIALS USED

1. NMOS
2. PMOS
3. Vdd
4. Voltage source
5. ground