Qifa(Richard) Wang

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Objective: An engineering graduate passionate about computer architecture design, SW/HW co-design, accelerated computing, HPC, quantum computing, and software engineering. **Authorized to work for any employer in the US**.

Education

Computer Science & Engineering — ***Master of Science in Engineering*** Aug 2023 - May 2025
Rackham Graduate School, University of Michigan GPA: 4.00

Computer Science, minors in Math and Physics — ***Bachelor of Science in Engineering*** Aug 2020 - May 2023
College of Engineering, University of Michigan *Summa Cum Laude, Dean's List, University Honors*, GPA: 3.77

Skills

- **Coursework:** Computer Architecture and Microarchitecture, Parallel Computing and Architecture, GPU Programming, Compiler Design, Data Structure and Algorithms, Operating System, Machine Learning, Web Systems, Quantum Computing and Architecture
- **Programming languages:** C/C++, Python, Java, Verilog, SystemVerilog, CUDA, OpenMP, MPI, Javascript, TypeScript, Tcl
- **Frameworks and tools:** RISC-V, Qiskit, PyTorch, Tensorflow, REST, AWS, Docker, Vulkan, Synopsys VCS, GNU, LLVM, NVCC

Work Experience

Apple Inc. — ***Silicon Validation SW Intern*** May 2024 - Present
- Implemented PPROC method to evaluate hardware coverage on pixel processing module down to bit-field level. Designed and optimized multi-threaded, fault-tolerant, and memo-based algorithm relying on PPROC method to maximize test coverage by generating test suites using optimal parameters. Automate validation process by integrating feedback loop into silicon testing platform.

EECS 498: Quantum Computing — ***Graduate Student Instructor*** May 2023 - May 2024
- Redesigned course materials with lead instructor. Improved project specifications and test suites. Prepared lab materials and taught two lab sections weekly with around 40 students. Held weekly office hours for 9 hours.

Werfen — ***Software & Algorithm Development Intern*** May 2021 - Aug 2021
- Drafted roadmaps and formalized criteria and limitations for Mercury Algorithm Prototype (MAP). Engineered pivotal elements such as backend modules, front-end web tool, and GUI.

Technical Projects

Team Design — ***R10K Out-of-Order Processor Redesign with RISC-V ISA*** Jan 2024 - May 2024
- Engineered advanced features like N-way superscalar, GShare-Best branch predictor, early tag broadcasting, and return address stack to reduce latency. Revamped memory hierarchy using prefetching, associative, multi-ported and non-blocking cache, along with victim caching strategies. Optimized dependent memory operations with a data-forwarding load-store queue.
- Designed, implemented and verified microarchitecture at RTL level for reservation stations, Icache, Dcache, and load-store queue. Successfully simulated and synthesized the processor and passed 100% of test suites. Performanced ranked top 25% among all.

Personal Project — ***Batched Quantum Circuit Simulation on GPU*** Sep 2023 - May 2024
- Engineered a CUDA framework for efficient, batched simulation of diverse quantum circuits on GPU in parallel.
- Achieved super-linear enhancements in both simulation efficiency and scalability, identifying potential bottleneck areas and proposing corresponding optimization strategies.

Team Design — ***Compiler Optimization for CUDA Memory Coalescing (COALDA)*** Sep 2023 - Dec 2023
- Boosted CUDA program efficiency by optimizing memory access patterns, targeting and restructuring uncoalesced memory accesses. Thorough static analysis and performance evaluations showed a notable reduction in L2 cache bandwidth usage.
- Established an NVCC-Clang compilation pipeline to make CUDA kernel available for IR-level optimization.

Team Design — ***Linux-Based Operating System*** Jan 2023 - May 2023
- Developed a custom thread library to simulate multi-cpu, multi-threaded execution using C/C++. Implemented a sophisticated kernel pager system for efficient management of applications' virtual memory, encompassing the creation, copying, destruction, and allocation of address spaces. Engineered robust, multi-threaded network file server for reliable data exchange. Designed a hierarchical file system with comprehensive access control and fine-grained locking mechanisms to secure file ownership and permissions.

Personal

- Competitive saber fencing athlete who also loves alpine skiing and playing tennis
- Founder of BeaverWorks engineering club with MIT Lincoln Lab and BAE & System as sponsors
- Multilingual: English, Mandarin, Cantonese, French