

# Qifa(Richard) WANG

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OBJECTIVE: Highly motivated engineering graduate with strong foundation in computer science and engineering. Passionate about computer architecture, SW/HW co-design, accelerated computing, HPC, quantum computing, and software engineering. Quick to adapt to new technologies and concepts.

## EDUCATION

**Computer Science & Engineering — *Master of Science in Engineering*** AUG 2023 - MAY 2025  
Rackham Graduate School, University of Michigan GPA: 4.00

- Graduate Student Instructor for EECS 498: Quantum Computing and EECS 587: Parallel Computing

**Computer Science, minors in Math and Physics — *Bachelor of Science in Engineering*** AUG 2020 - MAY 2023  
College of Engineering, University of Michigan *Summa Cum Laude, Dean's List, University Honors*, GPA: 3.77

## SKILLS

- **Coursework:** Computer Architecture and Microarchitecture, Parallel Computing and Architecture, GPU Programming, Compiler Design, Data Structure and Algorithms, Operating System, Machine Learning, Web Systems, Quantum Computing and Architecture
- **Languages:** C/C++, Python, Go, Rust, Java, CUDA, OpenMP, MPI, Verilog/SystemVerilog, Chisel, Tcl, Javascript, TypeScript
- **Frameworks and tools:** PyTorch, CUDA-Q, Qiskit, AWS, Docker, Chipyard, GPGPU-Sim, Synopsys (DC, VCS, Verdi), GNU, LLVM, Valgrind

## WORK EXPERIENCE

**Apple Inc. — *Hardware Technology Intern*** MAY 2024 - AUG 2024

- Implemented PPROC method to evaluate hardware coverage on pixel processing module down to bit-field-level. Coverage result provides feedback and guidance for arch test improvement. Constructed feedback loop using PPROC to optimize test coverage by adjusting parameters. Internalize hardware coverage PPROC method into C/C++ testing infrastructure to run and provide feedback on-the-fly.

**Werfen — *Software & Algorithm Development Intern*** MAY 2021 - AUG 2021

- Drafted roadmaps and formalized criteria and limitations for Mercury Algorithm Prototype (MAP). Engineered embedded modules, front-end web tool, and GUI for the prototype using C/C++ and Qt framework.

## TECHNICAL PROJECTS

**Team Design — *R10K Out-of-Order Processor Redesign with RISC-V ISA*** JAN 2024 - MAY 2024

- Engineered advanced features like N-way superscalar, GShare-Best branch predictor, early tag broadcasting, and return address stack to reduce latency. Revamped memory hierarchy using prefetching, associative, multi-ported and non-blocking cache, along with victim caching strategies. Optimized dependent memory operations with a data-forwarding load-store queue.
- Designed, implemented and verified microarchitecture at RTL level for reservation stations, Icache, Dcache, and load-store queue. Successfully simulated and synthesized the processor and passed 100% of test suites. Performanced ranked top 25% among all.

**Personal Project — *Batched Quantum Circuit Simulation on CUDA-ready GPU*** SEP 2023 - MAY 2024

- Engineered a CUDA framework for efficient, batched simulation of diverse quantum circuits on GPU in parallel.
- Achieved super-linear enhancements in both simulation efficiency and scalability, identifying potential bottleneck areas and proposing corresponding optimization strategies.

**Team Design — *Compiler Optimization for CUDA Memory Coalescing (COALDA)*** SEP 2023 - DEC 2023

- Boosted CUDA program efficiency by optimizing memory access patterns, targeting and restructuring uncoalesced memory accesses. Thorough **static analysis** and performance evaluations showed a notable reduction in L2 cache bandwidth usage.
- Established an NVCC-Clang compilation pipeline to make CUDA kernel available for IR-level optimization.

**Team Design — *Linux-Based Operating System*** JAN 2023 - MAY 2023

- Developed a custom thread library to simulate multi-cpu, multi-threaded execution using C/C++. Implemented a sophisticated kernel pager system for efficient management of applications' virtual memory, encompassing the creation, copying, destruction, and allocation of address spaces. Engineered robust, multi-threaded network file server for reliable data exchange. Designed a hierarchical file system with comprehensive access control and fine-grained locking mechanisms to secure file ownership and permissions.

## PERSONAL

- **Authorized to work for any employer in the US**
- Competitive saber fencing athlete who also loves alpine skiing and playing tennis
- Founder of BeaverWorks engineering club with MIT Lincoln Lab and BAE & System as sponsors
- Multilingual: English, Mandarin, Cantonese, French