Project Status Report

Overall Status: **On Track**

Project Name: Parallel Adder and Accumulator

Date

Status Code Legend

- On Track: Project is on schedule
- At Risk: Milestones missed but date intact
- High Risk: At risk, with a high risk of going off track
- Off Track: Date will be missed if action not taken

Scope	• Constructing a math unit that does matrix multiplication and matrix addition • Numbers will be selected from RAM, summed/subtracted with their result placed in a register, then the result written back to RAM
Deliverables	• Adder/subtractor module • Scalar Multiplication module • Multiply module • Transpose module • Valid testbench
Assumptions	• All matrices will be square • ModelSim accurately represents the behavior of a real FPGA • Ram and Registers work appropriately
Dependencies	• A specific testbench will have to be created for every module, while the final testbench will have to be postponed till the completion of all modules • RAM and register will have to be simulated while not in a functioning state
Issues:	N/A
Milestones accomplished the week of 10/31/3018 – 12/5/2018:	• Statement of Work
Milestones planned this week, but not achieved with variance:	• Block Diagram • Module development plan
Milestones planned for next week:	• At least 2 modules completed with testbenches

Areas/questions for discussion:	• RAM Decision
Last week's issues forwarded to this week:	N/A

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