Digital Design and Implementation of an Instantaneous Overcurrent Relay on FPGA

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***Abstract*—Overcurrent relays (OCRs) play a vital role in power system protection by isolating faulted sections and ensuring continuous power supply. This paper presents the simulation-based design of an *Instantaneous Overcurrent Relay* using a digital architecture suitable for FPGA implementation. The system consists of four modules: an Analog-to-Digital Converter (ADC), a Moving Average Filter (MAF) for signal smoothing, a Root Mean Square (RMS) estimation block using a moving window algorithm, and a Relay Emulating Module (REM) implementing IEEE Standard C37.112-1996 characteristics. The design is developed and verified in the *Xilinx Vivado* simulation environment, confirming accurate fault detection and trip signal generation under different current conditions. The results demonstrate the effectiveness of the proposed design and its potential for future FPGA-based hardware implementation.**

***Index Terms*—IRMS, IPickup, FPGA**

I. Introduction

A reliable and uninterrupted power supply is essential for maintaining the stability of electrical networks. Protective relays play a vital role in power system protection by detecting abnormal conditions and isolating faulted sections to prevent damage and ensure continuity of service. Among various types, the Overcurrent Relay (OCR) remains one of the most commonly used and cost-effective protection devices for medium-voltage distribution systems. Over the years, protective relays have evolved from electromechanical relays-which relied on mechanical movement and suffered from slow response and wear-to solid-state relays, which offered better accuracy but limited flexibility. The introduction of digital relays brought a major improvement in speed, precision, and reliability by processing current and voltage signals through digital algorithms. However, relays based on microprocessors (μP) and microcontrollers (μC) still face limitations due to their sequential processing nature, which increases computational time and restricts response speed under fault conditions. To overcome these challenges, Field Programmable Gate Arrays (FPGAs) have emerged as a powerful alternative for implementing high-speed, reconfigurable protection systems. This work presents the simulation design of an overcurrent relay using an FPGA-based architecture. The design includes four main functional modules: an Analog-to-Digital Converter (ADC), a Moving Average Filter (MAF), a Root Mean Square (RMS) estimation block, and a Relay Logic Module. The system is modeled and verified using the Xilinx Vivado Design Suite, confirming accurate fault detection and trip generation when the current exceeds the defined pickup level. The simulation results demonstrate the feasibility of implementing reliable and fast-acting OCRs using digital design principles.

II. OCR Characteristics

An overcurrent relay operates on a simple principle — it monitors the current flowing through a system and compares it with a predefined threshold known as the pickup current (Ip). Under normal operating conditions, the current remains below this pickup value, and the relay stays inactive. When a fault or abnormal condition occurs, the current magnitude rises beyond the pickup level. Once this happens, the relay detects the overcurrent condition and initiates a trip signal to disconnect the affected circuit from the supply. The relay thus acts as a protective device, preventing equipment damage and maintaining system stability by isolating only the faulted section. The pickup current setting determines the relay's sensitivity; if set too low, it may cause nuisance tripping, while a higher setting may delay fault clearance. In this project, the operation of the overcurrent relay is modeled based solely on this pickup current principle, focusing on accurate fault detection through current monitoring and trip initiation during simulation.

III. Functional Architecture and Simulation Design

The proposed overcurrent relay (OCR) design consists of several functional blocks that together perform the relay's protection operation. The overall simulation was developed in the **Xilinx Vivado** environment to model and verify each stage of signal processing and decision-making.

A. Analog-to-Digital Conversion (ADC) Module

The ADC module simulates the digitization of the sensed current signal obtained from a current transformer. It converts

the input analog waveform into discrete digital samples suitable for digital processing. The sampling frequency is chosen to accurately represent the waveform without distortion.

B. Low-Pass Filter (Moving Average Filter – MAF)

To eliminate unwanted high-frequency noise and harmonics from the digital signal, a simple Moving Average Filter is implemented. The MAF smooths the waveform by replacing each current sample with the mean of a fixed number of previous samples. This ensures that the RMS calculation receives a stable and clean signal, improving the accuracy of fault detection.

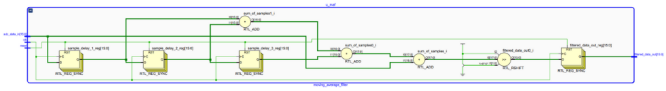

Fig. 1. Moving Average Filter Module

C. Root Mean Square (RMS) Estimation Module

This module computes the effective RMS value of the sampled current using a moving window technique. The RMS value is obtained by squaring each sample, summing over a fixed window, dividing by the number of samples, and then taking the square root. This process represents the true magnitude of the current flowing through the circuit and forms the basis for detecting overcurrent conditions in the relay.

D. Relay Logic Module

The relay logic compares the calculated RMS current with a predefined pickup current (Ip). When the RMS current exceeds the pickup threshold the module generates a trip signal. When the current returns below the pickup level, the relay resets. The simplified operating principle can be expressed as:

$If I_{RMS} > I_{pickup} \rightarrow Tripoutput = 1$

$If I_{RMS} < I_{pickup} \rightarrow Tripoutput = 0$

This structure allows clear simulation of fault detection and tripping behavior, providing a realistic representation of relay operation in a digital environment.

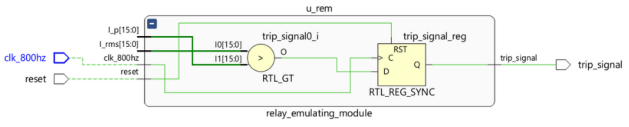

Fig. 2. Relay Logic Module

IV. RELAY ALGORITHM FLOW

The algorithm for the proposed instantaneous overcurrent relay operates as a direct, high-speed pipeline. It provides a simplified approach compared to the more complex IDMT-based flow, focusing on real-time response with minimal computational delay.

A. Start

Upon system reset, all registers and outputs are initialized to zero, ensuring a defined initial state for subsequent operations.

B. Sense

At every positive edge of the 800 Hz clock signal, a new 16-bit digital current sample is received from the Analog-to-Digital Converter (ADC).

C. Filter

The acquired sample is processed by the Moving Average Filter (MAF) module to produce a smoothed output, effectively reducing noise and harmonics.

D. RMS Estimation

The filtered data is then passed to the Root Mean Square (RMS) estimation module, which updates its moving window and computes the corresponding RMS current value .

E. Decision

The Relay Emulating Module (REM) compares the calculated RMS current with the predefined pickup current (Ip).

1) Trip Logic: If IRMS¿Ip, the relay logic asserts a trip signal, indicating an overcurrent condition.

If IRMS¡Ip, the relay remains inactive, ensuring no false tripping.

F. Loop

This process repeats continuously at each 800 Hz clock cycle, enabling real-time current monitoring and instantaneous relay operation.

V. VERIFICATION AND SIMULATION SETUP

The complete overcurrent relay design was verified through simulation using a comprehensive testbench developed in the Xilinx Vivado environment. The testbench integrates all major functional modules — the Analog-to-Digital Converter (ADC), Moving Average Filter (MAF), Root Mean Square (RMS) Estimation, and Relay Emulating Module (REM) — into a single pipeline to evaluate end-to-end system performance.

Simulation Setup: A master clock signal of 100 MHz was generated, and an internal clock divider was used to derive an 800 Hz clock for the relay modules, corresponding to the system's sampling frequency. The pickup current (Ip) was configured to a fixed reference value of 1500 units. Input current data, represented as a 16-sample sine wave, was continuously fed into the ADC module at each clock cycle to emulate real-time current waveform acquisition. **Test Sequence**

A. Initialization

The simulation began with a reset signal to initialize all modules and registers.

B. Normal Operation

After reset deactivation, a normal load current waveform (with an RMS value below IpI) was applied. During this stage, the relay correctly remained inactive, and no trip signal was generated.

C. Fault Condition Simulation

The input current was then increased to a higher amplitude to represent a fault condition (with RMS current exceeding Ip).

D. Trip Verification

As soon as the calculated RMS current exceeded the pickup threshold, the relay logic asserted the trip output, confirming proper fault detection and relay operation.

E. Reset Behavior

After the current returned to normal levels, the relay maintained its trip state until a system reset was applied, verifying correct latching and reset functionality.

The simulation results confirmed that the proposed relay design accurately computes the RMS current, reliably detects overcurrent faults, and promptly generates a trip signal at the predefined threshold. The system exhibited stable performance, rapid response, and consistent operation across all test conditions within the simulation environment.

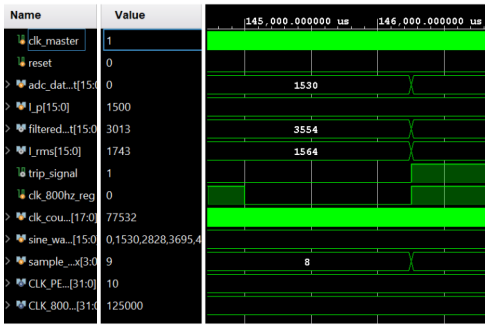

Fig. 3. Trip Signal Generated

VI. EXPECTED HARDWARE SETUP

The expected hardware setup for implementing the instantaneous overcurrent relay (OCR) is shown in Fig. 4. The system comprises key components such as the Current Transformer (CT), Signal Conditioning Circuit, Analog-to-Digital Converter (ADC), FPGA module, and the Circuit Breaker (CB) interface.

The Current Transformer (CT) senses the line current and steps it down to a measurable level. The secondary current from the CT is passed through a signal conditioning circuit, which includes amplification and isolation stages to protect the FPGA and ensure the input signal remains within the ADC's operating range.

The Analog-to-Digital Converter (ADC) samples the conditioned current signal and converts it into 16-bit digital data, which is then transferred to the FPGA. Inside the FPGA, the digital current data is processed sequentially by the functional modules:

- The Moving Average Filter (MAF) removes unwanted noise and harmonic components from the digitized current waveform.
- The Root Mean Square (RMS) Estimation Module computes the effective current magnitude in real time.
- The Relay Emulating Module (REM) compares the computed RMS current with the predefined pickup current (Ipickup)

When the RMS current (IRMS) exceeds Ipickup, the relay logic asserts a trip signal. This digital trip signal is transmitted to the Circuit Breaker (CB) through a Driver Circuit, which provides the required isolation and power amplification for actuation. Once the fault clears and the current falls below the pickup level, the relay resets automatically, restoring normal operation.

This setup provides a clear mapping between the simulated modules and their real-time hardware equivalents, allowing straightforward transition from simulation to hardware implementation in future work.

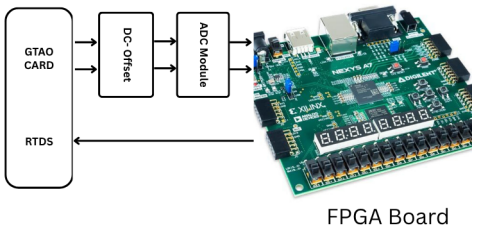

Fig. 4. Hardware Testing Setup

VII. CONCLUSION

This report presents the successful design, implementation, and verification of an FPGA-based instantaneous overcurrent relay. The design leverages a high-speed, parallel pipelined architecture, which highlights the inherent advantages of FPGA-based protection systems. The system is modular, consisting of a Moving Average Filter, an efficient moving-window RMS Estimation module using a CORDIC IP, and an Instantaneous Relay Emulating Module. Simulation results from the Verilog testbench confirm the relay's accurate operation, effectively distinguishing between normal (sub-1500 RMS) and fault (super-1500 RMS) conditions.

The implemented instantaneous relay provides a robust and

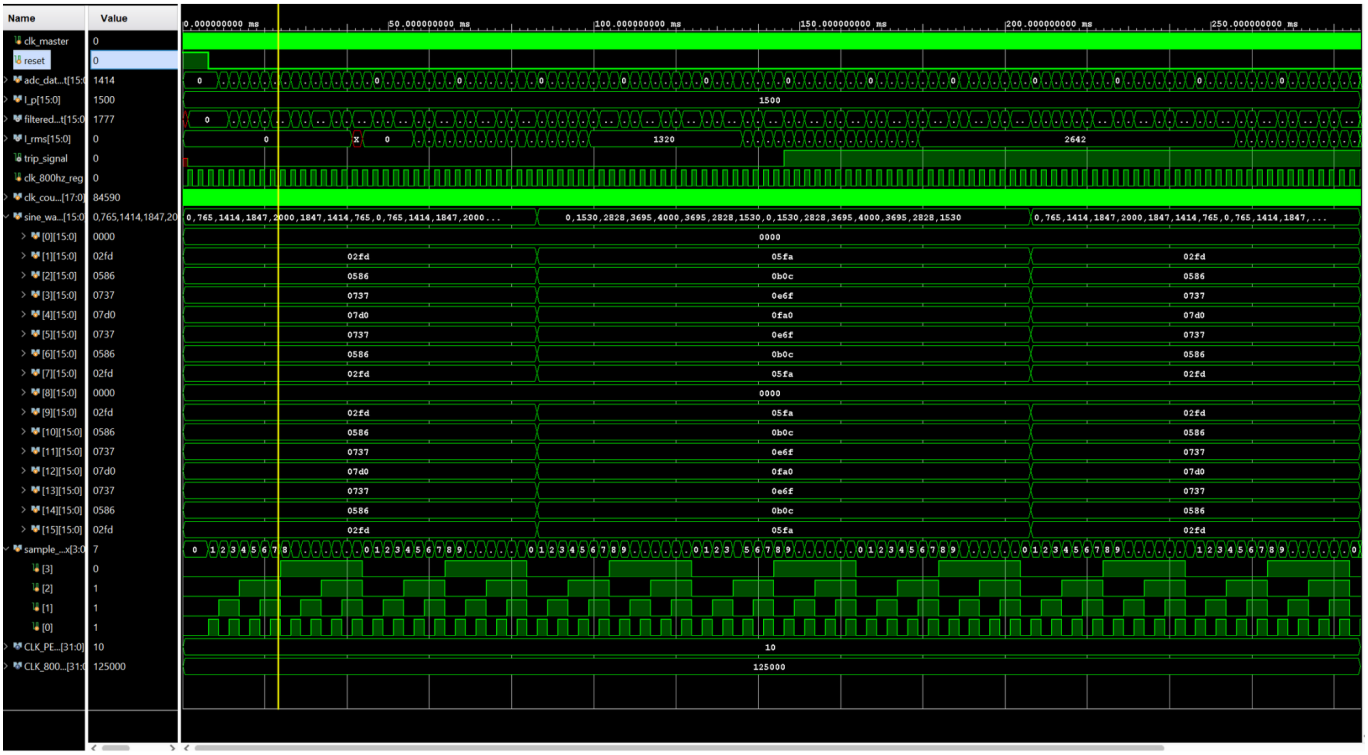

Fig. 5. Simulation

high-speed foundation for power system protection. Furthermore, it can be extended to more complex protection schemes, such as inverse definite minimum time (IDMT) relays, by enhancing the relay emulation module to incorporate inverse-time characteristic equations.

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