

Digital Design and Computer Organization Laboratory

3rd Semester, Academic Year 2024

Date: 09/08/2024

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Week# 1 Program Number: 1

**TITLE: WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT AND GATE.
GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE.
VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE**

- I. Verilog Code Screenshot
- II. Verilog VVP Output Screen Shot
- III. GTKWAVE Screenshot
- IV. Output Table to be completed and included

AND Gate

Code:

```

≡ and2.v
1 module andgate (y,a, b,);
2 input a, b;
3 output y;
4 assign y = a & b;
5 endmodule
6

```

```

≡ and2_tb.v
1 module and_test;
2 reg a,b;
3 wire y;
4 and(y,a,b);
5 initial
6 begin
7 #0 a=0;b=0;
8 #5 a=0;b=1;
9 #10 a=1;b=0;
10 #15 a=1;b=1;
11 end
12 initial
13 begin
14 $monitor($time,"a=%b,b=%b,y=%b",a,b,y);
15 end
16 initial
17 begin
18 $dumpfile("and2_test.vcd");
19 $dumpvars(0,and_test);
20 end
21 endmodule

```

Output:

```

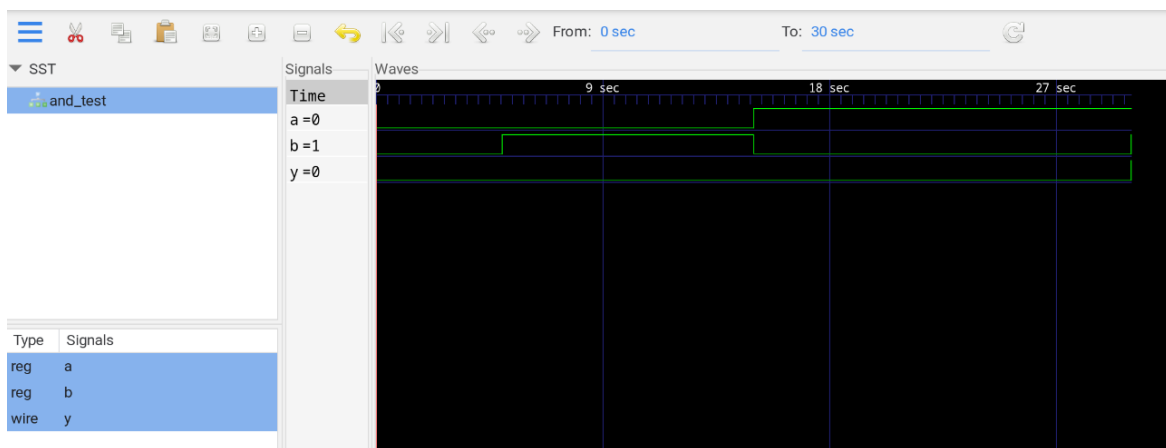
rithvikmatta@penguin:~/DDCO-sem-3$ iverilog -o test1 and2.v and2_tb.v
rithvikmatta@penguin:~/DDCO-sem-3$ vvp test1
VCD info: dumpfile and2_test.vcd opened for output.
      0a=0,b=0,y=0
      5a=0,b=1,y=0
     15a=1,b=0,y=0
     30a=1,b=1,y=1
rithvikmatta@penguin:~/DDCO-sem-3$ gtkwave and2_test.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[30] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.

```

GTK wave screenshot:





Output table:

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

WRITE A VERILOG PROGRAM TO MODEL A TWO INPUT OR GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE OR GATE TRUTH TABLE

- I. Verilog Code Screenshot
- II. Verilog VVP Output Screen Shot
- III. GTKWAVE Screenshot
- IV. Output Table to be completed and included

OR Gate

Code:

```

1 module orgate (y,a, b,);
2 input a, b;
3 output y;
4 assign y = a | b;
5 endmodule
6

```

```

1 module or_test;
2 reg a,b;
3 wire y;
4 or(y,a,b);
5 initial
6 begin
7 #0 a=0;b=0;
8 #5 a=0;b=1;
9 #10 a=1;b=0;
10 #15 a=1;b=1;
11 end
12 initial
13 begin
14 $monitor($time,"a=%b,b=%b,y=%b",a,b,y);
15 end
16 initial
17 begin
18 $dumpfile("or2_test.vcd");
19 $dumpvars([0,or_test]);
20 end
21 endmodule

```

Output:

```

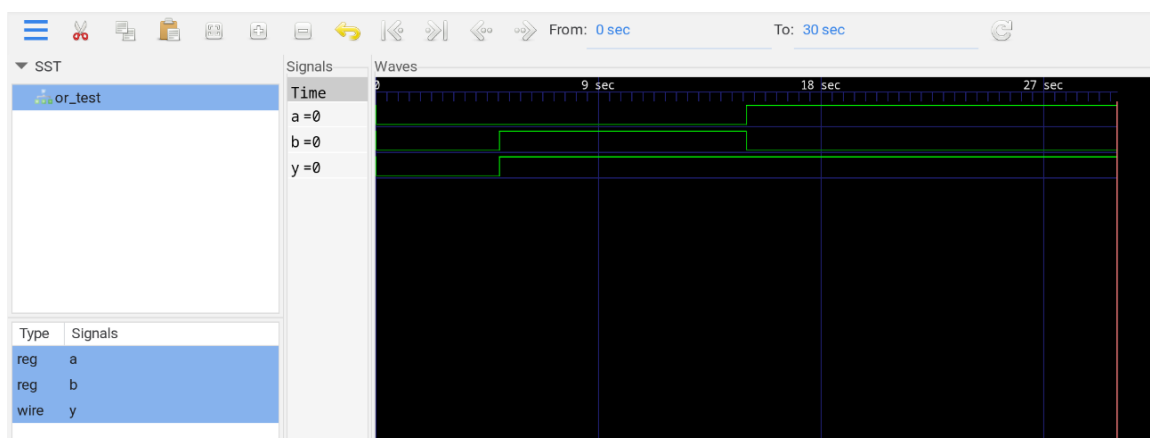
rithvikmatta@penguin:~/DDCO-sem-3$ iverilog -o test2 or2.v or2_tb.v
rithvikmatta@penguin:~/DDCO-sem-3$ vvp test2
VCD info: dumpfile or2_test.vcd opened for output.
      0a=0,b=0,y=0
      5a=0,b=1,y=1
     15a=1,b=0,y=1
     30a=1,b=1,y=1
rithvikmatta@penguin:~/DDCO-sem-3$ gtkwave or2_test.vcd

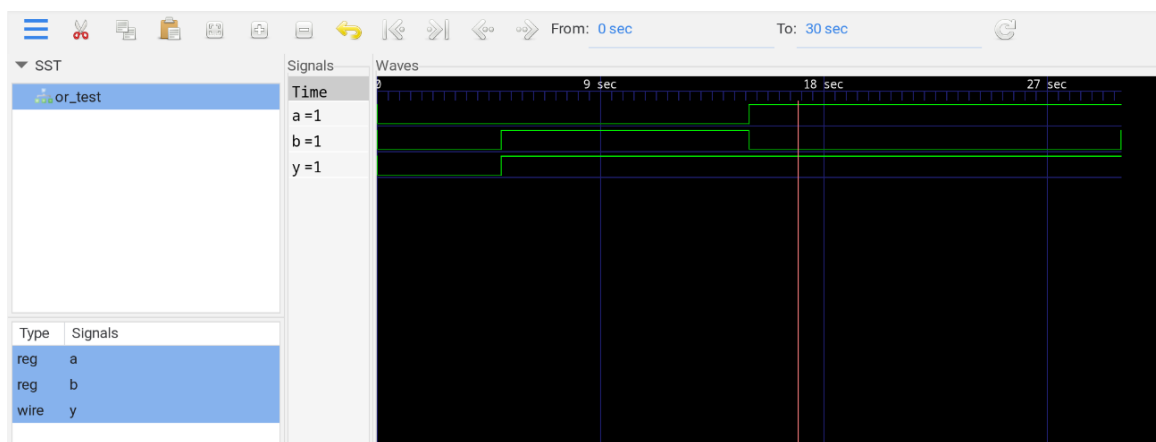
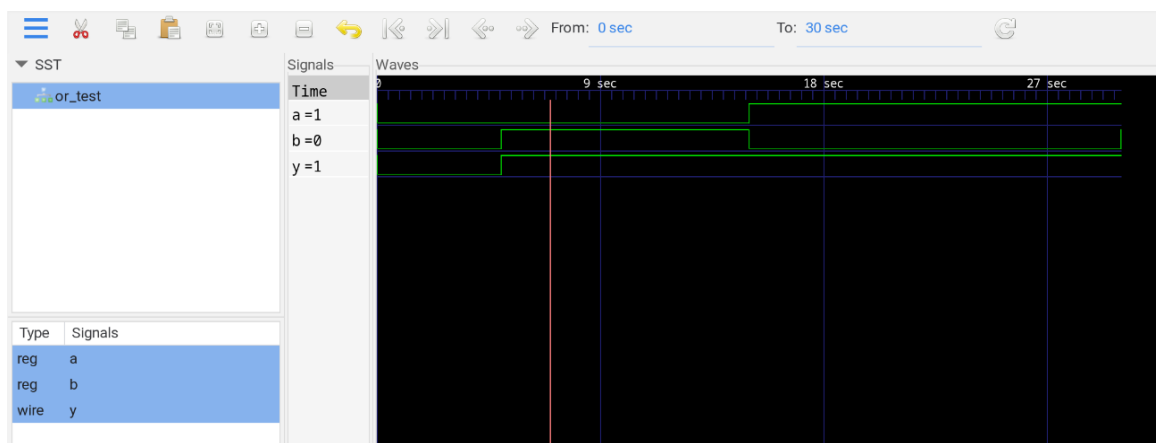
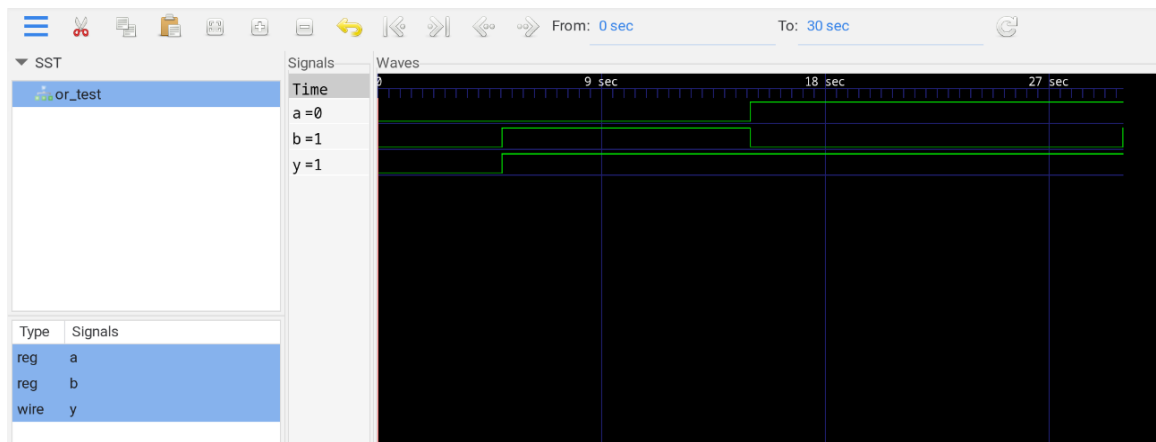
GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[30] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.

```

GTK wave screenshot:





Output table:

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

WRITE A VERILOG PROGRAM TO MODEL A ONE INPUT NOT GATE. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE NOT GATE TRUTH TABLE

- I. Verilog Code Screenshot
- II. Verilog VVP Output Screen Shot
- III. GTKWAVE Screenshot
- IV. Output Table to be completed and included

NOT Gate

Code:

```
not2.v
1  module andgate (y,a, b);
2  input a;
3  output y;
4  assign y = !a;
5  endmodule
6

not2_tb.v
1  module not_test;
2  reg a;
3  wire y;
4  not(y,a);
5  initial
6  begin
7  #0 a=0;
8  #15 a=1;
9  end
10 initial
11 begin
12 $monitor($time,"a=%b,y=%b",a,y);
13 end
14 initial
15 begin
16 $dumpfile("not2_test.vcd");
17 $dumpvars(0,not_test);
18 end
19 endmodule
```

Output:

```

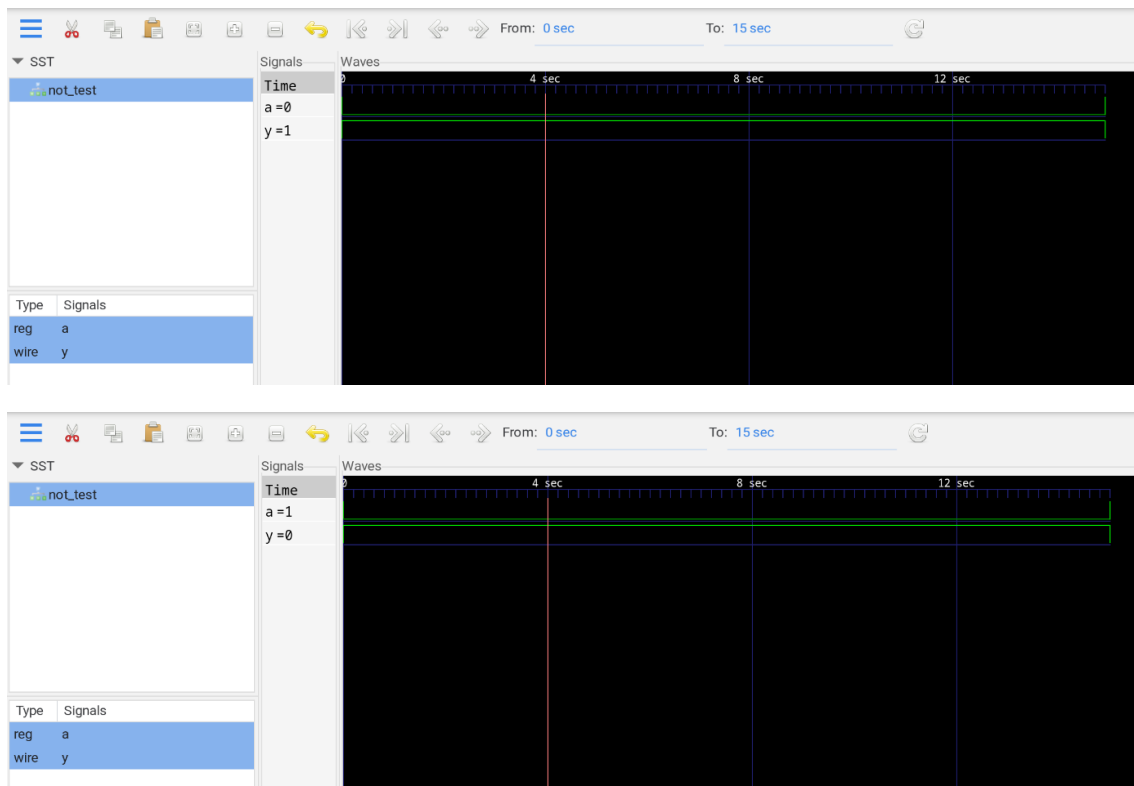
rithvikmatta@penguin:~/DDCO-sem-3$ iverilog -o test3 not2.v not2_tb.v
rithvikmatta@penguin:~/DDCO-sem-3$ vvp test3
VCD info: dumpfile not2_test.vcd opened for output.
      0a=0,y=1
      15a=1,y=0
rithvikmatta@penguin:~/DDCO-sem-3$ gtkwave not2_test.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[15] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.

```

GTK wave screenshot:

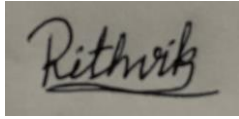


Output table:

A	Y
0	1
1	0

If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

A rectangular box containing a handwritten signature in black ink. The signature appears to be 'Rithvik' written in a cursive, slightly stylized font.

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Section: K

Date: 09/08/2024