Digital Design and Computer Organization Laboratory

3rd Semester, Academic Year 2024

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Week#____10_____ Program Number: ____10__

Aim of the Experiment:

CONSTRUCT A PROGRAM COUNTER, FOR EVERY CLOCK CYCLE.GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE TRUTH TABLE

I. Verilog Code Screenshot

week 10 - program counter > pc.v

```
module fa (input wire i0, i1, cin, output wire sum, cout);
    wire t0, t1, t2;
xor3 _i0 (i0, i1, cin, sum);
and2 _i1 (i0, i1, t0);
and2 _i2 (i1, cin, t1);
and2 _i3 (cin, i0, t2);
or3 _i4 (t0, t1, t2, cout);
endmodule

module addsub (input wire addsub, i0, i1, cin, output wire sumdiff, cout);
wire t;
fa _i0 (i0, t, cin, sumdiff, cout);
xor2 _i1 (i1, addsub, t);
endmodule

module pc_slice (input wire clk, reset, cin, load, inc, sub, offset,
  output wire cout, pc);
 wire in, inc_;
invert invert_0 (inc, inc_);
 and2 and2_0 (offset, inc_, t);
addsub addsub_0 (sub, pc, t, cin, in, cout);
 dfrl dfrl_0 (clk, reset, load, in, pc);
endmodule

module pc_slice0 (input wire clk, reset, cin, load, inc, sub, offset,  output wire cout, pc);
wire in;
 or2 or2_0 (offset, inc, t);
 addsub addsub_0 (sub, pc, t, cin, in, cout);
dfrl dfrl_0 (clk, reset, load, in, pc);
endmodule

module pc (input wire clk, reset, inc, add, sub, input wire [15:0] offset, output wire [15:0] pc);
 input wire load;
 input wire [15:0] c;
 or3 or3_0 (inc, add, sub, load);
pc_slice0 pc_slice_0 (clk, reset, sub, load, inc, sub, offset[0], c[0], pc[0]);
 pc_slice pc_slice_1 (clk, reset, c[0], load, inc, sub, offset[1], c[1], pc[1]);
pc_slice pc_slice_2 (clk, reset, c[1], load, inc, sub, offset[2], c[2], pc[2]);
 pc_slice pc_slice_3 (clk, reset, c[2], load, inc, sub, offset[3], c[3], pc[3]);
  pc_slice pc_slice_4 (clk, reset, c[3], load, inc, sub, offset[4], c[4], pc[4]);
 pc_slice pc_slice_5 (clk, reset, c[4], load, inc, sub, offset[5], c[5], pc[5]);
 pc_slice pc_slice_6 (clk, reset, c[5], load, inc, sub, offset[6], c[6], pc[6]);
 pc_slice pc_slice_7 (clk, reset, c[6], load, inc, sub, offset[7], c[7], pc[7]);
pc_slice pc_slice_8 (clk, reset, c[7], load, inc, sub, offset[8], c[8], pc[8]);
  pc_slice pc_slice_9 (clk, reset, c[8], load, inc, sub, offset[9], c[9], pc[9]);
pc_slice pc_slice_10 (clk, reset, c[9], load, inc, sub, offset[10], c[10], pc[10]);
pc_slice pc_slice_11 (clk, reset, c[10], load, inc, sub, offset[11], c[11], pc[11]);
pc_slice pc_slice_12 (clk, reset, c[11], load, inc, sub, offset[12], c[12], pc[12]);
  pc_slice pc_slice_13 (clk, reset, c[12], load, inc, sub, offset[13], c[13], pc[13]);
  pc_slice pc_slice_14 (clk, reset, c[13], load, inc, sub, offset[14], c[14], pc[14]);
  pc_slice pc_slice_15 (clk, reset, c[14], load, inc, sub, offset[15], c[15], pc[15]);
endmodule
```

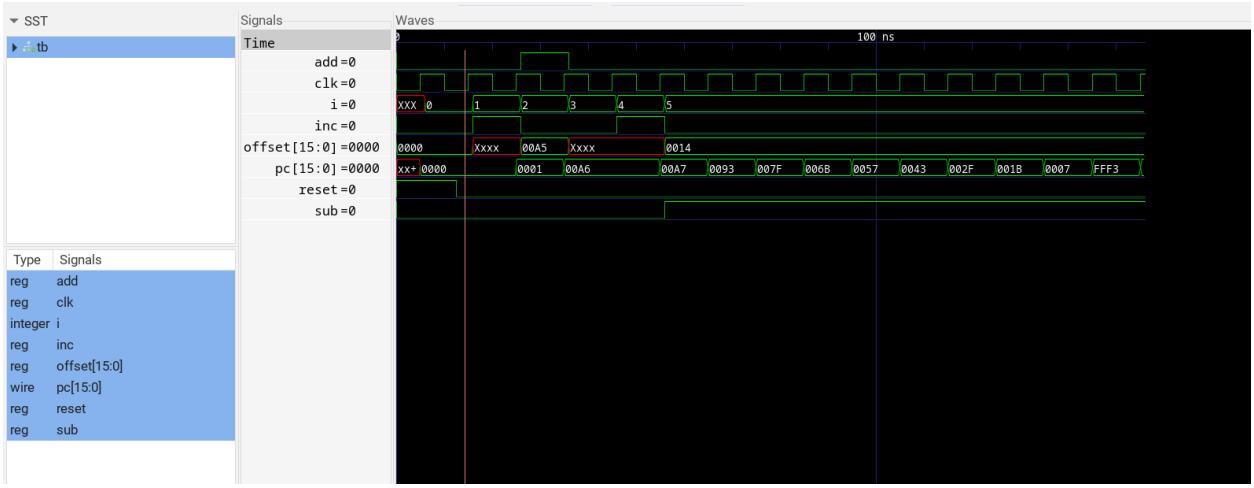
week 10 - program counter > pc_tb.v

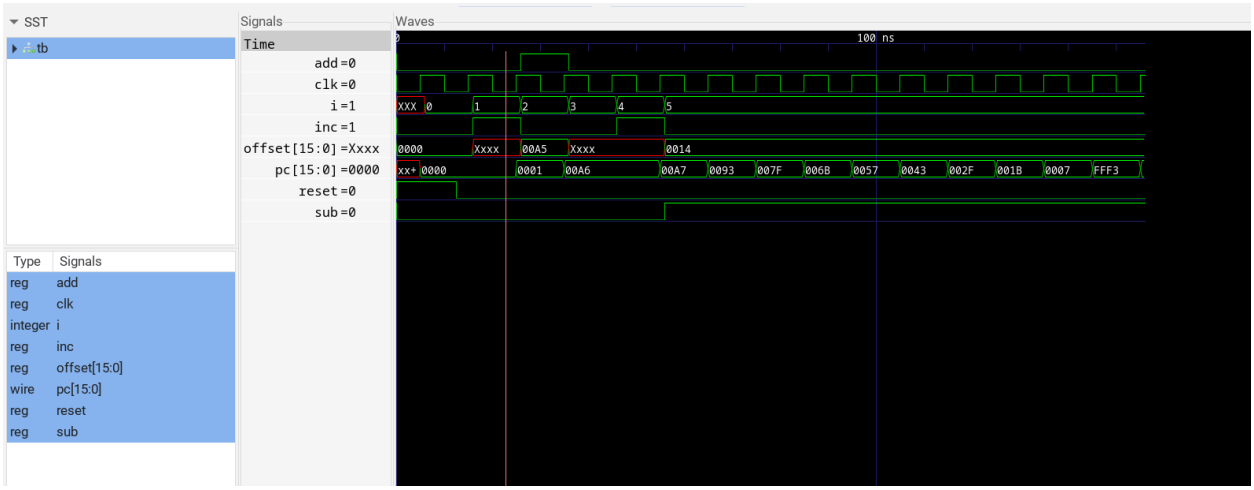
```
1  `timescale 1 ns / 100 ps
2  `define TESTVECS 5
3
4  module tb;
5    reg clk, reset, inc, add, sub;
6    reg [15:0] offset;
7    wire [15:0] pc;
8    reg [18:0] test_vecs [0:(`TESTVECS-1)];
9    integer i;
10   initial begin $dumpfile("tb_pc.vcd"); $dumpvars(0,tb); end
11   initial begin reset = 1'b1; #12.5 reset = 1'b0; end
12   initial clk = 1'b0; always #5 clk =~ clk;
13
14   initial begin
15     test_vecs[0][18] = 1'b1; test_vecs[0][17] = 1'b0; test_vecs[0][16] = 1'b0;
16     test_vecs[0][15:0] = 15'hxx;
17     test_vecs[1][18] = 1'b0; test_vecs[1][17] = 1'b1; test_vecs[1][16] = 1'b0;
18     test_vecs[1][15:0] = 15'ha5;
19     test_vecs[2][18] = 1'b0; test_vecs[2][17] = 1'b0; test_vecs[2][16] = 1'b0;
20     test_vecs[2][15:0] = 15'hxx;
21     test_vecs[3][18] = 1'b1; test_vecs[3][17] = 1'b0; test_vecs[3][16] = 1'b0;
22     test_vecs[3][15:0] = 15'hxx;
23     test_vecs[4][18] = 1'b0; test_vecs[4][17] = 1'b0; test_vecs[4][16] = 1'b1;
24     test_vecs[4][15:0] = 15'h14;
25   end
26
27   initial {inc, add, sub, offset} = 0;
28   pc pc_0 (clk, reset, inc, add, sub, offset, pc);
29   initial begin
30     #6 for(i=0;i<`TESTVECS;i=i+1)
31       begin #10 {inc, add, sub, offset}=test_vecs[i]; end
32     #100 $finish;
33   end
34
35 always@(reset or inc or add or sub )
36
37 $monitor("At time = %t, Reset= %b,inc=%b, add=%b,sub = %b,pc =%h ", $time,reset,inc,add,sub,pc);
38
39 endmodule
```

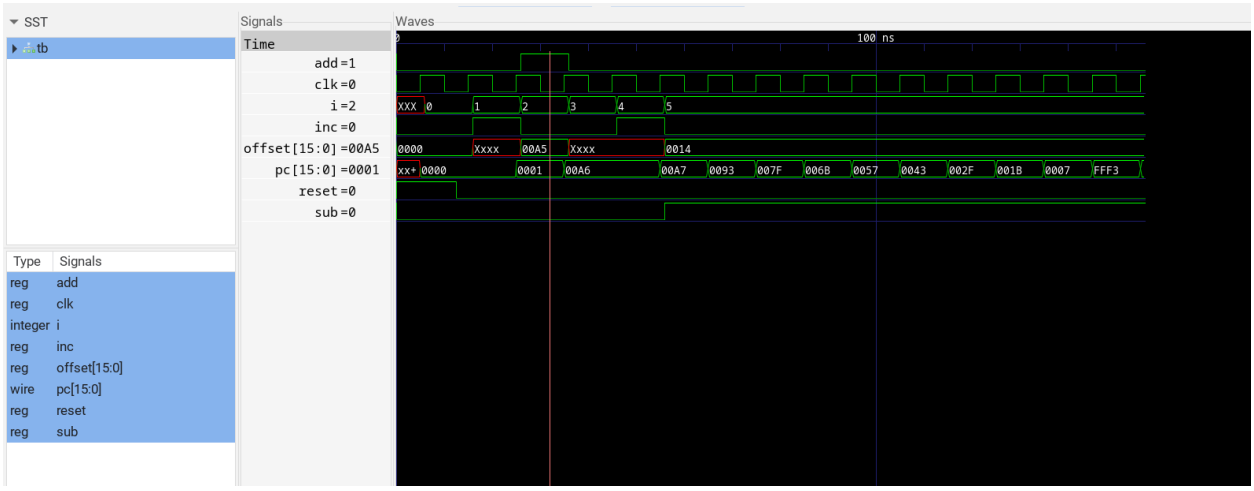
II. Verilog VVP Output Screen Shot

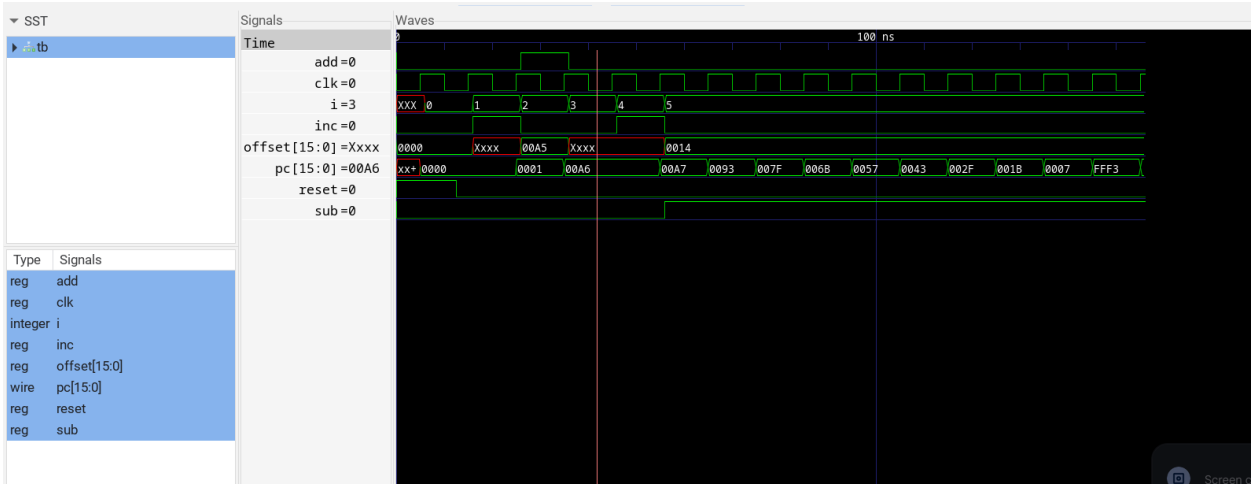
```
● rithvikmatta@penguin:~/PES/DDCO-sem-3/week 10 - program counter$ iverilog -o test lib.v pc.v pc_tb.v
● rithvikmatta@penguin:~/PES/DDCO-sem-3/week 10 - program counter$ vvp test
  VCD info: dumpfile tb_pc.vcd opened for output.
  At time =                    0, Reset= 1,inc=0, add=0,sub = 0,pc =xxxx
  At time =                   50, Reset= 1,inc=0, add=0,sub = 0,pc =0000
  At time =                  130, Reset= 0,inc=0, add=0,sub = 0,pc =0000
  At time =                  160, Reset= 0,inc=1, add=0,sub = 0,pc =0000
  At time =                  250, Reset= 0,inc=1, add=0,sub = 0,pc =0001
  At time =                  260, Reset= 0,inc=0, add=1,sub = 0,pc =0001
  At time =                  350, Reset= 0,inc=0, add=1,sub = 0,pc =00a6
  At time =                  360, Reset= 0,inc=0, add=0,sub = 0,pc =00a6
  At time =                  460, Reset= 0,inc=1, add=0,sub = 0,pc =00a6
  At time =                  550, Reset= 0,inc=1, add=0,sub = 0,pc =00a7
  At time =                  560, Reset= 0,inc=0, add=0,sub = 1,pc =00a7
  At time =                  650, Reset= 0,inc=0, add=0,sub = 1,pc =0093
  At time =                  750, Reset= 0,inc=0, add=0,sub = 1,pc =007f
  At time =                  850, Reset= 0,inc=0, add=0,sub = 1,pc =006b
  At time =                  950, Reset= 0,inc=0, add=0,sub = 1,pc =0057
  At time =                 1050, Reset= 0,inc=0, add=0,sub = 1,pc =0043
  At time =                 1150, Reset= 0,inc=0, add=0,sub = 1,pc =002f
  At time =                 1250, Reset= 0,inc=0, add=0,sub = 1,pc =001b
  At time =                 1350, Reset= 0,inc=0, add=0,sub = 1,pc =0007
  At time =                 1450, Reset= 0,inc=0, add=0,sub = 1,pc =fff3
  At time =                 1550, Reset= 0,inc=0, add=0,sub = 1,pc =ffdf
● rithvikmatta@penguin:~/PES/DDCO-sem-3/week 10 - program counter$ gtkwave tb_pc.vcd

  GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

  [0] start time.
  [156000] end time.
  GTKWAVE | Touch screen detected, enabling gestures.
  Exiting.
○ rithvikmatta@penguin:~/PES/DDCO-sem-3/week 10 - program counter$
```

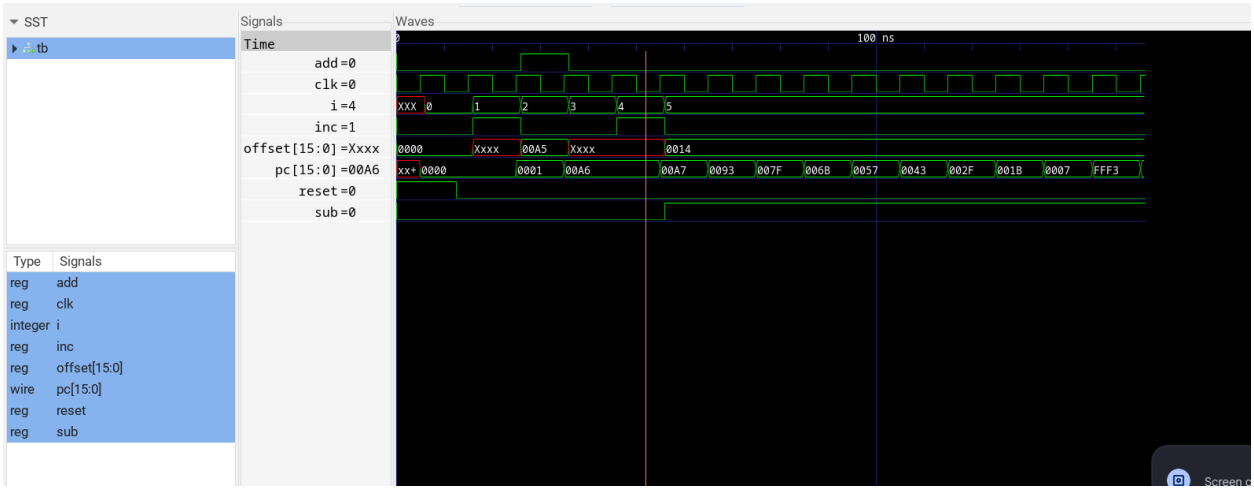
III. GTKWAVE Screenshot


SST
tb
Type Signals
reg add
reg clk
integer i
reg inc
reg offset[15:0]
wire pc[15:0]
reg reset
reg sub
Signals
Waves
Time
add =0
clk =0
i =0
inc =0
offset[15:0] =0000
pc[15:0] =0000
reset =0
sub =0
100 ns
XXX 0 1 2 3 4 5
0000 Xxxx 00A5 Xxxx 0014
xx+ 0000 0001 00A6 00A7 0093 007F 006B 0057 0043 002F 001B 0007 FFF3


SST
tb
Type Signals
reg add
reg clk
integer i
reg inc
reg offset[15:0]
wire pc[15:0]
reg reset
reg sub
Signals
Waves
Time
add =0
clk =0
i =1
inc =1
offset[15:0] =Xxxx
pc[15:0] =0000
reset =0
sub =0
100 ns
XXX 0 1 2 3 4 5
0000 Xxxx 00A5 Xxxx 0014
xx+ 0000 0001 00A6 00A7 0093 007F 006B 0057 0043 002F 001B 0007 FFF3


SST
tb
Type Signals
reg add
reg clk
integer i
reg inc
reg offset[15:0]
wire pc[15:0]
reg reset
reg sub
Signals
Waves
Time
add =1
clk =0
i =2
inc =0
offset[15:0] =00A5
pc[15:0] =0001
reset =0
sub =0
100 ns
XXX 0 1 2 3 4 5
0000 Xxxx 00A5 Xxxx 0014
xx+ 0000 0001 00A6 00A7 0093 007F 006B 0057 0043 002F 001B 0007 FFF3





IV. Output Table (Truth Table)

Time	Reset	Inc	Add	Sub	PC
0	1	0	0	0	xxxx
50	1	0	0	0	0000

130	0	0	0	0	0000
160	0	1	0	0	0000
250	0	1	0	0	0001
260	0	0	1	0	0001
350	0	0	1	0	00a6
360	0	0	0	0	00a6
460	0	1	0	0	00a6
550	0	1	0	0	00a7
560	0	0	0	1	00a7
650	0	0	0	1	0093
750	0	0	0	1	007f
850	0	0	0	1	006b
950	0	0	0	1	0057
1050	0	0	0	1	0043
1150	0	0	0	1	002f
1250	0	0	0	1	001b
1350	0	0	0	1	0007
1450	0	0	0	1	fff3
1550	0	0	0	1	ffdf

If found plagiarized, I will abide with the disciplinary action of the University.

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