Digital Design and Computer Organization Laboratory 3rd Semester, Academic Year 2024

Date: 30/08/2024

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Matta	PES2UG23CS485		
Week#4			

TITLE:

- Design 2:1 MUX
- Design 4:1 MUX using 2:1 MUX
- Design 1:2 DeMUX
- Design an Encoder
- Design a Decoder

GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

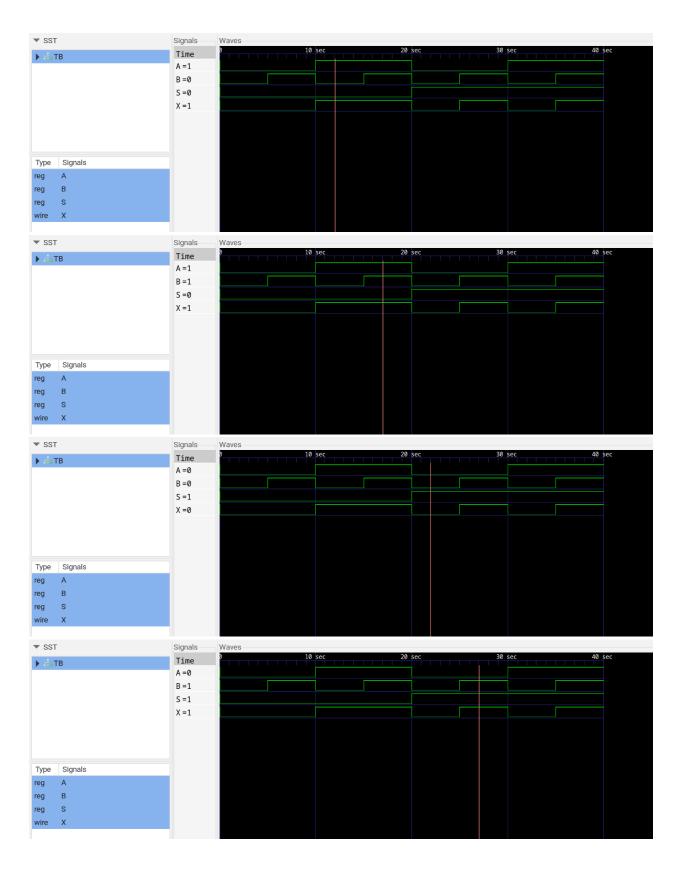
1) 2:1 MUX

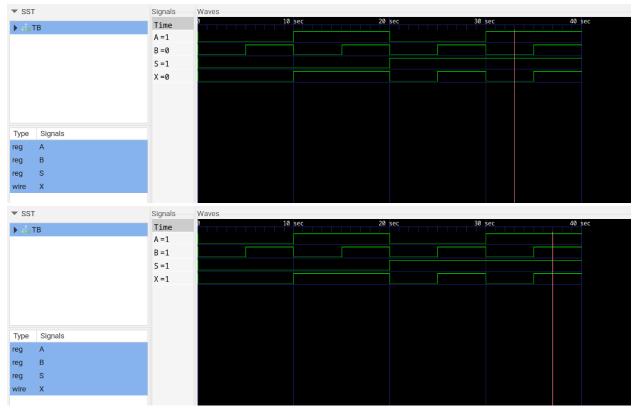
i 0	<i>i</i> ₁	j	У
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

```
week 4 > ≡ mux2_tb.v
      module TB;
      reg A, B, S;
      wire X;
      mux2 \ newMUX \ (.i0(A), .i1(B), .j(S), .o(X));
      initial
      begin
      #5; S = 1'b0; A = 1'b0; B = 1'b0;
      \#5; S = 1'b0; A = 1'b0; B = 1'b1;
      #5; S = 1'b0; A = 1'b1; B = 1'b0;
      #5; S = 1'b0; A = 1'b1; B = 1'b1;
      #5; S = 1'b1; A = 1'b0; B = 1'b0;
      #5; S = 1'b1; A = 1'b0; B = 1'b1;
      #5; S = 1'b1; A = 1'b1; B = 1'b0;
      #5; S = 1'b1; A = 1'b1; B = 1'b1;
 17
      end
      initial
      begin
      $monitor($time, " A=%b, B=%b, S=%b, X=%b", A, B, S, X);
      end
      initial
      begin
      $dumpfile("MUX2_test.vcd");
      $dumpvars(0, TB);
      end
      endmodule
```

```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ iverilog -o mux mux2.v mux2_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ vvp mux
VCD info: dumpfile MUX2_test.vcd opened for output.
                    0 A=0, B=0, S=0, X=0
                    5 A=0, B=1, S=0, X=0
                   10 A=1, B=0, S=0, X=1
                   15 A=1, B=1, S=0, X=1
                   20 A=0, B=0, S=1, X=0
                   25 A=0, B=1, S=1, X=1
                   30 A=1, B=0, S=1, X=0
                   35 A=1, B=1, S=1, X=1
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ gtkwave MUX2_test.vcd
GTKWave Analyzer v3.3.118 (w)1999-2023 BSI
[0] start time.
[40] end time.
GTKWAVE | Touch screen detected, enabling gestures.
WM Destroy
▼ SST
                         Signals
▶ ∰TB
                         Time
                         A =0
                         B =0
                         S =0
                         X =0
Type Signals
reg
    Α
    В
reg
reg
    S
wire
    Χ
▼ SST
                         Signals
                                 Waves
                         Time
▶ an TB
                         A =0
                         B=1
                         S =0
                         X =0
Туре
    Signals
reg
reg
    В
reg
    S
```

wire X





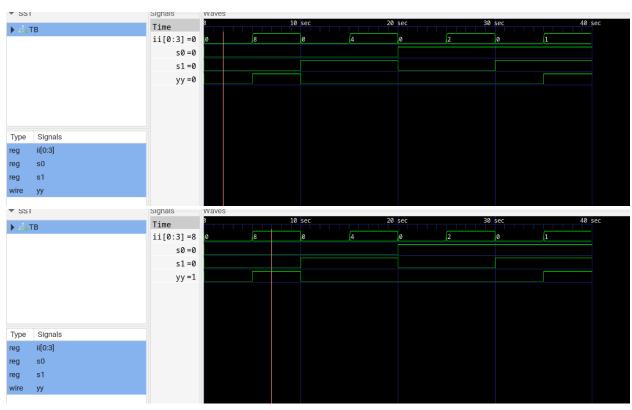
2) 4:1 MUX

iO	i1	i2	i3	s0	s1	У
0	0	0	0	0	0	0
1	0	0	0	0	0	1
0	0	0	0	0	1	0
0	1	0	0	0	1	1
0	0	0	0	1	1	0
0	0	1	0	1	1	1
0	0	0	0	1	1	0

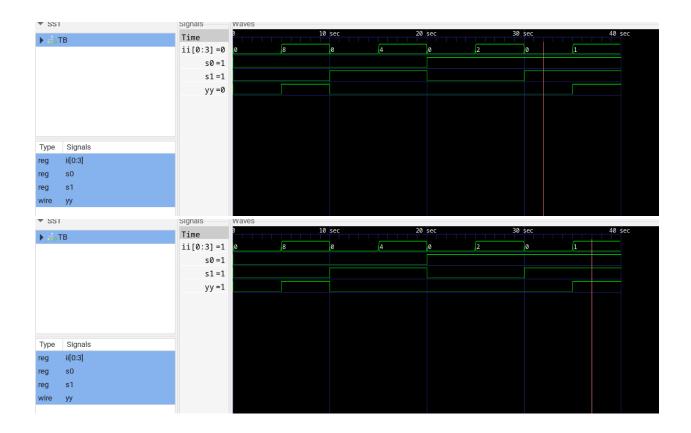
0 0 0 1 1 1 1

```
week 4 > ≡ mux4_tb.v
      module TB;
      reg [0:3] ii;
      reg s0, s1;
      wire yy;
      mux4 \ newMUX(.i(ii), .j0(s0), .j1(s1), .o(yy));
      initial begin
      \#5; ii = 4'b0000; s0 = 1'b0; s1 = 1'b0;
      #5; ii = 4'b1000; s0 = 1'b0; s1 = 1'b0;
      #5; ii = 4'b0000; s0 = 1'b0; s1 = 1'b1;
      #5; ii = 4'b0100; s0 = 1'b0; s1 = 1'b1;
      #5; ii = 4'b0000; s0 = 1'b1; s1 = 1'b0;
      #5; ii = 4'b0010; s0 = 1'b1; s1 = 1'b0;
      #5; ii = 4'b0000; s0 = 1'b1; s1 = 1'b1;
      #5; ii = 4'b0001; s0 = 1'b1; s1 = 1'b1;
      end
      initial
      begin
      $monitor($time, " ii=%b, s0=%b, s1=%b, yy=%b", ii, s0, s1, yy);
      initial begin
      $dumpfile("MUX4_test.vcd");
      $dumpvars(0, TB);
      end
      endmodule
```

```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ iverilog -o mux4 mux4.v mux4_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ vvp mux4
VCD info: dumpfile MUX4_test.vcd opened for output.
                   0 ii=0000, s0=0, s1=0, yy=0
                   5 ii=1000, s0=0, s1=0, yy=1
                  10 ii=0000, s0=0, s1=1, yy=0
                  15 ii=0100, s0=0, s1=1, yy=0
                  20 ii=0000, s0=1, s1=0, yy=0
                  25 ii=0010, s0=1, s1=0, yy=0
                  30 ii=0000, s0=1, s1=1, yy=0
                  35 ii=0001, s0=1, s1=1, yy=1
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ gtkwave MUX4_test.vcd
GTKWave Analyzer v3.3.118 (w)1999-2023 BSI
[0] start time.
[40] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.
```







3) 1:2 DEMUX

sel	in	y0	y1
0	0	0	0
0	1	1	0
1	0	0	0
1	1	0	1

```
week 4 > ≡ demux.v
       module demux(input wire i,sel,output wire y0,y1);
       assign y0 = (\sim sel) ? i : 1'b0;
       assign y1 = sel ? i : 1'b0;
       endmodule
week 4 > 3) 1:2 demux > ≡ demux_tb.v
      module TB;
      reg i;
      reg sel;
      wire y0;
      wire y1;
      demux uut (.i(i),.sel(sel),.y0(y0),.y1(y1));
      initial begin
      #0; i = 1'b0; sel = 1'b0;
      #5; i = 1'b0; sel = 1'b1;
      #5; i = 1'b1; sel = 1'b1;
 13
      end
      initial begin
      $monitor($time, " i=%b, sel=%b, y0=%b, y1=%b", i, sel, y0, y1);
      end
      initial begin
      $dumpfile("demux_test.vcd");
      $dumpvars(0, TB);
      end
      endmodule
```

```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4/3) 1:2 demux$ iverilog -o demux demux.v demux_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4/3) 1:2 demux$ vvp demux

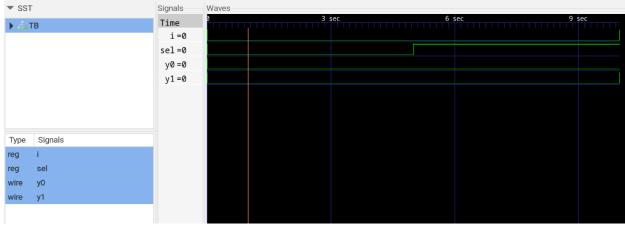
VCD info: dumpfile demux_test.vcd opened for output.

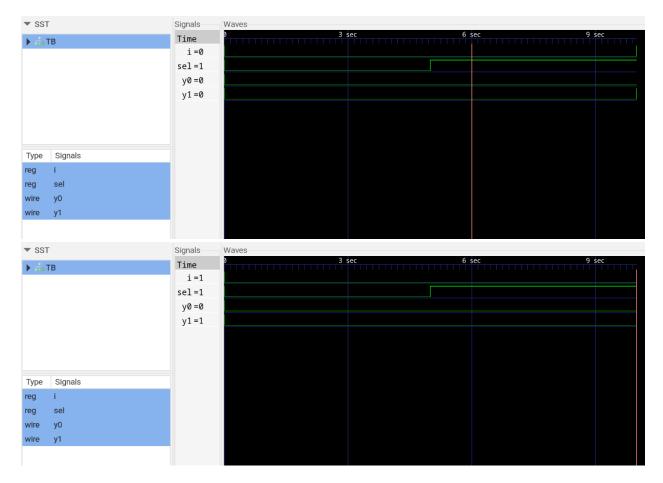
0 i=0, sel=0, y0=0, y1=0
5 i=0, sel=1, y0=0, y1=0
10 i=1, sel=1, y0=0, y1=1

rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4/3) 1:2 demux$ gtkwave demux_test.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[10] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.
```





4) ENCODER

Y3	Y2	Y1	Y0	A1	A0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

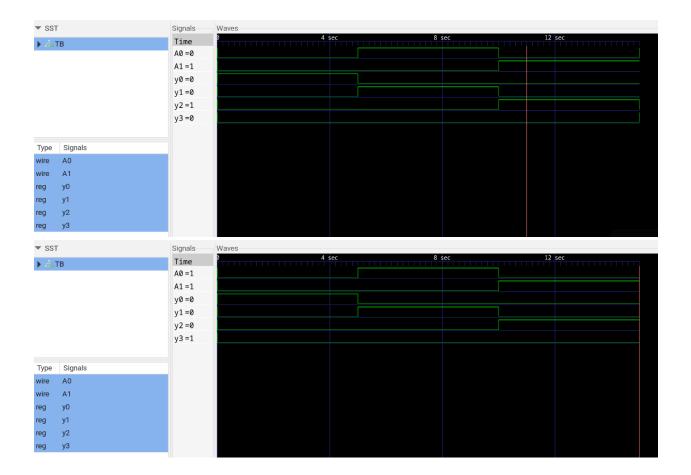
```
week 4 > \( \) encoder.v

1     module encoder4 (
2     input wire y3, y2, y1, y0,
3     output wire A1, A0
4     );
5
6     assign {A1, A0} = (y3 ? 2'b11 :
7     y2 ? 2'b10 :
8     y1 ? 2'b01 :
9     y0 ? 2'b00 : 2'b00);
10     endmodule
11
```

```
week 4 > ≡ encoder_tb.v
      module TB;
      reg y3, y2, y1, y0;
      wire A1, A0;
      encoder4 uut (.y3(y3),.y2(y2),.y1(y1),.y0(y0),.A1(A1),.A0(A0));
 8 initial begin
      #0; y3 = 1'b0; y2 = 1'b0; y1 = 1'b0; y0 = 1'b1;
      \#5; y3 = 1'b0; y2 = 1'b0; y1 = 1'b1; y0 = 1'b0;
      \#5; y3 = 1'b0; y2 = 1'b1; y1 = 1'b0; y0 = 1'b0;
      #5; y3 = 1'b1; y2 = 1'b0; y1 = 1'b0; y0 = 1'b0;
      end
      initial begin
      $monitor($time, " y3=%b, y2=%b, y1=%b, y0=%b, A1=%b, A0=%b", y3, y2, y1, y0, A1, A0);
      initial begin
      $dumpfile("encoder4_test.vcd");
      $dumpvars(0, TB);
      end
      endmodule
```

```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ iverilog -o encoder encoder.v encoder_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ vvp encoder
VCD info: dumpfile encoder4_test.vcd opened for output.
                    0 y3=0, y2=0, y1=0, y0=1, A1=0, A0=0
                    5 y3=0, y2=0, y1=1, y0=0, A1=0, A0=1
                   10 y3=0, y2=1, y1=0, y0=0, A1=1, A0=0
                   15 y3=1, y2=0, y1=0, y0=0, A1=1, A0=1
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ gtkwave encoder4_test.vcd
GTKWave Analyzer v3.3.118 (w)1999-2023 BSI
[0] start time.
[15] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.
▼ SST
                        Signals
                                Waves
▶ and TB
                        Time
                        A0 =0
                        A1 =0
                        y0 =1
                        y1 =0
                        y2 =0
                        y3 =0
Type Signals
wire A0
wire A1
reg y0
reg y1
reg
    уЗ
reg
▼ SST
                        Time
▶ am TB
                        A0 =1
                        A1 =0
                        y0 =0
                        y1=1
                        y2 =0
                        y3 =0
Type Signals
wire
    Α0
wire A1
reg y0
reg y1
reg y2
```

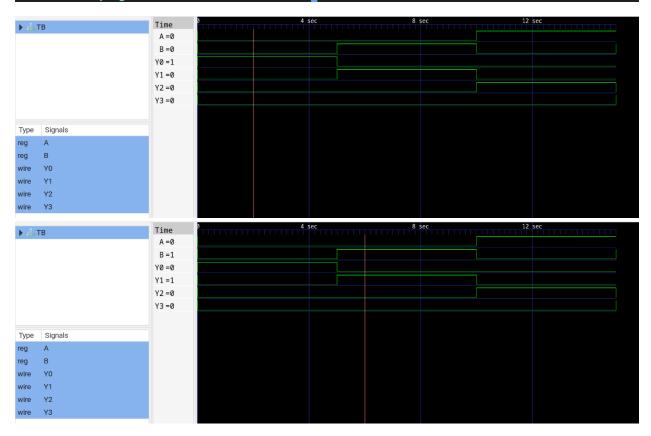
уЗ

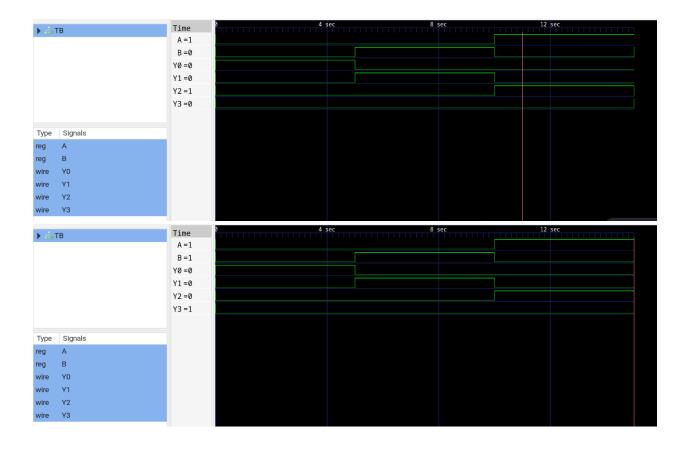


5) DECODER

Α	В	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

```
week 4 > ≡ decoder.v
        module decoder2to4 (
             input wire A, B,
   3
             output wire Y0, Y1, Y2, Y3
             assign Y0 = ~A \& ~B;
                                          // Y0 is active when A = 0, B = 0
             assign Y1 = ~A & B;
                                          // Y1 is active when A = 0, B = 1
             assign Y2 = A & \simB; // Y2 is active when A = 1, B = 0 assign Y3 = A & B; // Y3 is active when A = 1, B = 1
        endmodule
week 4 > ≡ decoder_tb.v
     module TB;
      reg A, B;
      decoder2to4 uut (.A(A),.B(B),.Y0(Y0),.Y1(Y1),.Y2(Y2),.Y3(Y3));
     initial begin
     #0; A = 1'b0; B = 1'b0;
      #5; A = 1'b0; B = 1'b1;
      #5; A = 1'b1; B = 1'b0;
      #5; A = 1'b1; B = 1'b1;
      initial begin
      $monitor($time, " A=%b, B=%b, Y0=%b, Y1=%b, Y2=%b, Y3=%b", A, B, Y0, Y1, Y2, Y3);
      end
      initial begin
      $dumpfile("decoder2to4_test.vcd");
      $dumpvars(0, TB);
      end
      endmodule
```





If found plagiarized, I will abide with the disciplinary action of the University.

Signature:

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Date: 30/08/2024