Digital Design and Computer Organization Laboratory

3rd Semester, Academic Year 2024

Date: 30/08/2024

Name: Rithvik Rajesh Matta	SRN: PES2UG23CS485	Section: H

Week#____4_____

TITLE:

- **Design 2:1 MUX**
- **Design 4:1 MUX using 2:1 MUX**
- **Design 1:2 DeMUX**
- **Design an Encoder**
- **Design a Decoder**

GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

1) 2:1 MUX

i_0	i_1	j	y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

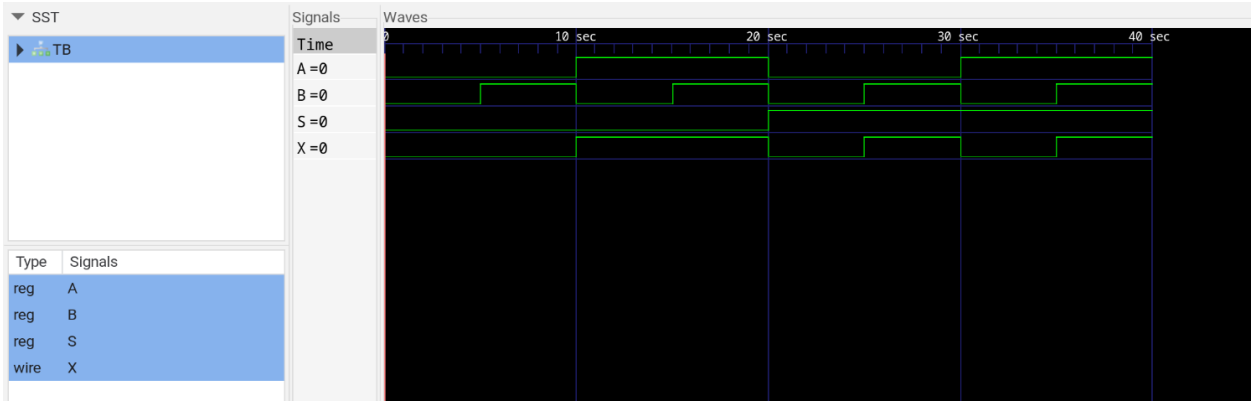
week 4 > mux2.v

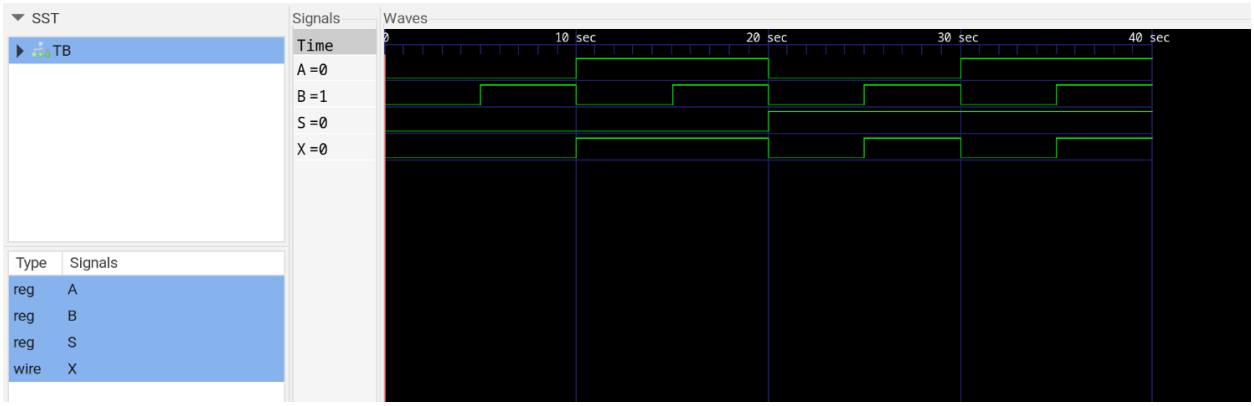
```v
module mux2 (input wire i0, i1, j, output wire o);
    assign o = j ? i1 : i0;
endmodule
```

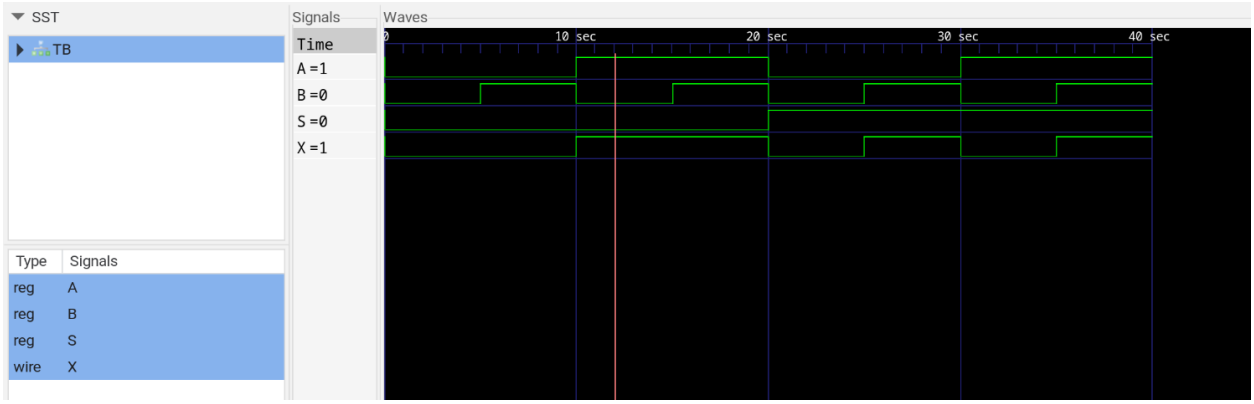
week 4 > mux2_tb.v

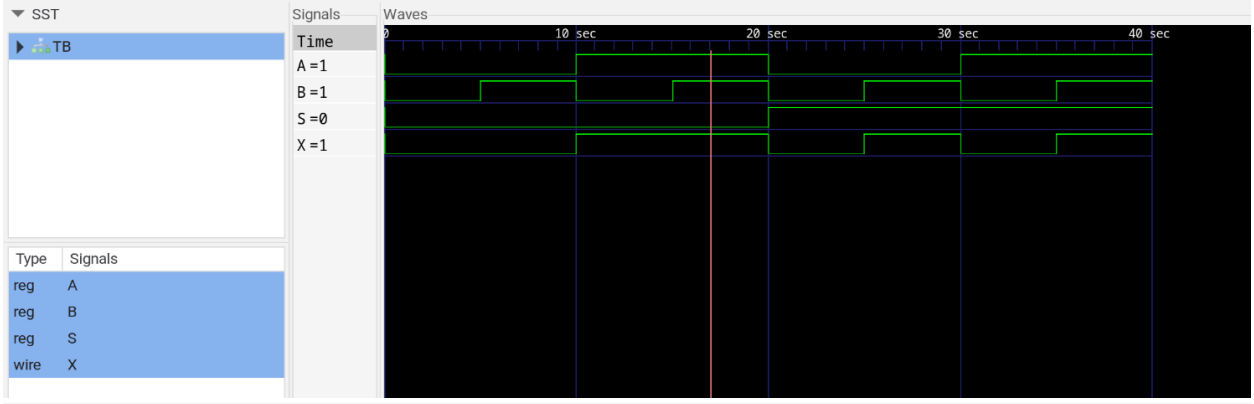
```v
module TB;
reg A, B, S;
wire X;

mux2 newMUX (.i0(A), .i1(B), .j(S), .o(X));

initial
begin
#5; S = 1'b0; A = 1'b0; B = 1'b0;
#5; S = 1'b0; A = 1'b0; B = 1'b1;
#5; S = 1'b0; A = 1'b1; B = 1'b0;
#5; S = 1'b0; A = 1'b1; B = 1'b1;
#5; S = 1'b1; A = 1'b0; B = 1'b0;
#5; S = 1'b1; A = 1'b0; B = 1'b1;
#5; S = 1'b1; A = 1'b1; B = 1'b0;
#5; S = 1'b1; A = 1'b1; B = 1'b1;
end

initial
begin
$monitor($time, " A=%b, B=%b, S=%b, X=%b", A, B, S, X);
end

initial
begin
$dumpfile("MUX2_test.vcd");
$dumpvars(0, TB);
end
endmodule
```

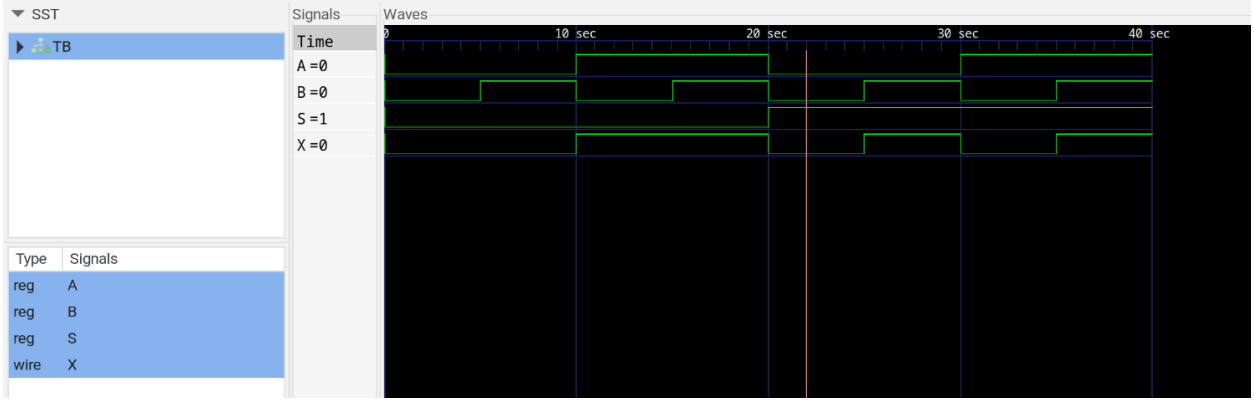
```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ iverilog -o mux mux2.v mux2_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ vvp mux
VCD info: dumpfile MUX2_test.vcd opened for output.
                   0 A=0, B=0, S=0, X=0
                   5 A=0, B=1, S=0, X=0
                  10 A=1, B=0, S=0, X=1
                  15 A=1, B=1, S=0, X=1
                  20 A=0, B=0, S=1, X=0
                  25 A=0, B=1, S=1, X=1
                  30 A=1, B=0, S=1, X=0
                  35 A=1, B=1, S=1, X=1
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ gtkwave MUX2_test.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[40] end time.
GTKWAVE | Touch screen detected, enabling gestures.
WM Destroy
```

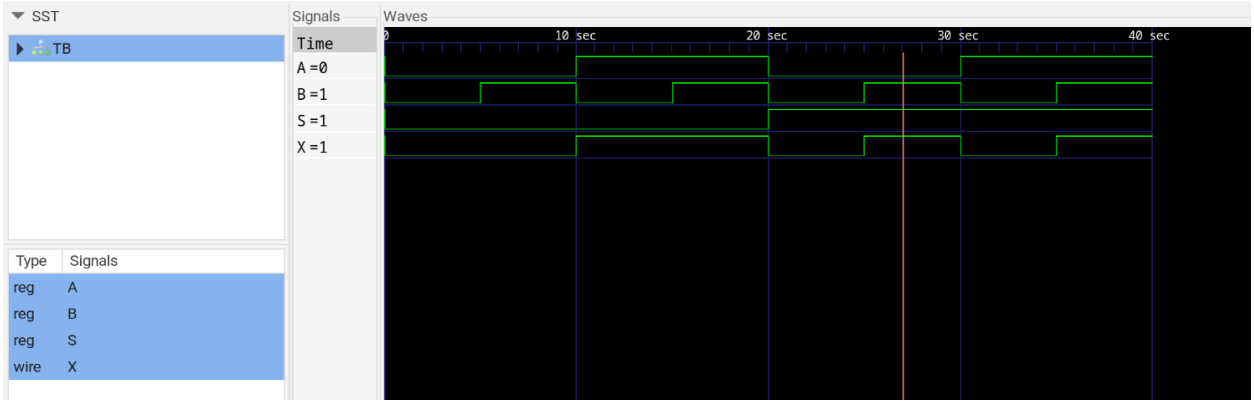


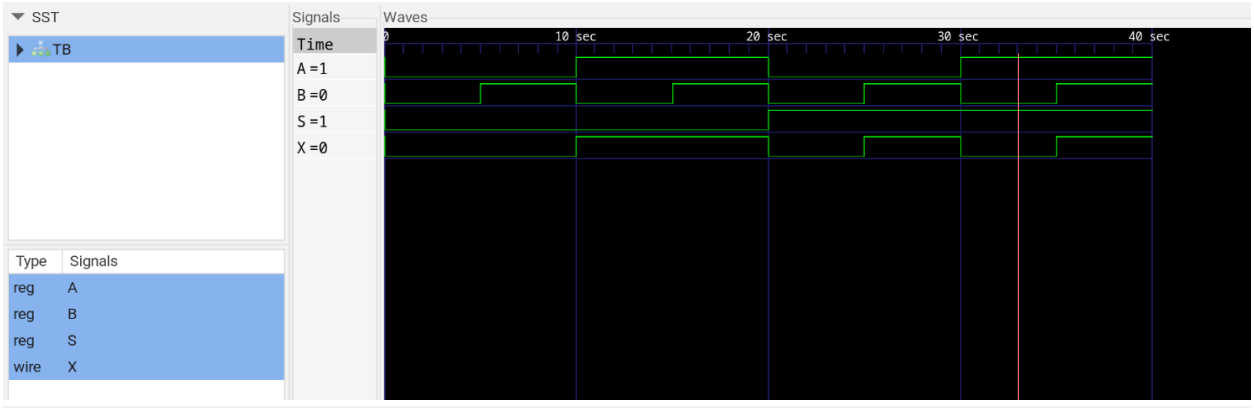


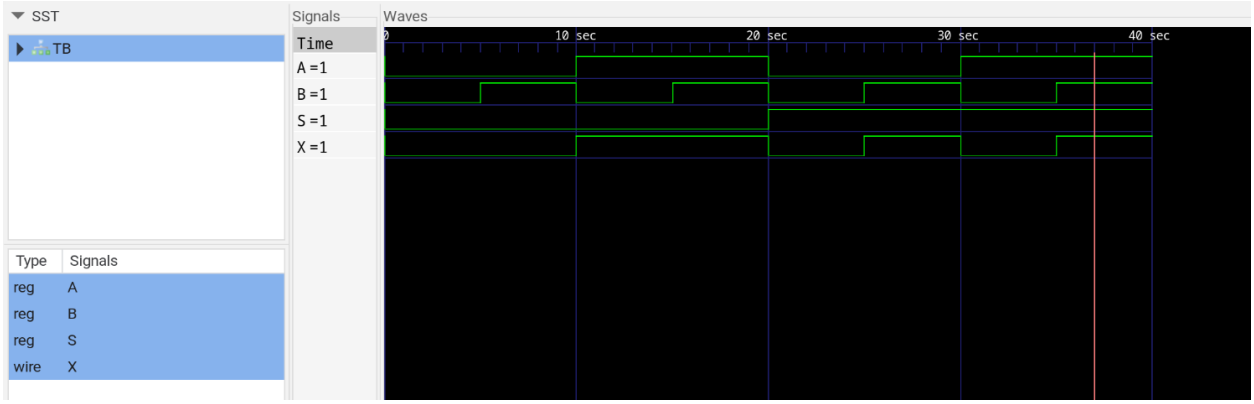

SST
TB
Type
Signals
reg
A
reg
B
reg
S
wire
X
Signals
Waves
Time
A =1
B =0
S =0
X =1
0
10 sec
20 sec
30 sec
40 sec


SST
TB
Type
Signals
reg
A
reg
B
reg
S
wire
X
Signals
Waves
Time
A =1
B =1
S =0
X =1
0
10 sec
20 sec
30 sec
40 sec


SST
TB
Type
Signals
reg
A
reg
B
reg
S
wire
X
Signals
Waves
Time
A =0
B =0
S =1
X =0
0
10 sec
20 sec
30 sec
40 sec


SST
TB
Type
Signals
reg
A
reg
B
reg
S
wire
X
Signals
Waves
Time
A =0
B =1
S =1
X =1
0
10 sec
20 sec
30 sec
40 sec

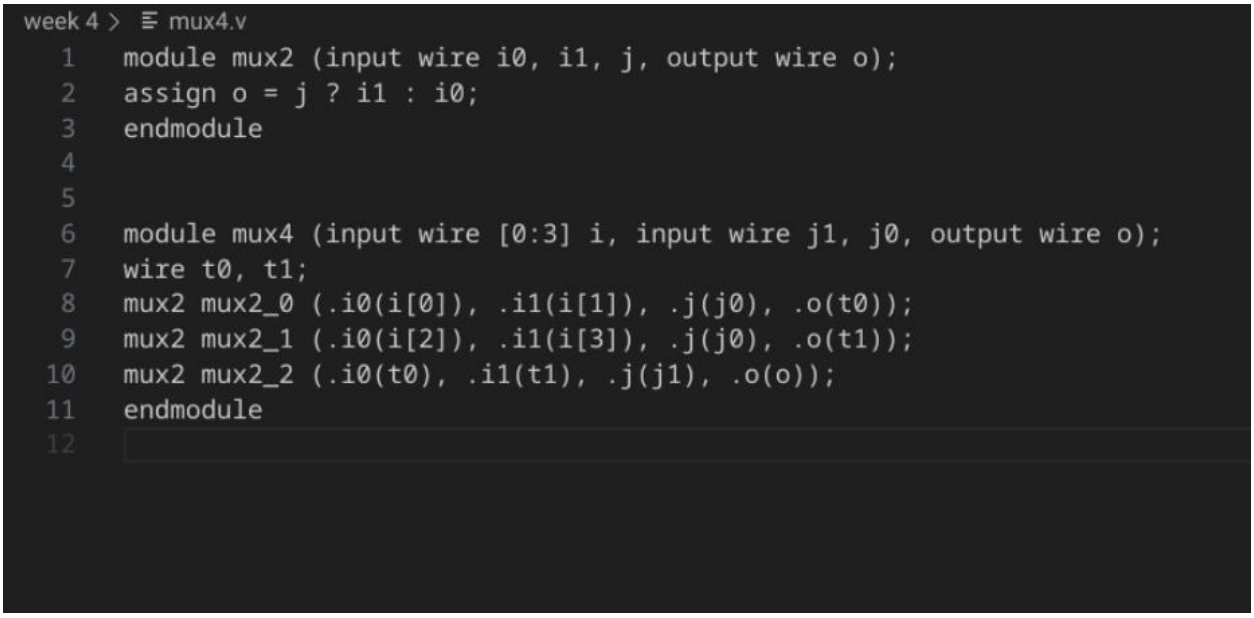




2) 4:1 MUX

i0	i1	i2	i3	s0	s1	y
0	0	0	0	0	0	**0**
1	0	0	0	0	0	**1**
0	0	0	0	0	1	**0**
0	1	0	0	0	1	**1**
0	0	0	0	1	1	**0**
0	0	1	0	1	1	**1**
0	0	0	0	1	1	**0**

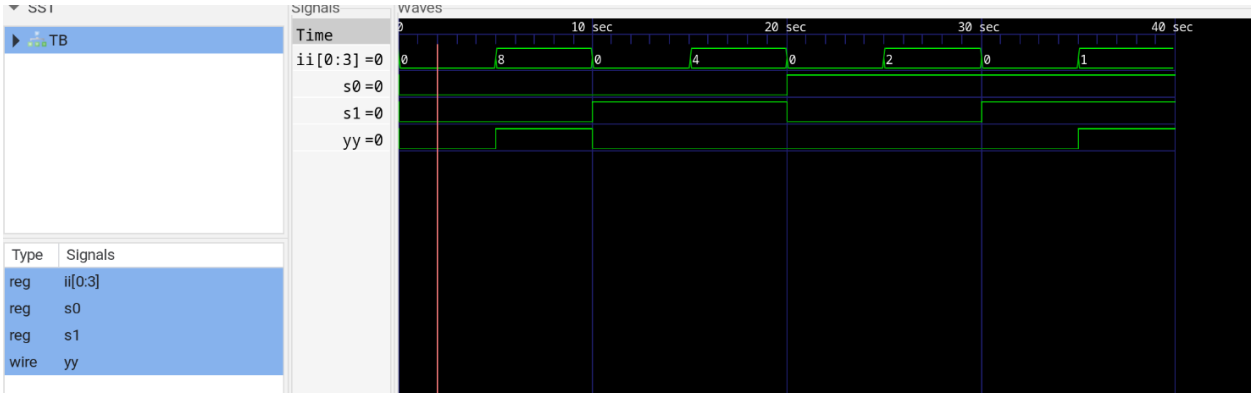
0	0	0	1	1	1	1

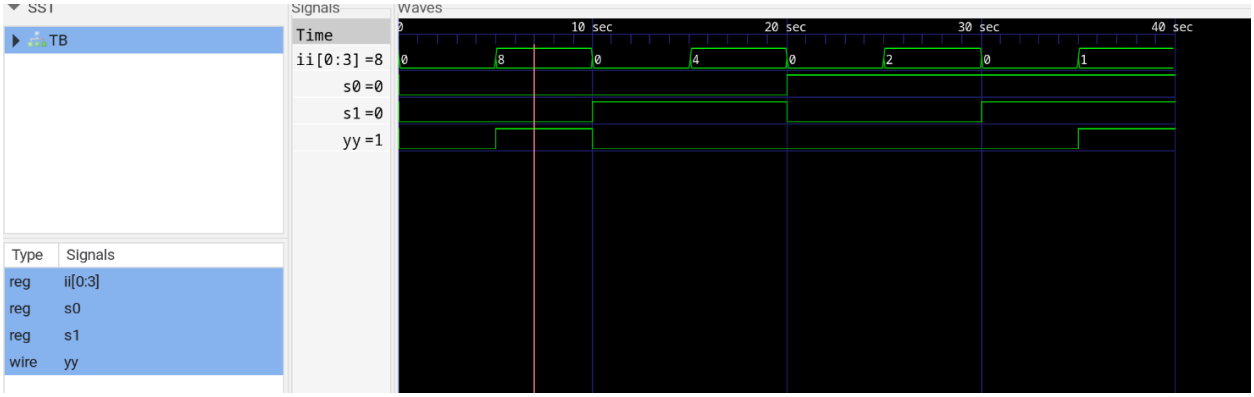

week 4 > mux4.v
1 module mux2 (input wire i0, i1, j, output wire o);
2 assign o = j ? i1 : i0;
3 endmodule
4
5
6 module mux4 (input wire [0:3] i, input wire j1, j0, output wire o);
7 wire t0, t1;
8 mux2 mux2_0 (.i0(i[0]), .i1(i[1]), .j(j0), .o(t0));
9 mux2 mux2_1 (.i0(i[2]), .i1(i[3]), .j(j0), .o(t1));
10 mux2 mux2_2 (.i0(t0), .i1(t1), .j(j1), .o(o));
11 endmodule
12

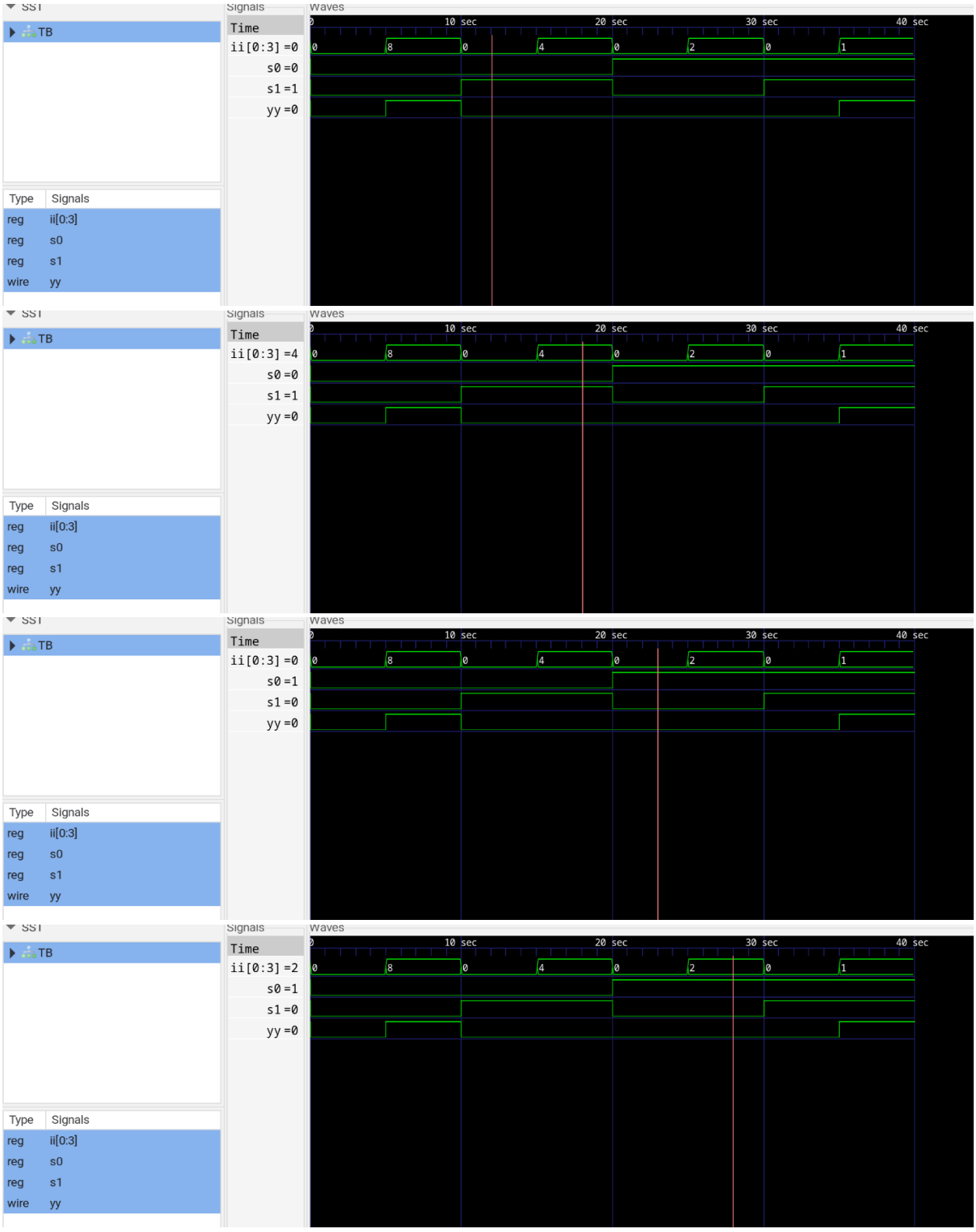
week 4 > mux4_tb.v

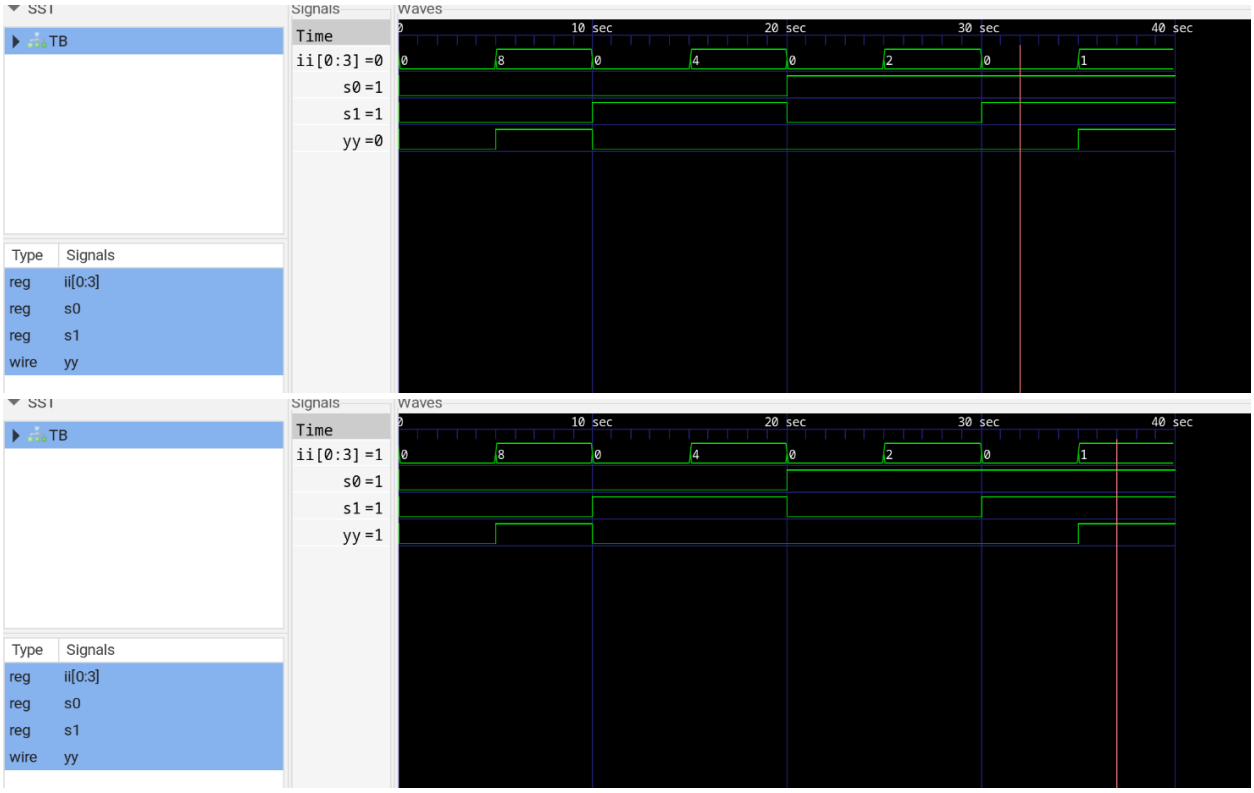
```
module TB;

reg [0:3] ii;
reg s0, s1;
wire yy;

mux4 newMUX(.i(ii), .j0(s0), .j1(s1), .o(yy));

initial begin
#5; ii = 4'b0000; s0 = 1'b0; s1 = 1'b0;
#5; ii = 4'b1000; s0 = 1'b0; s1 = 1'b0;
#5; ii = 4'b0000; s0 = 1'b0; s1 = 1'b1;
#5; ii = 4'b0100; s0 = 1'b0; s1 = 1'b1;
#5; ii = 4'b0000; s0 = 1'b1; s1 = 1'b0;
#5; ii = 4'b0010; s0 = 1'b1; s1 = 1'b0;
#5; ii = 4'b0000; s0 = 1'b1; s1 = 1'b1;
#5; ii = 4'b0001; s0 = 1'b1; s1 = 1'b1;
end

initial
begin
$monitor($time, " ii=%b, s0=%b, s1=%b, yy=%b", ii, s0, s1, yy);
end


initial begin
$dumpfile("MUX4_test.vcd");
$dumpvars(0, TB);
end

endmodule
```

```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ iverilog -o mux4 mux4.v mux4_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ vvp mux4
VCD info: dumpfile MUX4_test.vcd opened for output.
                   0 ii=0000, s0=0, s1=0, yy=0
                   5 ii=1000, s0=0, s1=0, yy=1
                  10 ii=0000, s0=0, s1=1, yy=0
                  15 ii=0100, s0=0, s1=1, yy=0
                  20 ii=0000, s0=1, s1=0, yy=0
                  25 ii=0010, s0=1, s1=0, yy=0
                  30 ii=0000, s0=1, s1=1, yy=0
                  35 ii=0001, s0=1, s1=1, yy=1
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ gtkwave MUX4_test.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[40] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.
```






SST
TB
Type
Signals
reg
ii[0:3]
reg
s0
reg
s1
wire
yy
Signals
Waves
Time
ii[0:3] =0
s0 =0
s1 =1
yy =0
10 sec
20 sec
30 sec
40 sec
ii[0:3] =4
ii[0:3] =0
s0 =1
s1 =0
ii[0:3] =2



3) 1:2 DEMUX

sel	in	y0	y1
0	0	0	0
0	1	1	0
1	0	0	0
1	1	0	1

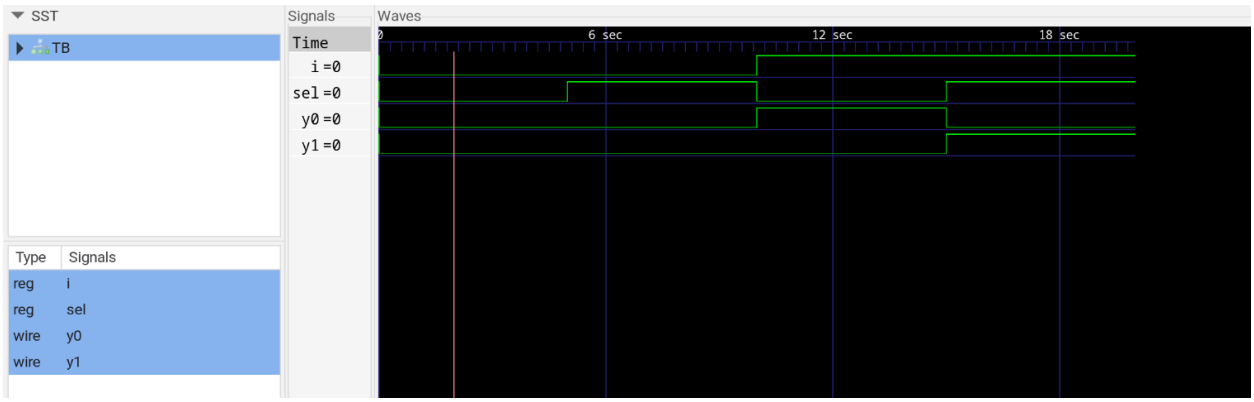
week 4 > demux.v

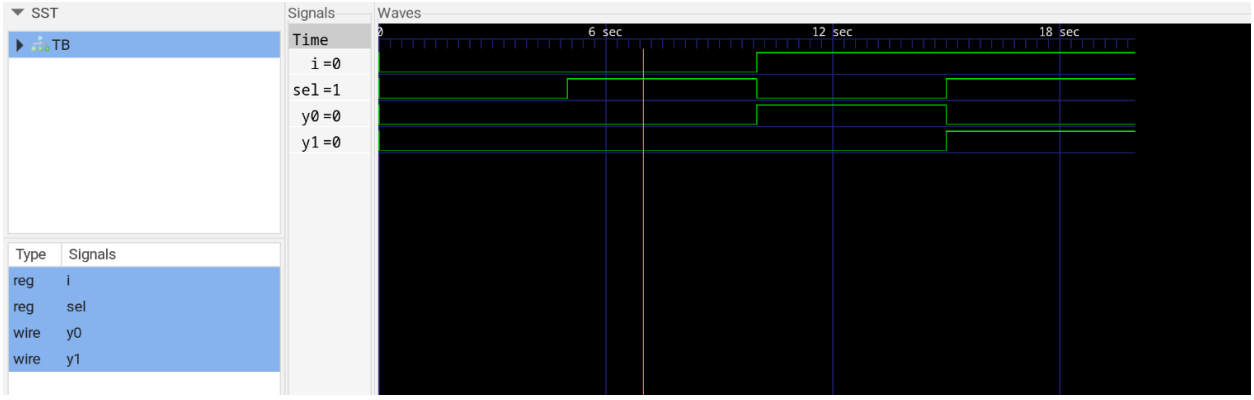
```v
module demux(input wire i,sel,output wire y0,y1);
assign y0 = (~sel) ? i : 1'b0;
assign y1 = sel ? i : 1'b0;
endmodule
```

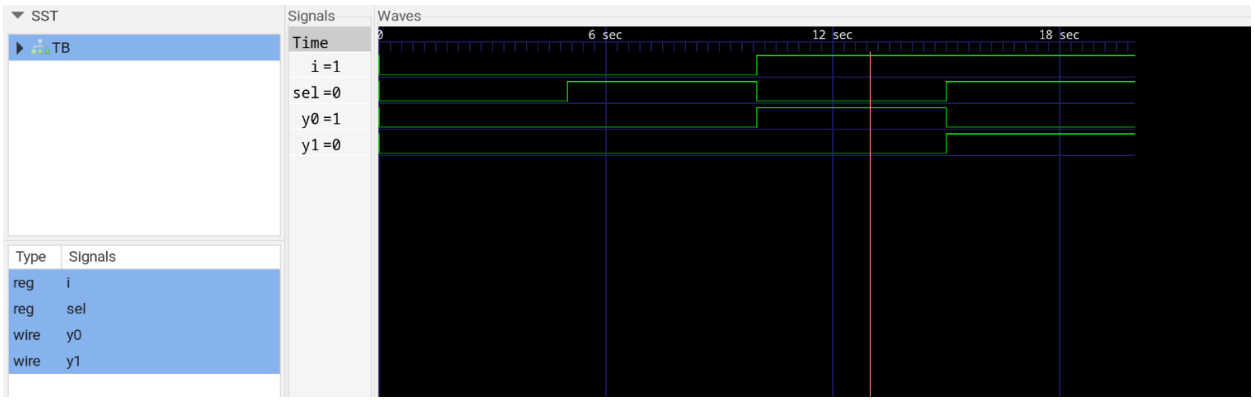
week 4 > 3) 1:2 demux > demux_tb.v

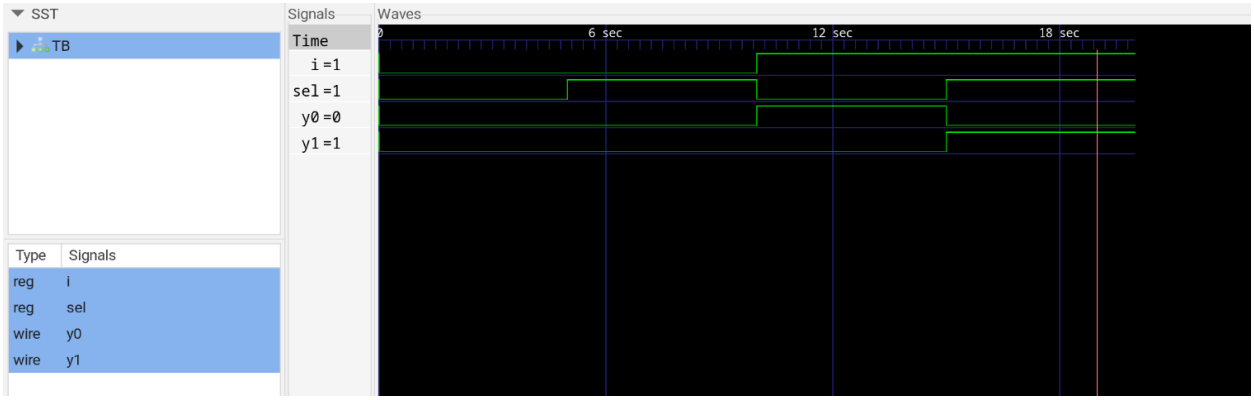
```v
module TB;
reg i;
reg sel;
wire y0;
wire y1;

demux uut (.i(i),.sel(sel),.y0(y0),.y1(y1));

initial begin
#0; i = 1'b0; sel = 1'b0;
#5; i = 1'b0; sel = 1'b1;
#5; i = 1'b1; sel = 1'b0;
#5; i = 1'b1; sel = 1'b1;
#5;
end

initial begin
$monitor($time, " i=%b, sel=%b, y0=%b, y1=%b", i, sel, y0, y1);
end

initial begin
$dumpfile("demux_test.vcd");
$dumpvars(0, TB);
end
endmodule
```

```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4/3) 1:2 demux$ iverilog -o demux demux.v demux_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4/3) 1:2 demux$ vvp demux
VCD info: dumpfile demux_test.vcd opened for output.
                   0 i=0, sel=0, y0=0, y1=0
                   5 i=0, sel=1, y0=0, y1=0
                  10 i=1, sel=0, y0=1, y1=0
                  15 i=1, sel=1, y0=0, y1=1
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4/3) 1:2 demux$ gtkwave demux_test.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[20] end time.
GTKWAVE | Touch screen detected, enabling gestures.
WM Destroy
```









4) ENCODER

Y3	Y2	Y1	Y0	A1	A0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

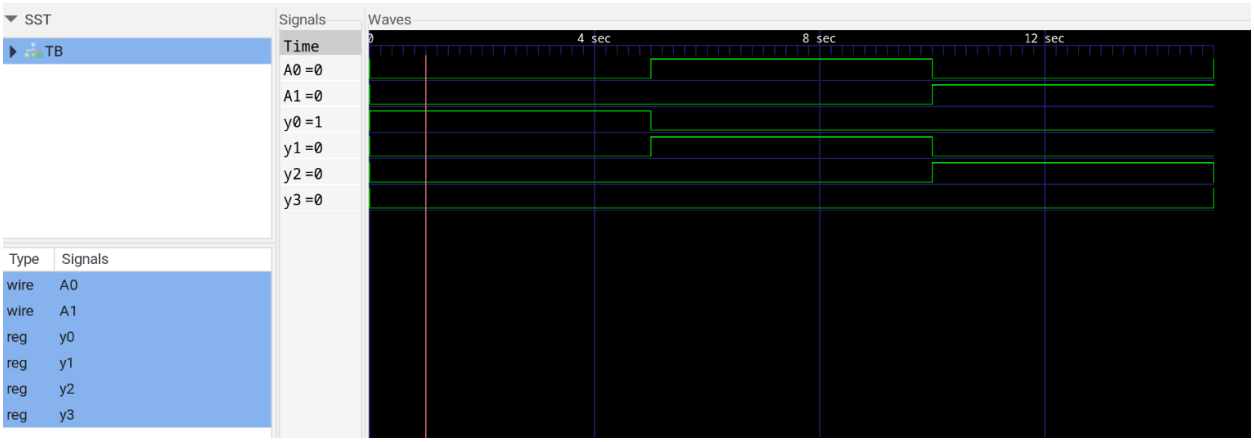
week 4 > encoder.v

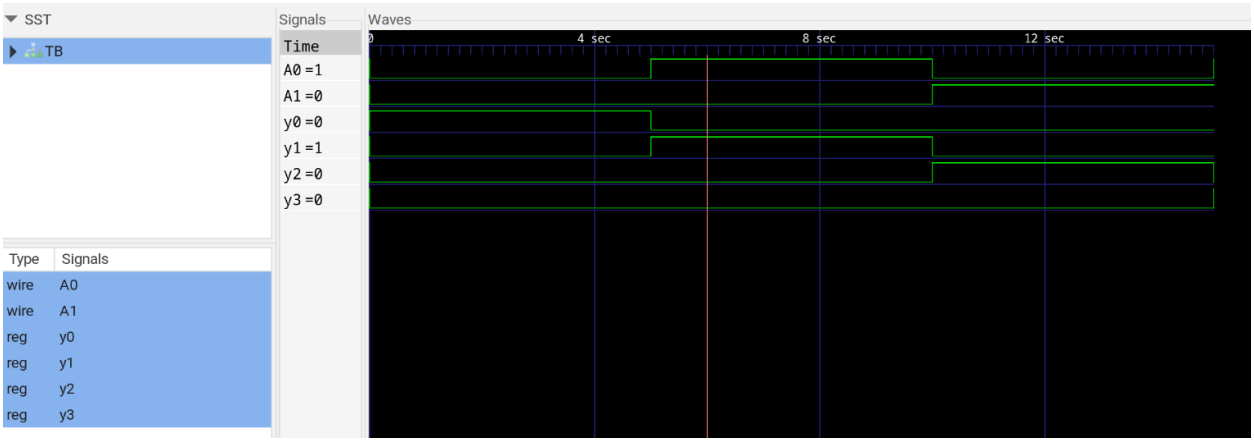
```
module encoder4 (
input wire y3, y2, y1, y0,
output wire A1, A0
);

assign {A1, A0} = (y3 ? 2'b11 :
y2 ? 2'b10 :
y1 ? 2'b01 :
y0 ? 2'b00 : 2'b00);
endmodule

```

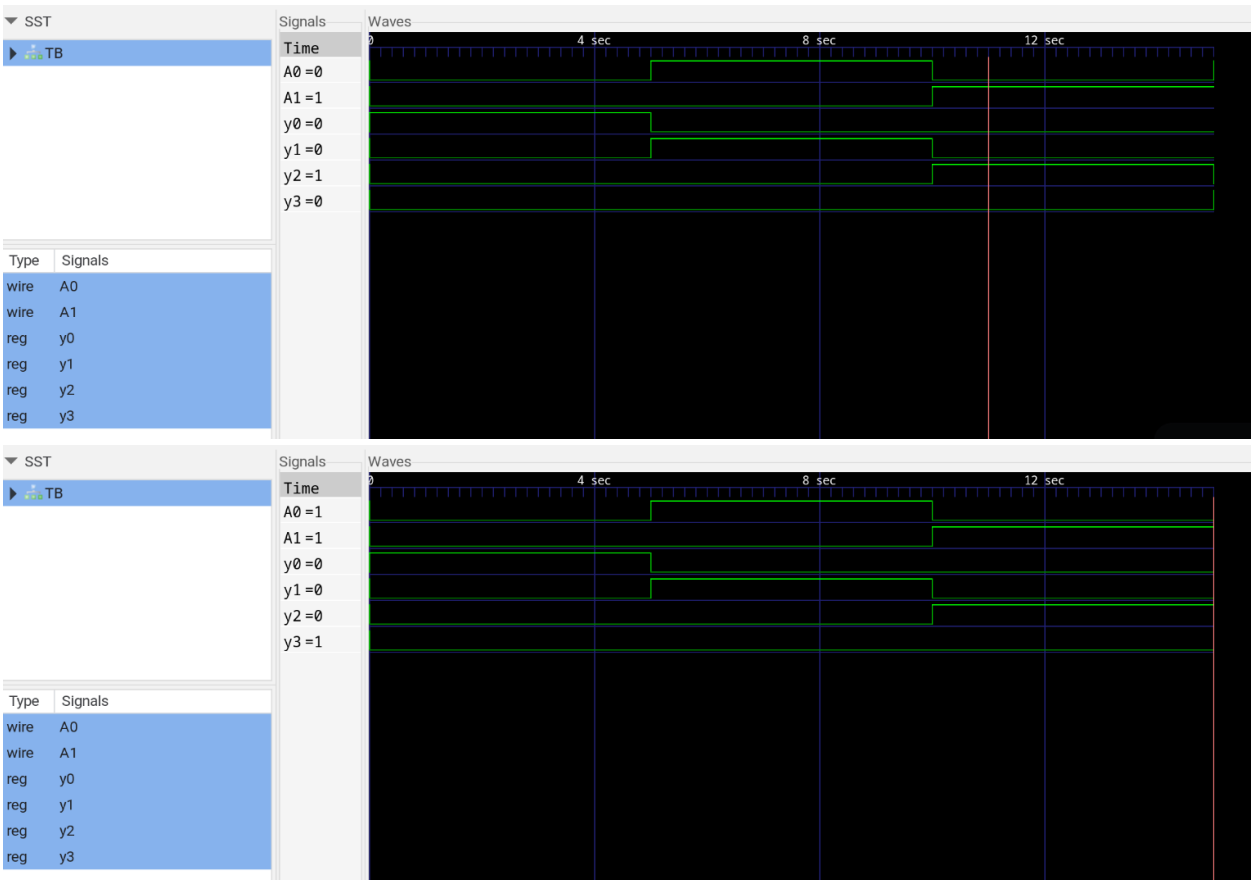
week 4 > encoder_tb.v

```
module TB;

reg y3, y2, y1, y0;
wire A1, A0;

encoder4 uut (.y3(y3),.y2(y2),.y1(y1),.y0(y0),.A1(A1),.A0(A0));

initial begin
#0; y3 = 1'b0; y2 = 1'b0; y1 = 1'b0; y0 = 1'b1;
#5; y3 = 1'b0; y2 = 1'b0; y1 = 1'b1; y0 = 1'b0;
#5; y3 = 1'b0; y2 = 1'b1; y1 = 1'b0; y0 = 1'b0;
#5; y3 = 1'b1; y2 = 1'b0; y1 = 1'b0; y0 = 1'b0;
end

initial begin
$monitor($time, " y3=%b, y2=%b, y1=%b, y0=%b, A1=%b, A0=%b", y3, y2, y1, y0, A1, A0);
end

initial begin
$dumpfile("encoder4_test.vcd");
$dumpvars(0, TB);
end

endmodule
```

```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ iverilog -o encoder encoder.v encoder_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ vvp encoder
VCD info: dumpfile encoder4_test.vcd opened for output.
                   0 y3=0, y2=0, y1=0, y0=1, A1=0, A0=0
                   5 y3=0, y2=0, y1=1, y0=0, A1=0, A0=1
                  10 y3=0, y2=1, y1=0, y0=0, A1=1, A0=0
                  15 y3=1, y2=0, y1=0, y0=0, A1=1, A0=1
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ gtkwave encoder4_test.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[15] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.
```







5) DECODER

A	B	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

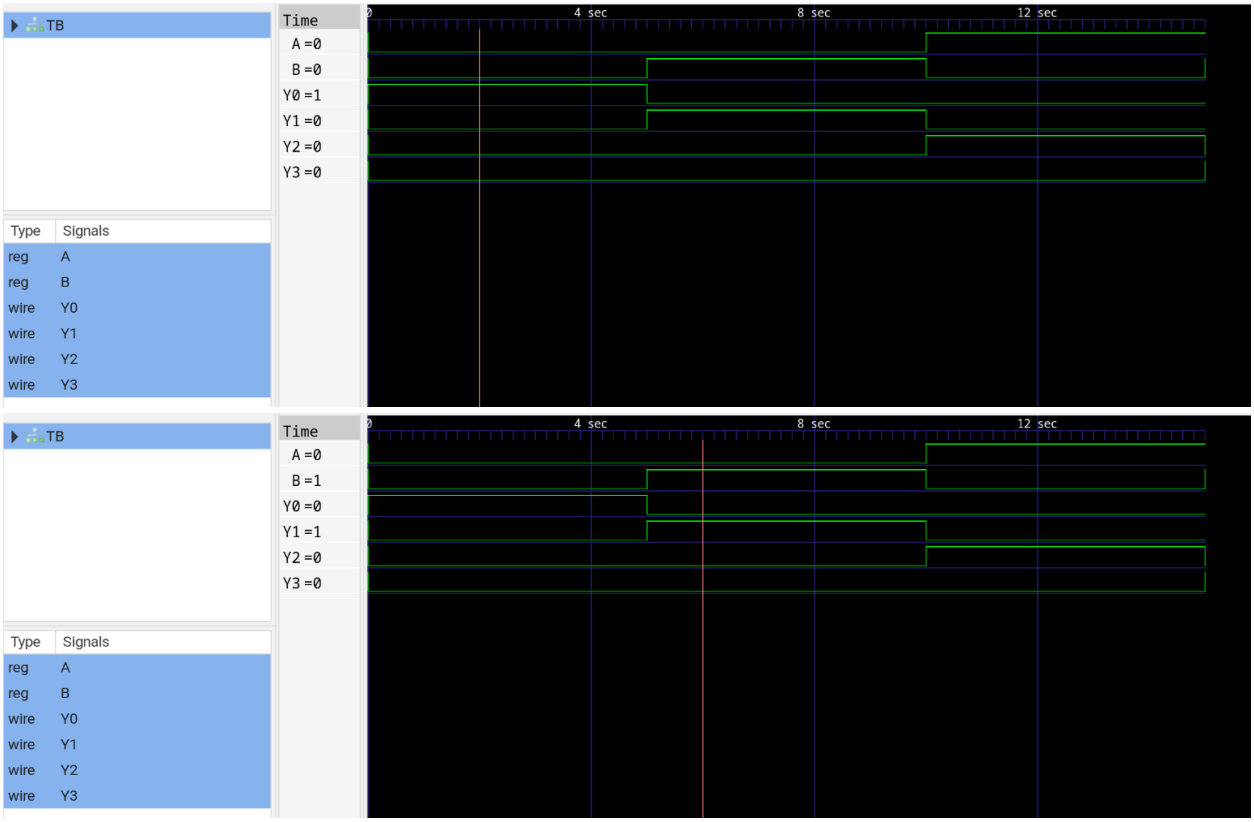
week 4 > decoder.v

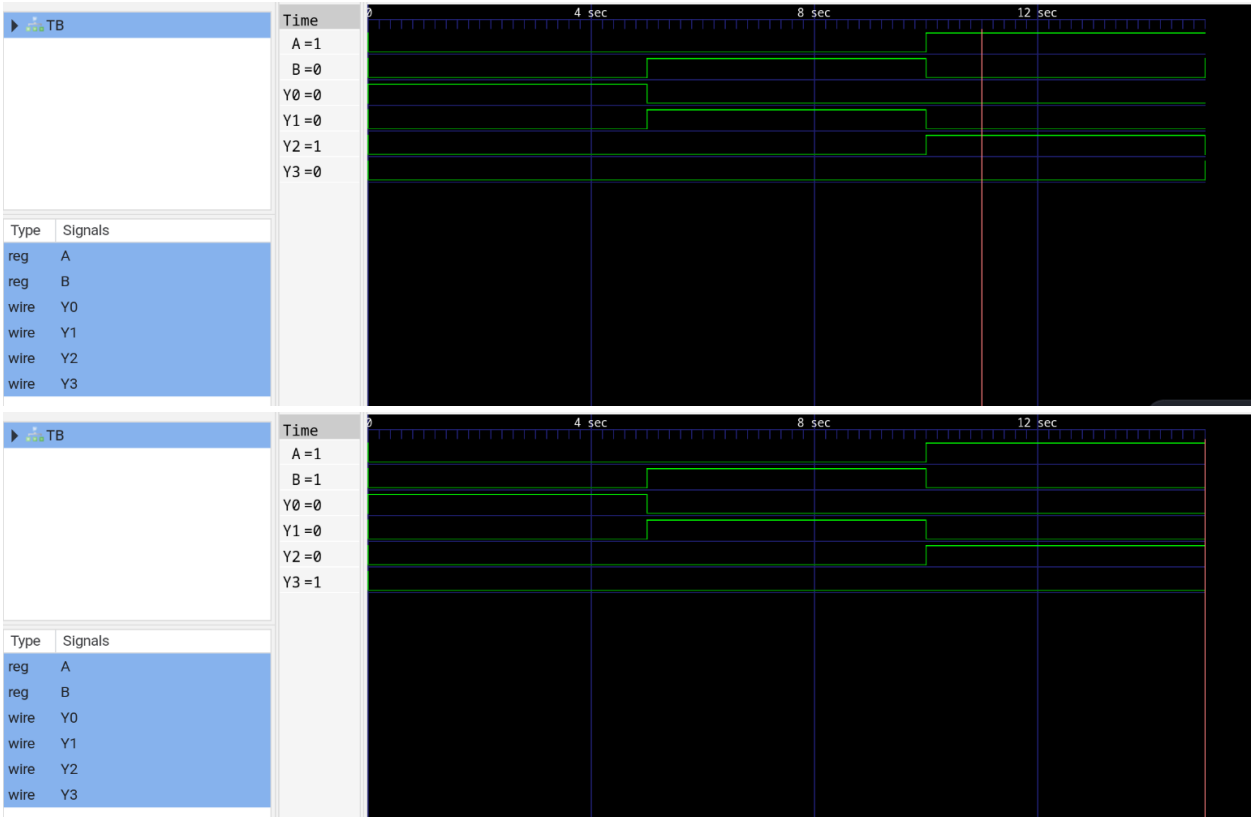
```
module decoder2to4 (
    input wire A, B,
    output wire Y0, Y1, Y2, Y3
);
    assign Y0 = ~A & ~B;    // Y0 is active when A = 0, B = 0
    assign Y1 = ~A & B;     // Y1 is active when A = 0, B = 1
    assign Y2 = A & ~B;     // Y2 is active when A = 1, B = 0
    assign Y3 = A & B;      // Y3 is active when A = 1, B = 1
endmodule
```

week 4 > decoder_tb.v

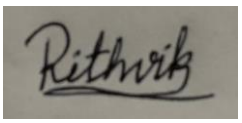
```
module TB;

reg A, B;
wire Y0, Y1, Y2, Y3;

decoder2to4 uut (.A(A),.B(B),.Y0(Y0),.Y1(Y1),.Y2(Y2),.Y3(Y3));

initial begin
#0; A = 1'b0; B = 1'b0;
#5; A = 1'b0; B = 1'b1;
#5; A = 1'b1; B = 1'b0;
#5; A = 1'b1; B = 1'b1;
end

initial begin
$monitor($time, " A=%b, B=%b, Y0=%b, Y1=%b, Y2=%b, Y3=%b", A, B, Y0, Y1, Y2, Y3);
end

initial begin
$dumpfile("decoder2to4_test.vcd");
$dumpvars(0, TB);
end

endmodule
```

```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ iverilog -o decoder decoder.v decoder_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ vvp decoder
VCD info: dumpfile decoder2to4_test.vcd opened for output.
                   0 A=0, B=0, Y0=1, Y1=0, Y2=0, Y3=0
                   5 A=0, B=1, Y0=0, Y1=1, Y2=0, Y3=0
                  10 A=1, B=0, Y0=0, Y1=0, Y2=1, Y3=0
                  15 A=1, B=1, Y0=0, Y1=0, Y2=0, Y3=1
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$ gtkwave decoder2to4_test.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[15] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 4$
```





If found plagiarized, I will abide with the disciplinary action of the University.

Signature: 

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