Digital Design and Computer Organization Laboratory

3rd Semester, Academic Year 2024

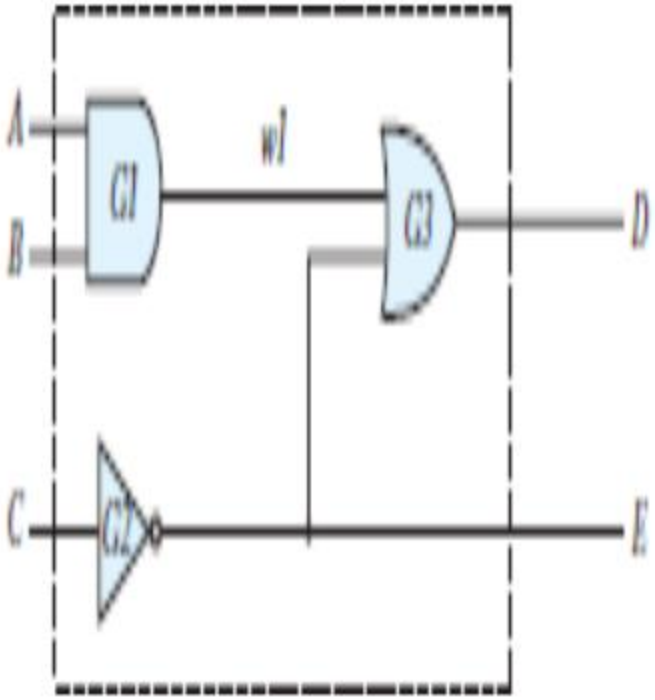
Date: 09/08/2024

Name: Rithvik Rajesh Matta	SRN: PES2UG23CS485	Section: H

Week#____2_____

TITLE:

WRITE A VERILOG PROGRAM TO MODEL A SIMPLE CIRCUIT. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE



A	B	C	D	E
0	0	0	1	1
0	0	1	0	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	0	0

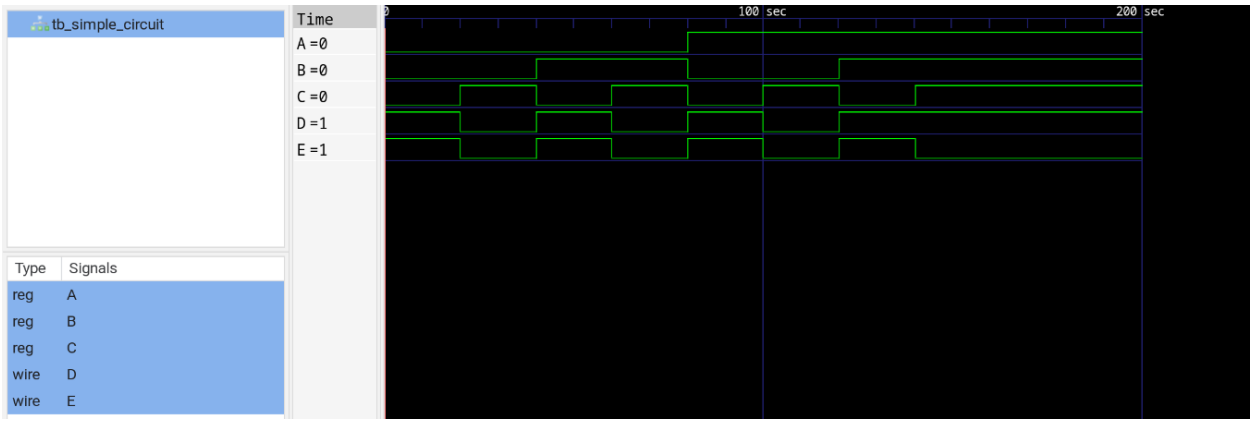
week 2 > simple_circuit1.v

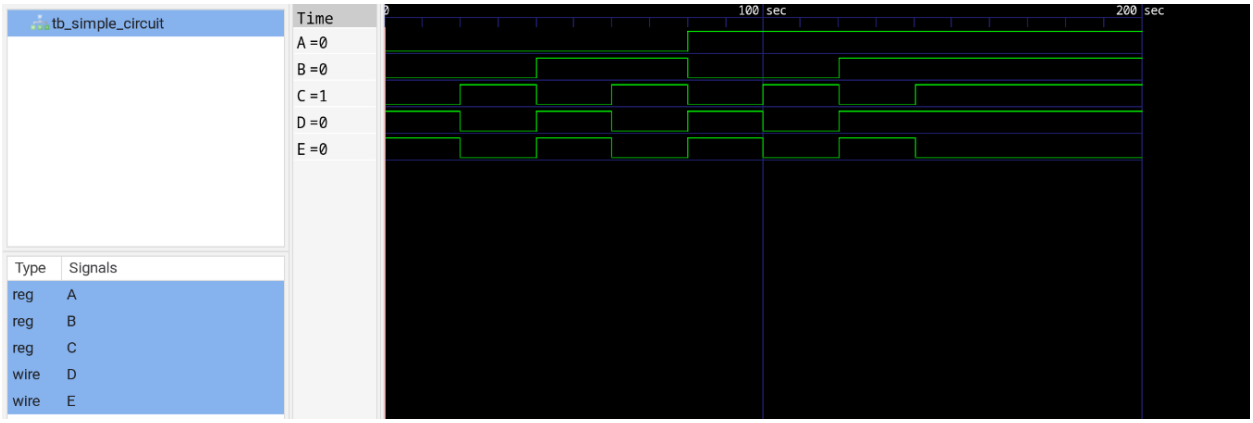
```v
module andgate (y, a, b);
input a, b;
output y;
assign y = a & b;
endmodule

module orgate (y, a, b);
input a, b;
output y;
assign y = a | b;
endmodule

module notgate (y, a);
input a;
output y;
assign y = !a;
endmodule

module simple_circuit1 (A, B, C, D, E);
output D, E;
input A, B, C;
wire w1;
andgate G1 (w1, A, B);
notgate G2 (E, C);
orgate G3 (D, w1, E);
endmodule
```

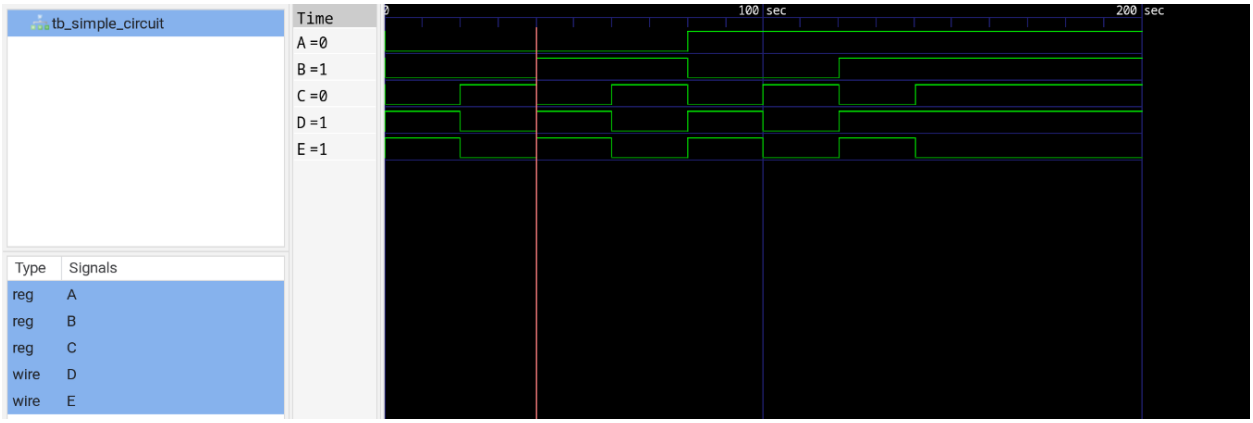
week 2 > C simple_circuit1_tb.v

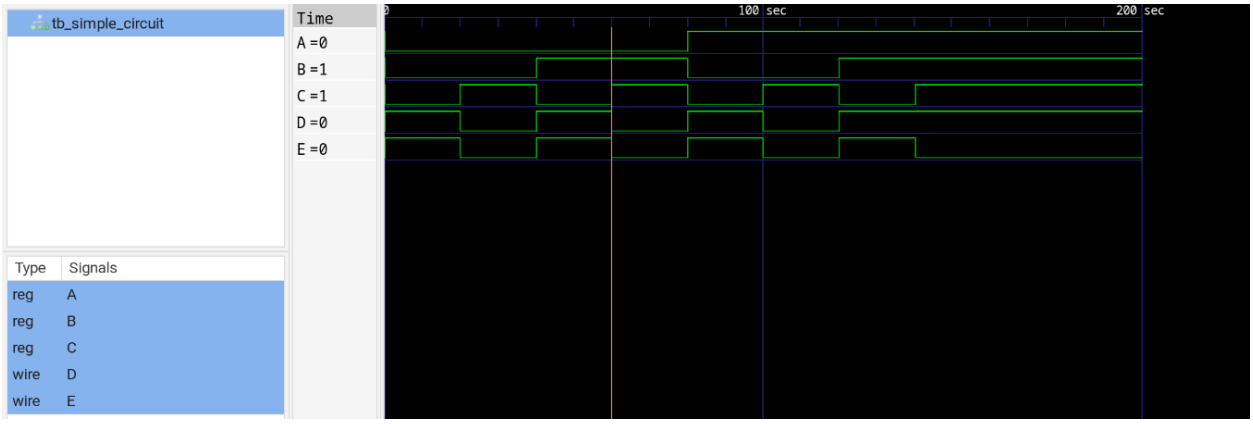
```
1   module tb_simple_circuit;
2   wire D, E;
3   reg A, B, C;
4
5   simple_circuit1 M1 (.A(A), .B(B), .C(C), .D(D), .E(E));
6
7   initial
8   begin
9   #0 A = 1'b0; B = 1'b0; C = 1'b0;
10  #20 A = 1'b0; B = 1'b0; C = 1'b1;
11  #20 A = 1'b0; B = 1'b1; C = 1'b0;
12  #20 A = 1'b0; B = 1'b1; C = 1'b1;
13  #20 A = 1'b1; B = 1'b0; C = 1'b0;
14  #20 A = 1'b1; B = 1'b0; C = 1'b1;
15  #20 A = 1'b1; B = 1'b1; C = 1'b0;
16  #20 A = 1'b1; B = 1'b1; C = 1'b1;
17  #20;
18  end
19
20  initial
21  begin
22  $monitor($time," A=%b, B=%b, C=%b, D=%b, E=%b", A, B, C, D, E);
23  end
24
25  initial begin
26  $dumpfile("simple.vcd");
27  $dumpvars(1, tb_simple_circuit);
28  #200;
29  $finish;
30  end
31  endmodule
```

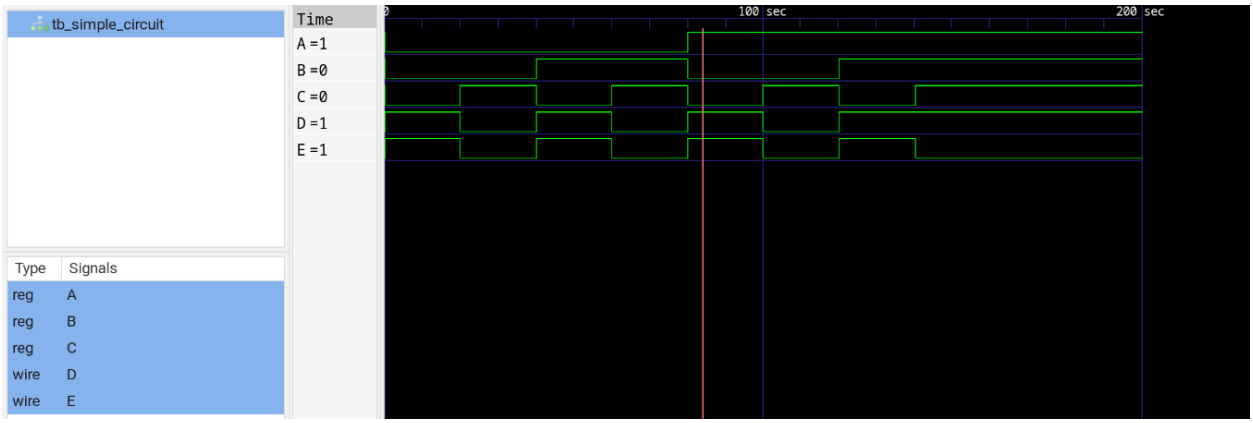
```
rithvikmatta@penguin:~/DDCO-sem-3/week 2$ iverilog -o simple1 simple_circuit1.v simple_circuit1_tb.v
rithvikmatta@penguin:~/DDCO-sem-3/week 2$ vvp simple1
VCD info: dumpfile simple.vcd opened for output.
                0 A=0, B=0, C=0, D=1, E=1
               20 A=0, B=0, C=1, D=0, E=0
               40 A=0, B=1, C=0, D=1, E=1
               60 A=0, B=1, C=1, D=0, E=0
               80 A=1, B=0, C=0, D=1, E=1
              100 A=1, B=0, C=1, D=0, E=0
              120 A=1, B=1, C=0, D=1, E=1
              140 A=1, B=1, C=1, D=1, E=0
rithvikmatta@penguin:~/DDCO-sem-3/week 2$ gtkwave simple.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[200] end time.
GTKWAVE | Touch screen detected, enabling gestures.
Exiting.
```

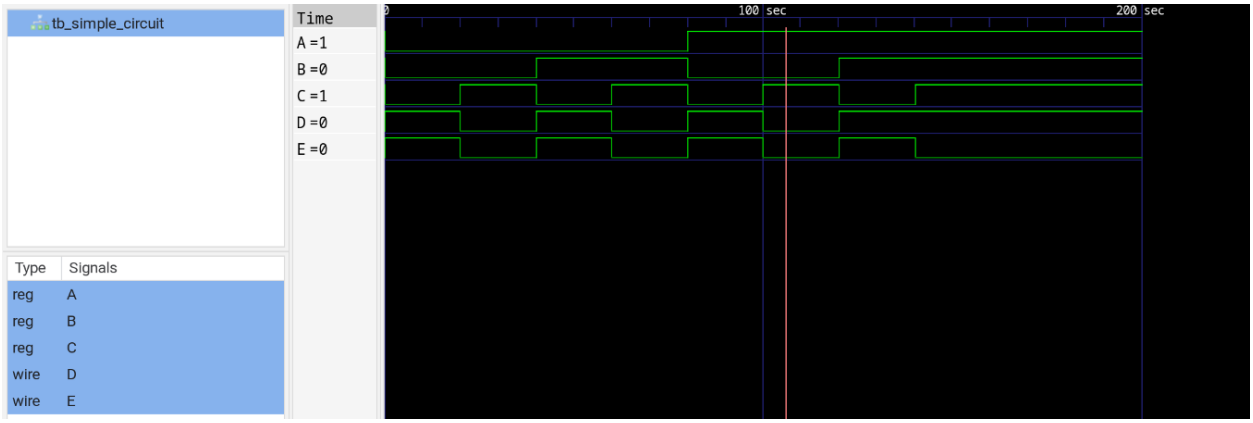

tb_simple_circuit
Type
Signals
reg A
reg B
reg C
wire D
wire E
Time
A =0
B =0
C =0
D =1
E =1
100 sec
200 sec

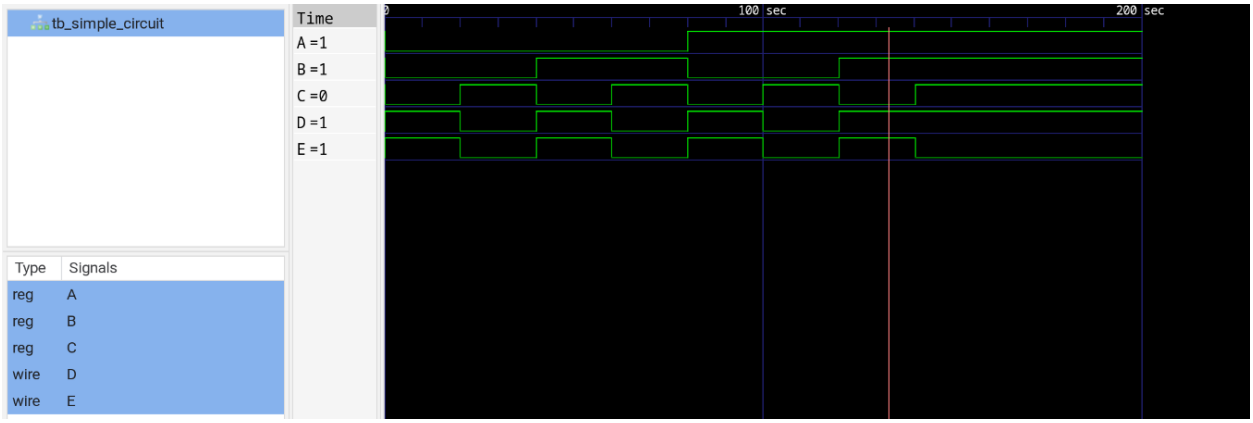

tb_simple_circuit
Type
Signals
reg A
reg B
reg C
wire D
wire E
Time
A =0
B =0
C =1
D =0
E =0
100 sec
200 sec

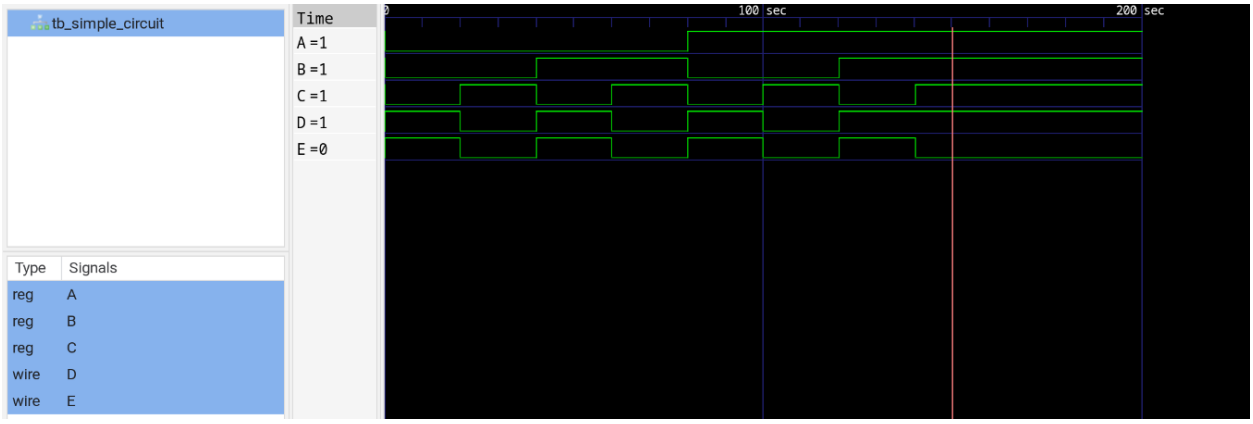

tb_simple_circuit
Type
Signals
reg A
reg B
reg C
wire D
wire E
Time
A =0
B =1
C =0
D =1
E =1
100 sec
200 sec


tb_simple_circuit
Type
Signals
reg A
reg B
reg C
wire D
wire E
Time
A =0
B =1
C =1
D =0
E =0
100 sec
200 sec


tb_simple_circuit
Type
Signals
reg
A
reg
B
reg
C
wire
D
wire
E
Time
A =1
B =0
C =0
D =1
E =1
0
100 sec
200 sec

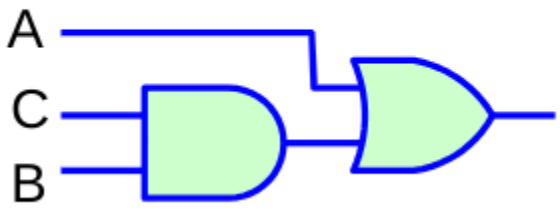

tb_simple_circuit
Type
Signals
reg
A
reg
B
reg
C
wire
D
wire
E
Time
A =1
B =0
C =1
D =0
E =0
0
100 sec
200 sec


tb_simple_circuit
Type
Signals
reg
A
reg
B
reg
C
wire
D
wire
E
Time
A =1
B =1
C =0
D =1
E =1
0
100 sec
200 sec


tb_simple_circuit
Type
Signals
reg
A
reg
B
reg
C
wire
D
wire
E
Time
A =1
B =1
C =1
D =1
E =0
0
100 sec
200 sec

WRITE A VERILOG PROGRAM TO MODEL A SIMPLE CIRCUIT. GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

CIRCUIT 1



A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

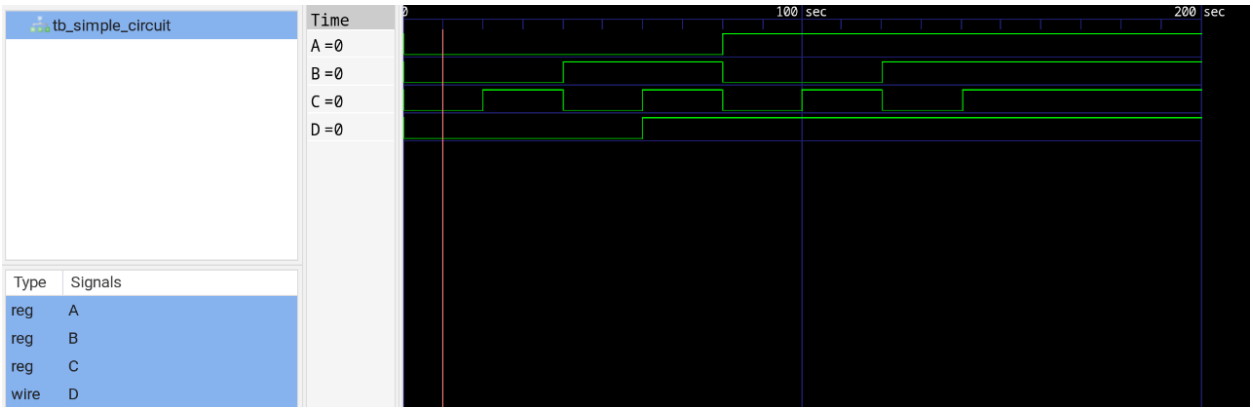
week 2 > ≡ simple_circuit2.v

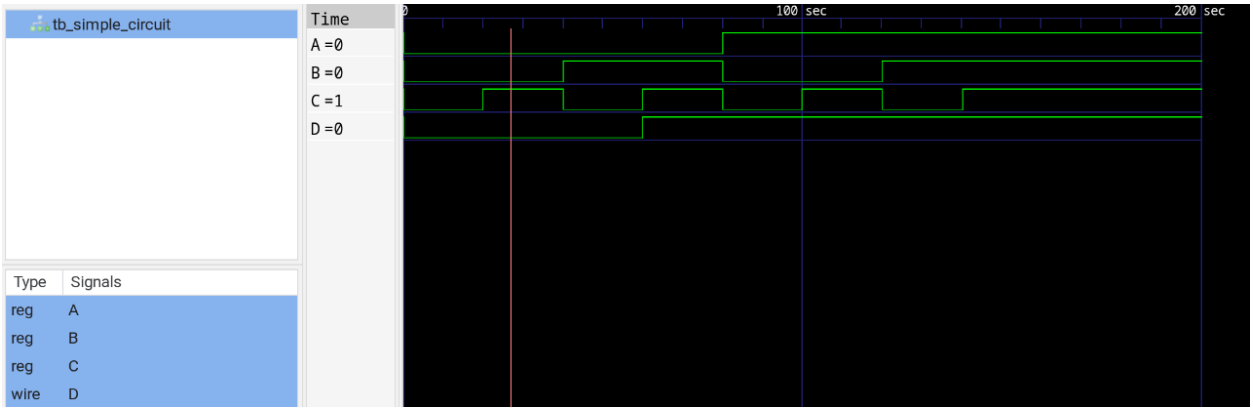
```
1   module andgate (y, a, b);
2   input a, b;
3   output y;
4   assign y = a & b;
5   endmodule
6
7   module orgate (y, a, b);
8   input a, b;
9   output y;
10  assign y = a | b;
11  endmodule
12
13  module notgate (y, a);
14  input a;
15  output y;
16  assign y = !a;
17  endmodule
18
19  module simple_circuit1 (A, B, C, D);
20  output D;
21  input A, B, C;
22  wire w1;
23  andgate G1 (w1, C, B);
24  orgate G3 (D, w1, A);
25  endmodule
```

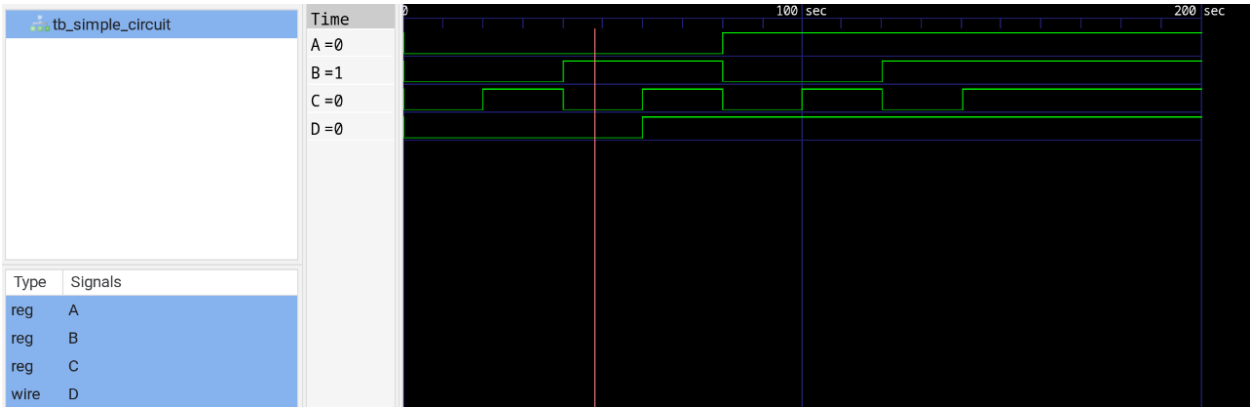
week 2 > simple_circuit2_tb.v

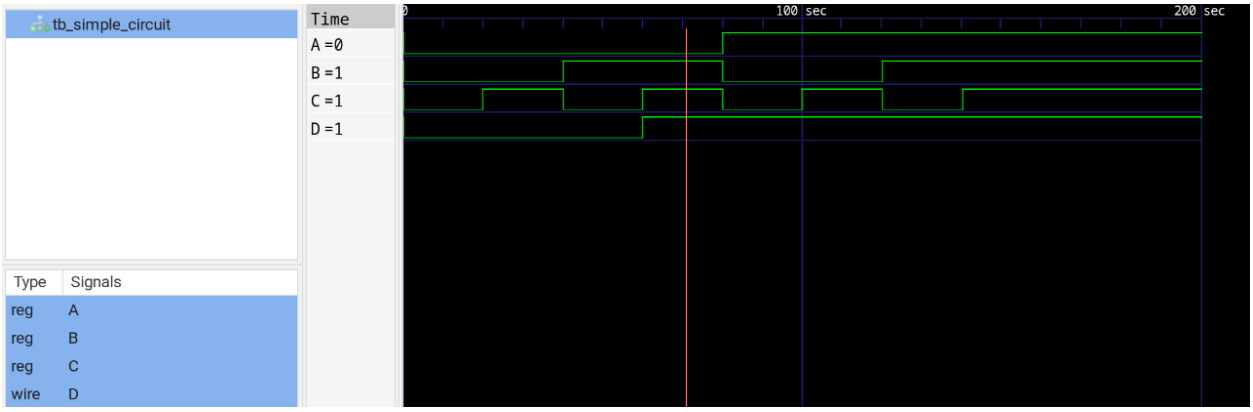
```
module tb_simple_circuit;
wire D;
reg A, B, C;

simple_circuit1 M1 (.A(A), .B(B), .C(C), .D(D));

initial begin
A = 1'b0; B = 1'b0; C = 1'b0;
#20 A = 1'b0; B = 1'b0; C = 1'b1;
#20 A = 1'b0; B = 1'b1; C = 1'b0;
#20 A = 1'b0; B = 1'b1; C = 1'b1;
#20 A = 1'b1; B = 1'b0; C = 1'b0;
#20 A = 1'b1; B = 1'b0; C = 1'b1;
#20 A = 1'b1; B = 1'b1; C = 1'b0;
#20 A = 1'b1; B = 1'b1; C = 1'b1;
#20;
end

initial begin
$monitor($time, " A=%b, B=%b, C=%b, D=%b", A, B, C, D);
end

initial begin
$dumpfile("simple.vcd");
$dumpvars(1, tb_simple_circuit);
#200;
$finish;
end
endmodule
```

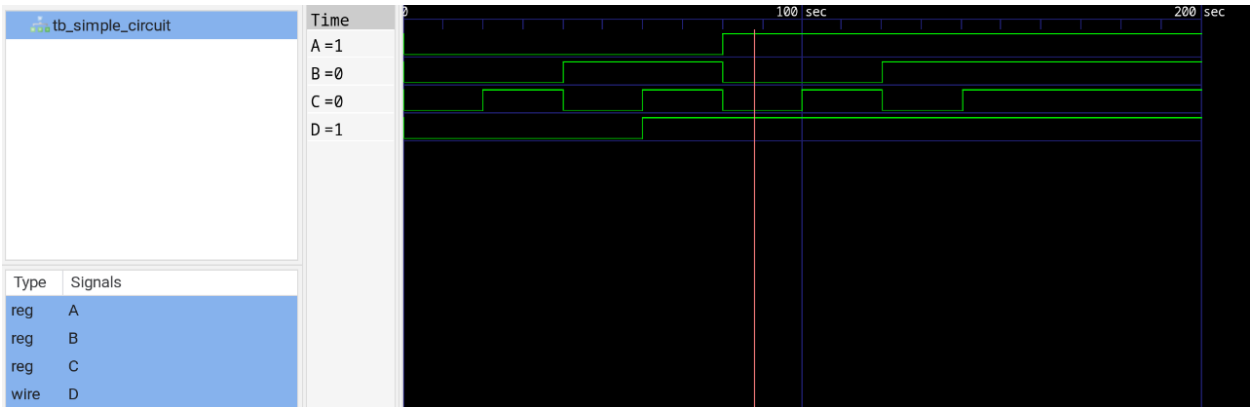
```
rithvikmatta@penguin:~/DDCO-sem-3/week 2$ iverilog -o simple2 simple_circuit2.v simple_circuit2_tb.v
rithvikmatta@penguin:~/DDCO-sem-3/week 2$ vvp simple2
VCD info: dumpfile simple2.vcd opened for output.
                0 A=0, B=0, C=0, D=0
               20 A=0, B=0, C=1, D=0
               40 A=0, B=1, C=0, D=0
               60 A=0, B=1, C=1, D=1
               80 A=1, B=0, C=0, D=1
              100 A=1, B=0, C=1, D=1
              120 A=1, B=1, C=0, D=1
              140 A=1, B=1, C=1, D=1
rithvikmatta@penguin:~/DDCO-sem-3/week 2$
```

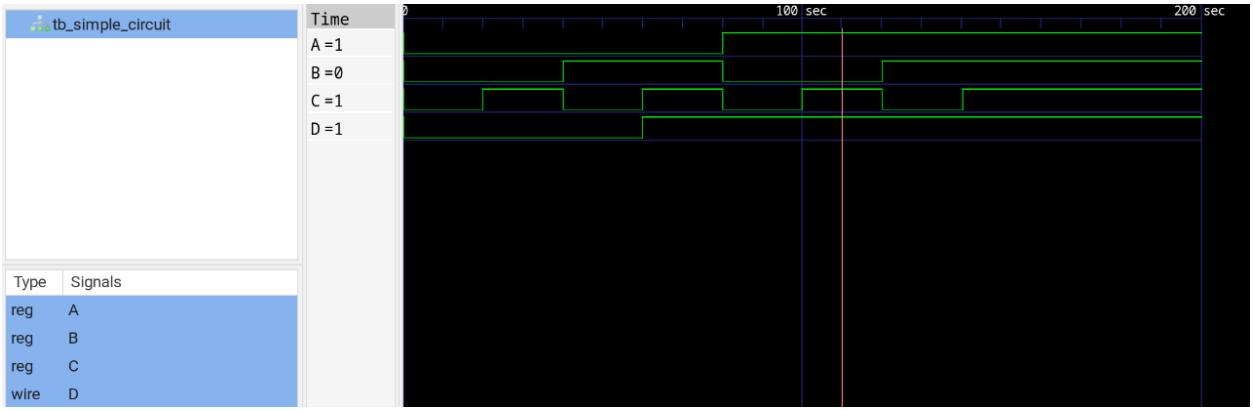

tb_simple_circuit
Type
Signals
reg
A
reg
B
reg
C
wire
D
Time
A =0
B =0
C =0
D =0
0
100 sec
200 sec

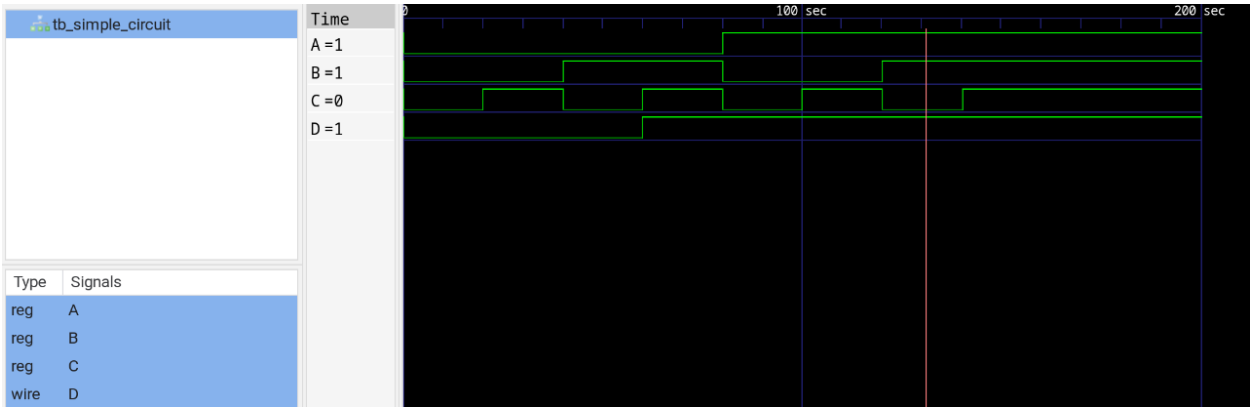

tb_simple_circuit
Type
Signals
reg
A
reg
B
reg
C
wire
D
Time
A =0
B =0
C =1
D =0
0
100 sec
200 sec

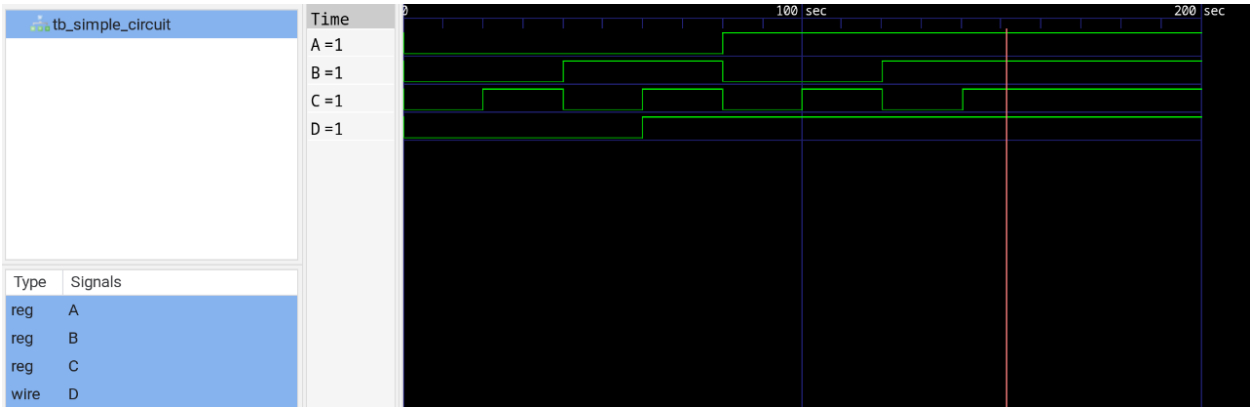

tb_simple_circuit
Type
Signals
reg
A
reg
B
reg
C
wire
D
Time
A =0
B =1
C =0
D =0
0
100 sec
200 sec


tb_simple_circuit
Type
Signals
reg
A
reg
B
reg
C
wire
D
Time
A =0
B =1
C =1
D =1
0
100 sec
200 sec



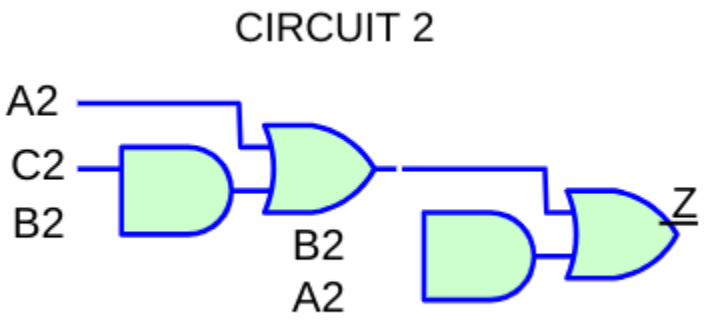






WRITE A VERILOG PROGRAM TO MODEL A SIMPLE CIRCUIT. GENERATE

THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH



A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

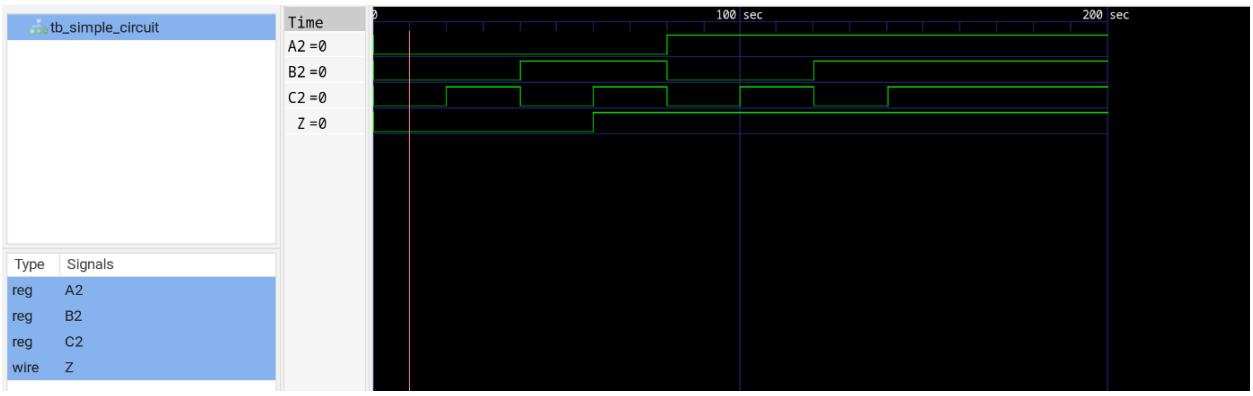
week 2 > simple_circuit3.v

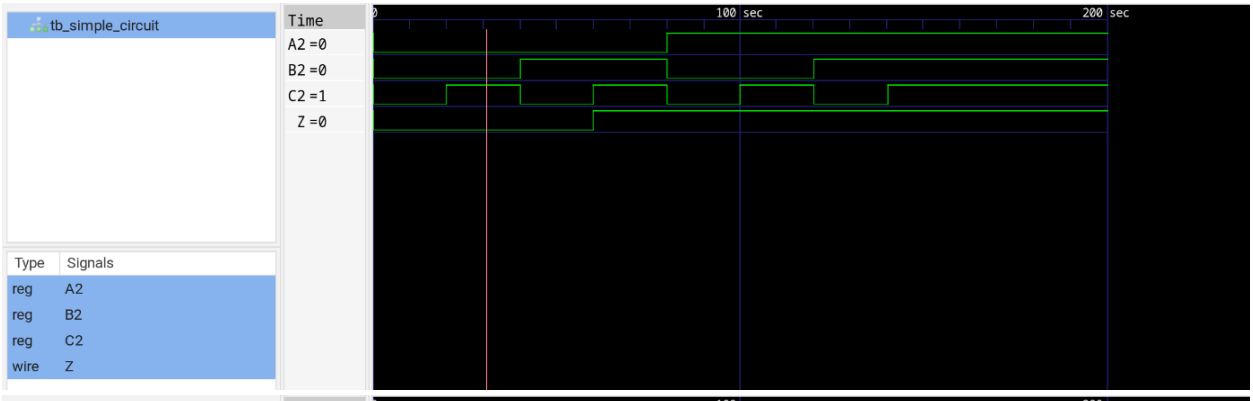
```
module andgate (y, a, b);
input a, b;
output y;
assign y = a & b;
endmodule

module orgate (y, a, b);
input a, b;
output y;
assign y = a | b;
endmodule

module notgate (y, a);
input a;
output y;
assign y = ~a;
endmodule

module simple_circuit1 (A2, B2, C2, Z);
output Z;
input A2, B2, C2;
wire w1, w2, w3;

andgate G1 (w1, C2, B2);
andgate G2 (w2, B2, A2);
orgate G3 (w3, w1, A2);
orgate G4 (Z, w3, w2);

endmodule
```

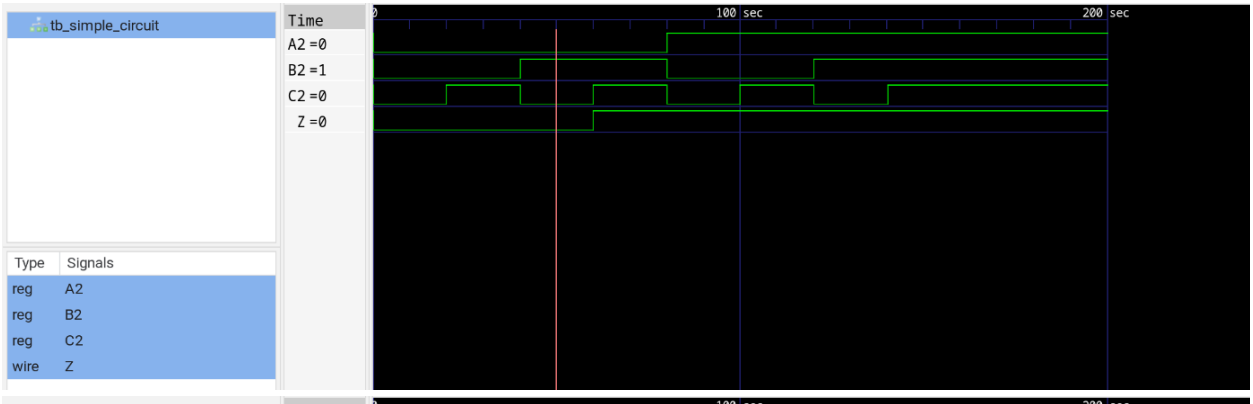
week 2 > simple_circuit3_tb.v

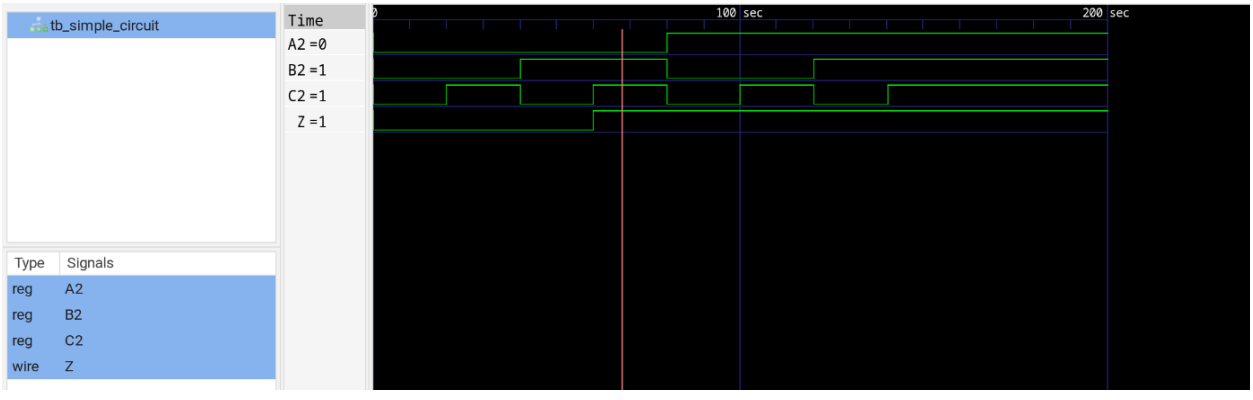
```v
module tb_simple_circuit;
    wire Z;
    reg A2, B2, C2;

    simple_circuit1 M1 (.A2(A2), .B2(B2), .C2(C2), .Z(Z));

    initial begin
        A2 = 1'b0; B2 = 1'b0; C2 = 1'b0;
        #20 A2 = 1'b0; B2 = 1'b0; C2 = 1'b1;
        #20 A2 = 1'b0; B2 = 1'b1; C2 = 1'b0;
        #20 A2 = 1'b0; B2 = 1'b1; C2 = 1'b1;
        #20 A2 = 1'b1; B2 = 1'b0; C2 = 1'b0;
        #20 A2 = 1'b1; B2 = 1'b0; C2 = 1'b1;
        #20 A2 = 1'b1; B2 = 1'b1; C2 = 1'b0;
        #20 A2 = 1'b1; B2 = 1'b1; C2 = 1'b1;
        #20;
    end

    initial begin
        $monitor($time, " A2=%b, B2=%b, C2=%b, Z=%b", A2, B2, C2, Z);
    end

    initial begin
        $dumpfile("simple3.vcd");
        $dumpvars(1, tb_simple_circuit);
        #200;
        $finish;
    end
endmodule
```

```
rithvikmatta@penguin:~/DDCO-sem-3/week 2$ iverilog -o simple3 simple_circuit3.v simple_circuit3_tb.v
rithvikmatta@penguin:~/DDCO-sem-3/week 2$ vvp simple3
VCD info: dumpfile simple3.vcd opened for output.
                0 A2=0, B2=0, C2=0, Z=0
               20 A2=0, B2=0, C2=1, Z=0
               40 A2=0, B2=1, C2=0, Z=0
               60 A2=0, B2=1, C2=1, Z=1
               80 A2=1, B2=0, C2=0, Z=1
              100 A2=1, B2=0, C2=1, Z=1
              120 A2=1, B2=1, C2=0, Z=1
              140 A2=1, B2=1, C2=1, Z=1
```


tb_simple_circuit
Type Signals
reg A2
reg B2
reg C2
wire Z
Time
A2 =0
B2 =0
C2 =0
Z =0
0
100 sec
200 sec

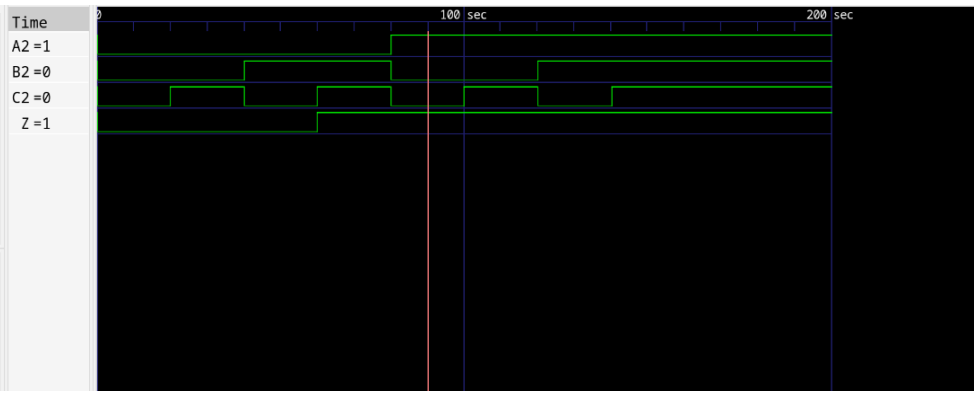

tb_simple_circuit
Type Signals
reg A2
reg B2
reg C2
wire Z
Time
A2 =0
B2 =0
C2 =1
Z =0
0
100 sec
200 sec


tb_simple_circuit
Type Signals
reg A2
reg B2
reg C2
wire Z
Time
A2 =0
B2 =1
C2 =0
Z =0
0
100 sec
200 sec


tb_simple_circuit
Type Signals
reg A2
reg B2
reg C2
wire Z
Time
A2 =0
B2 =1
C2 =1
Z =1
0
100 sec
200 sec

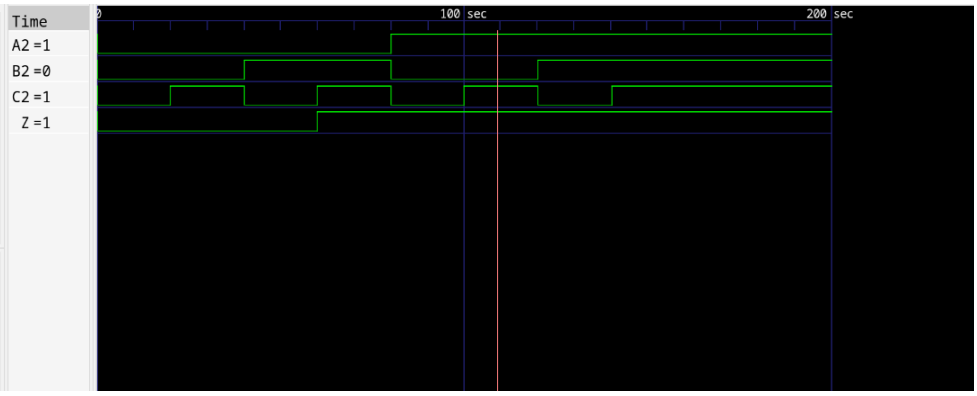
tb_simple_circuit

Type	Signals
reg	A2
reg	B2
reg	C2
wire	Z



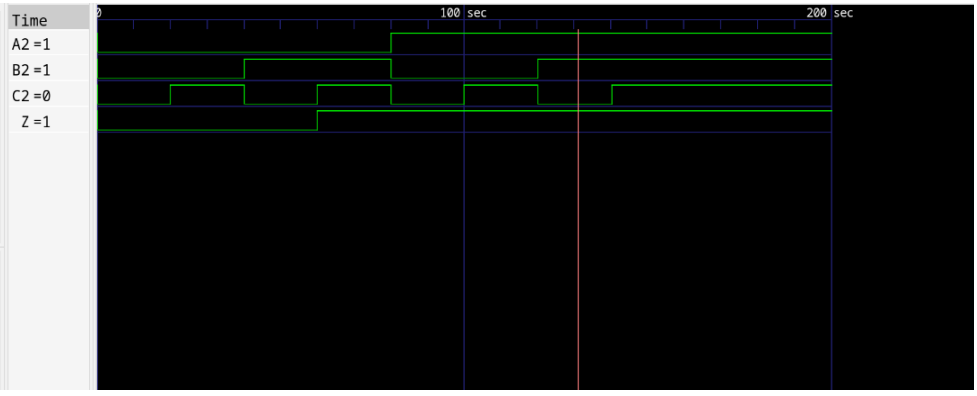
tb_simple_circuit

Type	Signals
reg	A2
reg	B2
reg	C2
wire	Z



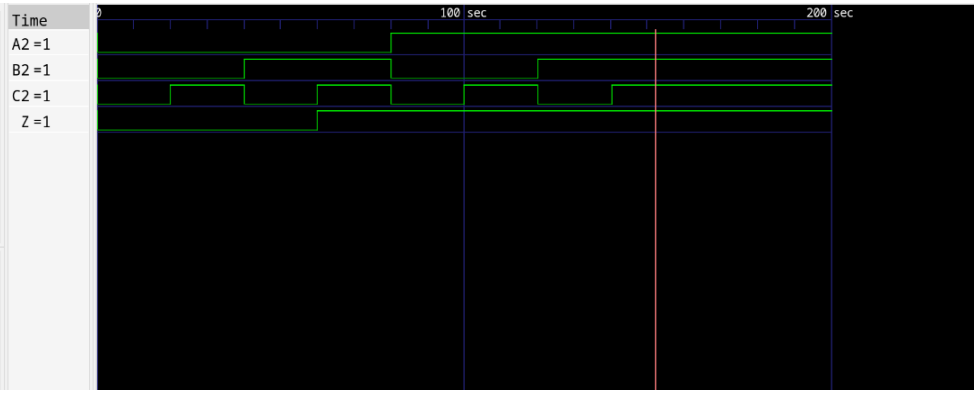
tb_simple_circuit

Type	Signals
reg	A2
reg	B2
reg	C2
wire	Z

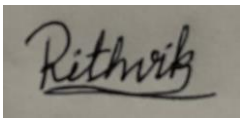


tb_simple_circuit

Type	Signals
reg	A2
reg	B2
reg	C2
wire	Z



If found plagiarized, I will abide with the disciplinary action of the University.

Signature: 

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