Digital Design and Computer Organization Laboratory

3rd Semester, Academic Year 2024

Date: 06/09/2024

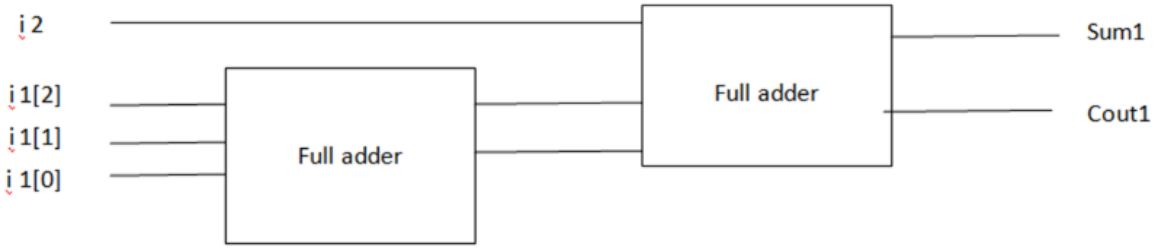
Name: Rithvik Rajesh Matta	SRN: PES2UG23CS485	Section: H

Week#____5_____

TITLE:

GENERATE THE VVP OUTPUT AND SIMULATION WAVEFORM USING GTKWAVE. VERIFY THE OUTPUT AND WAVEFORM WITH THE AND GATE TRUTH TABLE

1)Ckt1



i1	i2	Sum1	Cout1
000	0	0	0
001	1	0	1
010	0	1	0
011	1	0	1

010	0	1	0
011	1	0	1

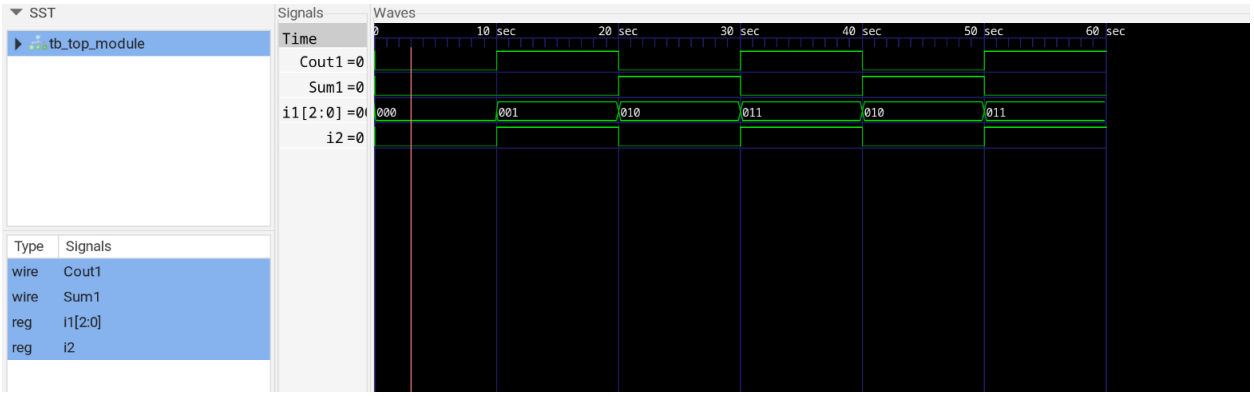
week 5 > ckt1.v

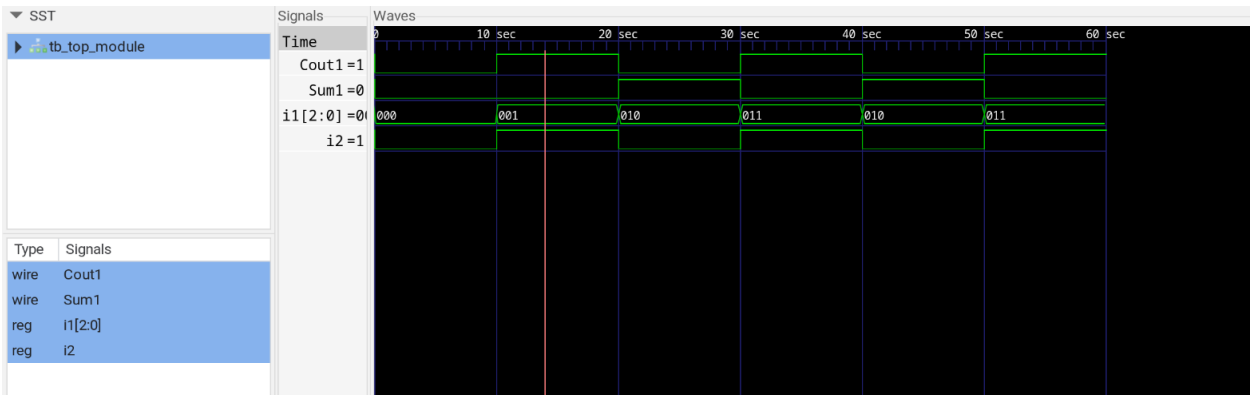
```v
module andgate (y, a, b);
input a, b;
output y;
assign y = a & b;
endmodule

module orgate (y, a, b);
input a, b;
output y;
assign y = a | b;
endmodule

module xorgate(y, a, b);
input a, b;
output y;
assign y = a ^ b;
endmodule

module halfadder(sum, carry, A, B);
input A, B;
output sum, carry;
xorgate X1(.y(sum), .a(A), .b(B));   // sum = A ^ B
andgate A1(.y(carry), .a(A), .b(B)); // carry = A & B
endmodule

module fulladder(sum, carry, A, B, C);
input A, B, C;
output sum, carry;
wire W1, W2, C1;
halfadder HA1(.sum(W1), .carry(W2), .A(A), .B(B)); // First half-adder
halfadder HA2(.sum(sum), .carry(C1), .A(W1), .B(C)); // Second half-adder
orgate OG(.y(carry), .a(W2), .b(C1));  // OR gate
endmodule


module top_module (input [2:0] i1, input i2,output Sum1,output Cout1 );
wire Sum0, Cout0;
fulladder FA0(.sum(Sum0),.carry(Cout0),.A(i1[1]),.B(i1[0]),.C(i1[2]));
fulladder FA1(.sum(Sum1),.carry(Cout1),.A(i2),.B(Sum0),.C(Cout0));
endmodule
```

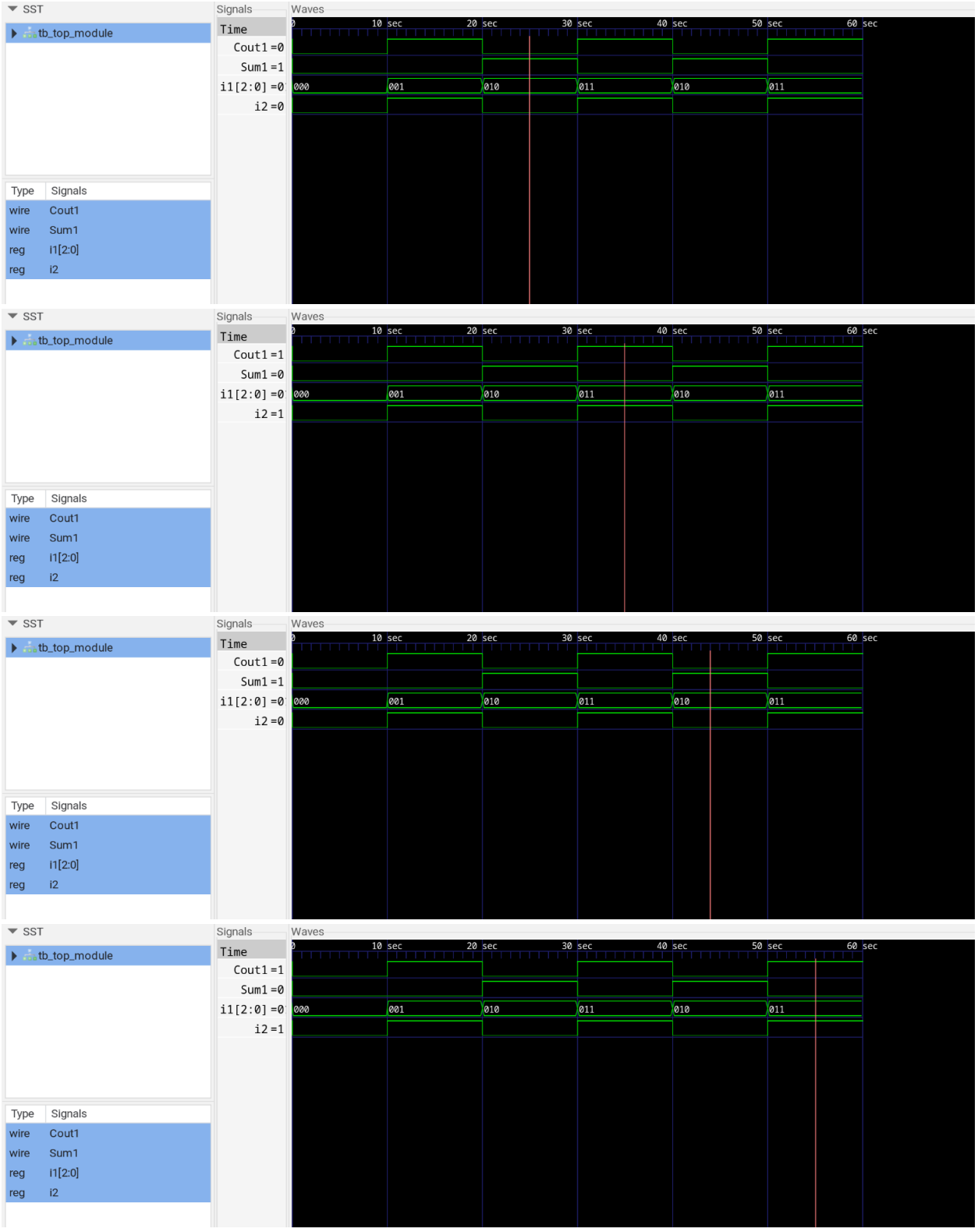
week 5 > ckt1_tb.v

```v
module tb_top_module;
reg [2:0] i1;
reg i2;
wire Sum1, Cout1;

top_module uut (.i1(i1), .i2(i2), .Sum1(Sum1), .Cout1(Cout1));
initial begin
i1 = 3'b000;i2 = 1'b0;
#10;i1 = 3'b001;i2 = 1'b1;
#10;i1 = 3'b010;i2 = 1'b0;
#10;i1 = 3'b011;i2 = 1'b1;
#10;i1 = 3'b010;i2 = 1'b0;
#10;i1 = 3'b011;i2 = 1'b1;
#10;

$finish;
end

initial begin
$monitor("Time = %0t , i1 = %b , i2 = %b , Sum1 = %b , Cout1 = %b", $time, i1, i2, Sum1, Cout1);
end

initial begin
$dumpfile("ckt1.vcd");
$dumpvars(0, tb_top_module);
end
endmodule
```

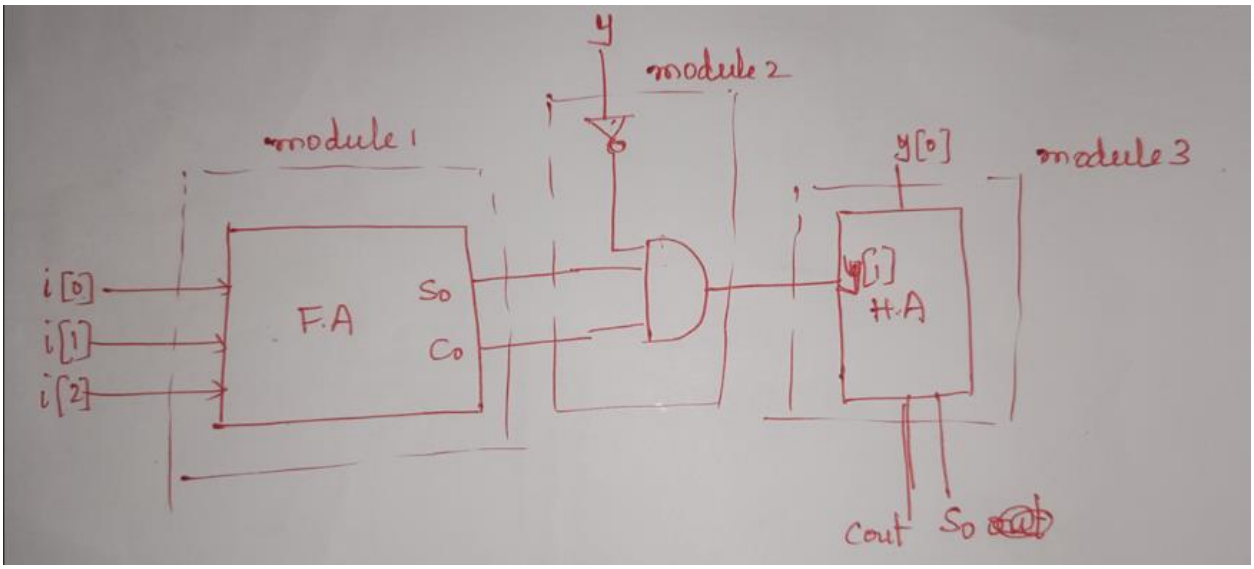
```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 5$ iverilog -o ckt1 ckt1.v ckt1_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 5$ vvp ckt1
VCD info: dumpfile ckt1.vcd opened for output.
Time = 0 , i1 = 000 , i2 = 0 , Sum1 = 0 , Cout1 = 0
Time = 10 , i1 = 001 , i2 = 1 , Sum1 = 0 , Cout1 = 1
Time = 20 , i1 = 010 , i2 = 0 , Sum1 = 1 , Cout1 = 0
Time = 30 , i1 = 011 , i2 = 1 , Sum1 = 0 , Cout1 = 1
Time = 40 , i1 = 010 , i2 = 0 , Sum1 = 1 , Cout1 = 0
Time = 50 , i1 = 011 , i2 = 1 , Sum1 = 0 , Cout1 = 1
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 5$ gtkwave ckt1.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[60] end time.
GTKWAVE | Touch screen detected, enabling gestures.
WM Destroy
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 5$
```






SST
tb_top_module
Type
Signals
wire
Cout1
wire
Sum1
reg
i1[2:0]
reg
i2
Signals
Waves
Time
Cout1 =0
Sum1 =1
i1[2:0] =0
i2 =0
0
10 sec
20 sec
30 sec
40 sec
50 sec
60 sec
000
001
010
011
010
011
SST
tb_top_module
Type
Signals
wire
Cout1
wire
Sum1
reg
i1[2:0]
reg
i2
Signals
Waves
Time
Cout1 =1
Sum1 =0
i1[2:0] =0
i2 =1
0
10 sec
20 sec
30 sec
40 sec
50 sec
60 sec
000
001
010
011
010
011
SST
tb_top_module
Type
Signals
wire
Cout1
wire
Sum1
reg
i1[2:0]
reg
i2
Signals
Waves
Time
Cout1 =0
Sum1 =1
i1[2:0] =0
i2 =0
0
10 sec
20 sec
30 sec
40 sec
50 sec
60 sec
000
001
010
011
010
011
SST
tb_top_module
Type
Signals
wire
Cout1
wire
Sum1
reg
i1[2:0]
reg
i2
Signals
Waves
Time
Cout1 =1
Sum1 =0
i1[2:0] =0
i2 =1
0
10 sec
20 sec
30 sec
40 sec
50 sec
60 sec
000
001
010
011
010
011

2)ckt2


y
module 2
module 1
y[0]
module 3
i[0]
i[1]
i[2]
F.A
So
Co
y[1]
H.A
Cout
So

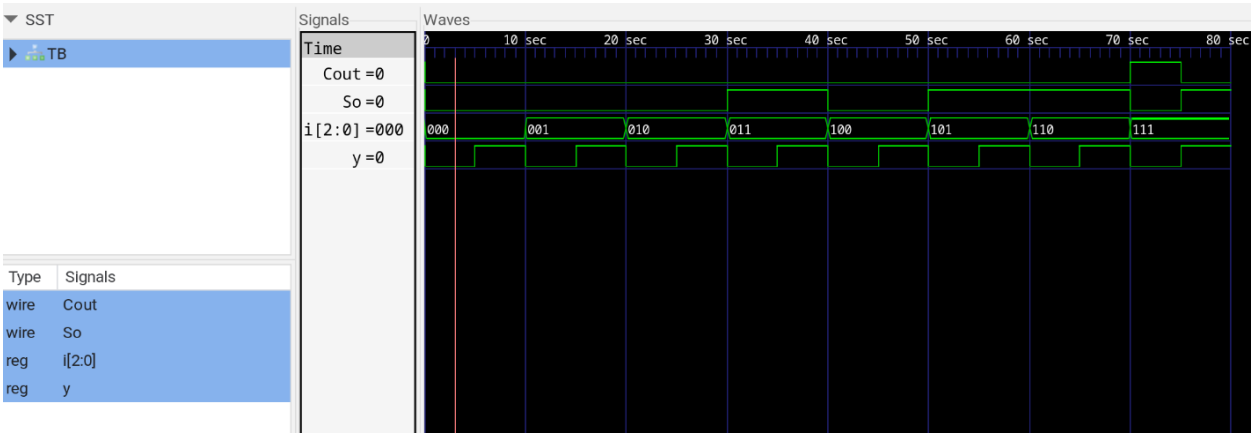
week 5 > ckt2.v

```v
module andgate (y, a, b);
input a, b;
output y;
assign y = a & b;
endmodule

module orgate (y, a, b);
input a, b;
output y;
assign y = a | b;
endmodule

module xorgate (y, a, b);
input a, b;
output y;
assign y = a ^ b;
endmodule

module notgate(y, a);
input a;
output y;
assign y = ~a;
endmodule

module halfadder(sum, carry, A, B);
input A, B;
output sum, carry;
xorgate X1(.y(sum), .a(A), .b(B));   // sum = A ^ B
andgate A1(.y(carry), .a(A), .b(B)); // carry = A & B
endmodule

module fulladder(sum, carry, A, B, C);
input A, B, C;
output sum, carry;
wire W1, W2, C1;
halfadder HA1(.sum(W1), .carry(W2), .A(A), .B(B)); // First half-adder
halfadder HA2(.sum(sum), .carry(C1), .A(W1), .B(C)); // Second half-adder
orgate OG(.y(carry), .a(W2), .b(C1));  // OR gate
endmodule

module top_module(input [2:0] i, input y, output So, output Cout);
wire Sum0, Co0, Not_y, And_out1, And_out2;
fulladder FA0 (.sum(Sum0), .carry(Co0), .A(i[0]), .B(i[1]), .C(i[2]));
notgate NG1 (.y(Not_y), .a(y));
andgate AND1 (.y(And_out1), .a(Sum0), .b(Not_y));
andgate AND2 (.y(And_out2), .a(And_out1), .b(Co0));
halfadder HA0 (.sum(So), .carry(Cout), .A(And_out2), .B(Co0));
endmodule
```

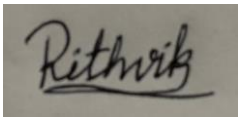
week 5 > ckt2_tb.v

```
module TB;
reg [2:0] i;
reg y;
wire So, Cout;

// Instantiate the top module
top_module uut (
.i(i),
.y(y),
.So(So),
.Cout(Cout)
);

initial begin
i = 3'b000; y = 1'b0;#5;
i = 3'b000; y = 1'b1;#5;
i = 3'b001; y = 1'b0;#5;
i = 3'b001; y = 1'b1;#5;
i = 3'b010; y = 1'b0;#5;
i = 3'b010; y = 1'b1;#5;
i = 3'b011; y = 1'b0;#5;
i = 3'b011; y = 1'b1;#5;
i = 3'b100; y = 1'b0;#5;
i = 3'b100; y = 1'b1;#5;
i = 3'b101; y = 1'b0;#5;
i = 3'b101; y = 1'b1;#5;
i = 3'b110; y = 1'b0;#5;
i = 3'b110; y = 1'b1;#5;
i = 3'b111; y = 1'b0;#5;
i = 3'b111; y = 1'b1;#5;
end

initial begin
$monitor($time, " i=%b, y=%b, So=%b, Cout=%b", i, y, So, Cout);
end

initial begin
$dumpfile("top_module_test.vcd");
$dumpvars(0, TB);
end

endmodule
```

```
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 5$ iverilog -o ckt2 ckt2.v ckt2_tb.v
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 5$ vvp ckt2
VCD info: dumpfile top_module_test.vcd opened for output.
                   0 i=000, y=0, So=0, Cout=0
                   5 i=000, y=1, So=0, Cout=0
                  10 i=001, y=0, So=0, Cout=0
                  15 i=001, y=1, So=0, Cout=0
                  20 i=010, y=0, So=0, Cout=0
                  25 i=010, y=1, So=0, Cout=0
                  30 i=011, y=0, So=1, Cout=0
                  35 i=011, y=1, So=1, Cout=0
                  40 i=100, y=0, So=0, Cout=0
                  45 i=100, y=1, So=0, Cout=0
                  50 i=101, y=0, So=1, Cout=0
                  55 i=101, y=1, So=1, Cout=0
                  60 i=110, y=0, So=1, Cout=0
                  65 i=110, y=1, So=1, Cout=0
                  70 i=111, y=0, So=0, Cout=1
                  75 i=111, y=1, So=1, Cout=0
rithvikmatta@penguin:~/PES/DDCO-sem-3/week 5$ gtkwave top_module_test.vcd

GTKWave Analyzer v3.3.118 (w)1999-2023 BSI

[0] start time.
[80] end time.
GTKWAVE | Touch screen detected, enabling gestures.
WM Destroy
```



If found plagiarized, I will abide with the disciplinary action of the University.

Signature: 

Name: Rithvik Rajesh Matta

SRN: PES2UG23CS485

Section: H

Date: 30/08/2024