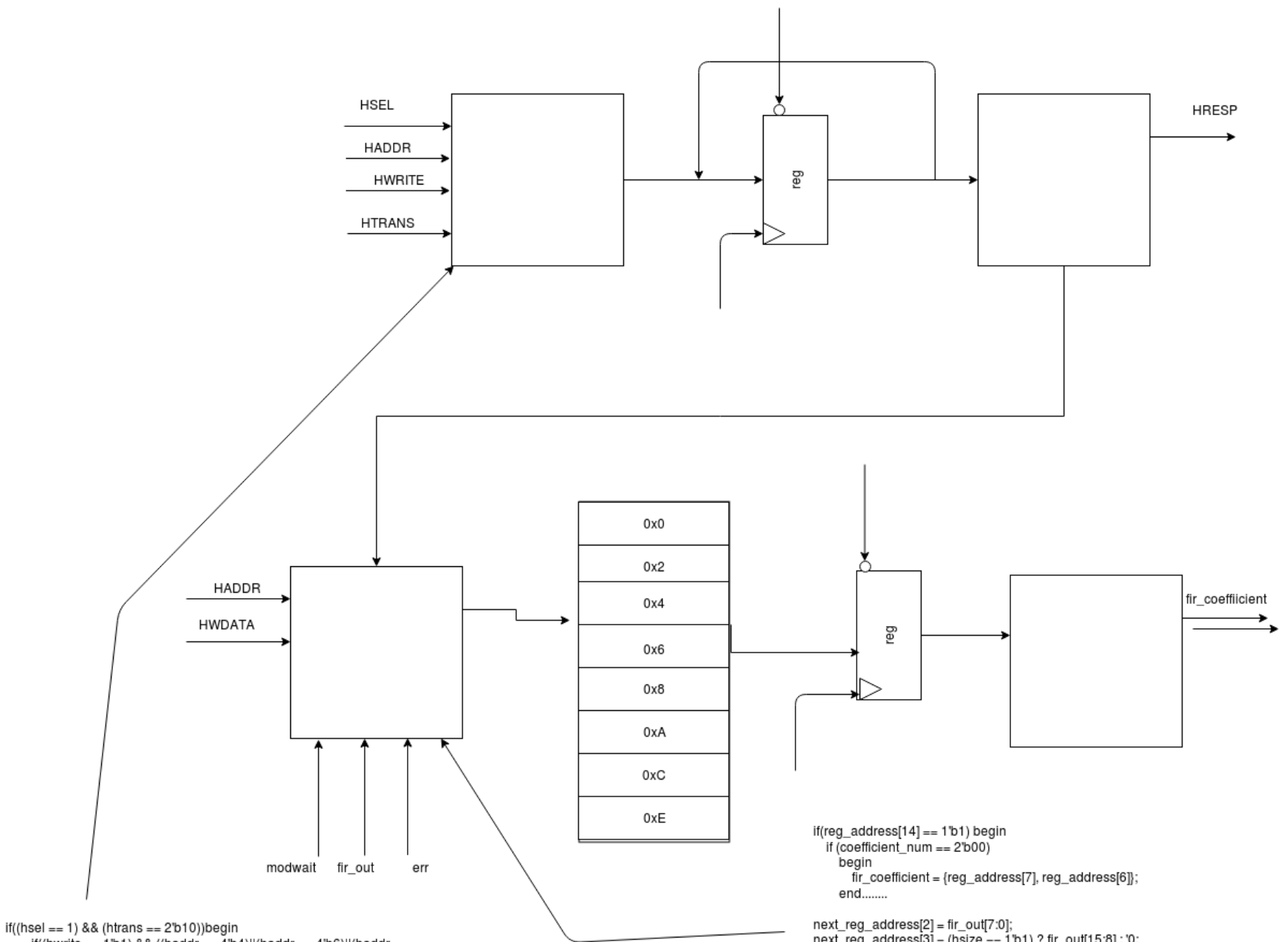
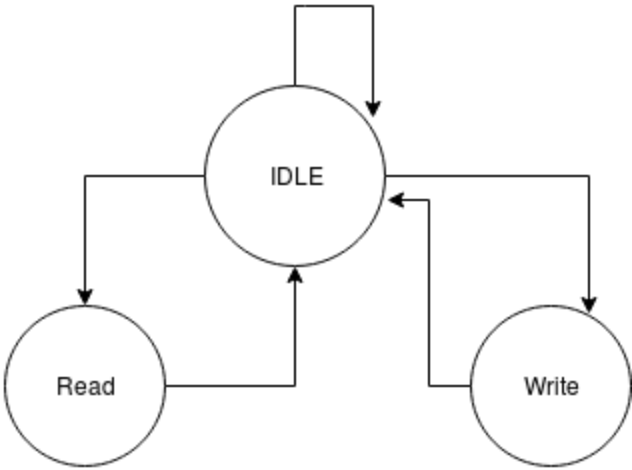



```
if((hsel == 1) && (htrans == 2'b10))begin
      if((hwrite == 1'b1) && ((haddr == 4'h4)||(haddr == 4'h6)||(haddr
== 4'h8)||(haddr == 4'hA)||(haddr == 4'hC)||(haddr == 4'hE)))begin
         state = WRITE;
      end
      else if ((hwrite == 1'b0) && ((haddr == 4'h0)||(haddr == 4'h2)||
(haddr == 4'h4)||(haddr == 4'h6)||(haddr == 4'h8)||(haddr == 4'hA)||
(haddr == 4'hC)||(haddr == 4'hE)))begin
         state = READ;
      end
         else begin
         state = IDLE;
      hresp = 1'b1;
         end
   end
```

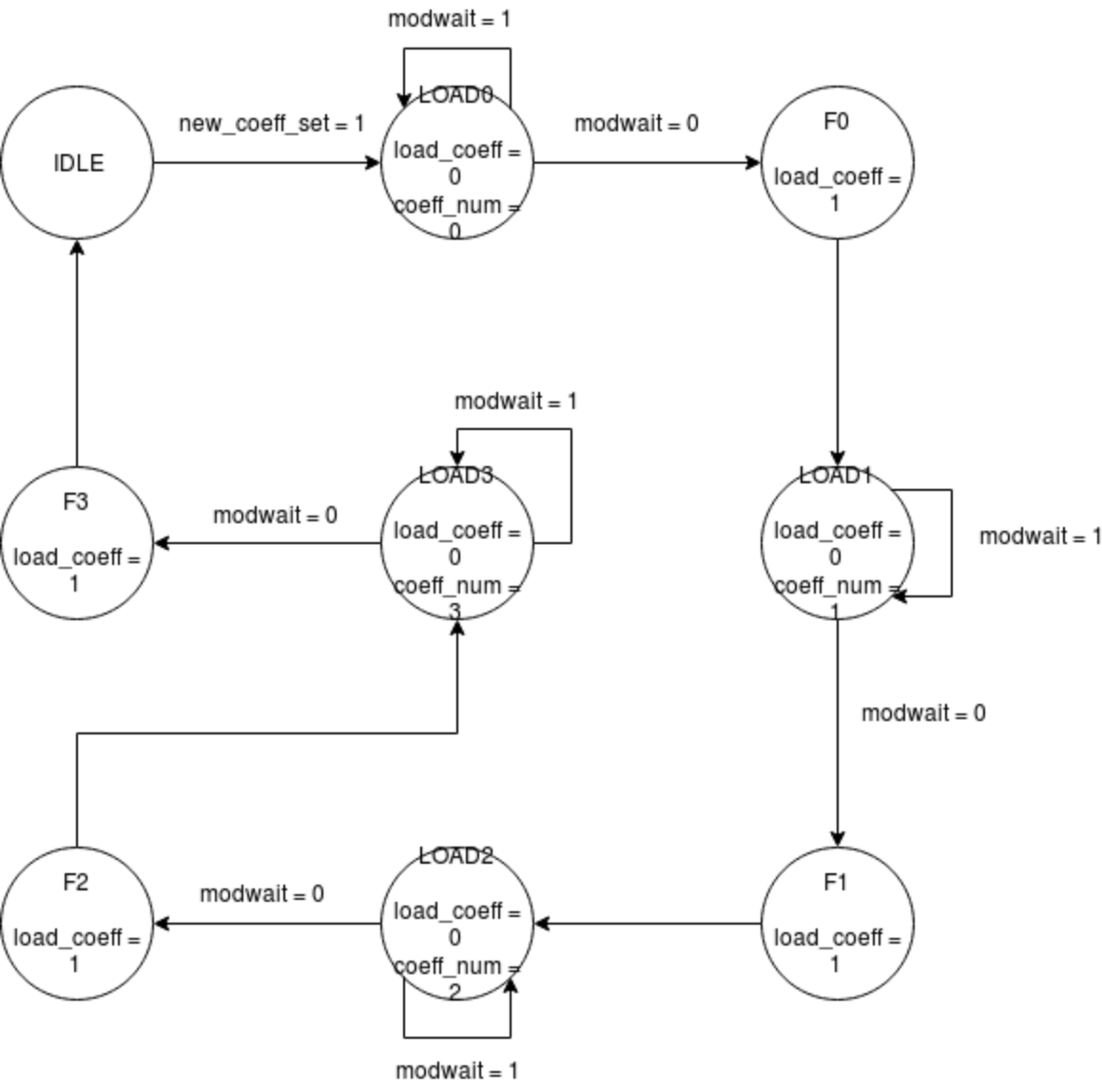
```
if(reg_address[14] == 1'b1) begin
   if (coefficient_num == 2'b00)
      begin
         fir_coefficient = {reg_address[7], reg_address[6]};
      end.....

next_reg_address[2] = fir_out[7:0];
next_reg_address[3] = (hsize == 1'b1) ? fir_out[15:8] : '0;

sample_data[7:0] = reg_address[4];
sample_data[15:8] = reg_address[5];
new_coefficient_set = reg_address[14]
```




```
if((hsel == 1) && (htrans == 2'b10))begin
    if((hwrite == 1'b1) && ((haddr == 4'h4)||(haddr == 4'h6)||(haddr
== 4'h8)||(haddr == 4'hA)||(haddr == 4'hC)||(haddr == 4'hE)))begin
      state = WRITE;
    end
    else if ((hwrite == 1'b0) && ((haddr == 4'h0)||(haddr == 4'h2)||
(haddr == 4'h4)||(haddr == 4'h6)||(haddr == 4'h8)||(haddr == 4'hA)||
(haddr == 4'hC)||(haddr == 4'hE)))begin
      state = READ;
    end
      else begin
      state = IDLE;
    hresp = 1'b1;
      end
  end
```


modwait = 1
LOAD0
load_coeff = 0
coeff_num = 0
IDLE
new_coeff_set = 1
modwait = 0
F0
load_coeff = 1
modwait = 1
LOAD3
load_coeff = 0
coeff_num = 3
F3
load_coeff = 1
modwait = 0
LOAD1
load_coeff = 0
coeff_num = 1
modwait = 1
modwait = 0
LOAD2
load_coeff = 0
coeff_num = 2
F2
load_coeff = 1
modwait = 0
F1
load_coeff = 1
modwait = 1