第四次作业补充说明

Exercise-1

补充：操作系统位数为32位

Suppose a cache divides addresses as follows:

tag	index (4 bits)	byte offset (3 bits)

Fill in the values for a direct-mapped or 4-way associative cache:

	Direct-mapped	4-way associative
Block size		
Number of blocks		
Total size of cache (e.g. 32 * 128 – don't have to multiply out)		
Tag size (# bits)		

Exercise-2

1. Suppose cache has:
   - 4 byte blocks
   - 128 blocks

   补充：4-way组相连

   Show how to break the following address into the tag, index, & byte offset.

   0000 1000 0101 1100 0001 0001 0111 1001

2. Same cache, but now 8-way associative. How does this change things?

   0000 1000 0101 1100 0001 0001 0111 1001

Exercise-3

- Given a cache that is:
  - 4-way associative
  - 32 blocks
  - 16 byte block size

  What is the cache index and byte offset for the following address:

  `0x3ab12395`

  Cache index =
  Byte offset =

  And this one:

  `0x70ff1213`

  Cache index =
  Byte offset =

  补充：在一个set里就算conflict

  Do these addresses conflict in the cache?