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POLYCRYSTALLINE THIN FILM SOLAR CELLS: Present Status and Future Potential

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ABSTRACT

Polycrystalline thin film solar cells on copper indium diselenide ($CuInSe_2$) and its alloys and cadmium telluride (CdTe) appear to be the most promising candidates for large-scale application of photovoltaic energy conversion because they have shown laboratory-efficiences in excess of 15%. Heterojunction devices with n-type cadmium sulfide (CdS) films show very low minority carrier recombination at the absorber grain boundaries and at the metallurgical interface, which results in high quantum efficiences. Open circuit voltages of these devices are relatively low owing to the recombination in the space charge region in the absorber. Further improvements in efficiency can be achieved by reducing the recombination current, especially in devices based on $CuInSe_2$ and its alloys. Low-cost manufacturing of modules requires better resolution of a number of other technical issues. For modules based on $CuInSe_2$ and its alloys, the role of Na and higher deposition rates on device performance need to be better understood. In addition, replacing the chemical bath deposition method for CdS film deposition with an equally effective, but more environmentally acceptable process is needed. For modules based on CdTe, more fundamental understanding of the effect of chloride/oxygen treatment and the development of more reproducible and manufacturable CdTe contacting schemes are necessary.

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INTRODUCTION

The photovoltaic (PV) effect was discovered in 1839, but it remained a laboratory curiosity until the mid 1950s when the US space program attempted to power satellites with PV cells. In 1954, single crystal silicon (sc-Si) PV cells of 6% efficiency were reported at Bell Laboratories. Following this development, commercial sc-Si PV cells were used routinely on US satellites. Because cost is not a major factor in space applications, these cells continue to be used on practically all satellite systems.

During the energy crisis of the early 1970s, and particularly given the technical success of PV cells in space applications, both public and private sectors became interested in terrestrial applications of PV energy generation. Initial efforts focused on lowering the cost of sc-Si solar cell modules since the basic technology already was well developed. Polycrystalline Si (pc-Si) solar-cell module technology was introduced to further lower manufacturing costs; however, the initial cost advantages of pc-Si technology are approximately offset by its lower efficiency, leaving the generated energy cost practically unchanged.

In the United States, Japan, and Germany, parallel efforts were also initiated to find alternative materials that could be processed in thin film form to provide a still lower-cost alternative to sc-Si and pc-Si. Initial efforts concentrated on thin film solar cells of polycrystalline Cu_2S/CdS and amorphous silicon. Cu_2S/CdS-type solar cells displayed severe stability problems, and their development was discontinued by the early 1980s. Amorphous silicon solar-cell technology has been more successful, and products based on this technology became available commercially. However, because these products have low conversion efficiencies (around 6% stabilized), their use is limited to special consumer applications.

To respond to the potential demand in the power generation market, which required module efficiencies in excess of 10%, research and development efforts shifted gradually to two other polycrystalline thin film material systems: copper indium diselenide ($CuInSe_2$)– and cadmium telluride (CdTe)–based solar cells. During the past twenty years, these research and development efforts resulted in conversion efficiency improvements from 6% to 17% for $CuInSe_2$-based, and from 8% to 16% for CdTe-based small-area laboratory devices. As a result, these materials systems are being considered seriously as the basis of PV module technologies for terrestrial power generation.

This review examines the state of our understanding and knowledge about the materials characteristics, device operation, and processing of these PV systems. It also discusses issues raised in translating the "proof-of-concept" device results to large-scale manufacturing of modules and proposes possible research and development directions for responding to these challenges.

SOLAR CELLS BASED ON $CuInSe_2$ AND RELATED ALLOYS

Materials and Electronic Properties of the Absorber

$CuInSe_2$ is a ternary compound that is stable as a chalcopyrite (g) or a sphalerite (d) structure. The pseudo-binary Cu_2Se/In_2Se_3 phase diagram of Figure 1 shows the stability regions of these two phases (1). The sphalerite phase is stable only at temperatures higher than 570°C, whereas the chalcopyrite structure, which

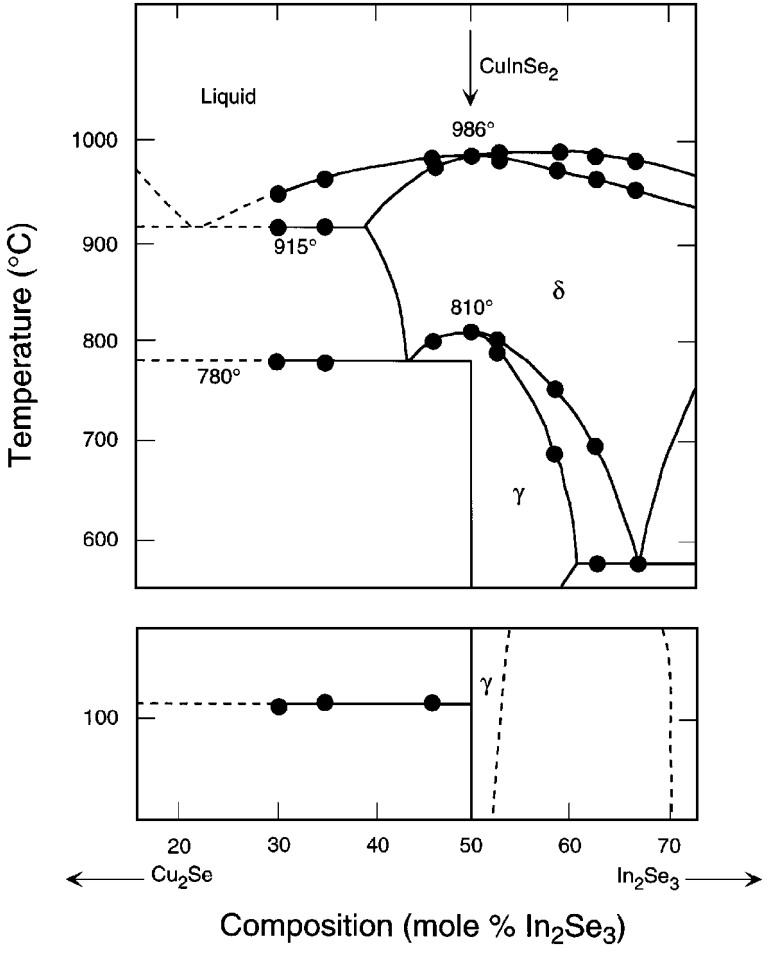

Figure 1 Pseudo-binary Cu_2Se/In_2Se_3 phase diagram (1).

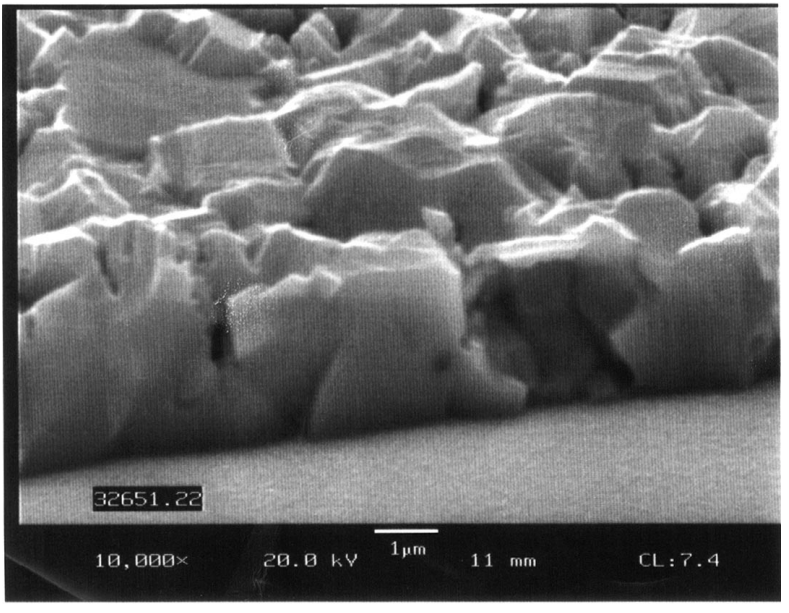

Figure 2 SEM micrograph showing a typical fractured cross-section and the surface of a $CuInSe_2$ film vapor deposited from elemental sources.

has lattice parameters of a $=$ 0.5789 Å and c $=$ 1.162 Å, is stable from room temperature up to 810°C. However, below 780°C the stability region of the g phase is at the In-rich side of perfect stoichiometry. The g phase is also retained in the direction of excess Se, although deviation from stoichiometry toward excess Cu results in the formation of a secondary Cu_2Se phase.

Thin films of $CuInSe_2$ (with thicknesses of approximately 2 μm) deposited on Mo-coated glass or ceramic substrates always exhibit strong (112) orientation (2, 3), with grain sizes approaching 1 μm on the surface (4). Figure 2 shows a typical fractured cross-section and the surface of a $CuInSe_2$ film vapor deposited from elemental sources. As can be seen in the figure the grain structure is columnar and equiaxed on the plane normal to the growth direction. Transmission electron microscopy (TEM) analysis of these films shows a complex defect structure with high densities of dislocations, stacking faults, twins, and intergranular pores (5).

The band gap of $CuInSe_2$ is direct, is 1.02 $\pm$ 0.01 eV at room temperature, and has a temperature coefficient of $-2 \pm 1 \times 10^{-4}$ eV/K in the lower temperature regime (6). The typical absorption coefficient is larger than 5×10^4 cm^{-1} at photon energies greater than 1.4 eV.

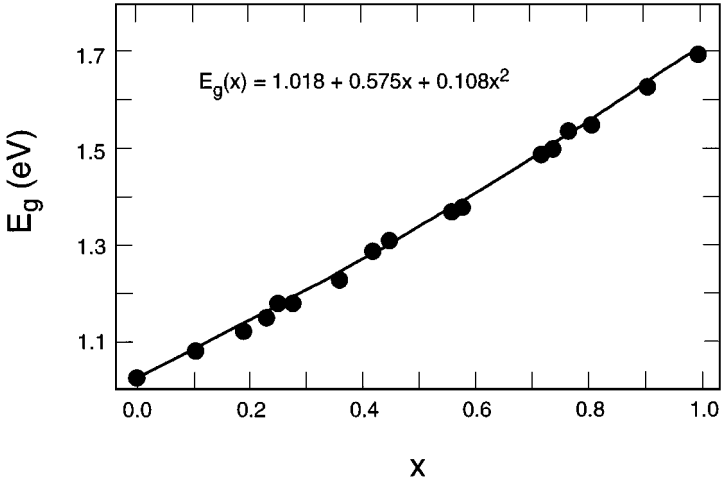

Figure 3 Band gap of $CuIn_{1-x}Ga_xSe_2$ thin film as a function of Ga content x (7).

The band gap of $CuInSe_2$ can be modified continuously over a wide range by substituting Ga for In. Figure 3 shows the variation of the band gap of $CuIn_{1-x}Ga_xSe_2$ thin film as a function of Ga content x (7). Similarly, one can also increase the band gap by substituting S for Se. Recent trends in $CuInSe_2$ research and development focus exclusively on these high band-gap alloys.

Electronic properties of $CuInSe_2$ are controlled largely by the intrinsic defect chemistry of the material. In general, the defect chemistry is complex; however, within ± 2 at % of the stoichiometric composition, various analyses of single crystals (8, 9) and thin films (10) give a relatively coherent model of the defect chemistry. Cu and In vacancies (excess Se), which are acceptors, yield strongly p-type material. In contrast, Se vacancies produce n-type material. Along or near the pseudo-binary tie line Cu_2Se-In_2Se_3, In-rich material have both In-on-Cu (In_{Cu}) antisite donor defects and Cu vacancy acceptors, resulting in heavily compensated n- or p-type material. In the case of excess Cu, dominant defects are Cu-on-In (Cu_{In}) antisite and In vacancy acceptors, which both contribute to a strongly p-type material. Mobilities determined by temperature-dependent transport measurements performed on single crystals (8, 9) were 15–150 $cm^2V^{-1}s^{-1}$ for p-type materials with carrier densities 0.15–2 $\times 10^{17}$ cm^{-3} at 300 K. For n-type materials, sample mobilities were 90–900 $cm^2V^{-1}s^{-1}$ for carrier densities from 1.8×10^{15} to 5×10^{17} cm^{-3} at 300 K. No correlations were found among carrier densities, mobilities, and composition.

Determination of the shallow level energies and their assignment to specific defects have not been very successful. Although substantial differences in these areas have been found between the above referenced transport studies and the photoluminescence data (11), electronic transport in $CuInSe_2$ and related alloys is dominated by intrinsic defects with heavy self-compensation. Polycrystalline thin films of $CuInSe_2$ can be used as absorbers in PV devices because their electronic transport is dominated by such defect structure. $CuInSe_2$ grain boundaries, which are parallel to the current-flow direction in these devices, can easily be modified electronically by dopants such as oxygen, and by low-temperature post-processing heat treatments, without affecting the bulk chemistry. As a result, grain boundaries can be made more p-type and thus are electronically benign since the minority carriers (i.e. electrons) cannot reach the grain boundaries to recombine.

Device Structure and Fabrication

$CuInSe_2$-based PV devices are obtained by forming p-n heterojunctions with thin films of CdS. In this type of structure, n-type CdS, which has a band gap of 2.4 eV, not only forms the p-n junction with p-type $CuInSe_2$ but also serves as a window layer that lets light through with relatively small absorption. Also, because the carrier density in CdS is much larger than in $CuInSe_2$, the depletion field is entirely in the $CuInSe_2$ film where electron-hole pairs are generated. As a result, minority carrier recombination at the metallurgical interface is minimized.

In the early 1980s the PV research group at Boeing was able to demonstrate 10% efficiency in a device with the "Mo/$CuInSe_2$ (3 μm)/CdS(2 μm)/AR Coating" structure (12). In this structure, 3 μm-thick $CuInSe_2$ was formed by thermal evaporation of the elemental constituents onto a Mo-coated alumina substrate. The deposition consisted of two stages in which the elemental fluxes were adjusted to be Cu-rich during the initial stage of the deposition at a substrate temperature of 350°C, forming a Cu-rich $CuInSe_2$ base film. In the final stage, the substrate temperature was raised to 450°C and the Cu:In flux ratio was reduced to less than 1. The stoichiometry of the completed $CuInSe_2$ film was Cu deficient. To complete the device structure, the In-doped CdS layer was then evaporated directly from the compound in a resistively heated Knudsen cell at a substrate temperature of approximately 175°C.

Investigation of Cu-rich (Cu-to-In ratio > 1) and Cu-deficient (Cu-to-In ratio < 1) $CuInSe_2$ films showed that the former had a matte appearance and a large grain structure while the latter had a specular appearance and a small grain structure (13). Thus it is likely that during two-stage deposition the Cu-rich base layer controls the structure while the Cu-deficient top layer controls the final composition. Furthermore, the same study showed that high-efficiency

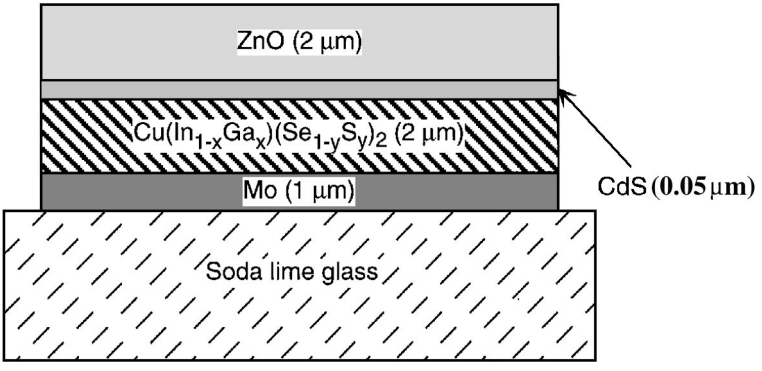

Figure 4 Typical structure of a $CuInSe_2$-based solar cell.

$CuInSe_2$ devices could be made from two-stage deposited $CuInSe_2$ films with large variation in the average composition as long as the overall Cu-to-In ratio is less than 1.

Over the years research groups have developed many variations of this basic structure in order to improve efficiency. The most recent structure, shown in its general form in Figure 4, incorporates three important variations:

1. It now seems certain that to retain proper junction characteristics and at the same time reduce absorption and resistive losses, CdS thickness must be reduced to 0.05 μm and a ZnO layer must be added onto the CdS layer as a transparent current-collecting conductor.

1. Substantial efficiency improvement can be achieved by partial substitution of In with Ga and S with Se because the higher band gap gives a better match to the solar spectrum.

2. Further improvements are obtained by incorporating Na into the $CuInSe_2$ layer, although the role Na plays in improving device efficiencies is not well known (14, 15). Soda lime glass used as substrate provides a practical, though uncontrollable, source of Na since at the process temperatures used, Na diffuses through the Mo layer into the $CuInSe_2$ film.

The chemical bath deposition (CBD) technique is the preferred method for depositing CdS films that are approximately 0.05 μm thick. This technique, which involves dipping the sample in an ammonia solution containing $CdSO_4$ and thiourea (16, 17), gives deposition rates on the order of 0.06 μm/min. The primary advantage of the CBD method is that it gives almost complete surface coverage even at such low thicknesses. Other vacuum deposition techniques

would require higher thicknesses to obtain complete surface coverage. However, because of environmental concerns related to cadmium, research efforts are being directed toward either finding a replacement for CdS or making direct rectifying contact with ZnO (18–20). However, at the present time, highest efficiencies are still obtained with CB deposited CdS films.

Deposition of the transparent conductor film ZnO is straightforward and is performed most commonly by room temperature sputtering in two steps. A 100- to 500-Å highly resistive ZnO film is deposited first, followed by a 0.1- to 2-μm highly conductive ($\approx$10–15 Ω/sq) film. The deposition rates are approximately 0.05 μm/min.

A variety of methods have been developed for the deposition of the $CuInSe_2$-based absorbers. In general, these processes can be divided into two categories: physical vapor deposition from three ($CuInSe_2$) or four ($CuIn_{1-x}Ga_xSe_2$) sources onto a heated substrate, and successive deposition of the metallic elements onto a substrate followed by reactive annealing of the resultant multi-layer structure in selenium- or selenium/sulfur-containing atmosphere.

MULTI-SOURCE THERMAL EVAPORATION To date, co-deposition from elemental sources has been the most successful approach to $CuInSe_2$ deposition, as it resulted in a 17.1%-efficiency $CuIn_{1-x}Ga_xSe_2$ device, the highest efficiency ever obtained in this material system (21). The $CuIn_{1-x}Ga_xSe_2$ films in high-efficiency devices contain 25–30% Ga, have a Cu:In ratio of 0.9–1.0, and are deposited at substrate temperatures of around 550°C and at rates on the order of 0.05 μm/min. During deposition, elemental fluxes are changed so that during film growth the Cu:(In+Ga) ratio is greater than 1 during the early stages of the deposition, similar to the Boeing process, creating a Cu-rich film. The Cu:(In+Ga) ratio is reduced to much less than 1 at the end of the deposition, which controls the stoichiometry of the final film. The final composition of the film is Cu deficient and the surface of the film appears to be terminated by an ordered vacancy compound (OVC) (22). The post-deposition elemental depth profile of these films does not show a detectable Cu gradient. As a result, researchers have conjectured that the clearly faceted large-grained microstructure resulting from the larger Cu flux at the early stages of film growth is maintained during later stages and is more conducive to higher conversion efficiencies. However, there are no quantitative correlations among time dependence of Cu flux, microstructure, and efficiency.

Other elemental gradients that maintain the desired Cu:(Ga+In) gradient, at least on the top portion of the film, also have been tried. Specifically, the Ga and In fluxes can be varied during growth, resulting in the variation of the Ga:(Ga+In) ratio in the film and, consequently, of the electronic properties through the film. The highest-efficiency solar cells have higher Ga content at

the back of the film. However, the important issue is that the Ga:(Ga+In) ratio can be varied through the thickness of the film, allowing the electronic properties of the $CuIn_{1-x}Ga_xSe_2$ film to be engineered to optimize the device structure. Several research groups are presently evaluating graded $CuIn_{1-x}Ga_xSe_2$ layers to improve device properties.

Another variant of the multi-source evaporation process involves the incorporation of a 2000-Å $CuGaSe_2$ layer, deposited at 350°C, between the Mo contact layer and the $CuIn_{1-x}Ga_xSe_2$ film. The absorber in the highest-efficiency device, referenced above, was deposited by this type of two-stage process; however, the precise mechanism by which the $CuGaSe_2$ intermediate layer improves efficiency is not well understood.

In principle, S may be incorporated into the absorber using a co-deposition process to obtain films with the general chemical formula of $CuIn_{1-x}Ga_x(Se_{1-y}S_y)_2$. Such systems are difficult to synthesize, however, and do not give encouraging results primarily because of excessive shunting and less-than-expected improvement in the open-circuit voltage. Nevertheless, a device efficiency of 12% has been obtained with a co-deposited $CuInS_2$ absorber (23).

REACTIVE ANNEALING OF PRECURSOR FILMS The second method for forming $CuInSe_2$-based absorber layers involves a two-step process. In the most commonly used variation, Cu and In of appropriate thicknesses are first deposited by room temperature sputtering onto Mo-coated glass substrates. In a second step, this multi-layer structure is annealed in H_2Se/Ar atmosphere at temperatures around 450–550°C for about 60 min, resulting in a final absorber thickness of 2.5 μm. Even though this is a two-step process and results in efficiencies less than that of the co-deposition process, it has attracted considerable attention because it is thought to be easier to use on a larger scale than is the co-deposition process.

Variations of this absorber-formation technique include cases where Cu/In/Se or $InSe_x$/Cu thin film structures are used as precursors, and Se vapor and even inert gases are used as annealing atmospheres (24). For example, Siemens Solar Industries in the United States developed a process in which metal precursor layers (e.g. Cu, In, Ga) are selenized in H_2Se/Ar in which H_2S gas is introduced in the final stages of the reaction. This process resulted in small-area cell efficiencies of around 16% (25). Most recently, Siemens AG in Germany developed a process in which Cu, In, Ga, and Se layers were deposited on Mo-coated substrates and subsequently subjected to rapid thermal processing (RTP) in an inert atmosphere. Small-area cell efficiencies of 13.3% and 14.6% were obtained for $CuIn_{1-x}Ga_xSe_2$- and $CuIn_{1-x}Ga_x(Se_{1-y}S_y)_2$-type cells, respectively (26).

In the previously described processes, Ga is distributed nonuniformly along the film thickness and migrates preferentially to the Mo-absorber interface.

Consequently, the junction does not contain Ga, and the device has the characteristics of a $CuInSe_2$ solar cell. Detailed analysis of this problem gives the following picture (27): Because of their higher reactivity to Se, Cu and In diffuse to the surface during the selenization reaction to form $CuInSe_2$. After the In is completely consumed to form $CuInSe_2$ and presumably some Cu_2Se on the surface, selenization of Ga and its reaction with Cu_2Se proceeds to form $CuGaSe_2$ at the Mo interface. In order to intermix $CuInSe_2$ and $CuGaSe_2$ layers to form single-phase $CuIn_{1-x}Ga_xSe_2$, the annealing step needs to be continued in an inert atmosphere at a temperature of at least 550°C. The inert atmosphere anneal is thought to be necessary to create a defect structure that facilitates In and Ga diffusion.

Devices utilizing the Siemens Solar process or the RTP process have Ga at the Mo interface and, as a result, do not use Ga to increase band gap. The band gap increase is achieved by the incorporation of S into the absorber. In contrast, because a Ga-containing interfacial layer seems to improve uniformity and adhesion, Ga is being used widely in absorber synthesis by reactive annealing of precursor films.

Device Analysis and Performance

Figure 5 illustrates the band diagram of the $CuInSe_2$/CdS heterostructure and is used commonly to model operational characteristics of the $CuInSe_2$-based photovoltaic devices (see also 28).

Carrier collection in these devices is quite efficient in that minority carrier recombination at the grain boundaries is minimized because the grain boundaries are more p-type compared to the bulk. Furthermore, minimal recombination is found at the metallurgical interface most likely owing to a combination of OVC surface structure of the $CuIn_{1-x}Ga_xSe_2$ film and the interaction with the solution-grown CdS modifying electronic properties of the interface. This observation is important because even under ideal processing conditions, the defect density at the metallurgical interface is quite high as a result of the lattice mismatch between CdS and $CuInSe_2$. In addition, because of the high absorption coefficient of $CuInSe_2$-based materials, most of the carriers are generated close to the interface, further aiding their efficient collection.

Current-voltage characteristics of a solar cell with a simple series resistance can be described as:

$$J = J_D - J_{sc} = \mathrm{q}vN\mathrm{e}^{\frac{-\mathrm{q}\phi}{\mathrm{k}T}}\mathrm{e}^{\frac{\mathrm{q}(V-JR_S)}{AkT}} - J_{sc}. \qquad 1.$$

In this equation J_D is the diode current, v is the carrier velocity, N is the density of states, ϕ is the barrier height, J is the current density, V is the voltage, A is the diode quality factor, and J_{sc} is the short-circuit current.

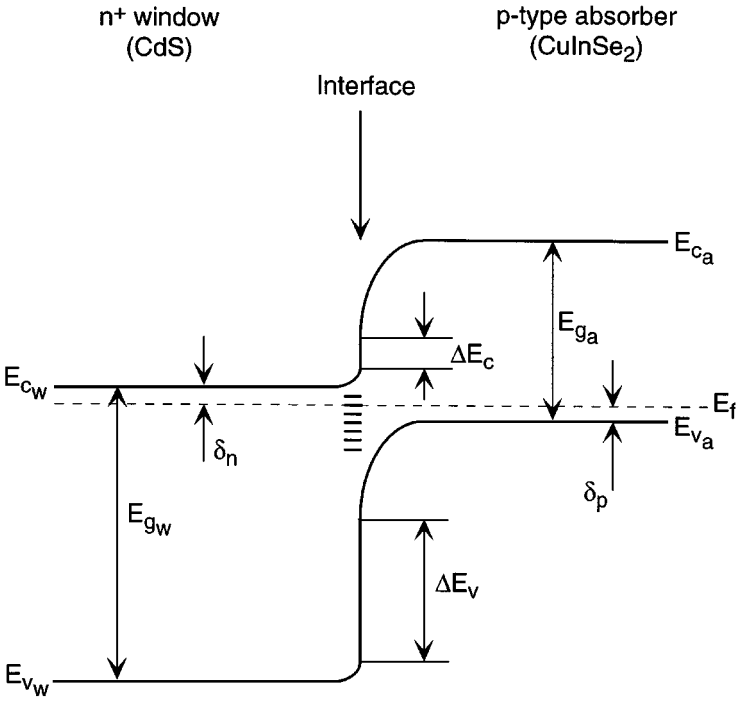

Figure 5 Energy band diagram of CdS/$CuInSe_2$ heterojunction.

The open-circuit voltage V_{oc} (i.e. $V_{at}\, J = 0$) of the device is given by:

$$V_{oc} = \frac{A}{\mathrm{q}} \left\{ \phi - (\mathrm{k}T)\mathrm{Ln}\left[\frac{J_{00}}{J_{sc}}\right] \right\}, \qquad 2.$$

where $J_{00} = \mathrm{q}vN$.

From Equation 2 it is easy to see that high-efficiency devices (i.e. when V_{oc} is high) require the diode current, J_D, to be as small as possible. In general, diode current is controlled by the highest of the electron injection, space charge recombination, and interface recombination currents. Each of these mechanisms is defined with a different set of so-called effective parameters: v, N, ϕ, and A. For $CuInSe_2$-based devices, a number of measurements indicate that the diode current is controlled by the recombination through a distribution of states in the space charge region, resulting in a diode quality factor between 1 and 2, and $\phi = \mathrm{E}_{\mathrm{g}_{\mathrm{CuInSe_2}}}$ (28).

Despite considerable effort, $CuInSe_2$ solar cells without Ga and/or S have been limited to V_{oc}s of 500 mV or less because the exact nature of the defects in

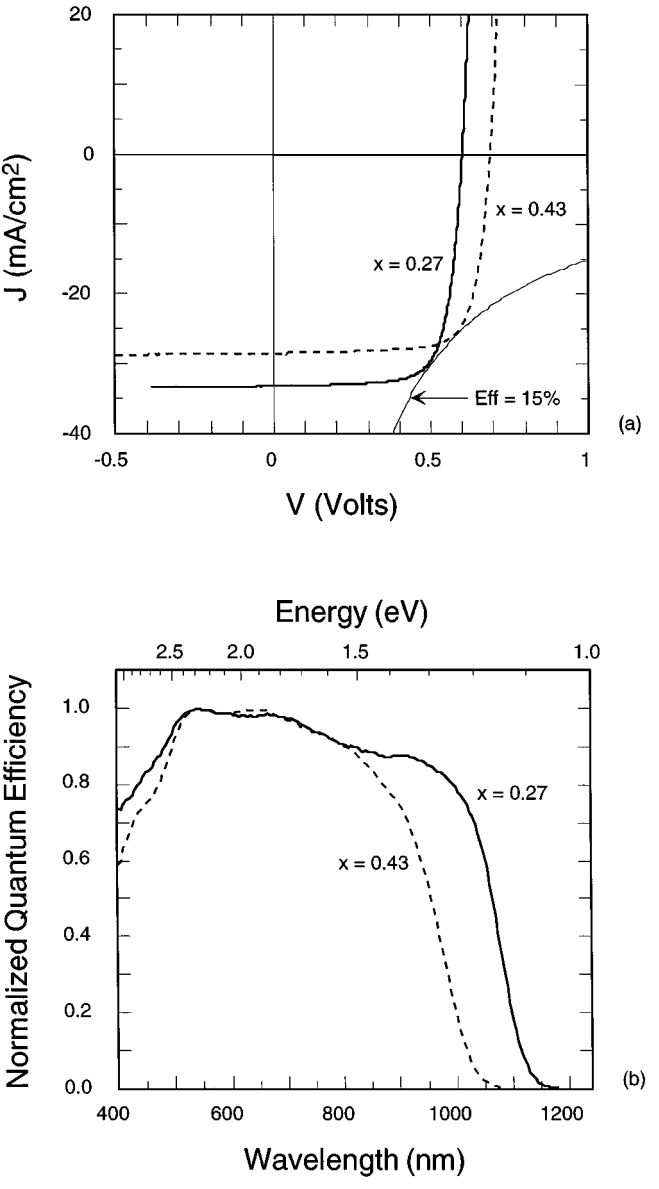

Figure 6 *J-V* characteristics (*a*), and quantum efficiencies (*b*) of two $CuIn_{1-x}Ga_xSe_2$ devices with different Ga content *x*.

the space charge region could not be identified and, as a result, recombination currents could not be reduced. Current research on improving the efficiency of $CuInSe_2$-based solar cells is focusing on increasing the band gap by alloying with Ga and to a lesser extent with S. This approach may not improve material quality, but it gives a better match of the band gap to the solar spectrum.

An extensive investigation of $CuIn_{1-x}Ga_x Se_2$-based, multi-source deposited, solar cells as a function of Ga content can be found in References 29 and 30. Figure 6 shows the *J-V* characteristics and the normalized quantum efficiencies of two devices with Ga contents of 27% and 43% (WN Shafarman, private communication). In this case, the open-circuit voltage gain achieved with the higher Ga content is offset by the lower short-circuit current density due to the reduced absorption and collection efficiency, resulting in similar efficiencies for both devices. The shift of the quantum efficiency curve to a lower wavelength with higher Ga content is consistent with the higher band gap absorber. Figure 7 shows the relationship between absorber energy gap and the open-circuit voltage and device efficiency for a large variation in Ga content (29, 30). These data

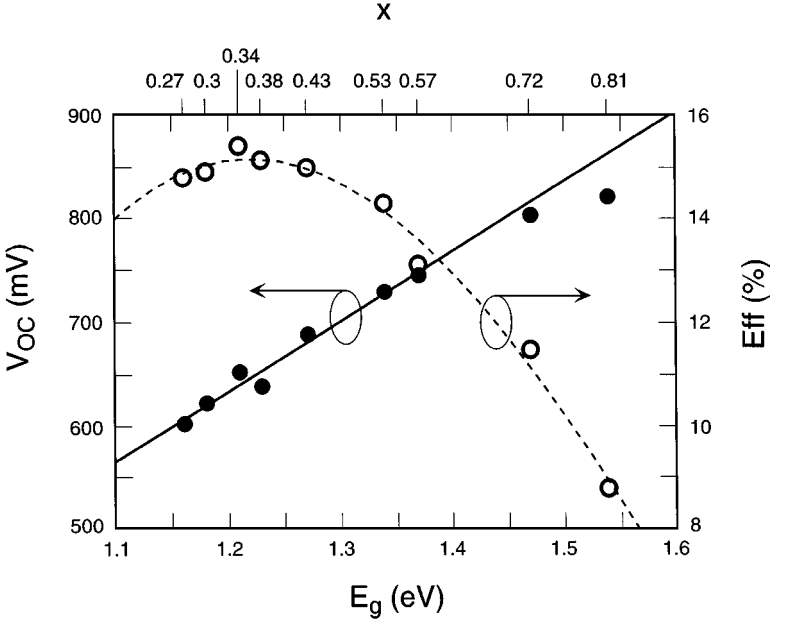

Figure 7 Open-circuit voltage and efficiency as a function of energy gap in $CuIn_{1-x}Ga_xSe_2$ devices. Ga content *x* is shown on top. Dashed line is for visual aid only. Data from References 27 and 28.

show that V_{oc} scales linearly with E_g over a wide range (up to 1.4 eV) of Ga concentration, but the efficiency does not reflect this increase in V_{oc} and, in fact, decreases when E_g is greater than 1.25 eV. This observation indicates that, within this range of Ga, current-collection efficiency decreases with Ga content. It is unknown whether this reduction results from the reduced carrier density in the material extending the space charge region (thus decreasing the field strength) or from the reduced diffusion length.

SOLAR CELLS BASED ON CdTe

Materials and Electronic Properties of the Absorber

CdTe is a compound semiconductor of II-VI type that has a cubic zincblende (sphalerite) structure with a lattice constant of 6.481 Å. Extensive information on the electronic properties and the defect chemistry of CdTe can be found in the literature (31–33). The stability region of the compound is extremely narrow (2×10^{-6} at.% wide) and is symmetrical around perfect stoichiometry at 400°C. Close to the melting point (1090°C), the stability region on the Te-rich side increases to about 10^{-5} at.%. In a vacuum, CdTe sublimates in such a way that the vapor phase consists of Cd atoms and Te_2 molecules in exact proportion to the solid, that is, $p_{Cd} = 2 \times p_{Te_2}$. Consequently, deposition of CdTe films by thermal evaporation does not present any compositional problems. The variation of the Cd partial pressure as a function of CdTe source temperature is shown in Figure 8 (31).

CdTe at room temperature has a direct band gap of 1.5 eV with a temperature coefficient of $2.3–5.4 \times 10^{-4}$ eV/K (31). This band gap is an ideal match to the solar spectrum for a photovoltaic absorber. As with $CuInSe_2$, the absorption coefficient is large (around 5×10^4 cm^{-1}) at photon energies of 1.8 eV or greater. As a result, a CdTe-based solar cell would have a theoretical conversion efficiency on the order of 28%; however, the highest conversion efficiency achieved to date is 15.8% (34).

In their as-deposited form, thin films of CdTe always show a columnar grain structure with submicron grain size unless the films are deposited by high-temperature processes (>500°C) such as close-space sublimation (CSS), screen printing, or spray pyrolysis. Figure 9 shows a vapor-deposited CdTe film on glass/ITO/CdS (BE McCandless, LV Moulton, RW Birkmire et al, unpublished information). This TEM cross-section micrograph illustrates a structure in which CdTe grain size seems to be determined by the grain size of the underlying CdS film, indicating pseudo-epitaxial growth. In the case of CdTe films deposited by high-temperature processes, the grain structure is still columnar in that the grain boundaries are normal to the substrate, but the grain sizes are much larger, on the order of film thicknesses 2 μm–15 μm, depending on the specific

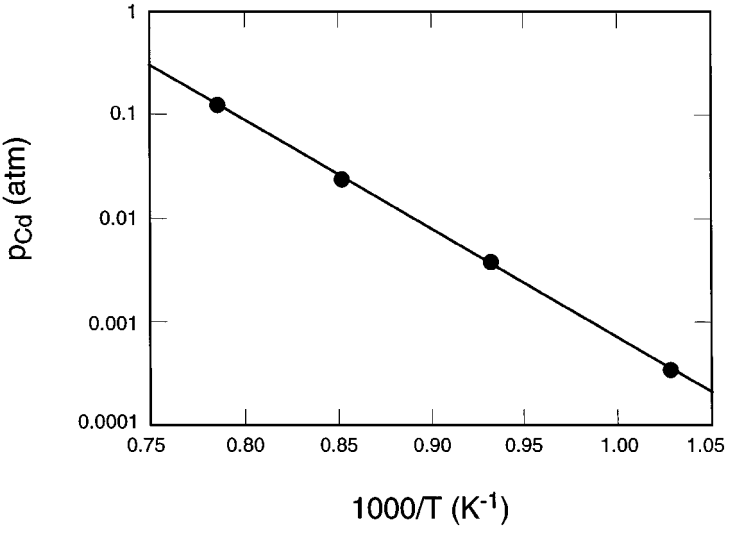

Figure 8 Variation of Cd partial pressure as a function of CdTe in free evaporation regime. Data from Reference 30.

process. Vapor-deposited films such as the one in Figure 9 show a somewhat pronounced (111) orientation. However, the orientation in CdTe films depends strongly on the type of processes used, and in some cases completely random films can be obtained. As a general rule, the lower the process temperature, the higher the preferred (111) orientation.

The predominant intrinsic defects in CdTe are cadmium interstitials (Cd_i) and cadmium vacancies (V_{Cd}). Energy levels associated with these defects are 0.02 eV below the conduction band and 0.15 eV above the conduction band, respectively (31). CdTe can be doped extrinsically in both n- and p-type forms. Indium in Cd site (In_{Cd}) forms a donor level at 0.60 eV below the conduction band, whereas Cu, Ag, and Au in Cd site (Cu_{Cd}, Ag_{Cd}, and Au_{Cd}) form acceptor levels 0.33 eV above the valance band (31). Room temperature mobilities up to 1100 $cm^2V^{-1}s^{-1}$ for electrons and up to 80 $cm^2\ V^{-1}s^{-1}$ for holes have been reported (35–38).

Controlled doping of single-crystal CdTe is a somewhat difficult process, especially for p-type materials, primarily because of (*a*) the compensation effects; (*b*) the large difference in the vapor pressure of Cd and Te, which makes it difficult to control stoichiometry; and (*c*) poor dopant solubility. Nevertheless, electrically active dopant densities up to 10^{17} cm^{-3} can be obtained in both n- and p-type materials. In polycrystalline thin films, doping becomes even more difficult because of the enhanced compensation and segregation effects at the

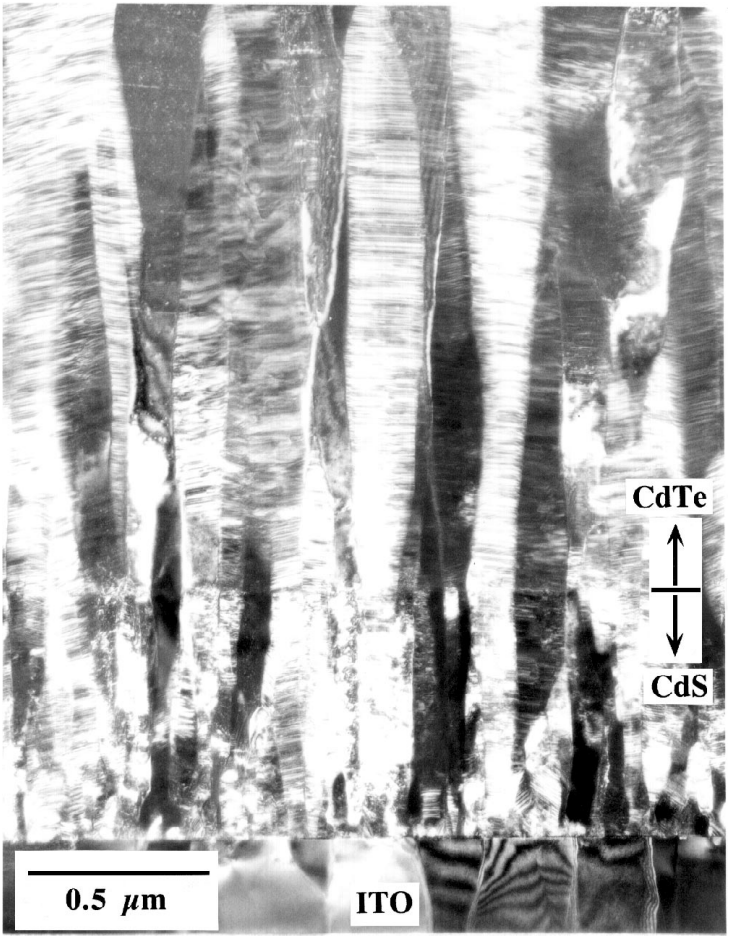

Figure 9 TEM micrograph showing the as-deposited cross-section of ITO/CdS/CdTe structure. Both CdS and CdTe are vapor deposited from the respective compounds.

grain boundaries. Difficulties encountered in doping of CdTe do not affect its PV performance, but they do create problems in making low-resistance ohmic contact to the material. In fact, because of these characteristics of the doping mechanism, the grain boundaries in polycrystalline CdTe thin films can be made more p-type than the bulk (similar to the $CuInSe_2$-based solar cells), reducing and even eliminating the minority carrier (i.e. electron) recombination at the grain boundaries.

Device Structure and Fabrication

CdTe solar cells are p-n heterojunction devices in which a thin film of CdS forms the n-type window layer. As in the case of $CuInSe_2$-based devices the depletion field is mostly in the CdTe. The structure is of superstrate type in that the transparent conductor and the window layer are first deposited onto a transparent substrate such as glass (Figure 10). The absorber, in this case CdTe, is deposited over the window layer.

The transparent conductor is deposited most commonly by sputtering in the case of ITO or by atmospheric pressure chemical vapor deposition (APCVD) in the case of SnO_2. The thickness is around 1 μm and is a compromise between the sheet resistance and the optical transmission. In general, a sheet resistance of 10 Ω/sq is adequate for current collection without appreciable resistive losses. The choice between ITO and SnO_2 is determined primarily by the deposition temperature of CdS and/or CdTe films. For low-temperature CdS and CdTe deposition processes, ITO is the material of choice because it has higher optical transmission for a given sheet resistance. For CdS or CdTe deposition processes requiring high temperatures, SnO_2 is the material of choice since it is more stable mainly because the APCVD process itself requires temperatures around 550°C.

Several processes, such as physical vapor deposition (PVD), chemical bath deposition (CBD), close-space sublimation (CSS), sputtering, screen printing, electrodeposition, and spray pyrolysis can be used to deposit the CdS layer. In high-efficiency devices, where high-transmission window layers are required, CdS film thicknesses must be less than 0.1 μm. Such thicknesses can be obtained by all the processes just mentioned except for screen printing and spray pyrolysis. However, CBD is the preferred choice for reasons stated previously

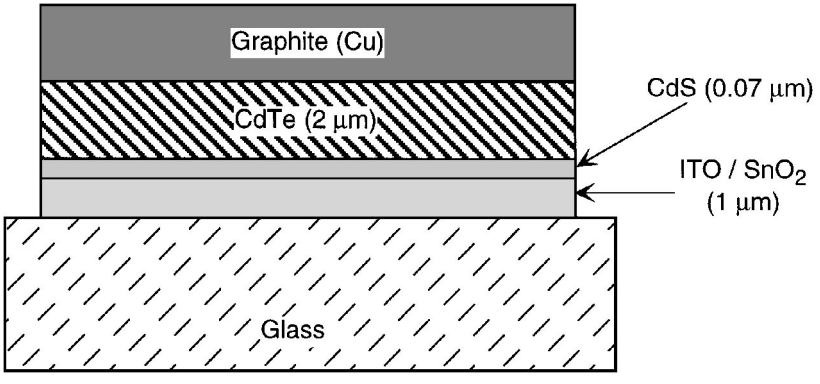

Figure 10 Typical structure of a CdS/CdTe solar cell.

in the case of $CuInSe_2$-based solar cells. Such thin films of CdS, deposited by low-temperature processes such as PVD, CBD, sputtering, and electrodeposition, benefit from a post-deposition treatment in a reducing atmosphere or in the presence of $CdCl_2$, which increases grain size and reduces defect density (39, 40). In the case of thin CdS films deposited by CSS at temperatures around 500°C, such a post-deposition heat treatment was unnecessary (41).

As in the case of CdS films, a variety of deposition techniques can be used for the deposition of CdTe films. The most widely used techniques are electrodeposition, PVD, CSS, screen printing, and spray pyrolysis. These techniques encompass a range of process temperatures from room temperature to 600°C and a range of thicknesses from 1.5 to 15 μm.

Electrodeposition of CdTe is performed in an aqueous electrolyte containing Cd^{2+} and $HTeO_2^+$ ions. The deposition takes place in two steps and can be represented by the following two reactions:

$$HTeO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O \qquad 3.$$

$$Te + Cd_2^+ + 2e^- \rightarrow CdTe \qquad 4.$$

Because of the low solubility of TeO_2, the deposition process is mass transport–controlled by the availability of $HTeO_2^+$ ions. Electrolyte that contains an excess of Cd^{2+} ions at all times is maintained at approximately 90°C. The process gives deposition rates on the order of 0.02 μm/min. Structurally the as-deposited films have columnar submicron grains with a (111) preferred orientation, similar to the films obtained by the PVD process (Figure 9).

PVD of CdTe consists of evaporating CdTe source material under high vacuum from a Knudsen cell onto a substrate heated to around 275°C. A deposition rate of 0.25 μm/min is obtained for a source temperature of 890°C and a source-to-substrate distance of 20 cm.

The CSS process is based on the reversible dissociation of CdTe at high temperature:

$$2CdTe(s) \leftrightarrow Cd(g) + Te_2(g) \qquad 5.$$

In practice, the CdTe source and the substrate, separated by 0.2 cm, are heated to 650–700°C and 550–600°C, respectively, in an ambient of 10 torr of argon, which may contain small amounts of oxygen (10% by pressure). Under these conditions CdTe films of well-faceted 3–5 μm grains are deposited at a rate of 1 μm/min. They exhibit a very weak (111) crystallographic orientation.

Screen printing is a simple nonvacuum process that starts with ball milling, in water, high-purity Cd and Te powders down to a few micron in size. A paste is prepared by adding approximately 1% by weight of $CdCl_2$ as the fluxing

agent and a suitable amount of propylene glycol as the binder. The paste is then screen printed through a 400 mesh stainless steel screen onto the substrate. Printed "green" film is then dried at 120°C for 1 h in nitrogen, and sintered at 600–700°C for 1 h in nitrogen or nitrogen/oxygen atmosphere. The CdTe film thus obtained has an overall thickness of approximately 15 μm and shows two distinct structures through its thickness. The top 10–12-μm portion of the film is porous and has a grain size of 3–5 μm. The remaining 3–5 μm in contact with the CdS layer is a one-grain-thick layer of dense $CdTe_{1-y}S_y$ resulting from the interdiffusion of CdTe and CdS (see below for further explanation). X-ray diffraction analysis indicates a randomly oriented grain structure.

The most successful spray pyrolysis method uses a spray mixture of deoxidized 0.3-μm CdTe powder, $CdCl_2$ and propylene glycol. This mixture is sprayed at room temperature and baked at 200°C. After the bake, the film is heat treated in an oxidizing atmosphere at temperatures from 300 to 550°C for about 60 min followed by a 40% densification of the film by physical compacting. In the final step, the film is recrystallized in an inert atmosphere at approximately 550°C for 60 min (42). Typical film thicknesses are 5–10 μm. Similar to the films obtained by screen printing, these films have a porous top portion and a dense structure in contact with a Te-saturated CdS layer. More detailed information on the characteristics of these layers is not available because of the proprietary nature of this process. Detailed descriptions of the other processes can be found in Reference 43.

In these processes the PV performance of the CdS/CdTe device in the as-deposited state is poor. Post-deposition heat treatment in chlorine- and oxygen-containing atmosphere is necessary to obtain the desired PV performance. Such a treatment, for example, consists of dipping the CdS/CdTe structure into a $CdCl_2$-methanol solution and heating it in air at 400°C for 10 to 30 min, after which the sample is rinsed in deionized water to remove excess $CdCl_2$ (44). Alternatively, the solution treatment can be replaced by performing the heat treatment in the presence of $CdCl_2$ vapors from a solid source kept at an appropriate temperature (45). In some cases, such as electrodeposition, spray pyrolysis, or screen printing, the process itself provides the chlorine, in which case the post-deposition heat treatment in an oxidizing atmosphere would not need to contain chlorine. The effect of the $CdCl_2/O_2$ treatment on the structure of the CdS/CdTe thin film couples prepared by the PVD method is documented, qualitatively, to a certain extent:

1. As can be seen from the TEM micrograph in Figure 11(BE McCandless, unpublished information), when compared to Figure 9, there is a factor of almost 10 growth in the grain size of both CdS and CdTe films. Columnar structure observed in the as-deposited state becomes equiaxed as a result of

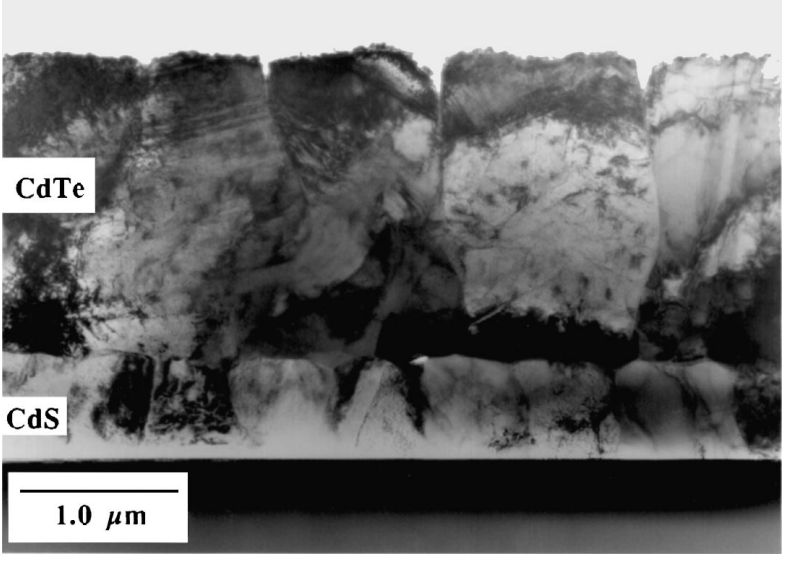

Figure 11 TEM micrograph showing the cross-section of CdS/CdTe structure vapor deposited from compound sources after $CdCl_2/O_2$ heat treatment.

the treatment. There is a marked reduction in the defects in CdS, but CdTe grains still show high levels of intragrain defects.

2. After the treatment, the preferred (111) orientation of the CdTe films is reduced, and in some cases disappears completely.

3. X-ray diffraction (XRD) analysis and the quantum efficiency measurements on the completed devices show that there is interdiffusion of S and Te into CdTe and CdS, respectively (46), forming a $CdS_{1-x}Te_x$ /$CdTe_{1-y}S_y$ junction. This interdiffusion was qualitatively in line with the pseudo-binary CdTe/CdS phase diagram (47), but the solubility limits were determined, more accurately, to be $x = 0.03$ and $y = 0.06$ at 415°C treatment temperature. As a result of this interdiffusion, the optical band gaps on either side of the junction are reduced to 1.45 eV in the absorber and to 2.1 eV in the window (48).

The exact mechanisms by which $CdCl_2/O_2$ treatment causes these structural changes is still unknown. More important, our understanding of the effects of this type of heat treatment on the operation of CdTe solar cells, either through the above structural changes or through other structural or electronic modifications yet unknown, are at best conjectural. As a result, the $CdCl_2/O_2$ treatment

is at this point a "recipe" that seems to be necessary for CdTe-based solar cells regardless of the methods of preparation. Detailed and quantitative understanding of this issue is necessary for further advances in the technology of CdTe solar cells.

The final step in completing the CdS/CdTe device is the formation of a low-resistance ohmic contact to carry the photogenerated current. The process, which is rather straightforward in other PV devices, is complicated in the case of CdTe. Because there is no metal with a large-enough work function to give a direct ohmic contact to p-type CdTe, it is necessary to produce, in a first step, a heavily doped or degenerate layer on the surface of the material. In general, the process starts with a wet chemical etch with bromine-methanol, which leaves a Te-rich surface layer. Then a p^+ layer is formed by depositing ZnTe-Cu; HgTe; PbTe; or p-type dopants such as Cu, Hg, Pb, or Au followed by a heat treatment at or above 150°C. Application of a secondary conductor having appropriate sheet resistance completes the device. The whole process is not well understood, and again has a "recipe" aspect to it in that every group working in this field seems to have its own contacting procedure. As a result, the reliability of the process of forming ohmic contacts on CdTe layers needs to be resolved (see 49).

Several processing methods are common to both CdS and CdTe films, such as PVD, CSS, screen printing, electrodeposition, and spray pyrolysis. This is an important fact when considering options for scale-up since there would be a significant manufacturing cost savings if the same process were used for the processing of the window layer and the absorber. In fact, all efforts to develop PV-module manufacturing systems have taken this approach. Nevertheless, the highest efficiency achieved so far in CdS/CdTe solar-cell research uses a hybrid approach, in which CdS is deposited by the CBD technique, and CdTe by CSS (34).

Device Analysis and Performance

Operating principles of CdTe PV devices are similar to the $CuInSe_2$-based devices, and the previous discussion presented for $CuInSe_2$ is valid for CdTe, including the heterojunction band diagram and the characteristic transport equations. These material systems perform well as PV devices because of the benign nature of the grain boundaries. Furthermore, reducing the recombination current in the space charge region, thus improving V_{oc}, is the main challenge facing researchers. Even the beneficial effects of oxygen heat treatments seem to be present in both material systems.

What is specific to CdTe-based devices is the magnitude of the effect of $CdCl_2/O_2$ heat treatments on the efficiency and the difficulty of making an ohmic contact to the CdTe layer. Figure 12 illustrates the effect of $CdCl_2/O_2$

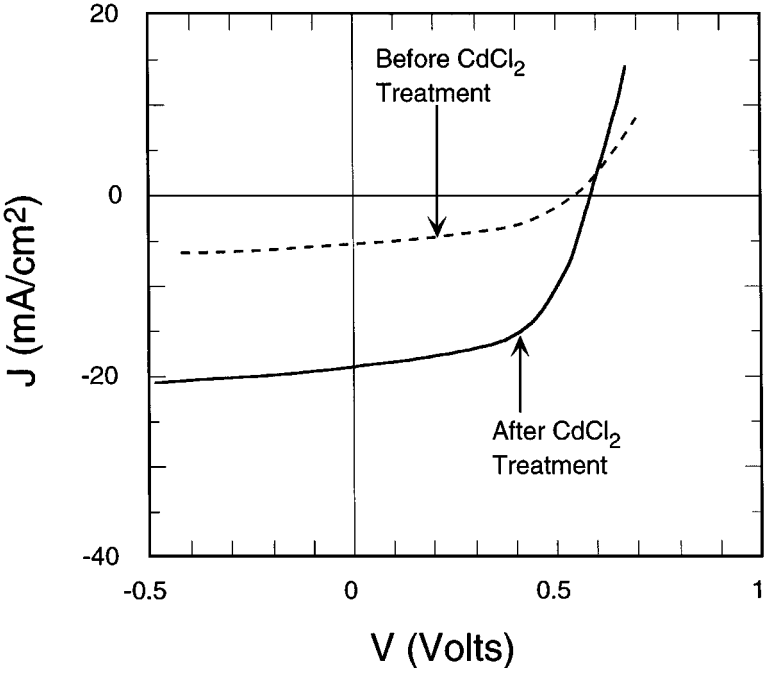

Figure 12 *J-V* characteristics of a CdS/CdTe device before and after $CdCl_2/O_2$ heat treatment.

heat treatment on the cell performance, showing the J-V characteristics of the device before and after the treatment. The figure illustrates that without $CdCl_2/O_2$ treatment the device does not even show an acceptable rectifying character. Figure 13, in contrast, compares the J-V characteristics of a device that has a low-resistivity ohmic contact to the CdTe layer with one in which the contact has some blocking character.

POTENTIAL FOR SCALE-UP

In order to analyze issues related to large-scale manufacturing of thin film polycrystalline PV modules, we must first quantify what is meant by *large-scale.* A typical commercial-size module would be 4×2 ft^2 in size and would have a number of cells, again typically defined and series-interconnected by laser scribing, a process commonly referred to as the *monolithic integration.* These cells would be slightly less than 4 ft long and have a width *w* determined by the highest sheet resistance of the two current-collecting conductive layers. Figure 14 shows the cross-section of such a module; a number of cells between

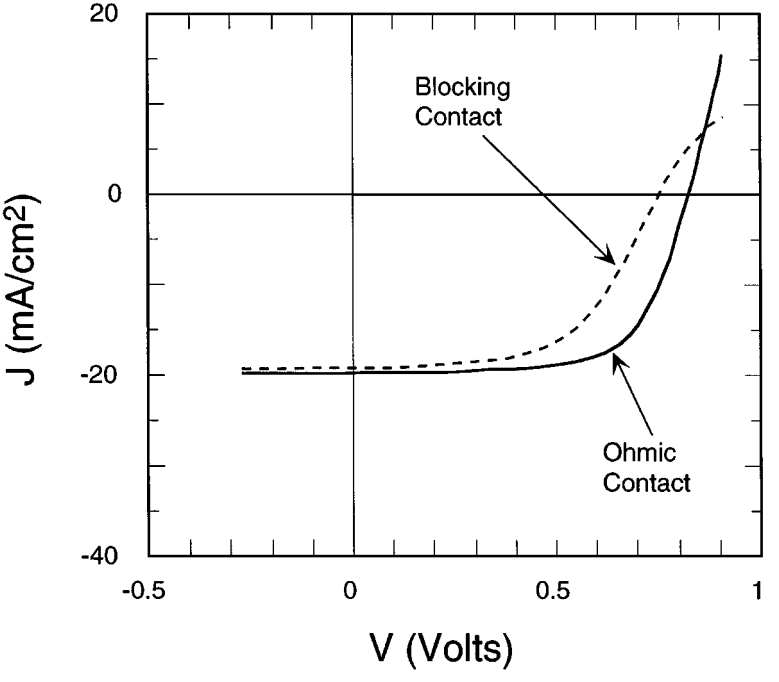

Figure 13 *J-V* characteristics of two CdS/CdTe devices showing the effect of blocking contact on CdTe.

the two edge contacts are omitted for clarity. The module is then completed by laying an encapsulant such as ethyl vinyl acetate (EVA) over the cells, covering it with another piece of glass, and curing the EVA. Finally, current leads are attached to the contacts for external connections.

A $CuIn_{1-x}Ga_xSe_2$ or CdTe module prepared using the processes that yield the best efficiencies in the laboratory would produce a power output of 80 W_p [peak watt, the unit of power, in Watts, that defines the maximum power a PV module can deliver under 100 mW/cm^2 solar radiation of air mass 1.5 spectrum (ASTM Stand. E891-82 and E892-82) and at 25°C], corresponding approximately to an active area efficiency of 10%. Assuming 100% yield, a factory with a nominal annual output of 10 MW_p, operating three shifts, 250 days/yr with 83% process up-time, would need to produce roughly one such module every 2.5 min. Furthermore, the cost of manufacturing must be low enough for widespread acceptance of such modules in the marketplace for a variety of applications. These numbers alone illustrate the magnitude of the challenges faced in the development of PV-module manufacturing technology.

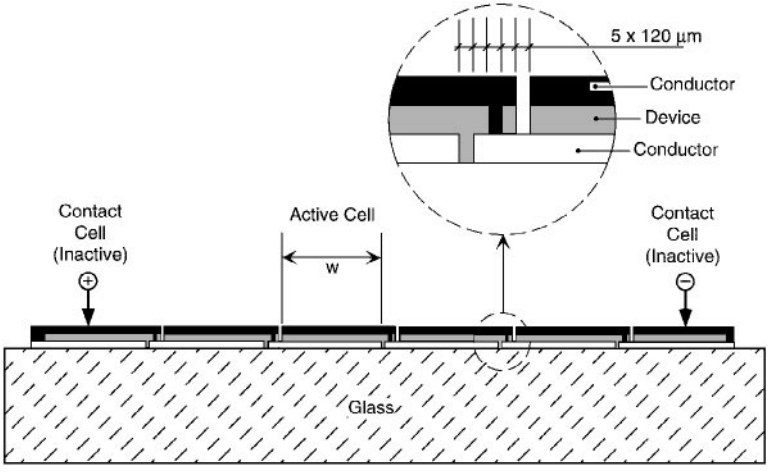

Figure 14 Schematic cross-sectional view of a polycrystalline thin film photovoltaic module.

The problem of scale-up raises several technical issues that can be divided into three categories: process-related issues, manufacturing costs, and environmental issues.

Process-Related Issues

For large-scale manufacturing of the $CuInSe_2$-based PV modules, further developments are needed in three important areas: high Ga devices, Mo deposition on glass, and controlled Na doping.

In the design of a typical module given in Figure 14 the sheet resistance of the ZnO transparent conductor cannot be made lower than 10 Ω/sq without excessive current loss due to the absorption of light in the ZnO layer. Under these circumstances the cell width w is a compromise between resistive and area losses. As the cell width is decreased, the resistive losses will decrease, but the active area losses, given by the ratio of the width of the scribe region to the cell width, will increase. In monolithically interconnected modules all resistive power losses are to a first approximation proportional to (J_{sc}/V_{oc}). Therefore, for a given efficiency it is more advantageous to have a high-voltage low-current device than the opposite. Unfortunately, the highest-efficiency $CuIn_{1-x}Ga_xSe_2$ devices currently available are low-voltage high-current (≈600 mV, 33 mA/cm^2) devices that result in a minimum total power loss of approximately 12% for a cell width of 0.5 cm. The solution to this problem lies in the development of high-Ga-content (60 to 70%) $CuIn_{1-x}Ga_xSe_2$ solar cells. A better understanding of the efficiency-limiting mechanisms in $CuIn_{1-x}Ga_xSe_2$ cells with high Ga content would bring about such a solution.

Poor adhesion of Mo on glass is another technical issue facing $CuIn_{1-x}Ga_xSe_2$ technology. Strong adhesion of metal films, especially as thick as 1–2 μm, has always been difficult to achieve. Because glass is such an inert material, chemisorption—which results in very strong bonding between the film and the glass substrate—does not play a role at temperatures encountered during sputtering. As a result, the primary forces controlling adhesion are weak Van der Waals forces. Under these conditions, one can improve adhesion by using a variety of extremely complicated glass-cleaning procedures before the deposition, but even then the physical strength of the interface would remain questionable, thus affecting manufacturing yield. Besides optimizing Mo thickness, low-cost adhesion-promoting interfacial films need to be developed to solve this problem.

It is now well accepted that Na incorporation into the $CuIn_{1-x}Ga_xSe_2$ film improves the device efficiency. In fact, a measurable efficiency improvement has been observed in every research group when soda lime glass replaced type 7059 glass as the substrate. From a manufacturing perspective, the use of soda lime glass substrate as a Na source is desirable, especially since the Na content of this type of glass is quite constant and uniformly distributed. However, the optimum amount and distribution of Na in the $CuIn_{1-x}Ga_xSe_2$ film, as well as the kinetics of the out-diffusion of Na from the soda lime glass and through the adhesion-promoting layer–Mo structure needs to be determined. In the absence of such quantitative information, reproducibility and yield associated with Na doping will be a major technical problem in the manufacturing environment.

In CdTe-module manufacturing the major process-related issues are $CdCl_2/O_2$ treatment and CdTe contacting. In both cases, processes developed in the laboratory so far have a "recipe" nature to them and are not acceptable as manufacturing processes. Further progress is needed in both areas in order to quantify the role of Cl_2 and O_2 in developing proper junction characteristics and the role of various surface pretreatments for proper contact formation. Such quantitative information is essential for the development of low-cost scaleable processes.

Manufacturing Costs

The most important factor in the cost of manufacturing thin film devices is the cost of the process equipment and raw materials. The most widely studied process for depositing $CuIn_{1-x}Ga_xSe_2$ films (and the one that produced the highest efficiency cells) is the four-source PVD. In this process, the deposition takes place in a vacuum environment at a rate of approximately 0.05 μm/min and at a substrate temperature of around 550°C, which is limited by the softening point of the soda lime glass. In order to achieve such rates, the Cu-source temperature would have to be greater than 1300°C, and the In- and Ga-source temperatures in excess of 1100°C. The equipment needed to produce 4×2 ft^2 modules under these conditions and at a rate of one module every 2.5 min

would be quite complex and, thus, costly. Furthermore, the need to operate at such high temperatures and under conditions of precise control of elemental fluxes would also add to the operating cost of the equipment. Given these constraints, the only way to reduce the manufacturing cost would be to increase the throughput, which can be brought about only by increasing deposition rate or by reducing the thickness of the absorber or both.

None of these approaches has been explored because the emphasis has always been on efficiency rather than manufacturability. Because the optical absorption coefficient of $CuInSe_2$ is greater than 5×10^4 cm^{-1} at photon energies higher than 1.4 eV, a thickness of approximately 1 μm would be large enough for total absorption of the solar spectrum. In addition, there is no known factor that would limit the deposition rate to 0.05 μm/min. If film thickness could be reduced to ranges commensurate with the magnitude of the optical absorption coefficient, and the deposition rate could be increased by a factor of two, the manufacturing cost related to capital equipment would be reduced immediately by a factor of four. Such a cost reduction could even justify some loss in efficiency. Similar arguments can also be made for the selenization of metal precursors. Research efforts should be directed toward understanding the effect of deposition rate and absorber thickness on conversion efficiency.

In the fabrication of CdTe-based PV modules, CSS is the most compatible process for large-scale manufacturing. Not only does this process have the highest deposition rates, but to date, it also yields the highest-efficiency laboratory cells. Even though it is a high-temperature/low-pressure process, the equipment cost is not as critical as it is in $CuIn_{1-x}Ga_xSe_2$ manufacturing since the deposition rate, and consequently the throughput, is considerably higher (1 μm/min). Furthermore, the CSS process can also be used for the deposition of the CdS window layer as well, thus simplifying the manufacturing operations. The major problem with the CSS process is the high cost of raw materials (e.g. high-purity CdTe). However, since CdTe has an absorption coefficient similar to that of $CuInSe_2$, methods for reducing its thickness in modules, even at the expense of some reduction in efficiency, should be investigated.

Reduction of the absorber thickness, in both material systems, would have a beneficial effect, from the manufacturing cost perspective, on the monolithic integration process as well as by reducing the thickness of the material to be removed during laser scribing.

Environmental Issues

$CuInSe_2$- and CdTe-based modules might be thought to represent environmental hazards when disposed of at the end of their useful life, since Cd metal is classified as a toxin/carcinogen. However, the stable nature of Cd compounds such as CdS and CdTe makes the disposal issue technically less relevant. However, if

the concept of "cradle-to-grave" management of hazardous materials is applied to Cd-containing PV modules, the cost of manufacturing such modules would be prohibitive. In this case, alternatives exist and are being investigated for the $CuInSe_2$-based modules, although no such alternatives exist for the CdTe-based modules.

In contrast, environmental issues in module production facilities are real and complex. Deposition of CdS by the solution growth process (CBD) would cause serious environmental problems in the workplace. This technique, as practiced in the laboratory, requires large quantities of basic aqueous solutions of complex ions containing Cd and S. The substrate is immersed in the solution, resulting in the heterogeneous deposition of CdS on the substrate as well as on the walls of the vessel, and homogeneous CdS particulate formation in the solution itself. The process releases all the Cd and S ions from the solution, requiring a fresh solution for each substrate. As a result, process efficiency in the laboratory is at best 1%. In a manufacturing environment the process could be modified to result in significant improvements in materials utilization. Nevertheless, for an annual production of 10 MW_p and a CdS thickness of 0.05 μm, the manufacturing process must include safe disposition of large quantities of strongly basic solutions containing CdS powder. The solution to be disposed of must not have any Cd^{+2} ions left in it; consequently, an alternative to CBD of CdS needs to be developed for large-scale production.

Even processes such as sputtering of CdS or CSS of CdTe and CdS would present environmental problems in the workplace. In these processes not all the material removed from the source will be deposited on the substrate. Some amount will be deposited on the walls and fixtures of the reactor in the form of a fine powder that needs to be removed and disposed of periodically. The solution in this case, in addition to reducing CdTe thickness to the minimum required for proper device operation, lies in the proper design of the manufacturing equipment to maximize the utilization of the source material and to facilitate removal of deposits.

CONCLUSION

The best $CuInSe_2$- and CdTe-based, small-area, thin film polycrystalline solar cells have reached laboratory efficiencies of 16–17%, which are approximately 80% of their theoretical maximum efficiencies. Furthermore, efficiencies above 13–14% have been obtained by more than one process for each class of solar cells. However, despite these achievements, commercial products based on these materials are not yet available because the fundamental research conducted so far has focused on improvements in efficiency. Now, however, the focus must shift to issues relevant to manufacturability.

These issues remain fundamental in nature. A potential problem with shifting the emphasis of research in this field may be related to the fact that this type of research has more immediate commercial value, resulting in reduced levels of cooperation between the private sector and the government and academia. This situation would be unfortunate because such cooperation has been the primary force behind the rather spectacular improvement in efficiencies in these devices. Furthermore, the nature of the unresolved problems are too fundamental to be addressed properly by the private sector alone, although the private sector is uniquely qualified to define the problems. It is hoped that such tri-partite cooperation would continue into the areas closer to commercialization, which would enable the widespread application of photovoltaic energy conversion.

ACKNOWLEDGMENTS

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