

Investigation of CdTe solar cells via capacitance and impedance measurements

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Abstract

Two CdTe solar cells with very different IV-characteristics were analysed using impedance spectroscopy (IS) and capacitance–voltage (CV) measurements at different temperatures and under dark and illuminated conditions. The two samples were distinguished by different durations of the nitric–phosphoric (NP) etching process applied before back contact deposition. The cell with a short etching time (30 s) shows a strong roll over in the forward bias region, and the cell with the surface that was etched for a longer time (3 min) showed a very strong decrease of the roll-over and a better fill factor. The results show that the etching process dramatically changes the CV characteristics, the resulting CdTe effective doping concentration and that this change can be correlated to different equivalent circuits obtained by the fitting of the impedance spectra of the two samples. © 2001 Elsevier Science B.V. All rights reserved.

Keywords: CdTe; Impedance spectroscopy; CV-measurements; Equivalent circuit; Roll over; Etching

1. Introduction

One of the issues in the production of thin-film CdTe/CdS solar cells is to form an ohmic back contact to the p-type CdTe. To achieve this, different surface treatments can be applied prior to the deposition of the metallic contact. One possibility consists of a nitric–phosphoric (NP) etch, which etches not only the surface but also the grain boundaries. It is known [1] that in this way, a layer of Te on the CdTe surface is produced and that this Te layer penetrates the grain boundaries down to the CdTe/CdS interface. We observed that a variation in the etching time caused a change in the electronic behaviour of the CdTe cells. The change was visible in the IV characteristics, where a very strong decrease of the roll-over could be observed. From previous studies [2], we know that in thin film devices, roll-over can be caused by the back

contact, by the TCO/window interface or by deep states within the window. For CdTe, it is still not clear if the decrease in the roll over is only given by a good ohmic contact or also by a compensation of impurities in the interface regions or the grain boundaries. A combination of CV, IV, and IS measurements gives additional insight into this effect. The thin film CdTe solar cells analysed in this work were fabricated by Antec GmbH, using CSS to deposit CdS and CdTe. Two different sets of cells (cell area of 0.25 cm²) were analysed. Within this paper, the two cells are referred to as cell 1 and cell 2; cell 1 having a much shorter etching process (30 s) than cell 2 (3 min).

2. Results and discussion

2.1. Current–voltage (IV) measurements

Fig. 1 shows the dark and illuminated IV curves of the two cells. After 30 s of NP etching, cell 1 shows still a very strong roll-over; only after 3 min of etching a

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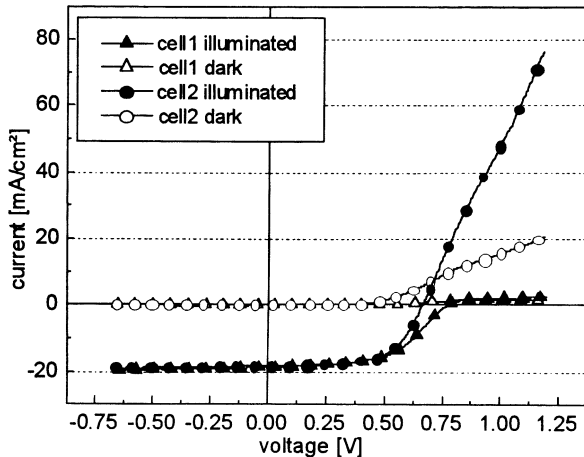


Fig. 1. Dark and illuminated IV-curves.

disappearing of the roll-over could be observed (see cell 2). The etching process influences not only the roll-over, but also the open circuit voltage, the fill factor of the devices and the light to dark IV curve cross-over. The open circuit voltage is strongly dependent on the processing conditions. After the etching process, the V_{oc} value seems to decrease ($V_{oc, cell 1} = 0.771$ V, $V_{oc, cell 2} = 0.667$ V), but the FF value ($FF_{cell 1} = 55.1\%$, $FF_{cell 2} = 63.8\%$) improves. The lower open circuit voltage could be caused by a reduction of the junction potential barrier due to the NP etching process. The cross-over of the light to dark IV curves is very pronounced for cell 2. Instead cell 1 only shows a low cross-over, which is probably due to the current limiting effect of the back contact in the forward bias region of the IV curve. The short circuit current seems to be independent of the etching process.

2.2. Capacitance–voltage (CV) measurements

The dark and illuminated capacitance voltage measurements were taken from -1.5 to 1.5 V, at a frequency of 60 kHz and in a temperature range of 20 – 70°C . Fig. 2 shows the CV and Fig. 3 the resulting $1/C^2$ vs. V curves of the two cells at 25°C . It is apparent that the etching process strongly influences the voltage dependence of the cell capacitance. Cell 2 shows behaviour typical of a p–i–n cell, wherein the capacitance is composed of the junction and the intrinsic layer capacitance, which is nearly independent of the applied voltage at reverse bias. Cell 1 shows a stronger capacitance voltage dependence instead. It is still not clear how the difference in the CV curves of a cell with roll-over (cell 1) and a cell without roll over (cell 2) can be explained, but we observed that the disappearing of the roll-over and the improvement of the FF is always connected to such a difference in the reverse bias region of the capacitance voltage curve.

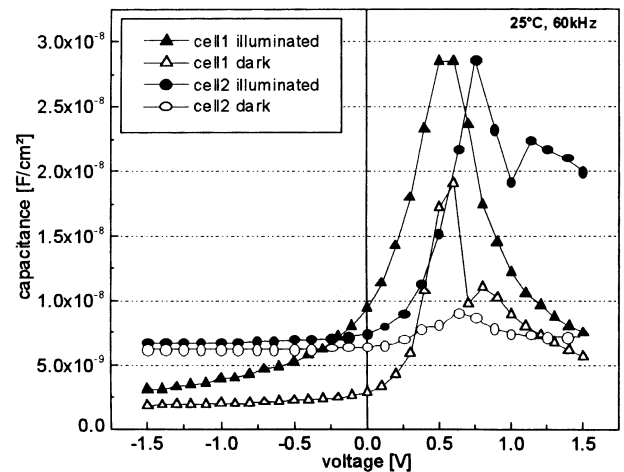
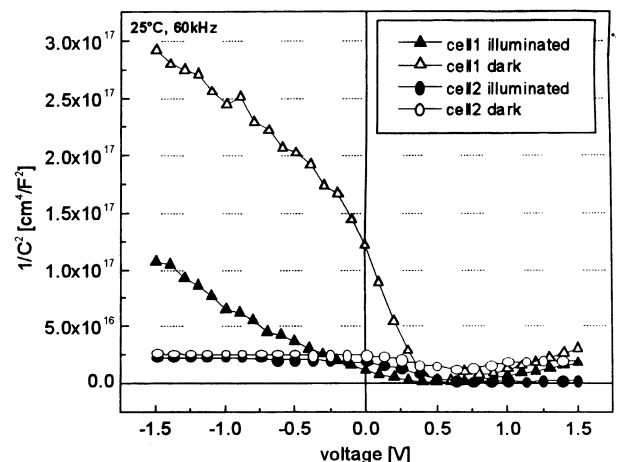


Fig. 2. Dark and illuminated C vs. V curves.

Another observation was that, at reverse bias, cell 1 exhibits a smaller effective capacitance than cell 2. This could be due to the influence of impurities present in the grain boundaries or in the interface regions of cell 1 which leads to an additional capacitance in series and, consequently, to a decrease in the total capacitance. The etching process reduces the impurities in cell 2 so that the additional capacitance can be neglected and the total cell capacitance is increased. The measurements from the dark $1/C^2$ vs. V curves resulted in effective doping concentration that was 60 times higher for cell 2 than cell 1 ($N_{d, cell 1} = 1.5 \times 10^{14} \text{ cm}^{-3}$; $N_{d, cell 2} = 8.5 \times 10^{15} \text{ cm}^{-3}$). To obtain the real doping concentration, it would be necessary to separate the impurity concentration from the real doping concentration. This could be done by determining the single capacitance values and the relative CV curves by an additional characterisation method, such as impedance spectroscopy. It is apparent that, generally, the capacitance increases with illumination. This is a consequence of a reduced depletion width under light.

Fig. 3. Dark and illuminated $1/C^2$ vs. V curves.

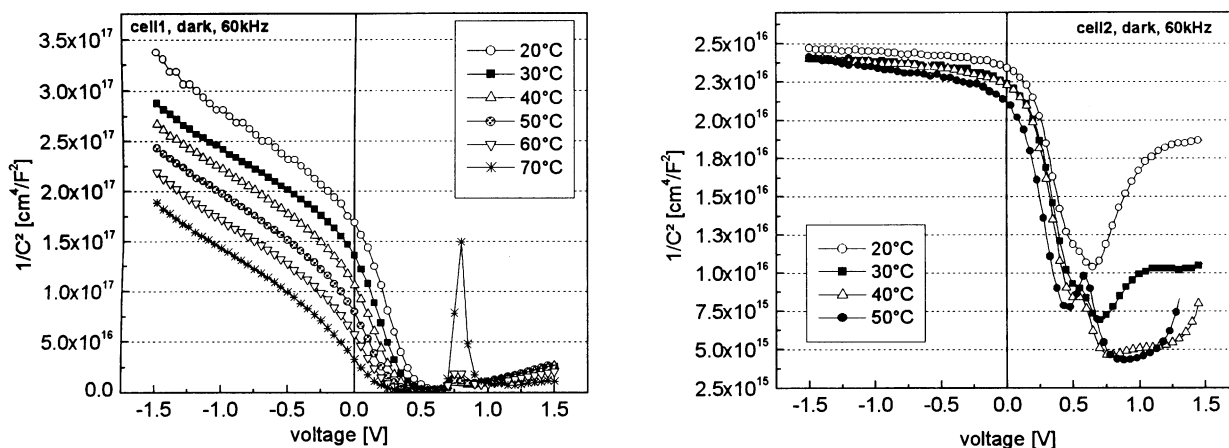


Fig. 4. Dark $1/C^2$ vs. V curves of cell 1 and cell 2 in a temperature range of 20–70°C.

Also in the forward bias region, the CV curves of the two cells differ consistently. It was supposed that the creation of a good back contact is due to the increase of Te on the etched surface. This is in accordance with the observed increase of the doping concentration near the back contact from $N_{d(\text{cell } 1)} = 4 \times 10^{14} \text{ cm}^{-3}$ to $N_{d(\text{cell } 2)} = 3 \times 10^{15} \text{ cm}^{-3}$. This doping concentration was obtained by the slope of the dark $1/C^2$ vs. V curve in the high forward bias region. The difference between the illuminated and the dark CV-curves and the correlation to the cross-over effect of the IV curves is still under investigation. Fig. 4 shows some results about the temperature dependency. It can be seen that cell 1 (high impurity concentration) shows a higher temperature dependence at reverse bias than cell 2.

2.3. Impedance spectroscopy (IS) measurements

Impedance spectra were measured in a frequency range of 1 MHz–100 Hz with an ac-signal amplitude of 10 mV and a bias voltage between -1.5 V and 1.5 V . All measurements were made under dark conditions

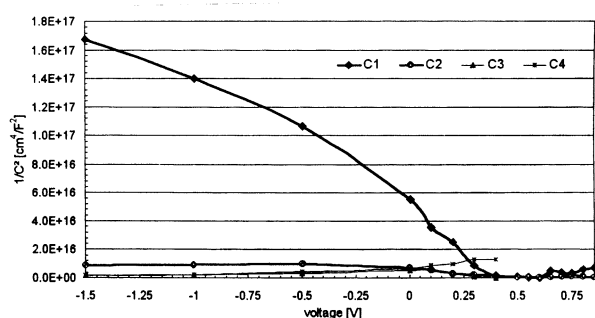


Fig. 5. Dark $1/C^2$ vs. V curves obtained by fitting the IS data of cell 1 at 25°C.

and in a temperature range of 20–60°C. The fitting and simulation of the acquired data was performed using Zplot software. The purpose of impedance spectroscopy is to find the appropriate equivalent circuit of the solar cells, so that the single components of the effective capacitance can be calculated and studied separately. The first observations were that a long enough etching process leads to impedance spectra which can be modelled in reverse and forward bias by a very simple RC equivalent circuit consisting of a parallel resistor R_p and capacitor C in series with a resistor R_s . In order to fit the impedance spectra of cell 1, a much more complicated model had to be used. Especially in the reverse bias region, the best fit was obtained by putting four of the simple RC equivalent circuits in series (see Fig. 5). Investigating the four capacitances ($C1$ to $C4$) and the relative CV curves, it was observed that two of the capacitances were dominant and that these were in good agreement with the one measured by the CV technique (see Fig. 3).

$C1$ shows the same trend as the effective capacitance measured by CV. The second ($C2$) exhibits behaviour typical for a p-i-n cell, as observed for cell 2. From these results, we concluded that the etching process leads to the disappearance of the capacitance $C1$. We assumed that $C1$ is correlated to the impurities present in the grain boundaries and the CdTe/CdS interface, and that these disappear because of the diffusion of the etching material into the grain boundaries and that after 3 min of NP etching also the CdTe/CdS interface region is reached. We calculated an impurity concentration of $4 \times 10^{14} \text{ cm}^{-3}$. As expected, in forward bias only cell 1 showed the presence of a second RC element deriving from the presence of a non-ohmic back contact. In cell 2, where the back contact was improved by the surface treatment, only a very small influence from a second RC element could be observed.

3. Conclusions

The etching of the surface prior to deposition of the metallic back contact leads to the creation of a Te-rich interface and, consequently, to a good back contact. Longer etching times increase the Te concentration and induce a diffusion of the etching material through the grain boundaries down to the CdTe/CdS interface. It has been shown that the effect of the etching process can be analysed by a combination of capacitance–voltage (CV) and impedance spectroscopy (IS) measurements.

Acknowledgements

The work presented here was partially supported by the European Commission, under the DGXII Non-Nuclear Energy Programme, contract nr. JOR3-CT98-0218

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