Special Issue

Thin-Film Solar Cells: Device Measurements and Analysis

Steven S. Hegedus*[,†] and William N. Shafarman

Institute of Energy Conversion, University of Delaware, Newark, DE 19716-3820, USA

Characterization of amorphous Si, CdTe, and Cu(InGa)Se$_2$-based thin-film solar cells is described with focus on the deviations in device behavior from standard device models. Quantum efficiency (QE), current–voltage (J–V), and admittance measurements are reviewed with regard to aspects of interpretation unique to the thin-film solar cells. In each case, methods are presented for characterizing parasitic effects common in these solar cells in order to identify loss mechanisms and reveal fundamental device properties. Differences between these thin-film solar cells and idealized devices are largely due to a high density of defect states in the absorbing layers and to parasitic losses due to the device structure and contacts. There is also commonly a voltage-dependent photocurrent collection which affects J–V and QE measurements. The voltage and light bias dependence of these measurements can be used to diagnose specific losses. Examples of how these losses impact the QE, J–V, and admittance characterization are shown for each type of solar cell. Copyright © 2004 John Wiley & Sons, Ltd.

INTRODUCTION

Thin-film solar cells (TFSCs) have achieved efficiencies approaching 15–20%. Much of the progress has occurred by empirical processing improvements and in spite of a relatively poor understanding of the underlying mechanisms and electronic defects which control the device behavior. However, as each technology matures, a more complete picture of the device operation has emerged to enable both a better understanding of the devices and identification of pathways to further improvements. In this article, differences between ideal crystalline solar cells and typical TFSCs will be identified. It will be shown that the photovoltaic performance of present day a-Si, CdTe, and Cu(InGa)Se$_2$-based devices have much in common, despite very different processing, device structures, and absorber properties. Experimental and analytical procedures will be described to characterize the quantum efficiency (QE), current–voltage (J–V), and admittance behavior. In each case, the approach will be based on eliminating parasitic effects common to the TFSCs in order to reveal the fundamental properties of the intrinsic junction and absorber. The objective of this article is to demonstrate methodology for analyzing TFSCs with examples from different devices rather than just to review previous work, so in many cases excellent work in the literature could not be cited.

*Correspondence to: Steven S. Hegedus, Institute of Energy Conversion, University of Delaware, Newark, DE 19716-3820, USA

[†]E-mail: ssh@udel.edu

Solar cell operation, either crystalline or thin film, can be described by identifying loss mechanisms. These can be divided into three categories. First are recombination losses which limit the open-circuit voltage V_{OC}. Second are parasitic losses, such as series resistance, shunt conductance, and voltage-dependent current collection, which primarily impact the fill factor (FF), but can also reduce short circuit current J_{SC} and V_{OC}. Finally, there are optical losses which limit generation of carriers and, therefore, J_{SC}. We focus on losses largely unique to TFSCs.

Physical and electrical properties of TFSCs which cause them to have different losses from the standard 'textbook' crystalline Si (c-Si) cells include:

- TFSC absorber layers have much higher absorption coefficients than c-Si so a large fraction of the photogeneration occurs near the interface and in the high field space charge region (SCR). This enables high currents, even with relatively small collection lengths;
- the semiconductor films often have a range of shallow and deep defect levels or defect bands within the bandgap. These result from imperfect crystallinity or amorphous structure and from the use of low-cost materials and processes optimized for high throughput and low cost as much as for high device efficiency. This can create different recombination mechanisms than radiative band-to-band recombination commonly found in ideal crystalline semiconductor devices;
- poor minority carrier lifetime, due to the above factors, leads to increased reliance on the electric field for sufficient minority carrier collection rather than diffusion alone. This often results in voltage-dependent collection of light-generated current;
- TFSCs are heterojunction device structures with high densities of defect states at interfaces which can provide a path for interface recombination;
- the grain boundaries in polycrystalline Cu(InGa)Se$_2$ and CdTe devices may act as high recombination surfaces or shunt paths. This leads to lateral field nonuniformity and recombination varying in two dimensions;
- non-ohmic or blocking contacts can limit current at forward bias.

Devices to be studied here include a-Si p–i–n or n–i–p type cells, and polycrystalline CdTe/CdS and Cu(InGa)Se$_2$/CdS p–n heterojunction cells. QE measurements will be used to determine optical losses, optical enhancements, and voltage-dependent photocurrent mechanisms. J–V measurements under standard test conditions will be shown and a systematic procedure to separate diode and parasitic effects will be presented. Standard C–V measurements often fail to provide much information on TFSC if they do not to yield a linear C^{-2}–V relation, so we will describe other types of ac (admittance) measurements and analyses which do provide quantitative interpretation.

SAMPLES

The TFSC devices characterized here were made by a variety of methods and have a variety of device structures. Generically, there are two types of TFSC superstrate or substrate devices, as shown in Figure 1. Superstrate devices are made on a transparent substrate such as glass, so the light enters the absorber through the first deposited layers. Substrate devices are typically made on opaque substrates such as metal foils or metallized
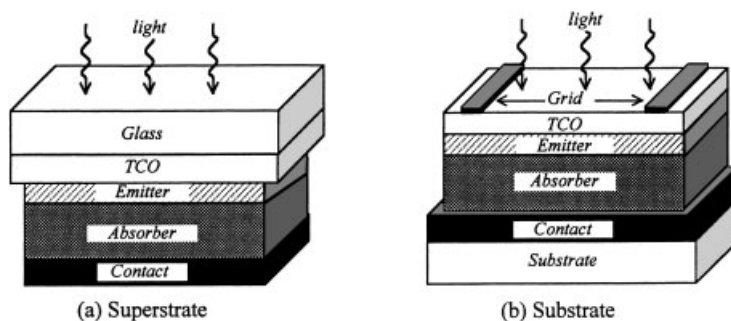

Figure 1. Typical superstrate (a) and substrate (b) TFSC configurations

glass and light enters the absorber through the last deposited layer. In this work, three types of TFSCs will be characterized. Most of them were fabricated at the Institute of Energy Conversion (IEC). Cu(InGa)Se$_2$-based solar cells have a substrate device structure of glass/Mo/Cu(InGa)Se$_2$/CdS/ZnO/ grid. The Cu(InGa)Se$_2$ layers deposited by elemental thermal evaporation were 2–3 μm thick, and their bandgap could be varied from 1·0 to 1·7 eV by varying Ga/(In + Ga). The CdTe based solar cells have a superstrate device structure of glass/SnO$_2$/ CdS/CdTe/metal. The CdTe layers were deposited by several techniques by different groups and were 2–4 μm thick. The a-Si-based solar cells have a superstrate device structure of glass/SnO$_2$/p-i-n/BR where the back reflector (BR) is either metal or ZnO/metal. The a-Si layers were deposited by rf plasma chemical vapor deposition and were about 0·4 μm thick. The critical component of the TFSC is the absorber layer, where the photogeneration and most of the recombination occurs. Devices will be referred to by their absorber layer: Cu(InGa)Se$_2$, CdTe, a-Si, or a-SiGe.

QUANTUM EFFICIENCY

Quantum efficiency (QE) measurements are valuable to characterize the photocurrent and are commonly used to determine the losses responsible for reducing the measured J_{SC} from the maximum achievable photocurrent. Typical measurement equipment and techniques are described elsewhere.[1] QE is a dimensionless parameter given by the number of electrons which exit the device per incident photon at each wavelength. The photocurrent is the integral over wavelength of the product of the measured external QE with the illumination spectrum, typically AM1·5 global for terrestrial solar cells. Thus, a good verification of the QE measurement is that the current calculated by integrating the QE, measured with 0 V bias, with the AM1·5 spectrum agrees with J_{SC}. Good agreement will typically be found in well-behaved devices such as crystalline Si solar cells, although significant differences between the integrated QE and the photocurrent can occur in TFSCs when the collection depends on the intensity and spectrum of the incident illumination.[2]

Device losses measured by QE can be optical, due to the front reflection and absorption in the window, transparent conductor, and other layers, or electronic, due to recombination losses in the absorber. Comparing the QE measured with different voltage bias is a powerful tool to separate electronic losses and optical losses since only the former should be affected by the applied bias. Figure 2 shows the QE for several high-efficiency TFSCs.[3–5]
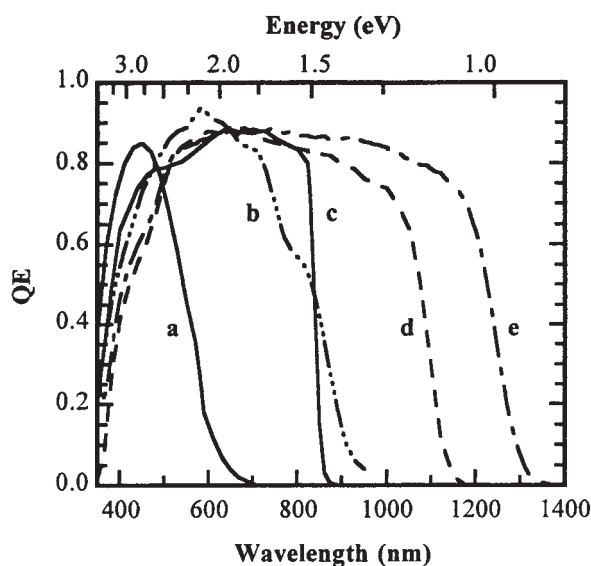

Figure 2. QE of high efficiency TFSCs: (a) a-Si thin top cell of a triple junction with no back reflector;[2] (b) a-SiGe, bottom cell with graded bandgap and back reflector;[2] (c) CdTe;[3] (d) Cu(InGa)Se$_2$ with Ga/(In + Ga) = 0·3 and E_g = 1·2 eV;[4] (e) CuInSe$_2$[4]

The differences in shape and cut-off at long wavelengths are primarily related to the absorber bandgap. The shape and magnitude at short wavelengths is related to device structure and window layers.

The TFSC is a multilayer optical stack, as illustrated in Figure 1. The light goes through several layers, including the TCO and emitter, before entering the absorber where the carrier generation occurs. The effect of these layers on reducing the amount of light available in the absorber can be numerically quantified and the measured QE can be corrected for their influence. What remains, after accounting for all the other known losses, is the internal QE (QE_{INT}), due only to the photogeneration and collection in the absorber. Sometimes QE_{INT} is defined as just $QE/(1-R)$ where R is the light reflected from the solar cell. In that case, QE_{INT} also includes window layer absorption losses. In this paper, we use the first definition.

Referring to Figure 1, impinging light first encounters front surface reflection from the air/glass/TCO/emitter or air/TCO/emitter interfaces, respectively. The transparent conducting oxide (TCO) may be SnO_2, ZnO, ITO, or other materials, but they all have similar refractive indices, hence reflective properties. There may also be an anti-reflection layer on the front to reduce the air/glass or air/TCO reflection. For analysis, these components of front-surface reflection are grouped together as R_F. In addition, substrate devices often have a metal grid on the thin TCO layer to provide low-resistance current collection. The grid shades a small fraction of the device thus reducing the active area and is accounted for by a wavelength-independent grid shadowing factor T_G which is typically >0.95 for small-area devices, with $T_G = 1$ for gridless superstrate devices. Light can be absorbed in the TCO and emitter layers as well. In CdTe and Cu(InGa)Se$_2$ devices, the emitter layer is typically CdS. In a-Si devices, the emitter is either an a-SiC or μc-Si p-layer. A common goal of all TFSC designs is to minimize emitter layer absorption by increasing its bandgap, decreasing its thickness or both. Most of the remaining light is absorbed in the absorber layer, generating the carriers which contribute to the photocurrent. Light that is not absorbed in the absorber layer impinges on the back contact where it is either absorbed and converted to heat or, as in the case of a-Si devices, partially reflected back into the absorber.

The fraction of incident light reaching the absorber layer is given by the product of the transmission through each of the front layers, or

$$T_F(\lambda) = T_G[1 - R_F(\lambda)][1 - A_{TCO}(\lambda)][1 - A_E(\lambda)] \tag{1}$$

where A_{TCO} and A_E are the absorption of the TCO (or TCO/glass) and emitter layer, respectively. Then the measured, or external, QE for a TFSC is

$$QE(\lambda, V, I) = T_F(\lambda)QE_{INT}(\lambda, V, I)\Gamma(\lambda, V, I) \tag{2}$$

where $\Gamma(\lambda, V, I)$ is a voltage-and-light-bias-dependent gain factor.

QE_{INT}, the internal collection, is dependent on the absorber layer's absorption coefficient α, thickness d, and an effective minority carrier collection length. It also depends on the external variables of the applied voltage V, and bias light intensity I. QE_{INT} decreases with increasing forward bias or increasing bias light intensity in most TFSCs, due to a reduction in field and space charge width[6,7] or due to series resistance effects.[8,9] At sufficient reverse bias QE_{INT} reaches an optically limited maximum where there are no electronic losses, i.e., complete collection occurs, provided there is no light absorbed at the back contact. Optical enhancement, which commonly occurs in a-Si due to light trapping, is included in QE_{INT}.

$\Gamma(\lambda, V, I)$ describes photoconductive effects in which the ac chopped light used for the QE measurement is coupled with the stronger dc bias light. In most cases, $\Gamma(\lambda, V, I) = 1$ unless the device is at far forward bias and/or has a spectrally filtered bias light spectrum. When $\Gamma(\lambda, V, I) \neq 1$ the measured QE should be referred to as the apparent QE (or AQE). In some cases this can be readily determined when the measured QE exceeds unity which violates energy conservation.

QE curves for a Cu(InGa)Se$_2$ TFSC at two different voltage biases, 0 and -1 V, along with the most common losses, are shown in Figure 3.[10] The losses are converted to equivalent photocurrent by integrating the reflection, absorption or QE with the AM1.5 illumination spectrum and are listed in Table I. Losses 1–5 are optical and 6 is electronic. In practice, the magnitude of each of these losses will depend on details of the device design and optical properties of the specific layers. Optical absorption losses in the emitter and TCO layers are determined
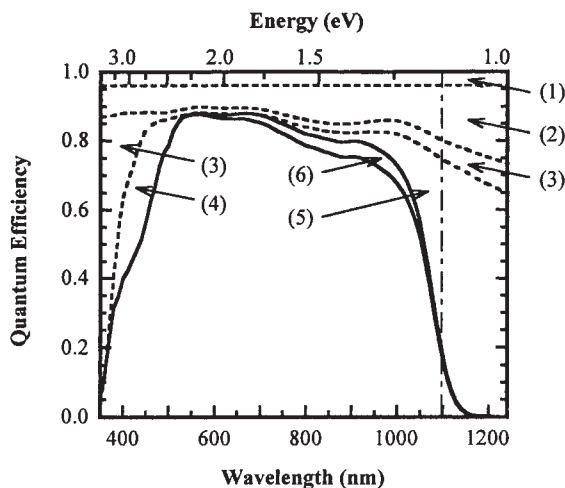
Figure 3. Quantum efficiency at 0 V (lower solid curve) and -1 V (upper solid curve) with optical losses for a Cu(InGa)Se$_2$ solar cell in which the Cu(InGa)Se$_2$ has $E_g = 1\cdot12$ eV; losses are identified in Table I

from separate optical measurements on control samples of these layers which were deposited on glass substrates. Referring to their numbers in Figure 3, the losses include:

1. Shading from the collection grid used for some substrate devices. This is the only wavelength-independent optical loss;
2. Front-surface reflection from the air/ZnO/CdS/CuInGaSe$_2$ interfaces. For high-efficiency 'champion' devices, this is often minimized with an anti-reflection layer. Typical reflection from a superstrate TFSC device is slightly lower (8–10%) than from substrate devices, owing to the lower index of glass compared with TCOs;
3. Absorption in the TCO layer. Typically there is 1–5% absorption through the visible wavelengths which increases in the near IR region ($\lambda > 900$ nm), due to free carrier absorption and at short wavelengths ($\lambda < 400$ nm) approaching the TCO bandgap. Superstrate devices on glass/SnO$_2$ have higher TCO absorption losses than substrate devices because the commonly used SnO$_2$ has higher absorption losses than ZnO or ITO for a given sheet resistance. These cells also have absorption losses in the low-cost glass;
4. Absorption in the emitter layer. For CdS as in Figure 3, this becomes appreciable at wavelengths below $\sim$520 nm corresponding to the CdS bandgap 2$\cdot$42 eV. The loss in QE for $\lambda < 500$nm for most emitters is proportional to the layer thickness since electron–hole pairs generated in the emitter are not collected. Figure 3 shows a device with a $\sim$40-nm-thick CdS layer. In practice, the CdS layer is often thicker and the absorption loss greater;
5. Incomplete absorption in the absorber layer near the Cu(InGa)Se$_2$ bandgap. Bandgap gradients, resulting from composition gradients in many Cu(InGa)Se$_2$ and a-SiGe absorbers, also affect the steepness of the long-wavelength part of the QE curve. If the absorber is made thinner than $1/\alpha_g$, where α_g is the absorption coefficient just above the bandgap, this loss becomes significant unless light trapping is employed;

Table I. Photocurrent loss due to the optical and collection losses for the Cu(InGa)Se$_2$ TFSC in Figure 3. $J_{tot} = 42\cdot8$ mA/cm^2 is the total photocurrent available for the AM1$\cdot$5 spectrum for E $> 1\cdot12$ eV

Region in Figure 3	Optical loss mechanism	ΔJ (mA/cm^2)	$\Delta J/J_{tot}$ (%)
1	Shading from grid with 4% area coverage	1$\cdot$7	4$\cdot$0
2	Reflection from Cu(InGa)Se$_2$/CdS/ZnO	3$\cdot$8	8$\cdot$9
3	Absorption in ZnO	1$\cdot$9	4$\cdot$5
4	Absorption in CdS	1$\cdot$1	2$\cdot$5
5	Incomplete generation in Cu(InGa)Se$_2$	1$\cdot$9	4$\cdot$4
6	Incomplete collection in Cu(InGa)Se$_2$	1$\cdot$0	2$\cdot$3

6. Incomplete collection of photogenerated carriers in the absorber. This is the only electrical loss factor and will be discussed below. At sufficient reverse bias, in this case −1V, all carriers are collected without any electrical losses. Generally the QE in a TFSC will increase with reverse bias.

QE Voltage Bias Dependence

Photocarrier collection proceeds differently in polycrystalline solar cells such as Cu(InGa)Se$_2$ and CdTe than in a-Si based TFSC because transport in the former is limited only by minority carrier electrons in the p-type absorber layers, while in the latter carriers are generated in the intrinsic layer and transport is ambipolar. This particularly affects the analysis of the voltage bias dependence of QE$_{INT}$ because of the difference in field profile and minority-carrier transport between the two types of devices. QE$_{INT}$ in Cu(InGa)Se$_2$ and CdTe devices will be discussed first.

For unipolar absorbers such as CuInGaSe$_2$ and CdTe, QE$_{INT}$ can be approximated[7,11] by:

$$QE_{INT}(\lambda, V) \cong 1 - \frac{\exp[-\alpha(\lambda)W(V)]}{\alpha(\lambda)L + 1} \qquad (3)$$

where $\alpha(\lambda)$ is the absorption coefficient, $W(V)$ is the space-charge width, and L is the minority carrier diffusion length (all pertaining to the absorber). This approximation assumes that all carriers generated in the space-charge region are collected without recombination loss and those generated in the neutral bulk diffuse to the depletion edge. It also assumes the absorber is relatively thick; $d > 1/\alpha_g$. A simple view is that carriers generated within one collection length $W(V) + L$ of the junction for polycrystalline materials are collected without recombination losses. In the limit of very short L, $\alpha L \ll 1$, Equation (3) reduces to $QE \cong 1 - \exp[-\alpha W(V)]$ which is the expression for collection in the space-charge region. Since $W(V)$ is a function of the applied voltage bias, QE$_{INT}$ and total light-generated current are, in general, voltage dependent, and the latter is referred to as $J_L(V)$. Incomplete collection of minority carriers generated beyond $L + W(V)$ into the TFSC absorber layer can be a significant loss mechanism. The effect of $J_L(V)$ on J–V behavior increases with forward voltage and will be discussed below.

Voltage-dependent collection is illustrated in Figure 3 by the increase in QE measured at −1V compared with that measured at 0 V. For Cu(InGa)Se$_2$, $W(0\,V) \approx 0{\cdot}1$-$0{\cdot}5\,\mu m$ and $L \simeq 0.1$–$1\,\mu m$ while for CdTe $W(0V) \simeq 2$–$3\,\mu m$ and $L \simeq 0.1$–$1\,\mu m$. Thus, the collection length at 0 V in Cu(InGa)Se$_2$ is less than the typical thickness (2–3 μm), but in CdTe, it is comparable to or greater than the thickness of typical devices (2–4 μm), so CdTe may have more complete collection at long wavelengths, but also greater voltage dependence. The assumption in Equation (3) of complete collection from within W may not apply, such as in the case of low carrier density and large depletion width. Then Equation (3) would need to be scaled by $\exp[-t(V)/\tau]$ where $t(V)$ is the transit time of the electron drifting to the junction and τ is the lifetime. This may be the case with CdTe devices.

QE$_{INT}$ for a-Si p–i–n cells differs from the polycrystalline heterojunctions described above for three reasons. First, the photocarrier collection is primarily field driven. There is no field-free neutral region for diffusion-limited collection and no clearly defined depletion width $W(V)$ from which it can be assumed that all generated carriers are collected. Second, collection of both holes and electrons must be considered, and recombination losses can be significant for either. The concept of the limiting carrier is critical to understanding ambipolar photocurrent collection.[12] The limiting carrier is the one which generates the smaller photocurrent and will have the smaller mobility-lifetime ($\mu\tau$) product. The complexity of ambipolar transport requires considerable simplification to develop an analytical model.[12] Third, optical enhancement is typically employed to increase the pathlength of long-wavelength photons via light trapping.

Because the limiting carrier typically changes from electrons at short wavelengths to holes at long wavelengths (for the case of light incident through the p-layer), it is not possible to derive a single analytical expression for the voltage dependence for a-Si solar cells valid at all wavelengths. The recombination mechanism for electrons, which determines the voltage dependence at short wavelengths, i.e., strongly absorbed light, is due to either back-diffusion into the p-layer (a p–i interface effect) or recombination while drifting across the i-layer (a bulk i-layer effect). The recombination mechanism for holes, which determines the voltage

dependence at long wavelengths, i.e., weakly absorbed light, is always due to recombination while drifting across the *i*-layer to the *p*-layer (a bulk *i*-layer effect). With considerable simplification, the QE_{INT} for a-Si devices is given by

$$QE_{INT}(\lambda, V) = A_i(\lambda)\eta_c(V) \tag{4}$$

The *i*-layer absorption $A_i(\lambda)$ is given as

$$A_i(\lambda) = 1 - \exp[-\alpha(\lambda)m(\lambda)d] \tag{5}$$

where *m* is a wavelength-dependent enhancement factor due to scattering and light trapping which describes the increase in optical pathlength over that of a completely specular device with no back reflector. The voltage dependent collection factor $\eta_C(V)$ depends on whether short- or long-wavelength collection is being considered.[12]

A model for $J_L(V)$ under the assumption of a uniform field gave, for weakly absorbed light where the hole is the limiting carrier:[6,12]

$$\eta_c(V) = X\left[1 - \exp\left(X^{-1}\right)\right] \tag{6}$$

with

$$X = \frac{L_C}{d}\left(1 - \frac{V}{V_{FB}}\right) \tag{7}$$

Here L_C is the collection drift length at zero bias given by

$$L_C(0) = \mu\tau E(0) = \mu\tau\frac{V_{FB}}{d} \tag{8}$$

$\mu\tau$ is for the holes (limiting carrier), $E(0)$ is the average field at 0 V bias, and V_{FB} is the flat-band voltage. Experimentally, V_{FB} is the voltage where $J(V) = J_D(V)$, or $J_L(V) = 0$, and is typically ~ 0.1 V greater than V_{OC}. Additional terms accounting for nonuniform fields and diffusion contribution have been given, but are relatively minor.[12] Determining L_C at different wavelengths can help separate bulk and interface recombination.[13] However, a single value obtained at long wavelengths is sufficient to characterize the dominant collection in the *i*-layer under white light.[14]

The voltage dependence of $QE_{INT}(V,\lambda)$ has been used empirically to characterize collection problems in a variety of cases, including: Cu(InGa)Se$_2$ devices with increasing bandgap[5] or lower deposition temperature;[15] a-Si devices due to impurity contamination in the *i*-layers;[16] interface buffer layers;[13,17,18] light degradation;[19] and a-SiGe grading;[20] and in CdTe devices due to interface recombination;[21] photoconductive CdS;[22] and Cu doping as a function of CdTe thickness.[23]

A useful method to characterize $J_L(V)$ is to consider the wavelength dependence of the ratio of QE measurements at different voltage biases. For example, the ratio QE(-1 V)/QE(0 V) is shown in Figure 4 for 4 Cu(InGa)Se$_2$ devices with increasing absorber layer bandgap. The increased voltage dependence at longer wavelengths indicates poor minority-carrier collection from the bulk of the absorber which becomes a more significant loss in the devices as the bandgap increases. This is accompanied by indications of $J_L(V)$ in *J–V* measurements, as discussed below. Figure 5 shows the QE voltage bias dependence as QE(-1 V)/QE(0 V) and QE($+0.5$ V)/QE(0 V) for two a-Si *p–i–n* cells having similar V_{OC} (~ 0.87 V) and J_{SC} (~ 15 mA/cm^2) but very different values of FF. Cell A (FF = 57%) has a large decrease in QE at long wavelengths with forward bias, suggesting poor collection of holes, since they have farther to drift compared with electrons. Cell B (FF = 69%) shows a slight increase in bias dependence at shorter wavelengths, which is often associated with low electron lifetime, or low fields at the *p–i* interface allowing electron back-diffusion into the *p*-layer.[16,19] Note that the ratio QE(-1 V)/QE(0 V) has less wavelength dependence than the ratio at 0.5 V, indicating that reduction in electric field with forward bias is responsible for the photocurrent losses. Nevertheless, the cells show greater dependence of both QE ratios in the same wavelength region respectively. For example, the QE of
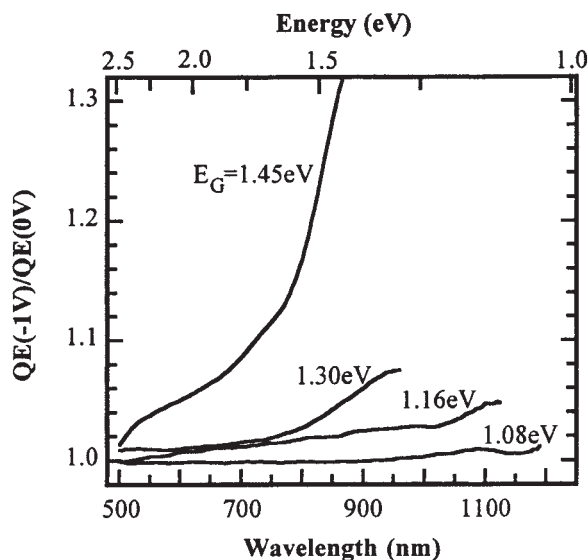
Figure 4. Reverse-bias QE ratio QE(-1 V)/QE(0 V) bias for four Cu(InGa)Se$_2$ devices with different bandgap absorber layers

cell B has greater change with bias at short wavelengths for either -1 V or $+0\cdot5$ V, indicating that the electron collection steadily decreases with decreasing electric field.

If the QE bias ratio is wavelength independent, it suggests a loss mechanism that affects all carriers equally, regardless of where in the device they were generated. Two such mechanisms occur at the heterojunction interface; interface recombination and a barrier due to heterojunction band-offsets. A third mechanism is related to the interaction between the equivalent series resistance and the operating bias point during the QE measurement.[8,9]

Specially fabricated solar cells having transparent back contacts allow for probing of the collection from either front or back. The measurements can be analyzed by simultaneously fitting the data to the equations for collection with illumination from the front and back side, after making corrections for optical losses to
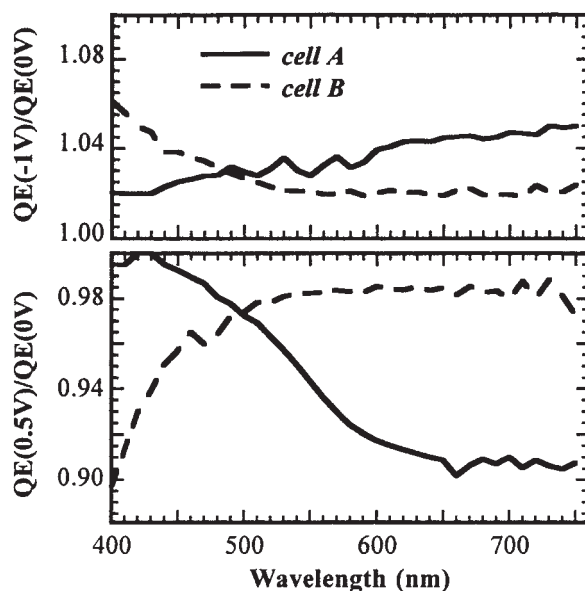

Figure 5. QE ratios for two a-Si devices at reverse (top) and forward (bottom) bias compared to 0V bias

determine QE_{INT} for each case. This has been used to separate the field-assisted and diffusion collection contributions for $CuInSe_2$[24] and to compare hole- with electron-limited collection in a-Si devices.[25]

Bias light dependence of QE

Standard *J–V* test conditions for solar cells use an illumination of $\sim$100 mW/cm^2. In contrast, the monochromatic probe beam in a typical QE measurement will be 3–4 orders of magnitude weaker. In an idealized solar cell, these differences are irrelevant, since the response is assumed to be linear with input. Bias light will have negligible effect on devices with low trap density, but some TFSCs have nonlinear output due to trapping and photoconductivity.[2] The effect of white bias light on the QE and collection in a-Si is due to an increase in the positive space charge from trapped charge,[26,27] which changes the electric field distribution and the regions with high or low drift-aided collection. Bias light can also affect polycrystalline heterojunction TFSCs, owing to photoconductive CdS changing the electric field distribution in the absorber which influences the voltage-dependent collection.[8,22] The bias light effects can be even greater for QE measurements under red or blue bias light.[27]

In general, to characterize the most relevant optical and collection effects in a device, the QE should be measured with white bias light and in the dark. Any significant difference requires further investigation of the bias and spectral dependence.

Optical enhancement

In the case of highly absorbing direct bandgap layers such as $Cu(InGa)Se_2$ and CdTe, most light is absorbed before it reaches the back contact, unless the absorber layer thickness is reduced sufficiently that $\alpha_g d \sim 1$ which requires $d < 1\ \mu m$. There is no need for light trapping and $m = 1$. However, a significant portion of the incident light is not absorbed in a single pass through the *i*-layer of a typical a-Si device. Therefore, textured substrates and reflective back contacts are used to scatter the light and increase the pathlength. Long-wavelength light that reaches the back contact is reflected back where it can make multiple passes to increase the probability for absorption leading to $m > 1$. Practical methods to use QE measurements to determine m have been presented.[28,29] First, all other optical losses must be quantified to determine T_F and the optical absorption coefficient of the a-Si *i*-layer must be determined. Then, the optically limited QE is measured at reverse bias. Thicker devices require greater reverse bias to achieve the same high electric field and to assure that all photogenerated carriers are collected. Finally, the QE calculated from Equations (2) and (5) is fit to the measured QE by adjusting m. Figure 6 shows the QE for three co-deposited *p–i–n* devices with $d = 0.39\ \mu m$, and $m(\lambda)$ derived from the
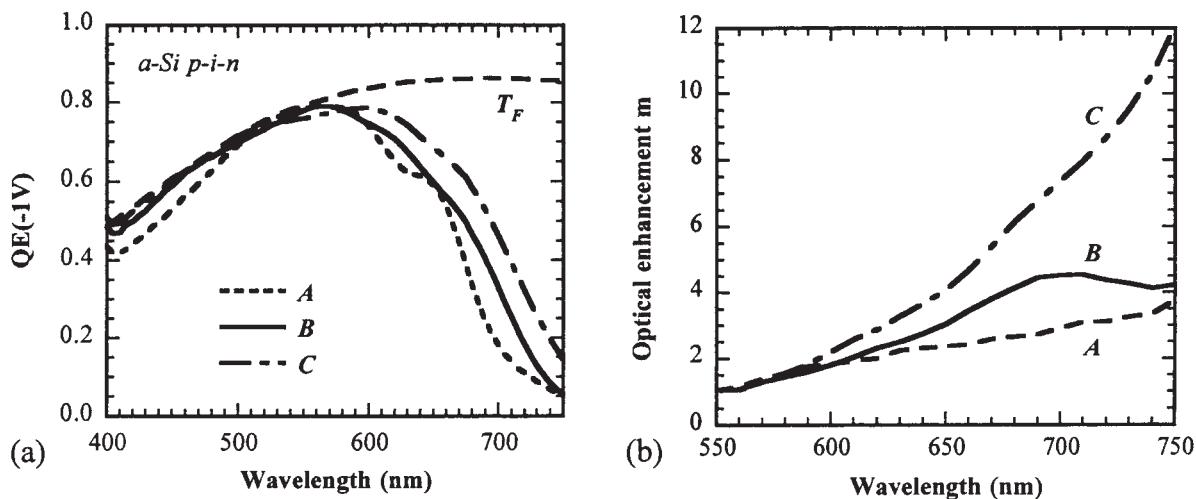

Figure 6. (a) QE at reverse bias and (b) optical enhancement, $m(\lambda)$, of three a-Si devices with different TCOs. Device A had low texture SnO_2 with an Al reflector, B had high texture with Al, and C had high texture with an ZnO/Ag reflector. Also shown in (a) is T_F from Equation (2) using measured values for device *C*

fitting. One device (A) had minimal optical enhancement, $m < 3$, due to only lightly textured SnO_2 and a low-reflectivity Al back contact. Another device (B) was deposited on more textured SnO_2, giving greater scattering and, hence, larger optical enhancement. A third device (C) had the more textured SnO_2 substrate and also a highly reflective back contact of ZnO/Ag. The J_{SC} increased accordingly from 12·5 to 14·1 to 14·7 mA/cm^2.[28] This device had m as high as 12, indicating efficient light trapping.

CURRENT–VOLTAGE ANALYSIS

Current-voltage ($J–V$) measurements under standard illumination conditions, 100 mW/cm^2 AM1·5 spectrum at 25°C, are the most common tool for solar cell evaluation and characterization. Measurement equipment and standardized techniques are described elsewhere.[1] Frequently, $J–V$ characterization means determination of the basic parameters V_{OC}, J_{SC}, FF, and efficiency (η) which are determined by only three points on the $J–V$ curve. While these parameters are well accepted indicators of solar cell performance and are particularly valuable for comparing and qualifying cells, there is a wealth of additional information that can be obtained by analyzing the entire $J–V$ curve. This is particularly so if the dependence on light intensity and temperature is considered.

With regard to characterizing $J–V$ behavior, the most important difference between TFSCs and high-efficiency solar cells based on single c-Si or III–V materials is the prevalence of parasitic losses, in the TFSCs. Thus, for analysis of the $J–V$ behavior to go beyond determining the basic parameters generally entails separation of the recombination losses from these other parasitic losses.

The $J–V$ behavior of a TFSC can be described by a general single exponential diode equation:

$$J = J_0 \exp\left[\frac{q}{AkT}(V - RJ)\right] + GV - J_L \tag{9}$$

for the case of constant J_L. The series resistance R and shunt conductance G are lumped circuit model representations of the losses that occur in series or parallel with the primary diode, respectively. The diode current J_0 is given by:

$$J_0 = J_{00} \exp\left(-\frac{\Phi_b}{AkT}\right) \tag{10}$$

with the ideality factor A, barrier height Φ_b, and prefactor J_{00} dependent on the specific recombination mechanism that dominates the forward current J_0. Combining Equations (9) and (10), for $G \ll J_L/V_{OC}$, the open-circuit voltage is:

$$V_{oc} = \frac{\Phi_b}{q} - \frac{AkT}{q}\ln\left(\frac{J_{00}}{J_L}\right) \tag{11}$$

A specific objective in the characterization of $J–V$ behavior of a solar cell is to determine the mechanism that limits V_{OC}. Any of several different recombination paths could dominate the device behavior at V_{OC}, including recombination currents in the space-charge or neutral regions of the absorber layer or at any of the critical interfaces, including the absorber/emitter interface or back contact in a Cu(InGa)Se$_2$ or CdTe device or the $p–i$ or $n–i$ interfaces in an a-Si device. Each of these mechanisms can be expressed by the general diode model of Equations (9) and (10) and specific formulations of these equations for each case can be compared.[11,30] Thus, experimental determination of these diode parameters is fundamental to determining the limiting behavior of these TFSCs. In practice, the recombination often may not fit the textbook cases due to, for example, recombination through defect bands rather than discrete states or by tunneling or multistep processes. Many authors have presented models for some of these cases to explain specific observations such as the temperature or voltage dependence of the diode parameters that cannot be explained by the standard textbook formulations. These details will not be addressed in this article.

The basic diode behavior and recombination mechanisms are the same for all the TFSCs. To illustrate this, it is helpful to look at the temperature dependence of V_{OC}. Figure 7 shows V_{OC} as a function of T for several
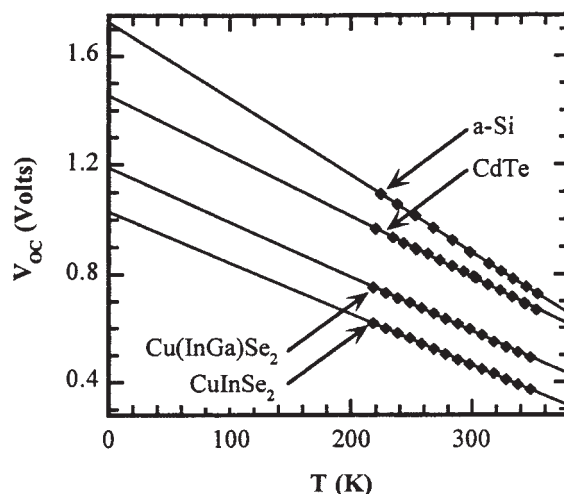
Figure 7. Temperature dependence of V_{OC} for four TFSC devices with different absorber materials, in each case $V_{OC} \rightarrow E_g/q$ (absorber) as $T \rightarrow 0$

TFSCs, including a-Si, CdTe, and Cu(InGa)Se$_2$ with two different bandgaps, with lines extrapolating each to $T = 0$. In each case the line fits the data well with intercept $V_{OC} \rightarrow E_g/q$ as $T \rightarrow 0$, where E_g is the bandgap of the primary light–absorbing layer. Thus, experiments show that the barrier height is $\Phi_b = E_g$ for these devices which indicates that the dominant recombination current occurs in the absorber layer. The measured temperature dependence of V_{OC} justifies writing the form of J_0 as in Equation (10).

Furthermore, for these TFSCs, the ideality factor of a well-behaved device is typically in the range $1 \cdot 3 \leqslant A \leqslant 2$. These results for Φ_b and A indicate that the solar cells operate with the diode current controlled by recombination through trap states in the space-charge region of the absorber layer. Typically this occurs in the few tenths of a micrometer closest to the junction in the absorber in a CdTe or Cu(InGa)Se$_2$ solar cell or within the i-layer of an a-Si device. The variation in A between 1 and 2 depends on the energies of the deep defects that act as dominant trap states[31] and its relatively small temperature dependence has been attributed to a distribution of traps[32] or a tunneling contribution to the space-charge recombination current.[33]

As shown in Figure 7, measuring the temperature dependence of V_{OC} enables Φ_b to be determined. To quantify the other terms which describe the recombination mechanism, A and J_0, it is tempting to simply perform a least-squares fit of the J–V data at a given temperature to Equation (9). However, this commonly leads to errors if it is not first verified that the J–V data are well-behaved in the sense that the basic diode model provides a complete description of the J–V data with R, G, and J_L independent of voltage over the range in which the data is analyzed. In practice, R, G, A, J_L and J_{00} can all be voltage and/or light dependent in TFSCs and these dependencies on extrinsic variables are a major source of complication in the analysis of TFSCs.

Analysis procedure

A practical procedure for verifying that the device is well-behaved and for determining the diode parameters is to use a set of four successive plots, each comparing data measured both in the dark and under white light illumination. In some cases, it is useful to make further comparison of data obtained at several illumination intensities. These plot types are:

(a) A standard linear J–V curve. This should include sufficient data in both the first and third quadrants where non-ideal effects not described by Equation (9), such as current blocking behavior or light-to-dark crossover in forward voltage bias or breakdown in reverse bias, which are commonly observed in TFSCs. The next three plots are derived from these light and dark J–V curves.

(b) A plot of the derivative $g(V) \equiv dJ/dV$ against V near J_{SC} and in reverse bias where the derivative of the diode term in Equation (9) becomes negligible. If the shunt term is ohmic and J_L is constant, $g(V)$ will be flat with

the value in reverse bias equal to G. In practice, the slope of most J–V curves is very small in this range so there may be some noise in calculating the derivative, particularly under illumination.

(c) The derivative $r(J) \equiv dV/dJ$ against $(J + J_{SC})^{-1}$ is plotted.[34,35] From Equation (9)

$$r(J) \equiv \frac{dV}{dJ} = R + \frac{AkT}{q}(J + J_L)^{-1} \tag{12}$$

for the case when $RG \ll 1$. So, a plot of $r(J)$ against $(J + J_L)^{-1}$ will yield a straight line with intercept R if J_L is independent of voltage. With constant J_L we can write $J_L = J_{SC}$ and more practically the data can be plotted against $(J + J_{SC})^{-1}$. A linear fit to the data gives an intercept of R and a slope AkT/q from which A can be calculated. A correction can be made for the case in which G is not negligible by plotting $(J + J_{SC} - GV)^{-1}$ on the abscissa.[35] For analysis of the dark J–V curve, $J_{SC} = J_L = 0$.

(d) A semilogarithmic plot of $J + J_{SC}$ against V-RJ using the value of R obtained from plot (c). A linear region over at least 1–2 orders of magnitude in current indicates a good fit to the diode equation. The intercept then gives J_0 and the slope in this case equals q/AkT so A can be calculated and compared with the value from plot (c). Again, a correction for G can be made, in this case by plotting $J + J_{SC} - GV$ on the ordinate.

This set of plots is shown in Figure 8 for a typical Cu(InGa)Se$_2$ cell with an efficiency of 15·5% and absorber layer bandgap $E_g = 1·2$ eV. Figure 8(a) shows plot type (a) and appears consistent with Equation (9); that is,
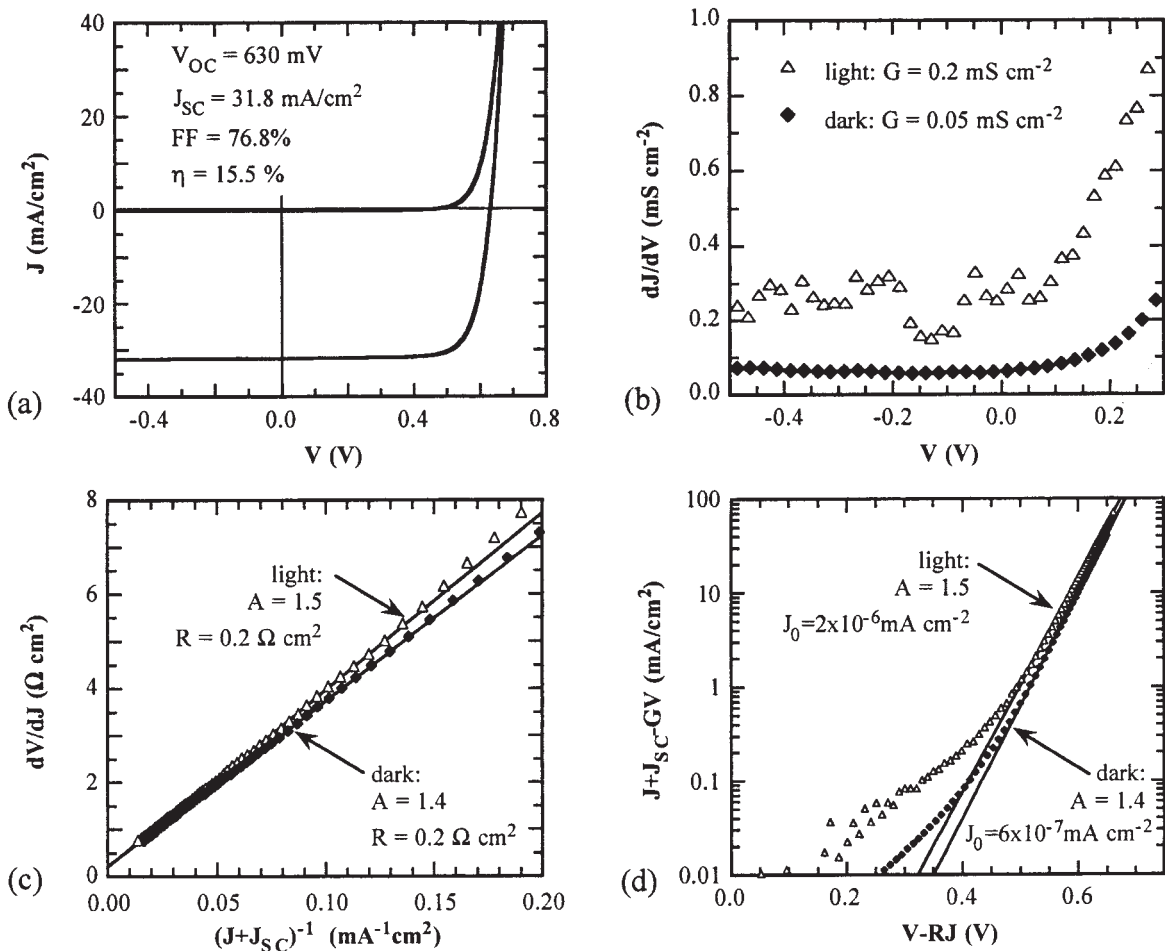

Figure 8. Light and dark J–V characteristics for a well-behaved Cu(InGa)Se$_2$ device: (a) standard J–V plot; (b) shunt characterization $g(V)$; (c) $r(J)$ with fit used to determine R and A; (d) $\ln(J + J_{SC})$ with fit used to determine A and J_0

there is no indication of non-ideal parasitic effects. Plot type (b) in Figure 8(b) shows that $g(V)$ is flat in reverse bias, and there is a small difference between the dark and illuminated results with $G(\text{dark}) = 0.05 \, \text{mS cm}^{-2}$ and $G(\text{light}) = 0.2 \, \text{mS cm}^{-2}$. Figure 8(c) shows plot type (c) for the same $Cu(InGa)Se_2$ device with nearly identical linear results for the dark and illuminated cases. For each, the line gives $R = 0.2 \, \Omega/\text{cm}^2$ and $A = 1.4–1.5$. Finally, plot type (d) in Figure 8(d) shows a linear region extending for $\sim$2 orders of magnitude in current with, again, good agreement between dark and illuminated data. The intercept for the dark data gives $J_0 = 6 \times 10^{-7} \, \text{mA/cm}^{-2}$ and the slope gives $A = 1.4$, in agreement with the value obtained from Figure 8(c).

Parasitic effects

Figure 8 showed the well-behaved case with R, G, J_L nearly independent of voltage and light intensity, as described by the basic diode equation. Deviations from this behavior are observed in different TFSCs and can be identified by the plots described above. One common cause for deviation from the diode behavior illustrated above is a voltage–dependent current collection, $J_L(V)$. The same analysis as above is shown in Figure 9 for a typical CdTe device. Again, there are no obvious deviations from the basic diode model evident in plot (a). However, in this case $g(V)$ plot (b) under illumination is voltage dependent over the entire range. The minimum value
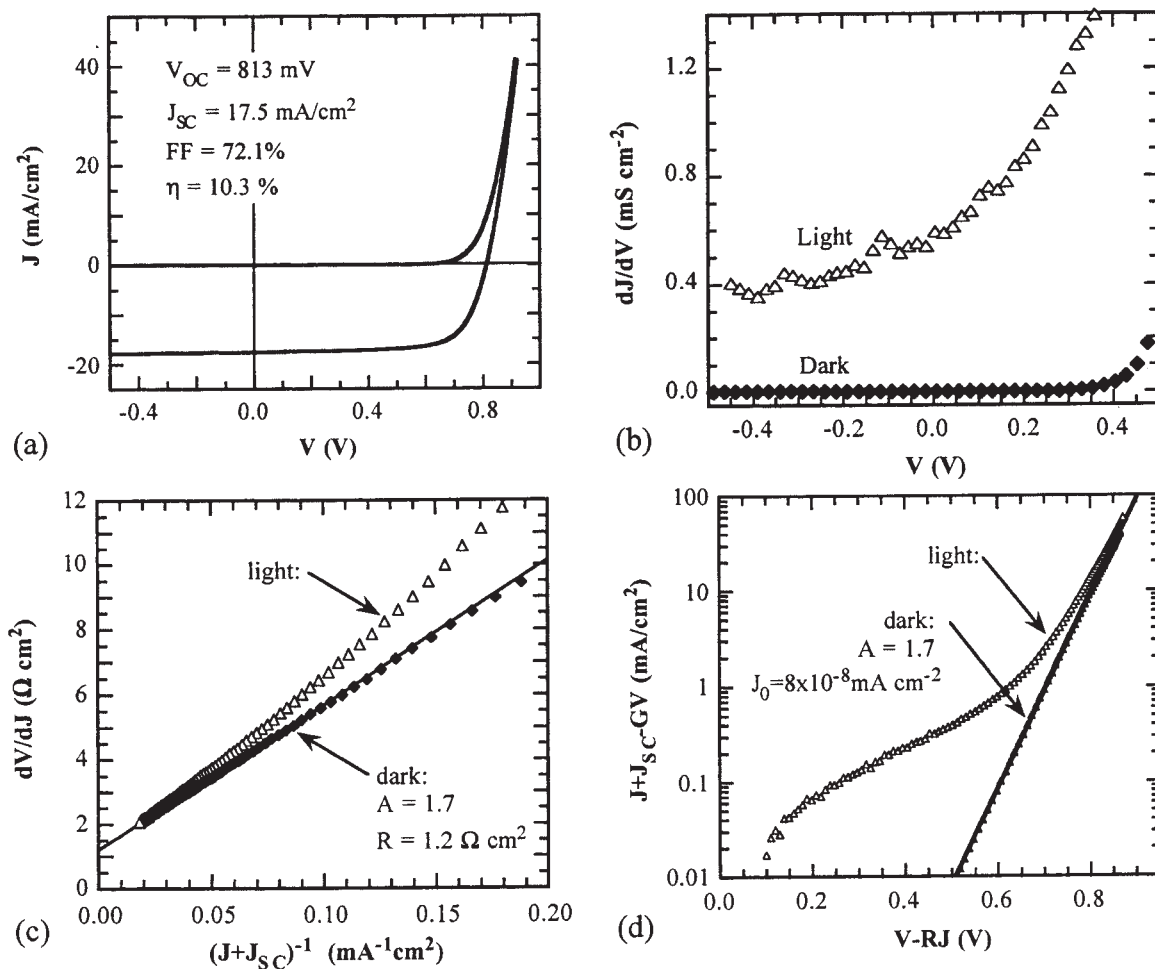

Figure 9. Light and dark J–V characteristics for a typical CdTe device: (a) standard J–V plot; (b) shunt characterization $g(V)$; (c) $r(J)$ with fit used to determine R and A for the dark data only; (d) $\ln(J + J_{SC})$ with fit used to determine A and J_0 for the dark data only

of $g(V)$ would give an upper bound to the shunt of $G(\text{light}) = 0.4\,\text{mS cm}^{-2}$ compared with the dark data for which the shunt term is neglible, $G(\text{dark}) = 0\,\text{mS cm}^{-2}$. Similarly $r(J)$ under illumination is not linear in Figure 9(c) with a discrepancy between the dark and illuminated data that increases with increasing $(J + J_{SC})^{-1}$. 1. The dark data in this case gives $R = 1.2\,\Omega\,\text{cm}^2$ and $A = 1.7$. Forcing a linear fit to the light data shown in Figure 9(c) would give A ranging from 2.5 to 1.8, depending on the range of data included in the fit. In general, an attempt to fit a line to the data in a case with $J_L(V)$ will overestimate, or at best give an upper bound to, the slope and A. Finally, in plot (d) of Figure 9, there is a large deviation in the current under illumination and the J–V data do not fit the simple exponential form of Equation (1) so A and J_0 cannot be reliably determined although it is well behaved in the dark. It is worth noting that this CdTe cell has relatively high FF = 72.1%. Many other cells with lower FF have a much larger range of uncertainty in the analysis of A and J_0.

In general, there are several possible explanations for the behavior shown under illumination in Figure 9 as any of the parameters in the diode equation could be illumination dependent. This J–V behavior could be $J_L(V)$ caused by field-dependent collection in the absorbing layer or a barrier to collection with barrier height changing as a function of voltage bias. These can be separated, as above, by the wavelength-and-voltage-bias-dependent QE. Similarly, the difference in FF under blue and red light can be used to distinguish $J_L(V)$ losses or to distinguish between p/i interface and i-layer recombination losses in an a-Si device. Generally the shunt term, which describes a path for current parallel to the main diode, is assumed to be ohmic, i.e., G is independent of V. A voltage-dependent shunt, $G(V)$ would affect light J–V measurements identically to $J_L(V)$, but could be distinguished from $J_L(V)$ because it would be expected to have the same effect on the dark data. Experience with many TFSCs has shown that voltage-dependent photocurrent collection is the most likely explanation when the dark J–V curve is well behaved, but the light photocurrent J–V curve deviates, as in Figure 9.

It is useful to describe the light generated current as:

$$J_L(V) = J_{L0}\eta_C(V) \tag{13}$$

to show explicitly the relation between the optically limited light generated current, J_{L0}, and the collection function $\eta_c(V)$. This equation is analogous to Equation (4), and $\eta_c(V)$ can be the same function for QE and J–V analysis. As previously, J_{L0} can be measured by the current with far reverse bias (in practice -0.5 to -1 V is sufficient in most cases). Then, a complete description of the light generated current can focus on determining $\eta_c(V)$ to quantify the mechanisms for losses due to incomplete collection. Several methods have been developed to experimentally determine $\eta_c(V)$, including the use of chopped ac measurement to separate light and dark currents[36] and the difference of J–V measurements made at several different light intensities.[37] In general, $\eta_c(V)$ will depend on some combination of field-assisted collection and diffusion. The model for $\eta_c(V)$ in the case of a uniform field presented in Equations (6–8) was applied to the J–V behavior of a-Si p–i–n solar cells.[6,12,14] Along with the basic diode parameters in Equation (9), this form of the collection function provides a useful parametric description of the voltage-dependent collection in a-Si and a-SiGe devices.[14]

Another method which is sometimes used to determine diode parameters is to plot J_{SC} on a logarithmic scale against V_{OC} with measurements at different light intensities. This would give linear behavior with intercept J_0 and slope $q/(AkT)$, but only, again, for the well-behaved case of constant J_L. In the case of voltage dependent $J_L(V)$ or $G(V)$, this method could also give erroneous results, overestimating A. One advantage to this method is that a series resistance correction can normally be ignored since it makes no contribution at V_{OC}, since $J = 0$, or at J_{SC}, except in the case of an extremely large resistance.

Other common parasitic effects that are observed in TFSCs include blocking behavior which can originate at a second junction in the device, such as a non-ohmic contact, or from an interface barrier that may block carrier collection in forward bias, as mentioned above. The latter situation could arise, for example, due to a step in the conduction band alignment at the p–n interface or the interface between the emitter and TCO layers.

In some cases, blocking behavior is easily seen just from the J–V curves. However, a more definitive way to detect such behavior in forward bias is from the plot of $r(J)$ against $(J + J_{SC})^{-1}$ as shown in Figure 10. The blocking behavior is apparent as an inflection in the data as $(J + J_{SC})^{-1}$ decreases. In CdTe, this is commonly attributed to a blocking back contact. Because the blocking contact or other barrier may not necessarily be apparent in plot type (a), it is always necessary to characterize the derivative as in plot type (c). In the example
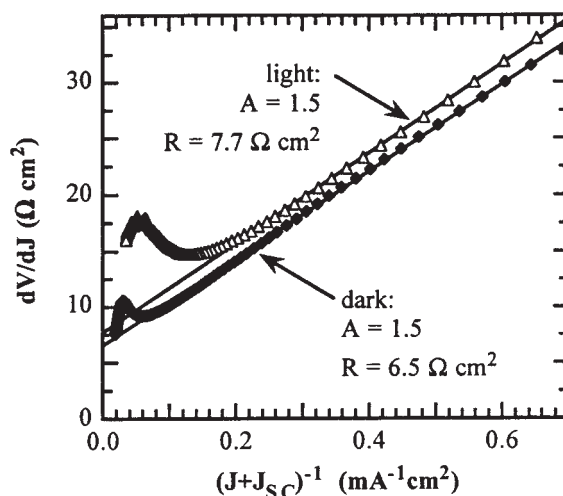
Figure 10. Plot of $r(J)$ against $(J + J_{SC})^{-1}$ for a CdTe device, showing the effect of a blocking back contact for a case where the diode parameters R and A can still be determined

shown, the blocking behavior affects the J–V curve only in far forward bias. The parameters A and R can still be obtained from a linear fit in Figure 10 and J_0 from plot type (d). Then the characteristics of the blocking diode can be quantitatively extracted by subtracting the characteristics of the primary diode calculated from Equation (9) and a barrier height determined by doing this analysis as a function of temperature.[38]

In most cases, deviations from the behavior predicted by Equation (9) can be attributed to parasitic effects such as non-ohmic or blocking contributions in series or shunt-like effects is parallel with the primary diode. One other cause for non-ideal behavior is light-to-dark crossover which can be caused by photoconductive effects or a light-dependent barrier. In some cases with crossover, plots of type (a–d) may appear well behaved, although with different values of R, A, or J_o obtained between the dark and illuminated data. Other, more fundamental reasons for the inability to describe the data with Equation (9) include the contributions of more than one recombination mechanism or a bias-voltage-dependent diode quality factor.[39] A final effect that should be checked when characterizing J–V results to determine fundamental diode behavior is that the J–V curves are stable over time and the same for either J–V sweep direction, i.e., beginning in forward or reverse bias. Otherwise, the parameters determined from the analysis may not describe stable or equilibrium behavior of the device.

The characterization described above in which the series resistance is obtained from the derivative $r(J)$ with plot (c) determines a lumped resistance parameter that likely includes the sum of several contributions. Specifically, these may include spreading resistance through front or back electrodes, contact resistances, and through film resistance in the active absorber, or emitter layers in the device. Some device structures incorporate a collection grid which can also contribute to the lumped resistance. Various methods to separate these contributions have been applied to TFSCs. In general, this can be done by fabricating devices with systematically varied geometries or lateral current paths on a single substrate with all vertical device layers identical. In particular, the device area can be varied to change the contact resistance contribution, and the lateral distance between devices and contacts can be varied to change the spreading resistance contributions.[40,41] Such a technique was used to compare devices with ZnO or SnO$_2$ contacts with the p-layer in a-Si devices. The ZnO/p contact gave lower V_{OC} and FF, which was widely attributed to a barrier or contact resistance.[42] R was determined as in plot (c) for cells with different path length in the ZnO or SnO$_2$ and the contact resistance was determined by extrapolating to zero path-length. This analysis showed that the ZnO/p contact was ohmic with low resistance, contrary to standard assumptions. A similar problem was encountered in CuInSe$_2$ devices which showed blocking behavior in forward bias, particularly at reduced temperature, that was generally attributed to a non-ohmic back contact. Specially constructed devices, with a gap in the Mo back contact enabled the voltage drop across the Mo/Cu(InGa)Se$_2$ contact to be separated from the rest of the device.[43] This showed that the blocking behavior did not occur at the back contact and it has since been attributed to the CdS/Cu(InGa)Se$_2$ interface.[44]

ADMITTANCE CHARACTERIZATION

Admittance measurements, typically capacitance–voltage (C–V), are well established techniques to obtain free carrier densities, depletion widths, deep trap densities and potential barriers from the ac response of p–n junctions, including solar cells. Admittance measurements in TFSC are complicated by extraneous or parasitic factors such as contact or lateral series resistance effects, inductance at high frequency, neutral bulk capacitance and resistance in series with the junction, short-term instability or hysteresis due to thermal and bias cycling, and light intensity dependence due to trapping. It is the junction capacitance or conductance which contains information about the deep states, free carriers, diffusion voltage, etc. To extract significant information, for example about the deep states, free carriers, or diffusion voltage, generally requires a circuit model approach to account for effects, including bulk and contact resistance, bulk capacitance, and inductance. Various circuit models have been proposed and applied to TFSC devices.[45–48] A practical complication is that typically one does not know *a priori* what range of frequency and temperature are required to allow extraction of the given parameter (i.e., deep or shallow states, free carrier density, diffusion voltage) from the measured admittance, as discussed below.

The standard analysis of an abrupt p–n junction assumes a uniform space-charge density created by a spatially uniform distribution of shallow ionized donors or acceptors. Analysis of the space charge electrostatics for this simple case is commonly found in many texts. It can be easily shown that

$$C(V)^{-2} = \frac{q\varepsilon N(W)}{2(V + V_D)} \tag{14}$$

where $C(V)$ is the capacitance per area, V_D is the diffusion voltage, and $N(W)$ is the net space charge density at the edge of the depletion width. When C^{-2} is plotted against V, a straight line is obtained whose slope is inversely related to N and whose intercept is V_D. It is a common misconception that the intercept of $C(V)^{-2}$ plotted against V is the built-in potential or barrier height $V_B = \Phi_b/q$. The band bending or diffusion potential V_D differs from built-in potential by the Fermi energy, $qV_B = E_F + qV_D$. With c-Si, $E_F \sim kT$, so V_B and V_D are numerically similar, but in TFSCs, E_F can be 0·1–0·8 eV, leading to large differences between V_B and V_D.

In most TFSCs, however, the simple ideal relationship in Equation (14) is rarely observed. It was realized in the early 1980s that capacitance was a valuable technique to characterize the deep states in the intrinsic layer in a-Si solar cells, but that new methods of measurement and analysis would be needed. In particular, a method called drive-level capacitance profiling (DLCP) was developed for TFSCs.[49]

An example of the failure of Equation (14) is shown in Figure 11 for two CdTe devices made by different processes, but both having ∼11% efficiency. This shows C^{-2} plotted against V measured at 100 kHz in the dark
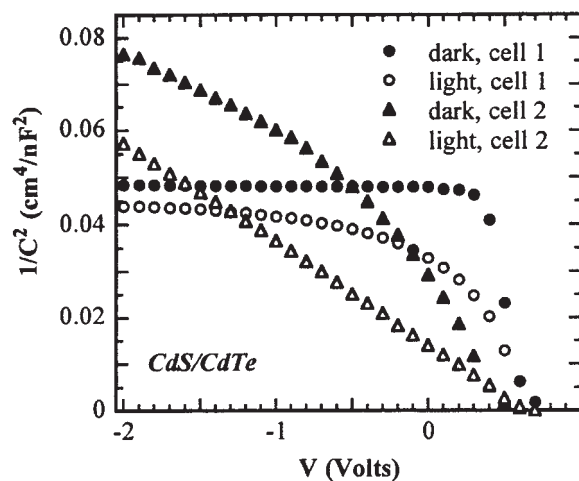

Figure 11. Plot of C^{-2} against V for two differently fabricated CdTe devices in light and dark at 100 kHz

and light for each device. In the dark, neither yields a straight line, the intercept or slope of which are physically meaningful. Cell 1 has the classic shape of a *p–i–n* type device where the highly resistive *i*-layer is totally depleted. The curve is independent of voltage until forward biased near V_D when the depletion region rapidly collapses leading to an increase in *C*. From the value of *C* at reverse bias, a CdTe layer thickness of 2·2 μm is calculated according to $C = \varepsilon/W$, with *W* assumed equal to the absorber layer thickness *d*. This agrees well with the thickness determined from growth rate and time. Most a-Si *p–i–n* devices have a dark *C–V* shape like CdTe Cell 1. Cell 2 in the dark has a varying slope implying a spatially varying *N*. It is not fully depleted even at −2V, unlike Cell 1. With ∼1 sun light bias, the shapes of C^{-2} plotted against *V* change for both cells. The data for Cell 1 become more rounded but still do not yield a linear relation, while the data for Cell 2 have developed into a straight line from which the slope and intercept yield a space-charge density of 5×10^{14} cm^{-3} and $V_D = 0.56$ V by fitting to Equation (14). This value of *N* is consistent with values from 1–6×10^{14} cm^{-3}, as reported for a variety of CdTe TFSCs, typically measured in the dark. This relatively low value of free carriers identifies one of the critical problems with CdTe technology, namely inability to dope the CdTe to a sufficiently high carrier density. The increase in capacitance seen in Figure 11 with light bias is due to trapping of photo-generated charge at extraneous states within the bandgap. Thus, the calculated value of *N* does not represent a true free carrier or shallow dopant density, as often assumed in standard derivations. These extraneous states, common to most TFSCs, make analysis and interpretation of the *C–V* data very challenging. They cause the capacitance to vary with bias light intensity and spectrum, ac frequency, and temperature. However, these same sensitivities can be exploited to determine the trap density.

There are many additional reasons why measurements and analyses of TFSC capacitance[50,51] are more challenging and less straightforward than simply applying Equation (14). The root cause for the complications is often the presence of deep trapping states in the TFSC. Often not mentioned is the problem of hysteresis where the admittance is different for increasing voltage bias compared with decreasing voltage bias. This is typically due to incomplete charging or discharging of deep states when the voltage sweep up–down retrace time is less than the deep state response time, so the device is not at steady state during the measurement. One requirement is that the dielectric relaxation time $\tau_d = \rho\varepsilon$ of the semiconductor must be less than the ac period ω^{-1}, otherwise the charge cannot move through the material to supply or empty the gap states. This is often overlooked in crystalline semiconductor *C–V* analysis because it is not a limitation in low-resistivity materials, but is necessary to consider with materials like a-Si or CdTe, especially at low measurement temperatures.

In crystalline and polycrystalline devices, the capacitance is determined by the space-charge density at the edge of the depletion width *N(W)* since this is where the ac field is modulating the space charge. Since *W* is a function of *V*, *N(W)* can be determined spatially by varying *V*. From Equation (14)

$$\frac{dC^{-2}}{dV} = \frac{2}{q\varepsilon N(W)} \tag{15}$$

or

$$N(W) = C^3 \left[q\varepsilon \frac{dC}{dV} \right]^{-1} \tag{16}$$

Then, a plot of *N(W)* against $W(V) = \varepsilon/C(V)$ gives the net charge density profile across some portion of the absorber. This is often called the *C–V* profile method. It has been widely applied to both CdTe and Cu(InGa)Se$_2$ TFSCs, but this is not a unique parameter to characterize the absorber, since *N(W)* gives the shallow carrier density $|N_A - N_D|$ plus the charge emitted from and captured at deep states which can empty and fill within the ac period. Since these rates depend on temperature and generation rate, *N(W)* will be a function of the ac frequency, light intensity and temperature.

In a semiconductor with a large density of deep trap states, the concept of depletion edge between neutral space charge and bulk regions is not very helpful in understanding admittance measurements. More useful is a demarcation length X_E which separates the material into a region between the junction and X_E in which charge can not respond to the ac signal, and one beyond X_E in which it can. This is illustrated in Figure 12 for a *p*-type
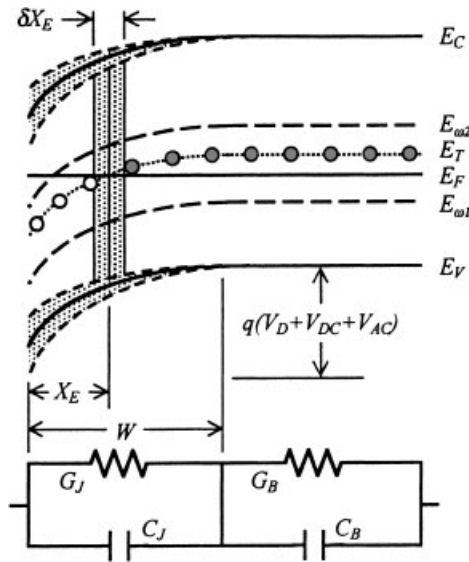
Figure 12. Band diagram of p-type semiconductor junction with a deep trap level E_T and two measurement energies $E_{\omega 1}$ and $E_{\omega 2}$. Shaded areas represent variations in band bending and energy response, δX_E. due to the oscillating ac voltage. The equivalent circuit shows the junction (C_J and G_J) in series with the bulk (C_B and G_B)

absorber with a single trap level E_T. X_E depends on the energy distribution of the deep state density as well the measurement temperature, frequency and bias voltage.

Trap occupancy is determined by the Fermi level. Hole traps above the Fermi level are assumed filled and those below empty, with the opposite for electron traps. In the presence of a modulating ac voltage V_{AC} of frequency $\omega = 2\pi f$, only states which can release their charge within the ac period will be able to contribute to the admittance. The cut-off energy dividing responsive from unresponsive states is

$$E_{\omega} = kT \ln\left(\frac{\nu}{\omega}\right) \tag{17}$$

Here ν is the attempt-to-escape frequency (phonon frequency), of the order of 10^{13} rad/s. For traps to respond to the ac signal, they must be shallower than E_{ω}. In Figure 12, $E_{\omega 1}$ represents a measurement condition where either T is too low or ω is too high for charge to respond. $E_{\omega 2}$ represents measurements at higher T and/or lower ω such that hole traps at E_T can respond to the ac signal. For the case of a continuous trap distribution as in a-Si, X_E is where $E_{\omega} = E_F$.

The region between the junction and X_E behaves like an insulator, or space-charge region, of thickness X_E where traps are empty since $E_T < E_F$. Far beyond X_E, trap states can respond much more rapidly than the ac cycle, so their charging and discharging can be described by the bulk capacitance $C_B = \varepsilon/(d-X_E)$ and conductance $G_B = \sigma/(d-X_E)$. Around X_E, states respond in approximately the same time as the ac period and therefore contribute to the ac capacitance C_{AC} (out-of-phase signal) and conductance G_{AC} (in-phase signal). There will be a static, or dc capacitance and conductance associated with response at X_E as well. Thus, the admittance Y_J of the junction region at X_E is

$$Y_J = [G_{DC} + G_{AC}(\omega)] + i\omega[C_{DC} + C_{AC}(\omega)] = G_J + i\omega C_J \tag{18}$$

where $G_{DC} = J(V)/AkT$ is the dynamic conductance of the diode current, and $C_{DC} = \varepsilon/L_0$ is the static or dc capacitance at X_E due to the charge screening length L_0. The correct series-parallel circuit model must be used to extract these parameters from measurements.[45,47,48] Equation (18) represents the case for junction capacitance and conductance in parallel. The total admittance of the device should include the parallel combination of bulk

elements C_B and G_B in series with the junction elements as in Figure 12. In general, the parameter of greatest interest in characterizing deep states in highly resistive material such as a-Si or CdTe is C_J while in lower resistivity material such as $Cu(InGa)Se_2$, both C_J and G_J can contain information about the trapping states.[52]

To ensure correct admittance measurements, the dissipation $D = G/(\omega C)$ of the net circuit should be monitored. D increases exponentially with increasing T or V since dc current through the conductance will dominate and effectively short out the capacitance, leading to incorrect values with very low phase angle. In general, D should be < 5–10, depending on the measurement circuit.

A completely general treatment of C_J yields

$$C_J = \varepsilon \left(X_E + \varepsilon \frac{E_E}{\rho_E} \right)^{-1} \qquad (19)$$

where E_E and ρ_E are the field and charge density at X_E.[49] In the case of an exponential density of midgap states, Equation (19) reduces to

$$C_J = \frac{\varepsilon}{X_E + L_0} \qquad (20)$$

where L_0 is the Debye screening length related to the midgap state density g_0.[53] This formulation describes the two capacitors in series, and predicts that the capacitance should depend on T and f through E_ω. Figure 13 shows C measured on an a-SiGe p–i–n cell over a range of temperatures at one frequency and over a range of frequencies at two temperatures plotted as a function of E_ω, determined by Equation (17). The data show a single capacitance response curve due to the dependence of the deep state response on E_ω, not on T and f individually. The solid line is the fit to this data, using the procedure described elsewhere.[53] Three regions are indicated in Figure 13. Region I is the 'freeze-out' region where no charge can respond since $E_\omega < E_F$, and the capacitance is ε/d. The increase in Region II is due to the deep state response and the peak value of the capacitance occurs for sufficiently low f, high T, or forward bias that $X_E = 0$ hence $C_J = \varepsilon/L_0$ according to Equation (20). The density of states at the Fermi level $g_0 = 3 \times 10^{17} \, cm^{-3} eV^{-1}$ can be readily obtained from this peak value. The fall-off in C in Region III occurs because the junction capacitance, now constant at ε/L_0, is shunted by the increasing current conduction through the junction diode term G_{DC}, as seen in the equivalent circuit. This example shows how obtaining information about deep traps from the measured capacitance requires understanding the TFSC device as a circuit to account for parasitic elements, and then making measurements in the right temperature and frequency space for the states to respond. It also shows that admittance measurements must be performed at a
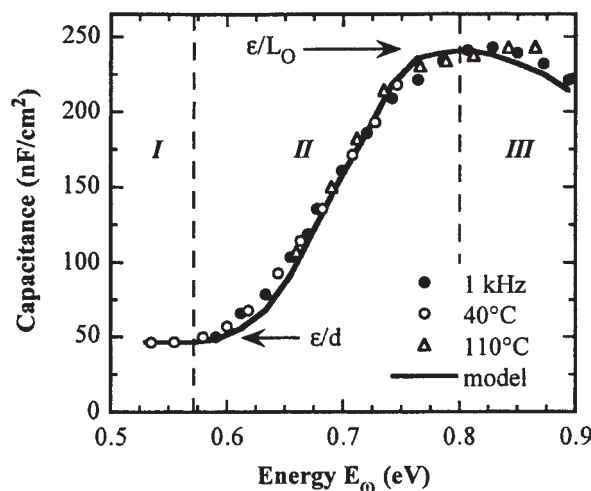
Figure 13. Plot of C against E_ω for a-SiGe p–i–n TFSC measured at 1 kHz with T varied from 0 to 140°C and at 40 or 110°C with f varied from 0·1 to 100 kHz. The solid line shows a fit to the data[53]

range of voltage, frequency and temperature to identify the region where the desired parameter determines C or G. For example, to obtain the absorber thickness from $d = \varepsilon/C(V)$ the entire absorber should be depleted ($V < 0$) and f should be high enough and/or T low enough that $E_\omega < E_F$. To obtain the maximum sensitivity to deep states, the entire absorber should not be depleted ($V \geqslant 0$) and f should be low enough and/or T should be high enough that $E_\omega > E_F$.

Equation (19) is also the basis for DLCP which has been applied to characterize the spatial and energetic distribution of defects in TFSC. In DLCP, the ac voltage amplitude V_{AC} is varied along with the dc bias voltage V_{DC}.[49] Drive level capacitance has been applied to study Ge defects in a-SiGe,[53] Cu doping in CdTe[54] and defects in Cu(InGa)Se$_2$ as a function of relative Ga content,[55] all obtained in a TFSC device configuration.

CONCLUSIONS

Many of the methods developed for characterization of crystalline semiconductor solar cells either do not apply or must be modified for valid application to TFSCs. The primary reasons are a high density of trapping and recombination states, which is related to the polycrystalline and amorphous materials, and parasitic losses, which can be related to the deep states and also to the device structure and contacts. One must always be wary when analyzing data from TFSCs that the actual properties being sought are not masked or influenced by the many possible losses or non-idealities which occur in these devices. Various methods have been presented for the characterization of QE, J–V, and admittance measurements of TFSCs that identify and, in some cases, correct for these extrinsic effects and enable analysis of the intrinsic junction behavior. These methods have contributed to the remarkable improvements in the performance and fundamental understanding of a-Si, CdTe, and Cu(InGa)Se$_2$ solar cells.

REFERENCES

1. Emery K. Measurement and characterization of solar cells and modules. In *Handbook of Photovoltaic Science and Engineering*, Luque A, Hegedus S (eds). Wiley: Chichester, 2003; Chap. 16.
2. Dalal V, Rothwarf A. Comment on 'A simple measurement of absolute solar cell efficiency'. *Journal of Applied Physics* 1979; **50**: 2980–2981.
3. Yang J, Banarjee A, Glatfelter T, Sugiyama S, Guha S. Recent progress in amorphous silicon alloy leading to 13% stable efficiency. *Proceedings of the 26th IEEE Photovoltaic Specialists Conference* 1997; 563–568.
4. Wu X, Dhere R, Yan Y. High efficiency polycrystalline CdTe thin film solar cells with oxygenated amorphous CdS window layer. *Proceedings of the 29th IEEE Photovoltaic Specialists Conference* 2002; 531–534.
5. Shafarman W, Klenk R, McCandless B. Device and material characterization of Cu(InGa)Se$_2$ solar cells with increasing bandgap. *Journal of Applied Physics* 1996; **79**: 7324–7328.
6. Crandall R. Modelling of thin film solar cells: uniform field approximation. *Journal of Applied Physics* 1983; **54**: 7176–7186.
7. Liu X, Sites J. Solar-cell collection efficiency and its variation with voltage. *Journal of Applied Physics* 1994; **75**: 577–581.
8. Phillips J, Roy M. Resistive and photoconductive effects in spectral response measurements. *Proceedings of the 20th IEEE Photovoltaic Specialists Conference* 1998; 1614–1616.
9. Sites J, Tavakolian H, Sasala R. Analysis of apparent quantum efficiency. *Solar Cells* 1990; **29**: 39–48.

10. Shafarman W, Stolt L. Cu(InGa)Se$_2$ solar cells. In *Handbook of Photovoltaic Science and Engineering*, Luque A, Hegedus S (eds). Wiley: Chichester UK, 2003; Chap. 13.

11. Fahrenbruch A, Bube R. *Fundamentals of Solar Cells*. Academic Press: New York, 1983; 231–234.

12. Misiakos K, Lindholm F. Analytical and numerical modeling of amorphous silicon *pi–n* solar cells. *Journal of Applied Physics* 1988; **64**: 383–393.

13. Arya R, Catalano A, Oswald R. Amorphous silicon *p–i–n* solar cells with graded interface. *Applied Physics Letters* 1986; **49**: 1089–1091.

14. Hegedus S. Current voltage analysis of a-Si and a-SiGe solar cells including voltage dependent photocurrent collection. *Progress in Photovoltaics Research and Applications* 1997; **5**: 151–168.

15. Shafarman W, Zhu J. *Material Research Society Symposium Proceedings* 2001; **668**: H2.3.

16. Dalal V, Leonard M, Booker J, Vaseashta A, Hegedus S. Quantum efficiency of amorphous alloy solar cells. *Proceedings of the 18th IEEE Photovoltaic Specialist Conference* 1985; 837–841.

17. Rocheleau R, Hegedus S, Buchanan W, Tullman R. Effects of impurities on film quality and device performance in a-Si:H deposited by photo-assisted CVD. *Proceedings of the 19th IEEE Photovoltaic Specialists Conference* 1987; 699–704.

18. Banerjee A, Xu X, Yang J, Guha S. Carrier collection losses in amorphous silicon and amorphous silicon-germanium alloy solar cells. *Applied Physics Letters* 1995; **67**: 2975–2977.

19. Fortmann C, Fischer D. Mobility, recombination kinetics, and solar cell performance. *Proceedings of the 23rd IEEE Photovoltaic Specialists Conference* 1993; 966–970.

20. Hegedus S, Buchanan W. Understanding graded a-SiGe solar cells using bifacial photocurrent collection. *Proceedings of the 23rd IEEE Photovoltaic Specialists Conference* 1993; 991–994.

21. Sudharsanan R, Rohatgi A. Investigation of metalorganic chemical vapor deposition grown CdTe/CdS solar cells. *Solar Cells* 1991; **31**: 143–150.

22. Agostinelli G, Bätzner D, Dunlop E. Apparent quantum efficiency in CdTe solar cells. *Proceedings of the 17th European Photovoltaic Solar Energy Conference* 2001; 1254–1257.

23. Toyama T, Suzuki T, Gotoh M. Reduction of infrared response of CdS/CdTe thin-film solar cell with decreased thickness of photovoltaic active layer. *Solar Energy Materials and Solar Cells* 2001; **67**: 41–47.

24. Phillips J. Determination of diffusion length from bi-facial spectral response. *Proceedings of the 20th IEEE Photovoltaic Specialists Conference* 1990; 782–786.

25. Crandall R, Sadlon K, Kalina J, Delahoy A. Direct measurement of mobility–lifetime product of holes and electrons in an amorphous silicon *p–i–n* cell. *Material Research Society Symposium Proceedings* 1989; **149**: 423–427.

26. Hegedus S, Lin H, Moore A. Light induced degradation in amorphous silicon studied by surface photovoltage technique: a comparison of lifetime vs. space charge effects. *Journal of Applied Physics* 1988; **64**: 1215–1219.

27. Chatterjee P, McElhenry P, Fonash S. Influence of illumination conditions on the spectral response of amorphous silicon Schottky barrier structures. *Journal of Applied Physics* 1990; **67**: 3803–3809.

28. Hegedus S, Kaplan R. Analysis of quantum efficiency and optical enhancement in amorphous Si *p–i–n* solar cells. *Progress in Photovoltaics Research and Applications* 2002; **10**: 257–269.

29. Lechner P, Geyer R, Schade H. Detailed accounting for quantum efficiency and optical losses in a-Si:H based solar cells. *Proceedings of the 28th IEEE Photovoltaic Specialists Conference* 2000; 861.

30. Phillips J, Birkmire R, McCandless B. Polycrystalline heterojunction solar cells. *Physica Status Solidi (b)* 1996; **194**: 31.

31. Sah C, Noyce R, Shockley W. Carrier generation and recombination in *P–N* junctions and *P–N* junction characteristics. *Proceedings of the Institution of Radio Engineers* 1957; **45**: 1228.

32. Walter T, Menner R, Koble CH, Schock H. Characterization and junction performance of highly efficient ZnO/CdS/CuInSe$_2$ solar cells. *Proceedings of the 12th European Photovoltaic Solar Energy Conference* 1994; 1755–1758.

33. Rau U. Tunneling-enhanced recombination in Cu(In,Ga)Se$_2$ heterojunction solar cells. *Applied Physics Letters* 1999; **74**: 111.

34. Swartz G. Computer model of amorphous silicon solar cell. *Journal of Applied Physics* 1982; **53**: 712.

35. Sites J, Mauk P. Diode quality factor determination for Solar Cells. *Solar Cells* 1987; **27**: 411.

36. Eron M, Rothwarf A. Effects of a voltage-dependent light-generated current on solar cell measurements: CuInSe$_2$/Cd(Zn)S. *Applied Physics Letters* 1984; **44**: 131.

37. Phillips J, Titus J, Hoffmann D. Determining the voltage dependence of the light current in CuInSe$_2$ solar cells. *Proceedings of the 26th IEEE Photovoltaic Specialists Conference* 1997; 463.

38. Roy M, Damaskinos S, Phillips J. The diode current mechanism in CuInSe$_2$/CdS Heterojunctions. *Proceedings of the 28th IEEE Photovoltaic Specialists Conference* 1988; 1618.

39. Lyakas M, Zaharia R, Eizenberg M. Analysis of nonideal Schottky and *p–n* junction diodes—extraction of parameters from *I–V* plots. *Journal of Applied Physics* 1995; **78**: 5481.

40. Meier M, Schroder D. Contact resistance: its measurement and relative importance to power loss in a solar cell. *IEEE Transactions on Electron Devices* 1984; **ED-31**: 647.

41. Schade H, Smith Z. Contact resistance measurements for hydrogenated amorphous silicon solar cell structures. *Journal of Applied Physics* 1986; **59**: 1682.

42. Hegedus S, Kaplan R, Ganguly G, Wood G. Characterization of the SnO_2/p and ZnO/*p* contact resistance and junction properties in a-Si *p–i–n* solar cells and modules. *Proceedings of the 28th IEEE Photovoltaic Specialists Conference* 2000; 728.

43. Shafarman W, Phillips J. Direct current–voltage measurements of the $Mo/CuInSe_2$ contact on operating solar cells. *Proceedings of the 25th IEEE Photovoltaic Specialists Conference* 1996; 917.

44. Eisgruber I, Granata J, Sites J. Blue-photon modification of nonstandard diode barrier in $CuInSe_2$ solar cells. *Solar Energy Materials and Solar Cells* 1998; **53**: 367.

45. Losee D. Admittance spectroscopy of impurity levels in Schottky barriers. *Journal of Applied Physics* 1975; **46**: 2204–2214.

46. Snell A, Mackenzie K, Le Comber P, Spear W. The interpretation of capacitance and conductance measurements on metal–amorphous silicon barriers. *Philosophical Magazine B* 1979; **40**: 1–15.

47. Viktorovitch P, Moddel G. Interpretation of the conductance and capacitance frequency dependence of hydrogenated amorphous silicon Schottky barrier diodes. *Journal of Applied Physics* 1980; **51**: 4847–4854.

48. Scofield J. Effects of series resistance and inductance on solar cell admittance measurements. *Solar Energy Materials and Solar Cells* 1995; **37**: 217–226.

49. Michelson C, Gelatos A, Cohen J. Drive-level capacitance profiling: its application to determining gap state densities in hydrogenated silicon films. *Applied Physics Letters* 1985; **47**: 412–414.

50. Eron M. Steady-state and transient capacitance of a *p–n* junction in the presence of high density of deep levels. *Journal of Applied Physics* 1985; **58**: 1064–1066.

51. Mauk P, Tavakolian H, Sites J. Interpretation of thin-film polycrystalline solar cell capacitance. *IEEE Transactions on Electron Devices* 1990; **37**: 422–427.

52. Walter T, Herberholz R, Müller C, Schock H. Determination of defect distributions from admittance measurements and application to Cu(In,Ga)Se₂ based heterojunctions. *Journal of Applied Physics* 1996; **80**: 4411–4420.

53. Hegedus S, Fagen E. Midgap states in a-Si:H and a-SiGe:H *p–i–n* solar cells and Schottky junctions by capacitance techniques. *Journal of Applied Physics* 1992; **71**: 5941–5951.

54. Gilmore A, Kaydanov V, Ohno T. Treatment effects on deep levels in CdTe based solar cells. *Proceedings of the 29th IEEE Photovoltaic Specialists Conference* 2002; 604–607.

55. Heath J, Cohen D, Shafarman W. Distinguishing metastable changes in bulk CIGS defect densities from interface effects. *Thin Solid Films* 2003; **431–432**: 426.