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New ways of developing glass/conducting glass/CdS/CdTe/metal thin-film solar cells based on a new model

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Abstract

Making use of the authors' experimental results and the evidence available in the literature, an alternative model for glass/conducting glass/CdS/CdTe/metal solar cells has been formulated. This model explains the device behaviour in terms of a combination of a hetero-junction and a large Schottky barrier at the CdTe/metal interface. The main experimental observations available to date are described and compared with the currently assumed p–n junction model and this proposed new model. It is shown that the proposed model explains almost all the experimental results more satisfactorily. The paper describes the guidelines to further increase the performance efficiencies based on the new model. Following these new guidelines, the authors have fabricated improved devices producing open circuit voltage (V_{oc}) values over 600 mV, fill factor (FF) values over 0.60 and the short-circuit current density (J_{sc}) values over 60 mA cm^{-2} for best devices. Although the V_{oc} and FF could be further improved, the remarkable improvement of J_{sc} indicates the possibility of further development of multilayer graded band gap tandem solar cells based on CdS/CdTe system.

1. Introduction

Development of a low-cost, thin-film solar cell device with a reasonable efficiency for terrestrial solar energy conversion has been the subject of active research over the past two decades. Two systems are currently under intense research and development worldwide, those using $CuInGaSe_2$ (CIGS) and CdTe absorber materials. CIGS-based solar cells are currently leading with the record efficiencies of 18.8% (Contreras *et al* 1999), whereas CdTe-based solar cells have achieved 16.5% (Wu *et al* 2001) for small scale laboratory devices to date. The very slow progress of CdS/CdTe solar cell development is noteworthy as it has taken eight years of worldwide research to increase the efficiency by only 0.6% from 15.9% (Britt and Ferekides 1993) to 16.5% (Wu *et al* 2001). It is suggested that the rapid development of the CdTe-based solar cell has been hampered mainly by a lack of understanding of the physics of this device structure. This paper briefly discusses the currently assumed model and puts forward a new model to describe the device structure. Based on this new model, ways to further improve the CdS/CdTe solar cells are proposed. This paper also briefly presents the authors' latest achievements following these new suggestions.

2. Currently accepted model based on a p–n junction

The CdTe-based thin-film solar cell, the main subject of this paper, consists of two semiconducting layers: a wide band gap n-type CdS ($E_g = 2.42$ eV) layer is used as the window material and a narrower band gap CdTe ($E_g = 1.45$ eV) layer is used as the absorber material. If the CdTe layer is p-type, then the active junction is a simple p–n type hetero-junction, and the required internal electric field within the device is provided by this interface.

To date, various methods have been used to grow the materials and fabricate these solar cell devices. A genuine p–n junction device could have a typical structure of metal-1/n-CdS/p-CdTe/metal-2, providing two ohmic contacts for the collection of current, as shown in figure 1. Metal-1 serves as the ohmic contact to the n-CdS layer and a suitable

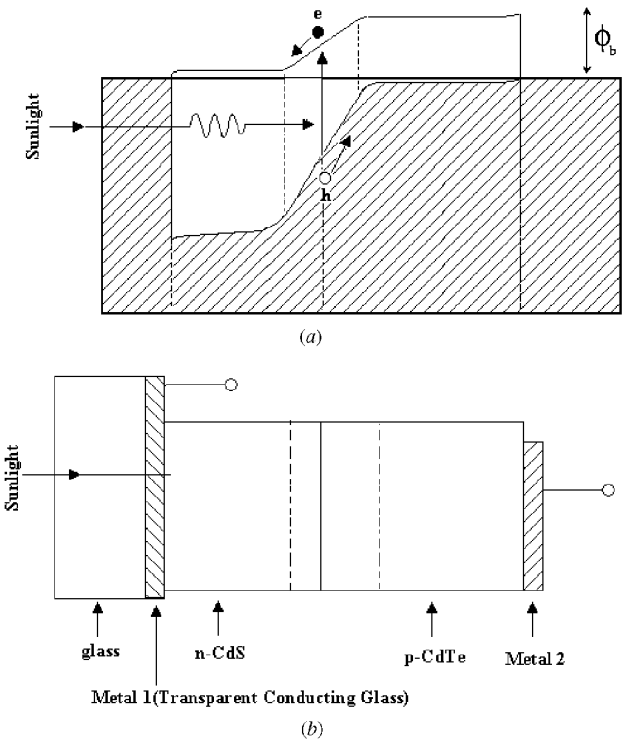

Figure 1. Energy band diagram and the material structure of the glass/CG(metal-1)/CdS/CdTe/metal-2 solar cell based on the assumed p–n junction model. (*a*) Energy band diagram of an n-CdS/p-CdTe hetrojunction. (*b*) Materials used in the device structure. Note the ohmic contact required for the p-type CdTe/metal interface according to this model (not to scale).

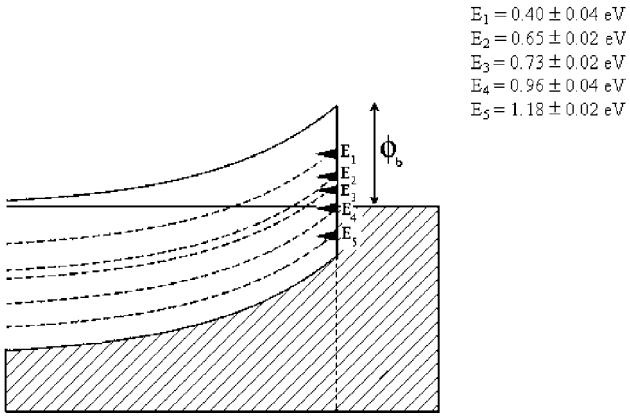

Figure 2. The ladder of Fermi level pinning positions, experimentally identified to date using bulk n-CdTe/metal contact work, photoluminescence, deep level transient spectroscopy (DLTS) and ballistic electron emission microscopy (BEEM) work (after Dharmadasa 1998).

metal contact such as Au, Cu/Au, Cu/Ni or Ni serves as the ohmic contact to the p-type CdTe layer. There are numerous publications on this type of genuine p–n junction type thin-film solar cell in the literature.

However, a large number of research groups have worked on glass/conducting glass(CG)/CdS/CdTe/metal structures using low-cost semiconducting layers and transparent glass/CG substrates as the starting material. The conducting glass used is usually indium tin oxide (ITO) or fluorine doped tin oxide (FTO) with metallic conduction and over 98% light transparency. The CdS layer used is always n-type and various growth methods such as chemical bath deposition (CBD), electrodeposition (ED), spray pyrolysis and vacuum evaporation have been used to produce this window layer. The thickness of this CdS window layer varies from 500 Å to a few microns according to the work reported in the literature. The absorber layer, CdTe, has also been produced using a variety of methods such as electrodeposition, screen printing and close spaced sublimation technique (CSST). The thickness of the CdTe layer varies from about 2 μm to 5 μm and a typical device may contain a 0.1 μm CdS and $\sim$2 μm CdTe layers. The fabrication process for the complete solar cell also includes chemical treatment, post deposition heat treatment, chemical etching and metallization. The chemical treatment of the CdTe layer with $CdCl_2$ and the heat treatment in air at 450 °C for $\sim$20 min are crucial steps for obtaining the photovoltaic activity. This device was first fabricated by Basol (1984) and the observed photovoltaic effect was explained in terms of complete type conversion of the CdTe layer during annealing in air forming the active p–n junction at the n-CdS/p-CdTe interface. Although this original work produced an excellent device with a good scientific explanation to describe its action, unfortunately, this explanation has been accepted without further confirmation, over the past two decades. Research activities have been carried out on the basis of this assumed model and hence the development of this device has been delayed due to lack of proper exploration, independent analysis and understanding. Comprehensive work by the first author on metal/CdTe interfaces over the last two decades has shed light on this complex system and the following sections describe an alternative model to describe the action of this solar cell, the ways of further improving its performance and the latest advances following these suggested guidelines.

3. New model for glass/CG/CdS/CdTe/metal solar cell

This model follows the work on metal contacts to II–VI semiconductors as reported in a recent review article (Dharmadasa 1998). As a result of a large body of information, it has been shown that a Schottky barrier forms at metal/n-CdTe interface as summarized in the last diagram of the article which is reproduced as figure 2. This work was carried out on various n-type bulk CdTe materials, and the Schottky barrier formation is found to be governed by Fermi level pinning at one of the five possible discrete levels. These experimentally identified defect levels are situated in the band gap at 0.40 $\pm$ 0.04, 0.65 $\pm$ 0.02, 0.73 $\pm$ 0.02, 0.96 $\pm$ 0.04 and 1.18 $\pm$ 0.02 eV below the conduction band minimum. Depending on the history of the material, fabrication process and the metal contact used, the Fermi level pinning will take place at one of the above five levels. The high density of these local defect states can be found in the top surface layer with a thickness of a few 100 Å, and some of these defects coincide with the native defects found in the bulk material. The thickness of this modified surface layer depends on the surface treatment and etching

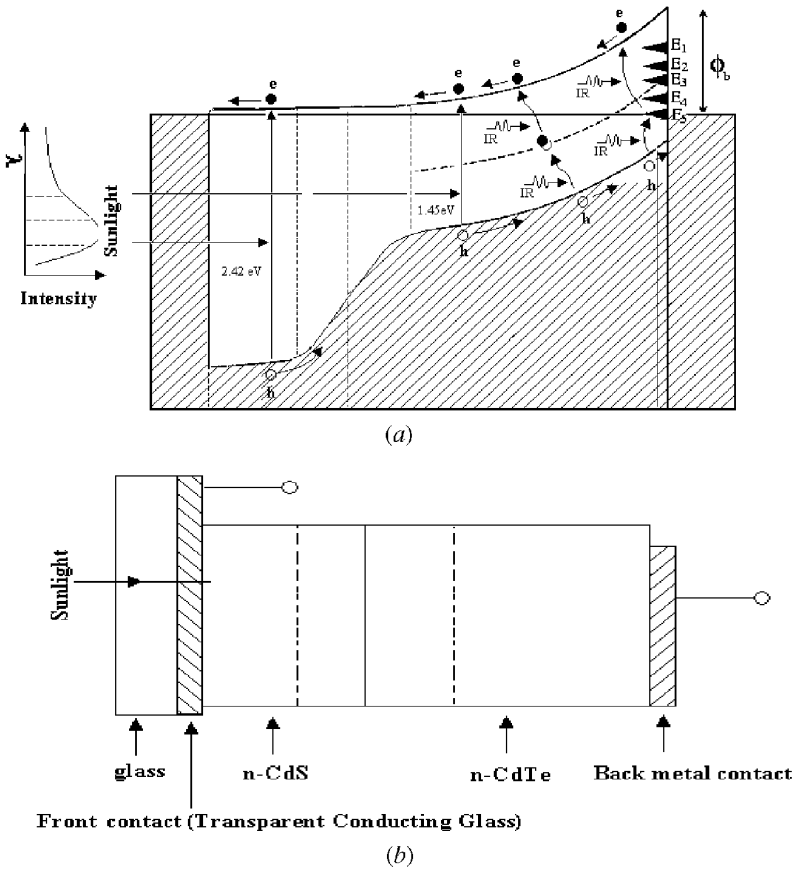

Figure 3. Energy band diagram and the material structure of the glass/CG/CdS/CdTe/metal solar cell based on the proposed alternative model. (*a*) Energy band diagram of an n-CdS/n-CdTe hetrojunction together with a large Schottky barrier at the back metal contact. (*b*) Materials used in the device structure. This model has been formulated using the complex results observed for metal/n-CdTe interfaces as summarized in figure 2. Although the photogeneration of charge carriers from different parts of the device is indicated with the help of the solar spectrum in the inset, the energy band diagram represents the thermodynamical equilibrium under dark conditions.

prior to metallization. Although this work was carried out in the past on bulk CdTe crystals, the principal author's subsequent work on electrodeposited CdTe thin layers has produced an identical picture as described in section 4.6. It is an astonishing property of CdTe that the same picture emerges from most of the published work in the literature, irrespective of the growth method used for production of CdTe layers.

When the glass/CG/CdS/CdTe/metal structure is fabricated using methods such as chemical bath deposition, closed spaced sublimation technique or electrodeposition, the energy band diagram of the device according to the new model takes the form shown in figure 3. The CdS layer is n-type and usually provides a better substrate than the conducting glass for growth of better quality CdTe material. During the annealing process intermixing of CdS and CdTe takes place forming ternary and/or quaternary compounds creating a graded band gap interface at the hetero-junction. Chemical treatments and the annealing process improve crystallinity of the semiconducting layers, form larger grains, remove unwanted defects in the material, passivate grain boundaries and bring the doping concentrations to moderate values in the range $\sim 10^{15}$–10^{17} cm^{-3}. The bulk of the CdTe layer remains n-type and the outermost layer contains high concentrations of defects responsible for Fermi level pinning at one of the five experimentally identified levels. The thickness of the top surface layer varies in the region of a few 100 Å, depending on the processing steps such as the heat treatment and etching procedure. If the Fermi level is pinned close to the valence band, at 0.96 ± 0.04 or 1.18 ± 0.02 eV below the conduction band minimum, a large Schottky barrier is formed at the metal/CdTe interface creating the required band bending across the device for photovoltaic activity. Then the top surface layer of the CdTe material can be considered as a p-type layer, since the Fermi level is close to the valence band maximum. The final device can be completely or partially depleted depending on the doping concentration achieved for the CdTe layer during growth and subsequent processing. As the energy band diagram shown in figure 3 indicates, the internal electric fields near the hetero-junction and the metal/CdTe interface add up and this becomes a tandem solar cell. If there is good alloying at the CdS/CdTe interface during the annealing process, the device structure is effectively a multilayer graded band gap tandem solar cell capable of absorbing a major part of the solar spectrum.

This new model has been formulated mainly using experimental evidence collected over the years. The possible band discontinuities and energy spikes at hetero-junctions have

been neglected for two main reasons. The first reason is the negligible effect of spikes at hetero-junctions when strong band bending is present in the device structure. The second reason is that the intermixing of materials used in the device structure removes energy spikes at the material boundaries and produces gradual changes in band gaps of intermediate phases. The presence of $CdS_xTe_{(1-x)}$ alloys in the device structure has been shown experimentally using photoluminescence and electroluminescense (Potter *et al* 2000), and also by x-ray diffraction and energy dispersive x-ray spectroscopy studies (Terheggen *et al* 2001) in the past. Jeagermann and co-workers (Fritsche *et al* 2001) have carried out a comprehensive and systematic study of the band off-sets at hetero-junctions involved in this device. Their findings using photoemission experiments are very similar to the band diagram proposed in this model excepting the most crucial Fermi level pinning situation at the n-CdTe/metal interface.

Under optimum conditions, such a device structure may produce large currents in excess of the theoretically predicted maximum current density of $\sim$25 mA cm^{-2} (Loferski 1956, M'baye 1980) for a p–n junction solar cell based on a single band gap of CdTe. In addition, this solar cell structure acts as an impurity photovoltaic cell creating electron-hole pairs by making use of defect levels within the bulk of the CdTe and at the CdTe/metal interface. Photons with energy less than the band gap (1.45 eV) are therefore able to create electron-hole pairs as shown in figure 3. In this case, since there is a strong electric field for charge carrier separation within the device, recombination and generation centres are favourably used to create more charge carriers to produce a higher current in the external circuit. According to this new model, conducting glass forms an ohmic contact to n-CdS and the back metal contact forms a large Schottky barrier at the metal/CdTe interface. In contrast, the currently assumed p–n junction model requires a completely opposite, ohmic contact at the back metal/CdTe interface.

4. Description of observed experimental results in terms of the two models

4.1. Current–voltage (I–V) measurements

When sunlight enters through the glass/CG side, the photogenerated charge carriers are created within the semiconducting layers, separated by the internal electric field and collected to create an electric current in the external circuit. In both models, electrons flow towards the conducting glass and holes flow towards the back metal contact making the CG layer negative and the metal contact positive in polarity. Both models produce similar polarity making it unnecessary to think differently from the already assumed p–n junction model.

4.2. Capacitance–voltage (C–V) measurements

According to both models, C–V measurements are possible due to the presence of at least one active interface within each device structure. If the device is fully depleted due to low doping concentrations of CdTe, in the region of 10^{15} cm^{-3} or below, capacitance values remain almost unchanged with the applied bias voltage and approximately equal to the geometric capacitance of the structure. If the doping concentration is such that the depletion region covers only a part of the CdTe layer, then the capacitance varies according to the applied bias voltage providing linear $1/C^2$ versus voltage plots and the estimated doping concentration lies in the range 10^{16}–10^{17} cm^{-3}. There are numerous examples of such C–V measurements in the literature and they demonstrate this behaviour giving doping concentrations in the range 10^{15}–10^{17} cm^{-3}. The work reported in (Raychaudhuri 1987, Chu *et al* 1988, Morris *et al* 1991, Das 1993) are good examples for devices with efficiencies close to 10%. Similar C–V observations could arise from both types of devices making it more difficult to distinguish between the two models applicable to this system.

4.3. Electron beam induced current (EBIC) measurements

There are various reports in the literature giving EBIC results for such devices with contradicting conclusions (Mitchell *et al* 1977, Nakayama *et al* 1980, Bhattacharya and Rajeswar 1985, Galloway and Durose 1995). This method should create a peak of EBIC at the junction area where the internal electric field is maximum. However, previous reports have shown peaks appearing at the CdS/CdTe interface, in the middle region of the CdTe layer and at the metal/CdTe interface, and therefore provide inconclusive EBIC results. In fact, if the device is fully depleted, the EBIC peak could appear at any place where the material quality is high and therefore the charge carrier collection is more efficient. The EBIC results reported in the past could be explained using both models for this device structure.

4.4. Results from electrical contacting work

Since the Schottky barrier at the metal/CdTe interface is determined by Fermi level pinning, almost any electrical contact shows the photovoltaic activity with different efficiencies for this device, provided the electrical contact used does not completely destroy the p-layer or the Fermi level pinning effect on the surface. For example, a metal such as Cu, a p-type dopant of CdTe helps to keep the Fermi level close to the valence band and hence produce a low resistance contact. This will provide good results for freshly made devices, but with ageing, Cu diffuses into the n-type CdTe region (i.e. beyond the surface p-layer) and forms a highly resistive layer due to self-compensation. Therefore, the device will rapidly deteriorate showing an increased contact resistance. However, a contact containing a small amount of Cu will reduce the contact resistance due to p^+-doping of the surface p-layer without getting into the n-CdTe region. For this reason Cu/Ni or Cu/Au contacts with less than $\sim$5% Cu should act as low resistance electrical contacts. If the device is a simple p–n junction, Cu should always produce a good ohmic contact to p-CdTe due to in-diffusion of this p-type dopant instead of forming highly resistive contacts with ageing. These experimental observations provide supporting evidence for the proposed alternative model, the p–n junction model fails to explain the results.

If group III elements such as indium or aluminium are used as the contact metal, photovoltaic activity may still be observed with a large series resistance and hence with

a very small fill factor. This is due to the compensation effect introduced by n-type dopants (In or Al) in the p-type CdTe surface layer. A series resistance of 2 MΩ has been observed for indium contacts, when copper containing contacts have shown only ∼50 Ω series resistance for 2 mm diameter devices (Dharmadasa *et al* 2002). In many situations, if the p-type surface layer is very thin and the interactions of indium and aluminium are considerable during the metallization step, the metal contacts completely consume the surface p-layer reaching the n-type CdTe producing an ohmic contact. In these situations, there is no photovoltaic activity observed for the device and the I–V curves show ohmic behaviour with low series resistance. These observations provide paramount information to move away from the p–n junction model and towards the proposed new model.

4.5. Doping of CdS and CdTe layers

The main improvement necessary in this type of device is the reduction of series resistance to increase the fill factor. Very thoughtful experiments have been carried out by some groups, on the basis of the assumed p–n junction model in the past, and the reports can be found in the literature (Dennison 1994). A typical device contains about 2 μm thick CdTe and a negligibly thin (0.05–0.10 μm) CdS layer grown on the conducting glass substrate. Therefore, the main body of this device contains CdTe, and if this material is assumed to be p-type, the most sensible doping is with a p-type dopant in CdTe to reduce the resistance. Both Na and Cu are well-established p-dopants in CdTe (Zanio 1978), and these elements have been added with fine control to the CdTe layers. The most unexpected results were observed with an improved shunt resistance, increased series resistance of the diodes and hence a drastic reduction of the efficiency mainly due to loss in the fill factor. This clearly shows that the main body of n-type CdTe material becomes resistive due to self-compensation during doping with p-type dopants such as Na and Cu. This experimental evidence strongly supports the new model proposed in this paper, and cannot be explained using the assumed p–n junction model.

The positive effects on device performance by 'magical' $CdCl_2$ treatment of both CdS and CdTe layers have been puzzling researchers during the past two decades (Basol *et al* 1986). In this $CdCl_2$ treatment, according to the new model, chlorine clearly helps the n-type doping of both semiconductor layers reducing the series resistance and hence improving the fill factor drastically. This treatment also helps to keep the CdTe surface rich in Cd, which is necessary for producing high quality Schottky barriers at metal/n-CdTe interfaces (Dharmadasa *et al* 1989). There may also be other benefits such as the cementing effect of chlorine to form larger grains, but there are contradictory reports indicating substantial improvement of efficiency without observing any grain size improvements (Fritsche *et al* 2001). All previous reports do not even discuss this possibility of n-type doping of the CdTe layer by chlorine since all the explanations are based on the assumed p–n junction device model. It should be noted that chlorine is a well-established n-type dopant for CdTe material (Zanio 1978). This most crucial $CdCl_2$ treatment needed for drastic device improvement therefore provides strong supporting evidence for the new model.

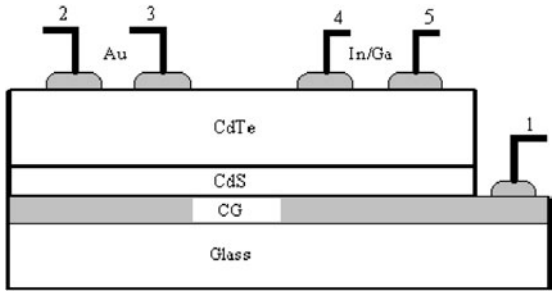

Figure 4. The electrical contacts used to identify the location of the rectifying interface. Au and In/Ga contacts are used side by side and In/Ga contacts have been heated using a sharp soldering iron tip to form ohmic contacts. The measurement results and conclusions are summarized in table 1. The CdS/CdTe device structures used to perform this experiment produced conversion efficiencies of approximately 10%.

4.6. Further experimental evidence to confirm the structure of the device

The observed results and interpretations presented in sections 4.4 and 4.5 provide strong supporting evidence for the proposed new model based on Fermi level pinning at metal/n-CdTe interface. The following experiments were carried out as a further test and for confirmation of the device structure.

Following the usual procedure to fabricate the device structure, Au contacts and In/Ga contacts were made side by side on the same sample as shown in figure 4. The In/Ga contacts were annealed using a fine soldering iron tip to consume the top surface layer and hence to form a good ohmic contact between In/Ga and n-type CdTe layer. Various contact combinations, as labelled in figure 4, were measured and the observations and conclusions are summarized in table 1.

The above measurements confirm the existence of a large Schottky barrier at the Au/CdTe interface and the non-existence of a considerable rectifying contact at the CdS/CdTe hetero-junction. Das and Morris' (1993) work on producing a better solar cell of 9.8% efficiency for ITO/SnO_2/CdTe/metal structure without CdS layer than a solar cell of 8.8% efficiency for ITO/SnO_2/CdS/CdTe/metal device with CdS layer is also noteworthy. This clearly indicates the rectifying contact required for photovoltaic activity is at the metal/CdTe interface rather than the CdS/CdTe hetero-junction. Our large body of subsequent measurements on glass/CG/CdS/CdTe/metal structures fabricated using electrodeposited materials also confirmed the Fermi level pinning at discrete levels (figure 5(*a*)). It is interesting to note exactly the same barrier heights observed for electrodeposited CdTe thin layers, as observed for metal contacts on bulk n-type CdTe (see figure 2). These different barrier heights appear for different batches of fabrication and their respective V_{oc} values also tend to produce values in discrete nature, as shown in figure 5(*b*). The V_{oc} values follow respective barrier heights since this parameter is a function of the barrier height. In order to produce high efficiency solar cells, the Fermi level should be pinned at either 0.96 ± 0.04 or 1.18 ± 0.02 eV level below the conduction band minimum.

Table 1. The summary of current–voltage measurements carried out between different electrical contacts made on the device as shown in figure 4, and the conclusions arising from these measurements. The CdS/CdTe device structures used to perform this experiment produced conversion efficiencies of approximately 10%.

Two contacts measured	Observations	Remarks
Measurements between (1 & 2) and (1 & 3)	Efficiency ∼10%. Rectifying contacts with reverse current of $\sim 10^{-7}$ A. Series resistance is ∼100 Ω	Good solar cells between Au and CG contacts
Measurements between (2 & 3)	Efficiency ∼0%, current in both directions are in the order of 10^{-7} A	Two Schottky diodes are back to back. Therefore the current measured is the reverse current of one of the diodes and there is no collection of charge carriers from this combination
Measurements between (1 & 4) and (1 & 5)	No photovoltaic activity and good ohmic currents are observed with series resistance of ∼80 Ω	Annealed In/Ga consume p-surface layer and make good ohmic contacts to n-CdTe layer. No considerable rectification at CdS/CdTe interface and therefore photovoltaic activity is minimal
Measurements between (4 & 5)	No photovoltaic activity and good ohmic currents with series resistance of ∼30 Ω are observed	In/Ga make ohmic contacts to n-CdTe and therefore conduction is through the CdTe layer
Measurements between (2 & 4) and (3 & 5)	Efficiency ∼10%. Rectifying contacts with reverse current $\sim 10^{-7}$ A. Series resistance is ∼40 Ω	In/Ga provide ohmic contact to n-CdTe and the rectifying contact is at the Au/CdTe interface

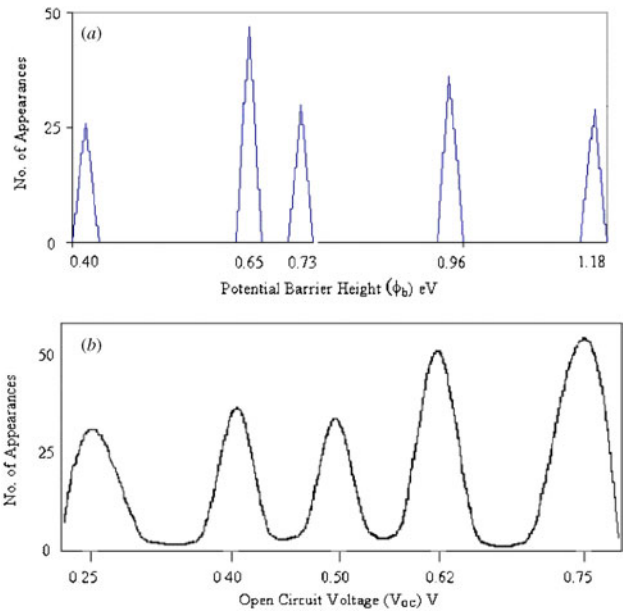

Figure 5. (*a*) The barrier heights obtained from dark current–voltage measurements for glass/CG/CdS/CdTe/metal solar cells, fabricated with electrodeposited CdS and CdTe thin layers. Note the observation of discrete barrier heights with a remarkable agreement with results obtained for bulk n-CdTe/metal Schottky diodes as summarized in figure 2. (*b*) The V_{oc} values under illumination also follow the same discrete trend and the vertical axes indicate the number of observations.

5. The way forward for further development of CdS/CdTe solar cell

The results reported in the literature (Dharmadasa 1998) combined with our unpublished results enabled us to put forward this alternative model, and hence the following main steps should allow further improvement of this solar cell structure to achieve higher efficiencies.

5.1. Improvements to window material

The use of glass/CG substrates with lowest sheet resistance and the selection of a suitable n-type window material with required qualities will be a good starting point. Better crystallinity, lowest possible defects and the doping concentration close to 10^{16} cm^{-3} will be desirable for the window material. In the case of n-CdS, the doping of the material with group III elements or group VII elements will enhance the electrical conductivity of the films. However, the introduction of some of these elements will disrupt the crystallinity reducing the mobility of charge carriers and hence reducing the required electrical conductivity. Obtaining the optimum electrical conductivity is a challenging task but every positive step will contribute to the enhancement of the device performance. The $CdCl_2$ treatment of the CdS layer has already shown the positive effects of doping with chlorine.

5.2. Improvements to absorber material

The absorber layer (CdTe) of the order of ∼2 μm thickness should have the desired semiconducting qualities such as better crystallinity, larger grains, grain boundary passivation, minimum possible recombination and generation centres and the lowest possible background impurities. The material layer should retain n-type electrical conduction and hence the ideal dopants will be group III or group VII elements. Achievement of doping concentrations in the desired region of $\sim 5 \times 10^{15}$–5×10^{17} cm^{-3} will be ideal for this device structure.

Many factors contribute to this ultimate doping concentration, and hence to achieving the optimum electrical conductivity for this layer. This requires systematic experimentation on materials growth, impurity identification and removal, doping and processing steps including heat treatment. The processing steps including chemical treatments with cadmium halide solutions, heat treatment in air and wet etching process should produce a CdTe layer with optimum n-type properties together with a p-like surface layer of the order of a few 100 Å, to achieve the Fermi level pinning close to the valence band maximum.

5.3. Improvements to back metal contact

For an efficient solar cell device, the Schottky barrier height should be either ∼0.96 or ∼1.18 eV for this system. The formation of lower barriers results in poor performance due to weak band bending or weak internal electric field created by the lower Schottky diode. Selection of a metal contact containing a small amount of p-type dopant such as Cu or Sb support the Fermi level pinning close to the valence band producing an efficient solar cell. Hence the Cu/Au, Cu/Ni or Sb containing contacts are good candidates to produce low resistance contacts to this device structure. However, the in-diffusion of a p-type dopant into the n-type CdTe layer should be avoided in order to eliminate the formation of a very resistive electrical contact with ageing. When this happens, and the efficiency drops down considerably, it should be possible to remove the entire back contact using chemical etching and reproduce the working device again if there is no damage to the thin-film structure. This procedure should re-produce the high efficiency devices again and our work has indeed confirmed this observation (Dharmadasa *et al* 2002). Introduction of a p-type thin semiconducting layer with a band gap larger than that of CdTe (e.g.: ZnTe), or Sb containing layers such as Sb_2Te_3, will protect the p-type top surface layer from reactions with metal contact, improving both the efficiency and the durability of the device. Romeo *et al* (1999) have indeed shown the positive effects of Sb_2Te_3 incorporation at the back metal contact. A suitable conducting polymer layer with p-type conduction and a band gap greater than that of CdTe will be an ideal candidate for this purpose to produce inorganic/organic hybrid devices and to increase both the efficiency and the lifetime of this solar cell. Another way of improving both the performance efficiency and the lifetime is by forming an MIS (metal-insulator-semiconductor) type contact with ultra thin insulating layer (Roberts *et al* 1981). Inorganic compounds such as CaF_2 and SrF_2 or any other insulator will be suitable for this purpose. There is an added value of this approach in the associated pin hole plugging of the device structure improving the yield of the device fabrication process.

5.4. Multilayer graded band gap approach

The introduction of a third layer with an intermediate energy band gap will enable strengthening and smoothing of the slope of the energy band diagram which is the internal electric field, in order to enhance the charge carrier collection. The energy band diagram of such a device is shown in figure 6, and CdSe, with an intermediate band gap of 1.70 eV, would be an ideal candidate since the element Cd is common for all three semiconductors used. During annealing treatments, the intermixing at hetero-junctions will take place and the device structure will become a graded band gap multilayer tandem device with better collection efficiencies. These devices will improve at their hetero-junctions with ageing and absorb a major part of the solar spectrum due to effective utilization of photons at different regions of the device structure. The photons in the infrared region with energy less than 1.45 eV are also utilized within the CdTe layer and closer to the back metal contact, as shown in figure 6, to create photogenerated charge carriers. These carriers will be collected efficiently, with the existing high internal electric field in these thin-film device structures. Since the theoretical efficiency predicted for this type of devices is ∼84% (Green 2001), the future potential of this device is extremely high.

6. Summary of our latest results

Our current efforts are devoted to the points raised in sections 5.1 to 5.4, in order to increase the device efficiencies. To test these new ideas and develop the solar cell, the CdS layer was deposited using chemical bath deposition and the CdTe layer was electrodeposited at 160 °C to improve the crystallinity (Carlos *et al* 1996). In addition to crystal structure improvements, the layers were doped with an n-type dopant, iodine, to improve the electrical conductivity. The following sections briefly describe the methods used and the achieved results.

6.1. Growth of CdS by chemical bath deposition

CdS films required for this solar cell were prepared by chemical bath deposition (CBD) technique. A typical bath contained 0.02 M $CdCl_2$, 0.07 M NH_4Cl and 0.14 M thiourea. All chemicals used were analytical grade of purity more than 99.9% and dissolved in milli-Q water. Ammonia solution was used to adjust the pH value of the bath to 9.5. The solution was continuously stirred during the coating at the temperature of 90 °C. After a deposition period of 15 min, the films were immediately cleaned ultrasonically in warm water, and dried in a stream of nitrogen gas. After complete drying, these layers were annealed at 450 °C for 20 min in ambient air in order to increase the electrical conductivity. The thickness of the resultant films was of the order of 0.1 μm.

6.2. Electrodeposition of CdTe films from non-aqueous medium

CdTe thin films were cathodically electrodeposited on to glass/CG/CdS substrates at 160 °C using a non-aqueous electrolytic bath. The CdS surfaces were etched in a dilute NaOH + $Na_2S_2O_3$ solution prior to CdTe deposition. The ethylene glycole containing 1 M $CdCl_2$, 200 ppm $TeCl_4$ and 0.05 M CdI_2 was used as the electrolytic bath. All chemicals used were analytical reageant grade of purity more than 99.9%. CdTe films of ∼2 μm thick were deposited in about 1.5 h while

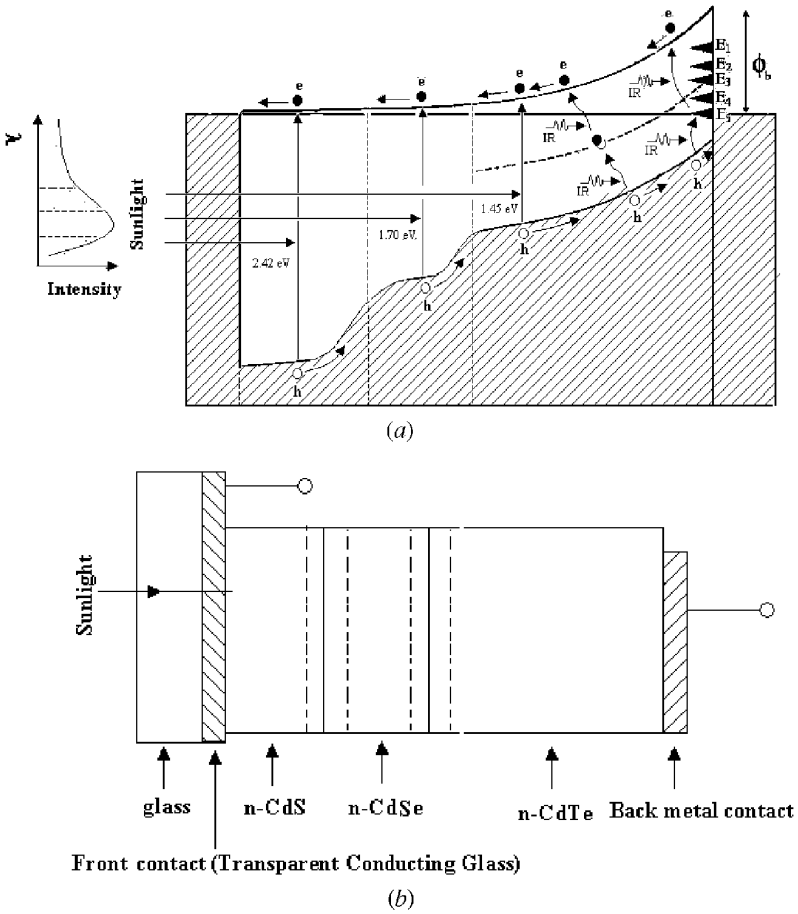

Figure 6. The energy band diagram of the 3-layer glass/CG/CdS/CdSe/CdTe/metal solar cell with an intermediate CdSe layer. (*a*) Energy band diagram of the multilayer device structure. (*b*) Materials used in the device structure. During annealing and ageing process, this structure becomes a multilayer graded band gap tandem solar cell due to intermixing of materials at two hetero-junctions. If there are no other detrimental effects within the device, this solar cell structure should improve its energy conversion with time. Although the photogeneration of charge carriers from different parts of the device is indicated with the help of the solar spectrum in the inset, the energy band diagram represents the thermodynamical equilibrium under dark conditions.

the solution is stirred continuously. A standard three electrode system was employed using saturated calomel electrode or metallic tellurium as a reference electrode, glass/CG/CdS as the working electrode (cathode) and graphite (carbon) plate as the counter electrode, all dipped into the electrolytic bath. A computerized Gillac ACM instrument was used for the deposition of CdTe film. Both iodine and cholorine present in the bath are n-type dopants to CdTe and hence increase the electrical conductivity of the layers. The deposited layers were dried, annealed at 400 °C for 20 min in air after $CdCl_2$ treatment, chemically etched in NaOH + $Na_2S_2O_3$ solution and metallized with Au to complete 1 mm diameter small devices.

6.3. Device characterization results and discussion

The completed glass/CG/CdS/CdTe/Au devices were characterized using *I–V* and *C–V* techniques to study the solar cell parameters. The *I–V* curves measured under dark conditions are shown in figures 7(*a*) and (*b*). The rectification factors as defined by I_F/I_R at 1.0 V, for best devices show over 4 orders of magnitude. It should be noted that to achieve over 12% efficiencies from this system, only 3 orders of magnitude rectification factor is sufficient (Dharmadasa *et al* 2002). The barrier heights extracted from the diodes which show ideality factors less than 1.40, provide potential barrier height values close to 1.18 eV, which is the desired Fermi level pinning position closest to the valence band maximum. Both the ideality factor and the potential barrier height values were evaluated using the standard method established for characterization of Schottky contacts (Rhoderick and Williams 1988).

A typical *I–V* curve under AM1.5 illumination for our latest devices is shown in figure 7(*c*). The V_{oc} over 600 mV, and fill factors about 0.60 are typical values obtained for these devices but the J_{sc} over 60 mA cm^{-2} is strikingly high as expected for a multilayer graded band gap tandem solar cell device. The above parameters produce efficiencies of ∼18%, which is above the highest value 16.5% (Wu *et al* 2001) reported to date and the work is under way to further improve the performance efficiency of this device structure.

The capacitances of the above structures were measured as a function of applied bias voltage, at a measurement frequency of 1 MHz. The results are shown in figure 8, and the device

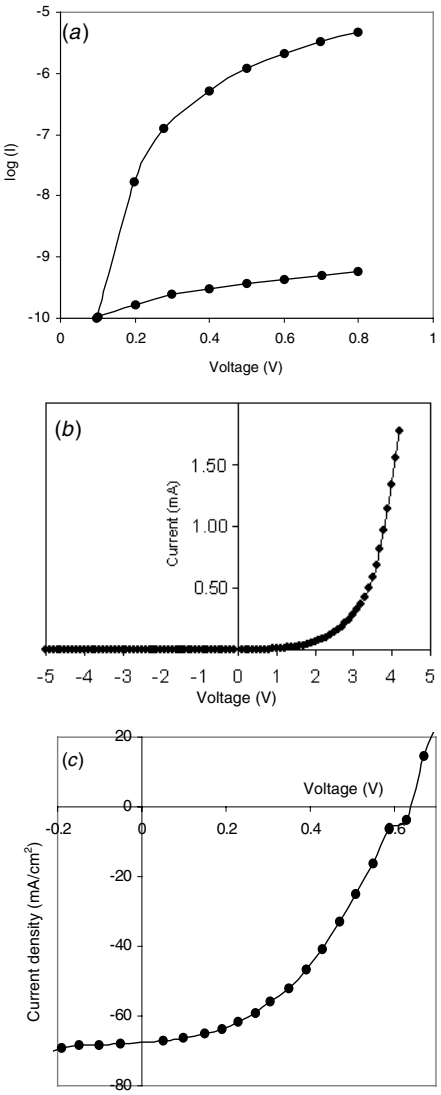

Figure 7. The current–voltage curves obtained under dark (*a*) and (*b*), and illuminated (AM1.5) (*c*) conditions for the improved devices fabricated following the ideas of the proposed new model. Note the barrier height of 1.18 eV due to the Fermi level pinning close to valence band maximum and the high J_{sc} over 60 mA cm^{-2}.

capacitance remains unchanged at ∼56 pF with the applied voltage. It is therefore evident that the depletion width of the device structure is greater than the combined thickness of CdS/CdTe layers. In other words, the device structure is fully depleted and therefore the complete semiconductor layers are photovoltaic active. The calculated geometrical capacitance of the 1 mm diameter contact is about 40 pF (assuming $\varepsilon_r = 11$ for CdTe and the thickness of the device is 2 μm), and comparable to the measured value of ∼56 pF. Because a constant capacitance of the same order as the geometrical capacitance is observed, further parameters such as potential barrier height or doping concentration cannot be extracted from conventional Schottky–Mott plots. This however, indicates the low doping concentrations below $\sim 10^{15}$ cm^{-3} in the CdTe layer, producing a wider depletion width greater than the complete device thickness.

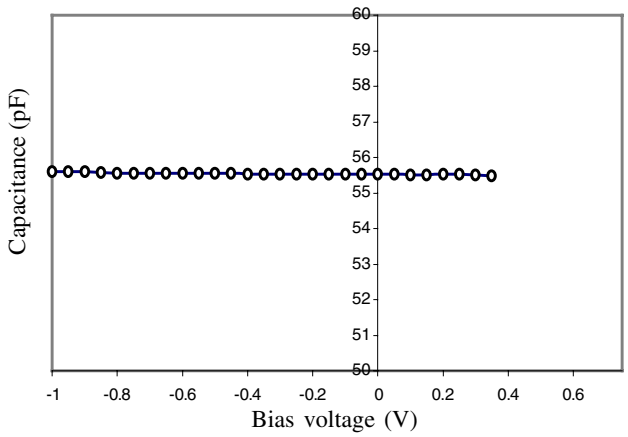

Figure 8. The capacitance of glass/CG/CdS/CdTe/Au solar cells observed at 1 MHz measurement frequency as a function of bias voltage. Note the constant capacitance value of ∼56 pF due to the presence of a fully depleted solar cell device.

A remarkably high short-circuit current density observed for this multilayer graded band gap tandem solar cell needs a detailed discussion. The theoretical calculations carried out for p–n junctions of single band gap materials show a maximum possible current density of ∼25 mA cm^{-2} (Loferski 1956, M'baye 1980). However, when two or more band gaps are present in the device structure, and two or more active junctions are added to enhance the internal electric field of the device, the situation is completely different. The number of photons absorbed increases rapidly without heating the device due to the presence of several band gap materials and the separation and collection efficiency increases due to enhancement of the internal electric field. In device structures described in this paper, the window material has a band gap of 2.42 eV (CdS) and the absorber material has a band gap of 1.45 eV (CdTe). In addition, there are intentionally added layers such as CdSe (1.70 eV) or varying band gap material layers consisting of alloys between CdS and CdTe formed during fabrication. Similar current densities of ∼70 mA cm^{-2} for multilayer CIGS solar cells (Dharmadasa *et al* 2002) and silicon solar cells (Li *et al* 1992) have also been observed. Li and co-workers reported a current density of 69.1 mA cm^{-2} for silicon solar cells processed by proton bombardment of the silicon surface. Strong inclusion of hydrogen into the silicon lattice and the formation of a wider band gap layer to form a graded band gap device structure during this process may be a possibility. The visible light emission from porous silicon reminds us of the possibility of formation of wider band gaps when the silicon crystal lattice is disturbed. These experimental observations of short-circuit current density values of over 60 mA cm^{-2} for all three major solar cells based on silicon (Li *et al* 1992), on CdTe (Chaure *et al* 2002) and on CIGS (Dharmadasa *et al* 2002) invite the theoretical PV community to calculate solar cell parameters for multilayer graded band gap tandem solar cells. Henry's (1980) calculations for a 36-layer solar cell structure producing a maximum efficiency of 72% for 1000 sun illumination is a good example and these experimental results urge the need for such theoretical work for newly designed solar cell structures. Recent

calculations by Dhingra and Rothwarf (1996) lead the way for accurate evaluation of theoretical parameters. The power density of the solar simulator used may vary slightly from laboratory to laboratory, but these experimentally observed and consistently high short-circuit current densities show the potential for rapid development of these types of devices.

7. Conclusions

The large body of experimental evidence available in the literature and the authors' work enabled the identification of an alternative model for the device structure, glass/CG/CdS/CdTe/metal, solar cell. This new model explains the device behaviour in terms of a combination of a hetero-junction and a large Schottky barrier at the CdTe/metal interface. The materials growth, chemical and heat treatments and wet chemical etching provide the right condition for the Fermi level pinning at one of the five experimentally identified energy levels (0.40 ± 0.04, 0.65 ± 0.02, 0.73 ± 0.02, 0.96 ± 0.04 and 1.18 ± 0.02 eV) at the metal/CdTe interface. To produce an efficient solar cell structure, the Fermi level should be pinned close to the valence band maximum (i.e. at 0.96 ± 0.04 or 1.18 ± 0.02 eV). Since both materials in the device structure remain n-type, this device can be treated as an n-n-Schottky barrier structure. The appropriate doping and improvements to metal contacts help the further development of this device from present achievements. The current devices fabricated in the authors' group show typical values of V_{oc} over 600 mV, fill factors about 0.60 and J_{sc} over 60 mA cm^{-2} which indicate remarkable improvements in the short-circuit current density indicating the possibility of achieving higher efficiencies in the future.

The impact of various features of this model on the efficiency of the cell is considerable. The ability to obtain Fermi level pinning near to the top of the valence band enables production of a barrier height of 1.18 ± 0.02 eV. This enables a high open circuit voltage to be achieved, since V_{oc} is a function of the potential barrier height. Since this is a metal/semiconductor (MS) type rectifying contact, the introduction of a thin insulating layer to form metal/insulator/semiconductor (MIS) type structure enables further enhancement of V_{oc} and the lifetime of the device. The main reason for degradation of this device is the intermixing at CdTe/metal interface, but the insulating layer in this case acts as a reaction barrier to improve the lifetime of the device. Since both window and absorber materials are n-type, doping with n-type dopants (according to the new model) instead of p-type dopants (according to the old model) will improve the electrical conductivity of the device structure to enhance both the short-circuit current density and the fill factor and hence enable the achievement of high efficiencies. In addition, this model would also explain the 'magic step' of empirical $CdCl_2$ treatment necessary for achieving high efficiencies. According to this new model, chlorine acts as an n-type dopant to both n-CdS and n-CdTe materials reducing the series resistance in addition to observed grain growths to enhance device parameters. The improved understanding of physics behind this device will enable the PV community to further develop this device rapidly in the future.

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