Electronically active layers and interfaces in polycrystalline devices: Cross-section mapping of CdS/CdTe solar cells

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Electronic mapping of cross sections of a polycrystalline device, the *n*-CdS/*p*-CdTe solar cell, show that the photovoltaic and metallurgical junctions coincide to within experimental resolution (50 nm), which rules out both type conversion of CdS and buried homojunctions. Compositional analysis of the CdS supports this. Mapping was done using scanning capacitance, complemented by scanning Kelvin probe microscopy. Our results explain why a high-resistance transparent conducting oxide layer is needed as contact to the CdS for successful device operation. They define limits on inputs for modeling performance of these devices. © *2003 American Institute of Physics.*
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Electronic mapping of device cross sections (XS) is a direct way to determine the location of internal junctions and fields, and to identify otherwise inaccessible subsurface layers and features. This can reveal the microscopic origin of macroscopic device behavior, relevant for thin-film devices made with polycrystalline materials. While such devices are expected to be electronically inhomogeneous, some, such as thin-film solar cells, show performance superior to that of their single-crystal counterparts. To understand this, we turned to high-resolution characterization of such a device.

Scanning probe microscopy requires minimal sample preparation and can be performed in ambient. We characterized XS of polycrystalline *n*-CdS/*p*-CdTe solar cells electronically, without topography-related artifacts, by use of scanning capacitance microscopy (SCM), complemented by scanning Kelvin probe microscopy (SKPM).[1] We succeeded in identifying the electronically active interfaces, especially the photovoltaic junction, and in characterizing the thickness and nature of the layers that form the junction.

These issues are important because the position of the metallurgical junction, defined by a change in overall chemical composition, and that of the electronic junction, defined by the change in electrical properties, do not need to coincide. Whether they do or not has direct implications for the mode of action of the cell and possibilities for its optimization. In the CdTe/CdS cell Te (from CdTe) and Cu (from the cell's back contact), both found throughout the CdS layer,[2,3] may, at sufficiently high concentrations, type-convert CdS.[4,5] Furthermore, S diffusion into the CdTe may type-convert part of the *p*-CdTe. Both effects would lead to a buried homo- rather than a heterojunction. Within our experimental uncertainty ($\sim$50 nm, *vide infra*) our results show the cell to be a heterojunction, with no evidence for CdS type conversion. They also provide a clear scientific reason for using a bilayer transparent conducting oxide structure as appropriate contact to the CdS.

SCM allows high-resolution mapping of the charge carrier types and concentrations close to the surface. SCM resolution, commonly comparable to the tip radius,[6] is, in our case, estimated to be $\sim$50 nm, the width of the tip's apex. In SKPM, a noncontact atomic force microscopy (AFM) method, a conductive tip serves as a Kelvin probe to measure the surface potential, or, more accurately, the local contact potential difference (CPD, the difference between tip and sample work functions). CPD is plotted as a function of tip position, creating a surface potential map.[1]

Most CdTe/CdS cell structures (without contact to CdTe) used were from University of South Florida (USF). For comparison, structures from First Solar, LLC were also studied. USF structures were on 7059 glass, coated with 700–1000 nm transparent conductive oxide made of a bilayer of low-resistance (LR) SnO_2:F, deposited directly on the glass, followed by high-resistivity (HR) SnO_2. Polycrystalline *n*-CdS (60–100 nm thick) was deposited on the HR SnO_2 from a chemical bath, followed by closed-space sublimation of the polycrystalline *p*-CdTe layer (3–7 μm thick) and $CdCl_2$ treatment at 400 °C.[7] First Solar structures were on soda-lime glass, coated by 450 nm SnO_2:F (Libby Owens Ford, TEC 15). Three hundred nanometers of CdS were deposited by vapor transport on the SnO_2:F, followed by vapor deposition of 3.5–4 μm of CdTe. These structures were $CdCl_2$-vapor-treated at 420 °C.[8]

Samples were prepared by fracturing the cell structures with the CdTe film under tensile stress, to achieve relatively flat XS.[9] The obtained XS was not smoothed further, either mechanically or chemically, so as not to introduce extraneous surface defects that might affect the electronic properties. For SCM, samples were stored in room ambient for 48 h to grow the insulating oxide on the CdTe part of the XS ($\sim$4 nm thick oxide).[10] No insulating oxide is expected to grow on SnO_2 and CdS,[11] leading to a semiconductor/metal configuration for tip/surface contact. Samples were biased via the SnO_2. The CdS layer composition was determined

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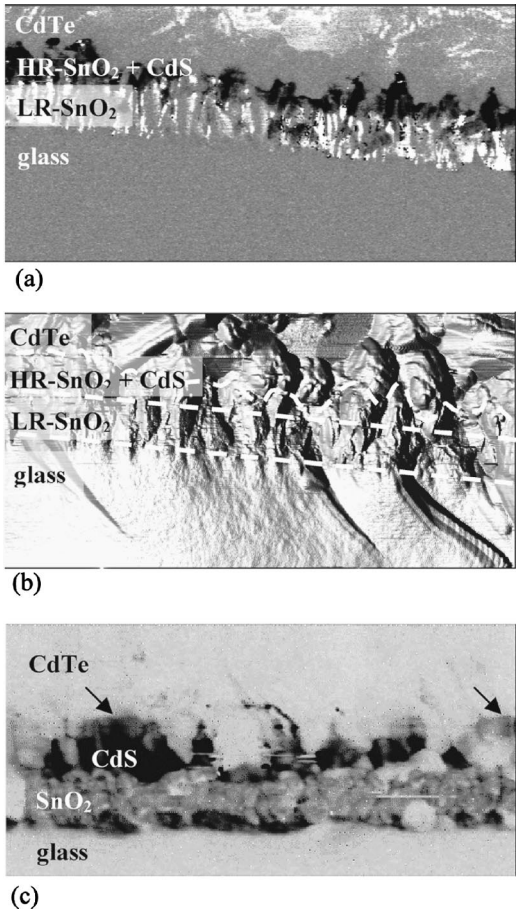

FIG. 1. (a) SCM image of a USF CdS/CdTe cell cross section (after contacting with a Cu-containing graphite paste). (b) AFM topography image of the same cross section, taken simultaneously. The contrast is enhanced by ''illumination'' from the left-hand side. Dashed lines indicate the borders of the layers, as deduced from the SCM image (a). (c) SCM image of a First Solar cell cross section. The CdS layer appears discontinuous, probably due to small fragments of CdTe (from the fracture) covering the CdS. Arrows indicate two isolated groups of type-converted CdTe grains. Scan sizes: 2 μm$\times$4 μm; tips: $PtIr_5$-coated Si (Nanosensors). Ac bias: (a) 1 V, (c) 2 V, at 90 kHz; $V_{DC}=0$. The layers are identified on the images. SCM measurements were made in air on a *Dimension 3100* (DI-Veeco, Santa Barbara). Its parameters were such that positive signals (brighter than a reference level) correspond to *p*-, and negative (darker) signals to *n*-type material and zero signal indicates conducting or insulating material. SCM measurements were found to be almost unaffected by topography.

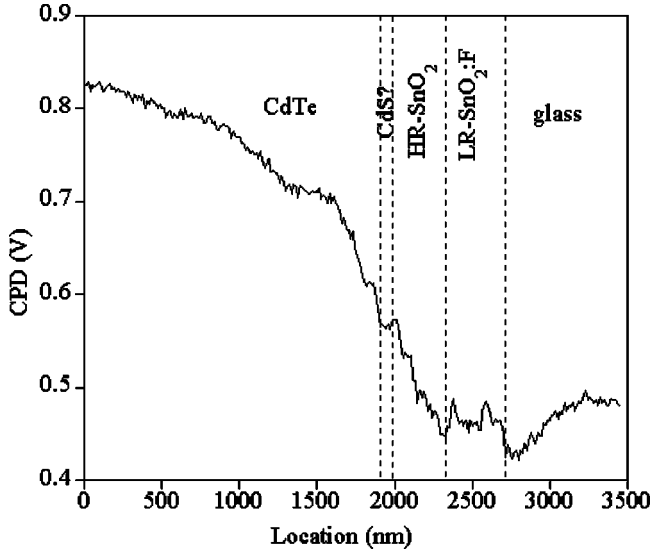

FIG. 2. SKPM line scan taken across a CdTe/CdS cell, with no external bias. The layers' locations were determined from the corresponding topography scans (not shown). SKPM measurements were performed in air on a *P47 Solver Scanning Probe* microscope (NT-MDT, Zelenograd). The ever-present topography effect on SKPM signals is minimized by making the measurements in a two pass technique, at increased tip–surface distance.

with high-resolution ($<$50 nm) Auger electron spectroscopy (AES) on the sample XS, and with secondary ion mass spectroscopy (SIMS) after removing both the back contact by chemical etch and the CdTe layer by sputtering.[12]

The XS SCM image of a USF cell clearly shows the layer sequence in the cell [Fig. 1(a)], with the two-layer SnO_2 structure. The unstable, noisy signal from the LR layer (SnO_2:F) adjacent to the glass substrate is probably related to unwanted current flow in the capacitance sensor circuit, due to high conductivity and lack of a surface dielectric layer, resulting in erroneous SCM results. The LR layer thickness is 300–500 nm.

The adjacent *n*-type layer (dark under any dc bias between -2 and $+2$ V) consists of both the HR SnO_2 and the CdS layer, *which are electronically indistinguishable* [Fig. 1(a)]. Although part of this layer should be depleted, with carrier concentration below the SCM detection limit, it is reasonable to assume that this part's thickness is below the SCM lateral resolution.[13] The *n*-type layer's thickness varies from 150 to 250 nm, due to irregular fracture, which yields a discontinuous CdS layer, as seen in scanning electron microscope XS images (not shown). To check if both HR SnO_2 and CdS are included in the observed *n*-type layer, we measured similar structures without the CdS layer (not shown). These gave a layer sequence similar to that of a conventional cell, but with a 50–80 nm thinner *n*-type layer, adjacent to the CdTe. Conversion of the CdS to *p*-type is excluded by AES, which shows a Te/S ratio in the CdS layer of $\leqslant 0.6$, while a ratio of at least 0.8 is needed for thin-film CdS-type conversion.[4] SIMS of similar cells (with Cu-containing back contact) showed 1.5×10^{20} Cu atoms/cm^3 in the CdS. While this will reduce CdS conductivity, it cannot type-convert it.[14]

XS-SCM of First Solar structures [Fig. 1(c)] reveals a 100- to 180-nm-thick *n*-SnO_2 layer on top of the glass substrate, probably from the commercial manufacturing process. Its affect on cell operation is minimal, since the photocurrent flows through the high-conductivity SnO_2 to the external circuit. This layer is covered by 350 ± 30 nm high-conductivity SnO_2 (with negative or zero SCM signal). The CdS layer (200–300 nm thick) is clearly distinguishable from the SnO_2 and gives a dark *n*-type signal. This larger CdS thickness (compared to USF) makes an HR SnO_2 layer here probably superfluous for good cell performance. No *p*-type signal is found in the CdS layer. Therefore, there is no type conversion of the CdS in these samples either.

The SKPM profile without external bias of a USF sample (Fig. 2) shows the change in CPD between the different layers, expected from their different work functions.[15,16] The total CPD change, from the CdTe to the SnO_2, is smaller than expected from their work function difference. This could be due to the photovoltage induced by illumination from the AFM detection laser (670 nm, $\sim$2 mW), or to CdTe surface oxidation and Fermi-level pinning.[17] The small CPD changes within a given layer are

caused by the convolution with rough topography features of the XS. The higher CPD of the thin CdS layer, relative to that of the HR SnO_2, is unexpected. It is probably an artifact of averaging effects with the other layers, caused by long-range electrostatic forces. As SKPM shows a voltage drop across the HR SnO_2, even with no corresponding topography features, this indicates that this layer supports the junction band-bending/open-circuit voltage (*vide infra*).

We conclude that, contrary to what has been suggested recently,[18] CdS in CdTe/CdS solar cells is not type converted. To support the high open-circuit voltage, the *n*-type layer must have some minimal thickness (around 300 nm in the cells studied here). The role of the HR (conductive) oxide that replaces part of the CdS is to improve the cell's blue response, due to its larger bandgap. A thin CdS layer is still needed to provide a photovoltaic junction with low defect concentration and high open-circuit voltage.[19] Indeed, there are several examples of high-efficiency cells with such an HR buffer layer.[7,20] Particularly, the HR SnO_2 is thought to make good electrical contact to CdS, due to alignment of the conduction band minima.[21]

The SCM maps (and line scans, not shown) demonstrate that, generally, the cell junction is located at the metallurgical junction (within the SCM accuracy; here ~ 50 nm), as seen by comparing corresponding SCM and topographical images (Figs. 1(a) and 1(b)). The gradual disappearance of the dark *n*-type signal 10–20 nm beyond the CdS layer into the CdTe, seen in some CdTe grains, is due to the limited SCM resolution. No evidence for a buried homojunction is found in First Solar structures either.

A layer of CdTe grains with very weak (almost no) SCM signal is seen adjacent to the HR SnO_2/CdS layer in the USF samples, 200–350 nm thick. We interpret these to be recrystallized and regrown CdTe grains, due to cell processing, in agreement with earlier transmission electron microscopy data.[22] Type conversion of this CdTe layer is not expected as the highest S concentration found at the CdTe/CdS interface is 10 at. % or less,[2,23] while type conversion will occur only above 22.5 at. % S.[4] The SCM signal shows clear *p*-type behavior further into the CdTe layer [Fig. 1(a)]. No such well-defined recrystallized layer is seen in First Solar samples. In some places, a few *n*-type grains, with 100–150 nm diameter, are seen adjacent to the CdS layer [see Fig. 1(c)]. While we cannot exclude that these might possibly be type-converted CdTe grains, this cannot be taken as an indication for a buried homojunctions, because these grains do not form a continuous layer.

To conclude, type conversion of CdS in CdTe/CdS solar cells was disproved. CdS and the high-resistance SnO_2 layer in USF cells were found to be electronically similar, rationalizing the need for a HR layer in cells with very thin CdS for supporting the junction photovoltage, without reducing the cell's blue response. Most importantly, combined XS SCM and SKPM of CdTe/CdS cells show that the photovoltaic and metallurgical junctions coincide. As this is found in CdTe/ CdS cells from two different sources, it appears to be a general property of such cells.

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