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CdTe thin film solar cells: device and technology issues

C.S. Ferekides *, U. Balasubramanian, R. Mamazza, V. Viswanathan, H. Zhao, D.L. Morel

University of South Florida, Department of Electrical Engineering, Clean Energy Research Center (CERC), 4202 E. Fowler Ave., Tampa, FL 33620, USA

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Abstract

Polycrystalline thin film CdTe continues to be a leading material for the development of cost effective and reliable photovoltaics. Thin film CdTe solar cells and modules are typically heterojunctions with CdS being the n-type partner, or window layer. The preferred configuration for CdTe solar cells is the superstrate structure. The cadmium chloride heat treatment, the back contact formation process, and the utilization of resistive, buffer layers in tandem with a thin cadmium sulfide window layer, are important areas of research in thin film CdTe solar cells. This paper reviews work on CdTe thin film solar cells sponsored by the National Renewable Energy Laboratory. Results for a vapor chloride heat treatment with high throughput characteristics, a dry back contact process, and a comparative study of resistive buffer layers and their effect on the performance of CdTe solar cells are presented.

Keywords: CdTe-1; CdS-2; Thin films-3; Transparent conductors-4

1. Introduction

Cadmium telluride continues to be a leading candidate for the development of cost effective photovoltaics for terrestrial applications. The two key properties of this material are its near ideal band gap for photovoltaic conversion efficiency of 1.45 eV, and its high optical absorption coefficient. A thin film of CdTe with thickness of approximately 2 μm will absorb nearly 100% of the incident solar radiation. Another advantage of the CdTe technology is the flexibility with regards to the method of manufacture. Although to-date the highest reported efficiencies for CdTe laboratory devices have been achieved with the close spaced sublimation (CSS) process (Wu et al., 2001; Ohyama et al., 1997; Ferekides and Britt, 1994; Wu et al., 2002), several other technologies such as physical vapor deposition (PVD), electrodeposition (ED), and sputtering have also demonstrate the potential of achieving high performance levels (Birkmire, 1997). Large area module efficiencies in the 10–11% range have been demonstrated by three technologies/groups (Ullal, 2004). The most effective heterojunction partner for CdTe, also referred to as a window layer, is cadmium sulfide (CdS). A key reason for the high quality and efficient CdTe/CdS junctions

* Corresponding author. Tel.: +1 813 974 4818; fax: +1 813 974 5250.
E-mail address: ferekide@eng.usf.edu (C.S. Ferekides).

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is the fact that CdTe and CdS are miscible, and a reaction between these two materials during the cell fabrication process leads to the formation of an interfacial layer of $CdS_{1-x}Te_x$ (Ferekides et al., 2000). The formation of this layer is believed to be responsible for lowering the interfacial defect density resulting in high efficiency devices. The $CdS_{1-x}Te_x$ layer can form during the CdTe deposition process, if this process involves the use of high deposition temperatures (>550 °C), or during a post-deposition heat treatment of the CdTe/CdS structure in the presence of $CdCl_2$. The latter is a process used by virtually all CdTe solar cell research groups. The enhanced conversion efficiencies achieved as a result of the use of this heat treatment are primarily due to: (a) the formation of the interfacial layer mentioned above, (b) recrystallization and grain growth in the CdTe film, whenever the as-deposited CdTe is of submicron size, and (c) defect passivation/carrier lifetime improvement in the absorber (Levi et al., 1994). Although CdTe/CdS junctions have demonstrated the highest performances reported to-date, the use of CdS as a window layer also presents a limitation to the maximum achievable performance. A significant amount of the solar spectrum falls below 510 nm, the wavelength that corresponds to the band gap of CdS. Due to the poor properties of the CdS layer, essentially all photo-generated carriers in this layer recombine, not contributing to the output photocurrent. The photocurrent that can be potentially lost due to absorption in CdS is approximately 7 mA/cm^2 (of a maximum theoretical of 30.5 mA/cm^2). In most cases, CdTe/CdS solar cells are fabricated using a thin layer of CdS (typically less than 100 nm) in order to reduce absorption in this layer and enhance the output current. However, the fabrication of continuous and pinhole free CdS films with small thicknesses presents significant challenges, especially at the manufacturing level. The formation of pinholes leads to the CdTe coming in direct contact with the transparent contact (typically tin oxide (SnO_2)) leading to the formation of CdTe/SnO_2 microjunctions which are not as efficient as CdTe/CdS and act as micro-shunts reducing the overall efficiency of the device. The use of a bi-layer transparent contact, one that consists of a low/high resistivity (ρ) stack of transparent films has been found to effectively minimize efficiency losses resulting from the use of thin CdS films (Wu et al., 2001; Visoly-Fisher et al., 2003). The thin CdS film appears to be necessary for forming the low defect density solar cell interface, and the adjacent high resistivity transparent oxide (buffer) serves as an extension of CdS or simply does not permit the CdTe to come in direct contact with the highly conductive TCO, therefore eliminating the formation of shunting microjunctions.

Back contact options for CdTe thin film solar cells include the use of semiconductors such as ZnTe, metallic bi-layers of Cu/Au, and doped graphite (Gessert et al., 1997; McCandless et al., 1994). A critical step in the formation of the back contact is the use of a cleaning/surface modification solution typically Br_2/methanol, or nitric-phosphoric (NP) acid mixture (McCandless et al., 1994; Levi et al., 1997). The NP etch is a preferential etch leaving the CdTe surface Te-rich therefore increasing the surface conductivity and aiding the formation of a tunneling junction (Levi et al., 1997). In most cases, the formation of the back contact includes copper, which has been found to form a thin Cu_2Te layer on the surface of the CdTe, which also appears to be critical to the formation of an effective back contact.

This paper reviews results obtained from three different activities being carried out under the CdTe solar cell program at the University of South Florida sponsored by the National Renewable Energy Laboratory of the Department of Energy (NREL/DOE): (a) Study of various transparent bi-layers and their influence on solar cell efficiency, (b) the development of an effective vapor based $CdCl_2$ heat treatment with high throughput characteristics, and (c) back contact optimization using dry processing.

2. Experimental

All thin film CdTe/CdS solar cells to be discussed in this paper are of the superstrate configuration, which is shown in Fig. 1. The substrates were borosilicate glass (Corning 7059), and prior to solar cell fabrication were cleaned in dilute hydrofluoric acid solution (HF:H_2O 1:20) for 10 s, and subsequently rinsed with deionized water. The baseline front contact structure consists of a SnO_2 bi-layer (low-ρ/high-ρ), deposited by chemical vapor deposition (CVD); the thickness and sheet resistance of the bi-layer were approximately 1 μm and 7–8 Ω/□ respectively. All materials used in the bi-layer structure, other than SnO_2, were deposited using sputtering; materials discussed in this paper include $CdIn_2O_4$, In_2O_3, Cd_2SnO_4, and Zn_2SnO_4. Typically, sputter-deposited layers were deposited at room temperature and subsequently annealed prior to the deposition of the CdS and CdTe films. Additional processing details will be included in subsequent sections. The CdS films were deposited using the chemical bath deposition

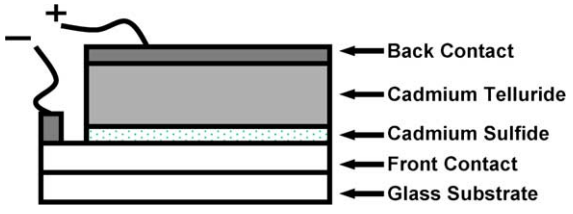

Fig. 1. The CdTe thin film solar cell superstrate configuration.

(CBD) process in an aqueous bath at 85 °C to a thickness of approximately 800–1000 Å. The CdTe films were deposited by CSS at substrate temperatures in the 500–620 °C range. Following the CdTe deposition, all structures were subjected to a heat treatment in the presence of $CdCl_2$. The baseline $CdCl_2$ process was carried out by first depositing $CdCl_2$ onto the CdTe surface by evaporation, and subsequently heat treating the structures at 400 °C at atmospheric pressure in the presence of O_2. A vapor-based version of the $CdCl_2$ treatment was carried out in a 2-zone atmospheric pressure annealing furnace. The substrate and $CdCl_2$ powder were placed in each of the two zones respectively where their temperature was controlled independently. A carrier gas, the composition of which varied, was used to transport $CdCl_2$ vapors over the sample zone; He, H_2, and O_2 were used as carrier gases. The baseline back contact process consisted of a cleaning step, where the CdTe surface was etched using 0.01% by vol. Br_2/methanol solution for 10 s, followed by the application of a graphite paste doped with HgTe:Cu, and a heat treatment in inert ambient at temperatures in the 250–280 °C range. Dry back contact processing involved replacing the Br_2 etch with sputter cleaning the samples in a rf-sputter etch chamber after the $CdCl_2$ treatment, with all other cell fabrication steps remaining the same. After formation of the back contact, excess CdTe was removed and indium was soldered around the cell areas to serve as a front electrode. Solar cells were characterized using standard solar cell techniques such as dark and light *J–V*, and spectral response (SR) measurements.

3. Results

3.1. Transparent bi-layer oxides

A significant effort in CdTe solar cell research is being dedicated to improving solar cell efficiencies. Considering the typical state-of-the-art performance characteristics of 840–850 mV, 74–76%, and 24–26 mA/cm^2, for open-circuit voltage (V_{OC}), fill factor (FF) and short-circuit current density (J_{SC}) respectively, one approach to advancing efficiencies is by increasing J_{SC}. Based on the ideal band gap of CdTe the maximum theoretical J_{SC} is 30.5 mA/cm^2. Approximately 7 mA are above the band gap of CdS (510 nm) and since carrier collection in this layer is essentially zero, it is important that solar cells are engineered to allow this portion of the solar spectrum to reach the CdTe. Therefore, the thickness of the CdS window layer becomes important, and utilizing the smallest CdS thickness possible is the ultimate objective. However, since all films that comprise the CdTe structure are polycrystalline, it is difficult to deposit very thin and continuous CdS layers i.e. free of pinholes. Considering that portion of the CdS reacts with CdTe during processing to form a $CdS_{1-x}Te_x$ mixed crystal, the requirement for high quality continuous CdS films becomes even more important. The formation of CdTe/SnO_2 junctions that act as microshunts and reduce the overall performance of the CdTe/CdS junction must be avoided. The use of a resistive or "buffer" layer in addition to the conductive TCO appears to be beneficial to solar cell performance especially for devices fabricated with CdS films of small thickness. This section describes solar cell results obtained for various combinations of low-ρ/high-ρ bi-layers as the front contact to CdTe solar cells.

3.1.1. Low-ρ CVD SnO_2/high-ρ SnO_2

Solar cells discussed in this section were fabricated using SnO_2, the most commonly used transparent front contact for CdTe thin film solar cells. Both conductive (low-ρ) SnO_2 and high-ρ films were deposited by MOCVD (Ferekides et al., 2000). This combination has previously resulted in over 15% efficiencies, and the comparison between cells fabricated on a single conductive layer and a bi-layer SnO_2 structure are presented to demonstrate the benefits of bi-layers, and as a reference point for comparison with the rest of the bi-layer structures in this section. Fig. 2 shows the light *J–V* characteristics for CdTe/CdS cells fabricated on conductive SnO_2 and a bi-layer low-ρ/high-ρ SnO_2. The most significant difference in the performance of these two devices is in the V_{OC}, which is about 90 mV higher for the device fabricated with the bi-layer SnO_2 (740 vs. 830 mV). There is also a 5% improvement in the FF for the bi-layer device. The slope of the *J–V* characteristics at reverse bias, which is used as an approximation of the shunt resistance (R_{SH}), is also higher for the bi-layer device (1000 vs. 2800 Ω cm^2). This difference in the slope of the *J–V* could also be a result of differences in collection between these devices. However, regardless of the mechanism responsible for this, the results clearly indicate that the use of a bi-layer TCO structure leads to

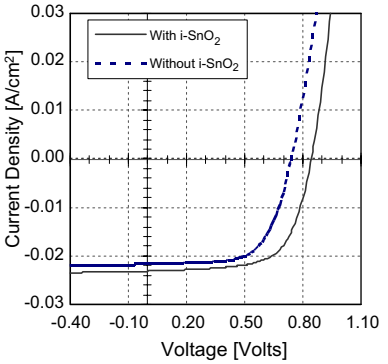

Fig. 2. Light *J–V* characteristics for CdTe solar cells fabricated with and without a resistive SnO_2 layer.

Table 1
Summary of device results obtained with SnO_2(CVD)/SnO_2 (reactively sputtered) bi-layer structures

Sputtered SnO_2 thickness (Å)	V_{oc} (mV)	FF (%)	J_{sc} (mA/cm^2)	EFF (%)	R_{SH} (Ω cm^2)
0	740	62.0	23.44	10.8	1100
125	823	72.4	23.41	13.9	2700
250	847	72.5	23.72	14.6	2200
500	820	71.7	23.50	13.8	3100
1000	830	73.9	23.46	14.4	2700

improved solar cell characteristics. Several devices were also fabricated using a high-ρ SnO_2 layer deposited by reactive rf-sputtering (on MOCVD low-ρ SnO_2). Reactive sputtering is a well developed large area deposition technique and it could offer manufacturing advantages over CVD. Table 1 lists solar cell characteristics for CdTe devices fabricated using reactively sputtered SnO_2 of various thicknesses as the high-ρ layer. Even at the smallest thickness of 125 Å, the improvement in performance is evident. Even though the best performers in this group are cells fabricated with 250 and 1000 Å, the variations are well within experimental variations/errors, and it cannot be concluded that these two thicknesses are optimum. The values for J_{SC} are based on spectral response measurements; the SR in the blue region (400–500 nm) was in the 50–60% range for all the devices listed, indicating that the CdS thickness was small to allow a significant portion of light above its band gap to reach the CdTe.

3.1.2. Low-ρ $CdIn_2O_4$/high-ρ In_2O_3

Although, SnO_2 and ITO are the most commonly utilized TCO's for CdTe cells, for this work $CdIn_2O_4$ was also incorporated in solar cell structures. It has been demonstrated previously that this material possesses the electro-optical properties required for solar cell applications (Mamazza et al., 2002). It was used in a bi-layer structure with In_2O_3 as the high-ρ material. Both films were deposited at room temperature by reactive sputtering in O_2 ambient from metallic targets ($CdIn_2O_4$ was deposited by co-sputtering of Cd and In). One of the variables investigated was the annealing temperature for $CdIn_2O_4$, which is amorphous when deposited at room temperature (Mamazza et al., 2002). Table 2 lists solar cell performance for devices fabricated on low-ρ $CdIn_2O_4$ annealed at different temperatures, with and without a high-ρ In_2O_3 layer (In_2O_3 was deposited on $CdIn_2O_4$ after the latter was annealed). The performance of devices without the high-ρ layer improves with annealing temperature. Although both V_{OC} and FF improve, they remain substantially below state-of-the-art values. The increases are believed to be associated with improvements in the overall properties of $CdIn_2O_4$, most importantly its crystallinity (Mamazza et al., 2002). Amorphous films (heat treated at 300 °C or less) may undergo significant recrystallization during the cell fabrication procedure, a process that appears to degrade the junction characteristics. A similar trend in performance is obtained for devices fabricated when In_2O_3 is used to form a bi-layer TCO structure. However, the performance characteristics are overall superior to the devices without the In_2O_3 layer, with V_{OC} values over 800 mV, and FFs approaching the 70% mark, once again demonstrating the positive effect of the high-ρ layer. The FFs for these devices were influenced by what appears to be a "barrier" like behavior. Their light J–V characteristics are shown in Fig. 3; the behavior of the J–V curves around V_{OC} improves with increasing temperature. The mechanism affecting the J–V data in this region does not appear to be a simple increase in the series resistance (linear), but rather a non-linear effect most likely associated with the band alignment at the front contact that depends on the properties of $CdIn_2O_4$. This issue was beyond the scope of this work and was not further investigated; however, it is clear from the results above that cell performance degrades considerably if the $CdIn_2O_4$ is incorporated into the solar cell structure in amorphous form.

3.1.3. CVD SnO_2/high-ρ SnO_2

The most successful combination of a bi-layer structure to-date has been Cd_2SnO_4/Zn_2SnO_4 (Wu et al., 2001). Two advantages associated with this combination

Table 2
Summary of device results obtained with $CdIn_2O_4$, and $CdIn_2O_4$/In_2O_3 as front contacts

Anneal temp. (°C)	$CdIn_2O_4$			$CdIn_2O_4$/In_2O_3		
	V_{oc} (mV)	FF (%)	J_{SC} (mA/cm^2)	V_{oc} (mV)	FF (%)	J_{SC} (mA/cm^2)
–	619	53.5	23.30	830	65.5	23.20
300	645	57.9	23.29	820	63.6	22.80
400	755	61.2	23.63	826	66.2	23.00
500	760	61.9	23.52	825	69.3	23.20

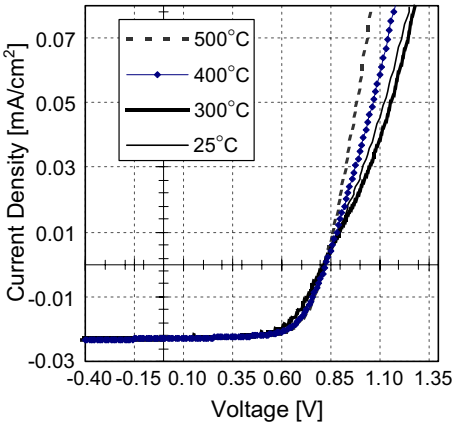

Fig. 3. Light J–V characteristics for $CdIn_2O_4/In_2O_3$ devices with the $CdIn_2O_4$ annealed at different temperatures.

of materials, are (a) the superior electro-optical properties of Cd_2SnO_4 and (b) the fact that Zn_2SnO_4 and CdS appear to react during the cell fabrication process resulting in thinner CdS and therefore increased response in the short wavelength range. The best results obtained in this work yielded V_{OC}s of 830 mV, FFs of 69–70%, and J_{SC}s over 24 mA/cm^2. Although, further development of this bi-layer combination is expected to yield yet better performance, the advantage of incorporating it into the CdTe solar cell structure is displayed in Fig. 4, where the SR of several CdTe devices is shown: (a) a device where the CdS thickness was large to demonstrate the potential losses in J_{SC}, (b) a device fabricated on a SnO_2 bi-layer structure and (c) a device fabricated on a Cd_2SnO_4/Zn_2SnO_4 bi-layer. The starting CdS thickness for (b) and (c) was the same, indicating that in addition to the portion of CdS that reacts to form a $CdS_{1-x}Te_x$ layer at the interface, a portion of this material is also consumed in Zn_2SnO_4.

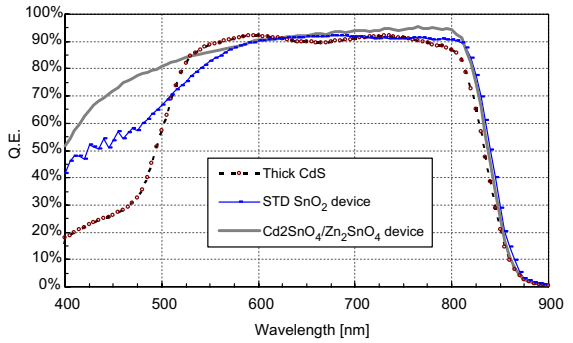

Fig. 4. Spectral response for devices with different current generation above the CdS band gap; the starting CdS thickness was the same for the SnO_2 and Cd_2SnO_4/Zn_2SnO_4 devices.

The results presented above clearly show that the use of a bi-layer front contact can lead to significant improvements in the performance of CdTe solar cells. Various materials can serve as the high-ρ layer, the selection of which will depend on the overall characteristics of the solar cell fabrication process, such as highest processing temperatures, annealing ambients etc. The use of Zn_2SnO_4 appears to offer the additional advantage of improved SR in the blue region as a result of a reaction with the CdS consuming a portion of this material.

3.2. Vapor chloride treatment

The most common processing step in the fabrication of CdTe solar cells is a heat treatment carried out in the presence of $CdCl_2$. During the early stages of development, this process involved applying $CdCl_2$ directly onto the CdTe surface and subjecting the entire structure to a heat treatment in air for approximately 30 min. With the maturing of the CdTe technology, it has become necessary for some of the processing procedures to be improved in order to be easily integrated into a continuous manufacturing process. With regards to the $CdCl_2$ treatment, a vapor-based approach has been the subject of various investigations including industrial groups (McCandless et al., 1996; Zhou et al., 1994). The advantage of such a process is the elimination of significant amounts of Cd-containing waste, and the ease of integration in an in-line vacuum manufacturing process. This section describes a vapor $CdCl_2$ heat treatment process where the primary objective was to improve the throughput without sacrificing solar cell performance. Solar cells described in this section were of the following configuration: Glass/bi-SnO_2/CdS(CBD)/CdTe/(CSS)/C-HgTe:Cu. In an effort to eliminate additional wet processing steps from the cell fabrication process, and further simplify the overall process, the back contact was applied to CdTe immediately following the vapor treatment without the use of a Br_2 or NP etch. The vapor treatment studies focused on evaluating the effect of the ambient/carrier gas with ultimate goal to optimize the temperature–time parameters for short annealing times.

The performance characteristics for several CdTe solar cells vapor treated at various substrate temperatures in O_2 ambient and for different anneal times are shown in Fig. 5. The V_{OC} data suggest that as the annealing temperature is increased the annealing time for optimum performance decreases. It is known that the $CdCl_2$ treatment affects CdTe solar cells in several ways, including CdTe grain enhancement, interdiffusion between the CdTe and CdS, and formation of Cl-related complexes in CdTe. The grain size of the as-deposited CSS-CdTe films utilized in this work is typically larger than 2 μm, and no recrystallization takes place during

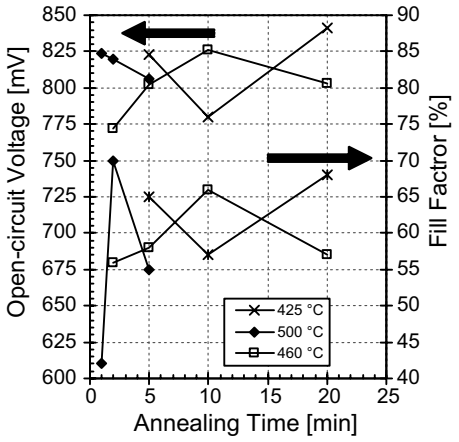

Fig. 5. V_{OC} and FF for CdTe cells vapor-treated in the presence of O_2.

the $CdCl_2$ process (Levi et al., 1994). It is also known that interdiffusion at the CdTe/CdS interface takes place during the high temperature CSS deposition of the CdTe (Ferekides et al., 2000). It is therefore believed that the major effect of the $CdCl_2$ treatment for these devices is to modify the defect structure in CdTe resulting in better overall transport properties. The results in Fig. 5 clearly suggest that this process is accelerated at higher temperatures, possibly by enhanced diffusion of $CdCl_2$ into CdTe, and therefore the annealing times can be significantly decreased. However, the behavior of the FF in the same data set does not consistently follow the trends exhibited by V_{OC}. For example, for devices vapor treated at 500 °C the V_{OC} increases with decreasing annealing time, but the FF shows a dramatic decrease for the shortest annealing time (1 min). The light J–V characteristics for the three devices (500 °C) are shown in Fig. 6.

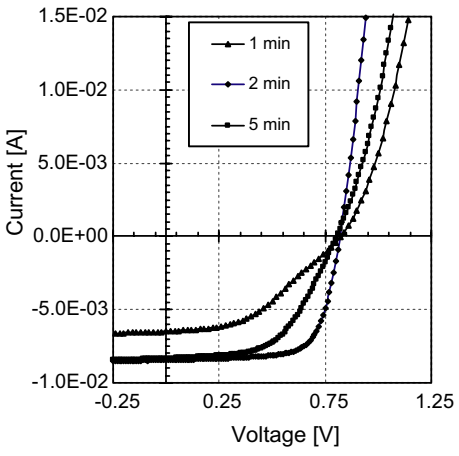

Fig. 6. Light J–V of vapor-treated CdTe solar cells exhibiting characteristics consistent with the presence of a back barrier.

The data clearly indicates that the most significant differences among these devices is the curvature observed around V_{OC} for two of these (1 and 5 min), which is believed to be due to the presence of a barrier at the back contact, and leads to low FFs. As indicated earlier, these cells were fabricated without the use of a cleaning step (Br_2 etch) prior to the application of the back contact. Therefore, the back barrier is believed to have formed due to the presence of oxides on the surface of CdTe. These oxides could have formed during the vapor $CdCl_2$ treatment since in this case the ambient contained O_2, or simply while the cells were kept in storage prior to being heat-treated. Nevertheless, the improved V_{OC}'s suggest that as a result of the vapor treatment the junction properties improve, and the remaining issue is to avoid the formation of surface oxides, especially in cases where a surface cleaning/modification step is to be eliminated.

In addition to the O_2 ambient CdTe cells were also heat-treated in the presence of inert (He) and H_2 ambient. Table 3 lists the best overall performance obtained for each ambient, demonstrating the superior performance obtained with O_2. The J–V characteristics of the O_2-annealed devices indicated that these devices were characterized by low dark currents indicative of improved junction properties (Zhao et al., 2002). The presence of O_2 during the $CdCl_2$ treatment has been previously found to affect the consumption of CdS and the defect structure in CdTe (McCandless et al., 1996; Nollet et al., 2002). As short annealing times were one of the key objectives in pursuing the optimization of this process, several devices were vapor-treated for times less than 1 min. The data shown in Fig. 7 represent the best performance obtained to-date for the various ambient conditions indicated. It should be noted that the annealing times (of less than 1 min) indicated in this figure, refer to the time period from the instant that the cells reached the desired temperature until the heater power was turned off; the actual heating time required to reach this temperature was approximately 11/2 min. As such, the annealing times in Fig. 7 should be considered primarily relative to the results presented within this manuscript, and as an existence proof of the potential throughput of this process. Nevertheless, it is clear that the duration of this essential processing step can be significantly reduced, offering significant throughput advantages in a manufacturing process.

Table 3
Best V_{OC}/FF combinations (same cell results) obtained with the vapor $CdCl_2$ treatment under different ambient conditions

Ambient	V_{OC} (mV)	FF (%)
O_2	834	72.5
He	830	64.4
H_2	790	68.5

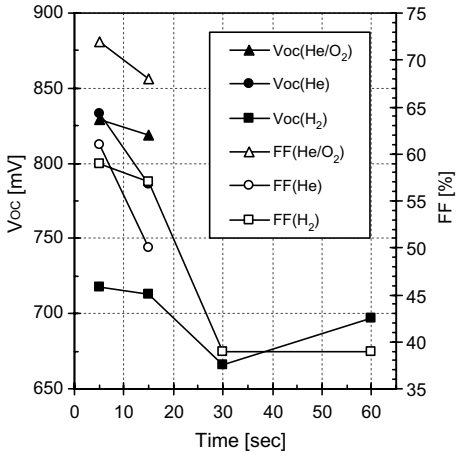

Fig. 7. V_{OC} and FF for CdTe cells vapor-treated for very short times.

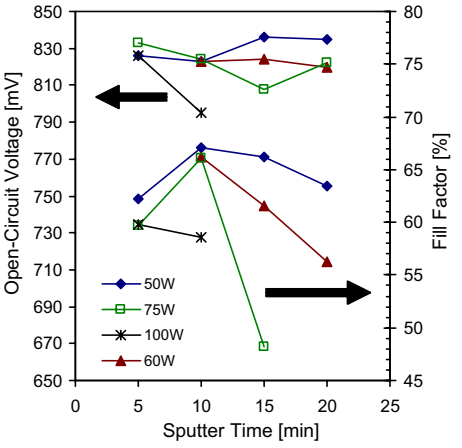

Fig. 8. V_{OC} and FF for CdTe cells fabricated using a dry etch process (rf sputter etch).

3.3. Dry back contact processing

The formation of an effective back contact to CdTe solar cells was initially a major obstacle in the development of this technology. The large work function of this material and self-compensation that hinders efforts to achieve high carrier concentrations, were the two issues to be addressed. Rectifying or blocking contacts severely limit the FF of the device and therefore the overall efficiency. However, the formation of effective, most likely tunneling contacts has become routine. The two characteristics of the back contact process are: (a) a chemical surface treatment to remove oxides and/or leave a tellurium-rich and therefore p^+ surface, and (b) the use of copper, which forms a Cu_2Te surface layer that is critical in achieving an effective contact. The most commonly used etching solutions for the surface treatment are Br_2/methanol and nitric/phosphoric mixtures. Both processes have been used for the formation of non-blocking back contacts yielding state of the art FFs and efficiencies. The use of etching solutions although practical in a laboratory environment it may not be very practical for a manufacturing process. This section describes results obtained on CdTe solar cells for which the back contact did not include a wet processing step, but rather the CdTe surface was cleaned using dry processing, sputter etching, prior to the contact application. For the results presented in this section, CdTe solar cells were exposed to an rf plasma using a MARCH Plasmod sputter etcher, following the $CdCl_2$ heat treatment. Gases utilized included N_2, Ar, and O_2; the devices were sputter–etched using plasma power ranging from 50–100 W, and gas pressures ranging from 150–400 mTorr.

The effect of sputter–etch time on solar cell performance is shown in Fig. 8 for four plasma power settings, using N_2 as the sputtering gas. The V_{OC} does not vary significantly (in the 810–835 mV range) for this set of parameters, with the exception of the device corresponding to a power of 100 W and etch time of 10 min. The FF varies considerably and it is at the highest levels for the lower power setting shown (50 W); power settings below 50 W did not yield further performance improvements. The low FFs for short annealing times were due to the presence of a back barrier suggesting that the removal of surface oxides was not complete. However, the same was true for long anneal times i.e. formation of a back barrier. In this case it is believed that the surface of the CdTe was damaged forming a highly defective (compensated) region that leads to the formation of a back contact barrier. Low FFs due to the presence of a back contact barrier were also a result of increasing sputter power, also suggesting that the CdTe surface was damaged during the sputter–etch process. Fig. 9 shows the

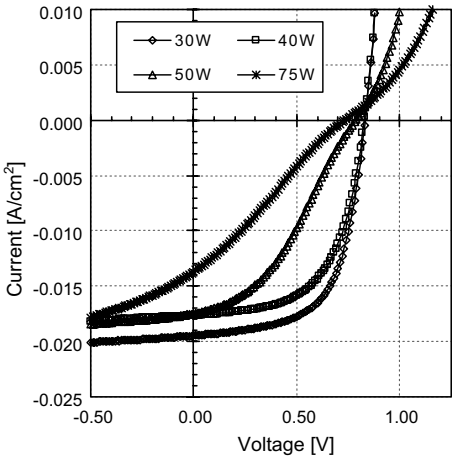

Fig. 9. Light J–V characteristics for CdTe cells sputter etched at different power levels, using Ar prior to contact application.

light J–V characteristics of several cells in this case sputter–etched in Ar, for various power settings. It is clear that at high power levels, the back contact is rectifying significantly limiting the FFs, and as the power is decreased the characteristics improve and the presence of a back barrier is no longer evident.

Comparing the results obtained with Ar and N_2, optimum performance for Ar was obtained at lower power settings (30 vs. 50 W); rectification was also observed at lower power (50 vs. 75 W). Both results indicate that Ar, being a heavier atom, is more effective for cleaning the CdTe surface at low powers, but also causes more damage than N_2 when the power is increased. The solar cell performance achieved ($V_{OC} > 830$ mV, FF 69–70%) using the above described sputter etch process indicates that the wet cleaning procedures typical of this technology can be eliminated, further improving the manufacturing advantages of this technology.

4. Summary

Results in three key areas of thin film CdTe cells have been presented. The use of bi-layer films as front contacts for CdTe solar cells can significantly improve device performance. Various films can serve as resistive layers including SnO_2, In_2O_3, and Zn_2SnO_4. The use of Zn_2SnO_4 appears to lead to thinning of the CdS resulting in further improvements in the blue response of the cells. A vapor-based $CdCl_2$ treatment has been optimized to yield state-of-the-art performance at very short annealing times, improving the manufacturing advantages of the CdTe technology. The best overall performance was obtained when O_2 was used in the carrier gas. Current–voltage characteristics indicated that oxides can form on the CdTe surface which can hinder the performance of the device if a cleaning step is not included. Encouraging results have also been obtained for devices processed without the use of a wet etch step for the formation of the back contact. Key process parameters for the rf sputter etch of CdTe were optimized to yield optimum solar cell performance. The work presented in this paper was sponsored by the National Renewable Energy Laboratory of the Department of Energy.

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