The effects of $CdCl_2$ on the electronic properties of molecular-beam epitaxially grown CdTe/CdS heterojunction solar cells

S. A. Ringel, A. W. Smith, M. H. MacDougal, and A. Rohatgi
School of Electrical Engineering and Microelectronics Research Center, Georgia Institute of Technology, Atlanta, Georgia 30332

(Received 26 February 1991; accepted for publication 8 April 1991)

Significant improvements in CdTe/CdS solar cell efficiency are commonly observed as a result of a postdeposition $CdCl_2$ dip followed by a 400 °C heat treatment during cell processing which increases CdTe grain size. In this paper, we investigate the electronic mechanisms responsible for $CdCl_2$-induced improvement in cell performance along with possible performance-limiting defects resulting from this process in molecular-beam epitaxy-grown polycrystalline CdTe/CdS solar cells. Current density-voltage-temperature (J-V-T) analysis revealed that the $CdCl_2$ treatment changes the dominant current transport mechanism from interface recombination/tunneling to depletion region recombination, suggesting a decrease in the density and dominance of interface states due to the $CdCl_2$ treatment. It is shown that the change in transport mechanism is associated with (a) an increase in heterojunction barrier height from 0.56 to 0.85 eV, (b) a decrease in dark leakage current from 4.7×10^{-7} A/cm^2 to 2.6×10^{-9} A/cm^2 and, (c) an increase in cell V_{oc} from 385 to 720 mV. The $CdCl_2$ also improved the optical response of the cell. Substantial increases in the surface photovoltage and quantum efficiency accompanied by a decrease in the bias dependence of the spectral response in the $CdCl_2$-treated structures indicate that the $CdCl_2$ treatment improves carrier collection from the bulk as well as across the heterointerface. However, deep level transient spectroscopy measurements detected a hole trap within the CdTe depletion region of the $CdCl_2$-treated devices at $E_v + 0.64$ eV which is attributed to the formation of V_{Cd}-related defects during the annealing process after the $CdCl_2$ dip. J-V-T analysis demonstrated that this trap is the probable source of dominant recombination in the $CdCl_2$-treated cells. An inverse correlation was found between the density of the $E_v + 0.64$ eV trap and cell V_{oc}, suggesting that the heat treatment with $CdCl_2$ may eventually limit the CdTe/CdS cell performance unless the formation of this defect complex is controlled or eliminated.

I. INTRODUCTION

Solar cells based on CdTe are one of the leading candidates for low-cost conversion of solar energy due to their near optimum band gap (1.45 eV), high absorption coefficient, and manufacturability of thin-film devices. High-efficiency ($\sim>10\%$) polycrystalline CdTe/CdS solar cells have been fabricated by electrodeposition,[1] physical vapor deposition,[2] close-spaced vapor transport (CSVT),[3] sintering,[4] metalorganic chemical vapor deposition (MOCVD),[5] and molecular-beam epitaxy (MBE).[5] To obtain high efficiency in all of these approaches, it is necessary to have CdTe grain sizes of ~1 μm or greater to avoid significant bulk recombination, large interface state density, and high resistance. A commonly used procedure to enhance the grain size and densify the CdTe film is the introduction of an annealing (or sintering) aid such as $CdCl_2$ either during or after CdTe film growth.[6–8] The influence of the $CdCl_2$ treatment on CdTe microstructure and solar cell performance has been previously investigated for CdTe films prepared by a high-temperature ($T>600$ °C) sintering process[6–8] which requires incorporation of $CdCl_2$ in the CdTe slurry prior to CdTe film formation. This method has resulted in CdTe cell efficiencies in excess of 10%. However, polycrystalline CdTe films prepared by techniques such as electrodeposition, physical vapor deposition, MBE and MOCVD require a postdeposition heat treatment in the presence of $CdCl_2$ to obtain high efficiency.[9] To date, the observed beneficial effects of the $CdCl_2$ treatment on device characteristics and performance are at best qualitatively understood. In order to improve present-day CdTe/CdS cell efficiency beyond 12%–13%, it is necessary to quantify and improve the fundamental understanding of process-induced effects on the bulk and interface properties of these cells.

In this paper, MBE-grown polycrystalline CdTe/CdS solar cells are investigated to quantify the mechanisms responsible for improved cell performance due to the $CdCl_2$ treatment and reveal process-induced defects which may dictate the device characteristics after the $CdCl_2$ treatment. First, microstructural changes in the CdTe films due to postdeposition annealing with and without the $CdCl_2$ dip are investigated by scanning electron microscopy (SEM). Second, electrochemical surface photovoltage (SPV) and bias-dependent spectral response measurements are used to estimate the improvement in bulk and interface quality of the CdTe/CdS cells due to the $CdCl_2$ treatment. Third, the dominant current transport mechanisms in CdTe/CdS cells processed with and without the $CdCl_2$ treatment are studied by current density-voltage-

 0021-8979/91/020881-09$03.00 © 1991 American Institute of Physics

Downloaded 16 Aug 2011 to 138.253.100.121. Redistribution subject to AIP license or copyright; see http://jap.aip.org/about/rights_and_permissions

temperature (J-V-T) analysis. Finally, deep-level transient spectroscopy (DLTS) measurements are performed to identify traps which may dominate the current transport and limit the $CdCl_2$-treated CdTe/CdS cell performance. Attempts are made to correlate transport mechanisms and traps within the CdTe cells to film microstructure, SPV and spectral response, and solar cell performance in order to provide guidelines for achieving higher efficiencies.

II. EXPERIMENTAL TECHNIQUES

A. CdTe growth and cell processing

Polycrystalline CdTe films were grown to a thickness of 2 μm by MBE on n-type CdS/SnO_2/glass substrates suitable for solar cell applications.[10] Prior to CdTe deposition, the surface doping density of the CdS was found to be 5×10^{16} cm^{-3} by electrochemical C-V measurements. After the CdTe film deposition, CdTe/CdS structures were dipped in a saturated $CdCl_2$:CH_3OH solution and then annealed in air at 400 °C for 35 min.[5,9] Selected samples from the same growth run were annealed in air at 400 °C for 35 min without the $CdCl_2$ solution to distinguish the effects of $CdCl_2$ on CdTe material and device properties. Cell fabrication was completed by etching the annealed CdTe surface in ~0.1% Br_2:CH_3OH to remove residual surface oxides, followed by a DI water rinse and blow dry in N_2. Ohmic back contacts were formed on the etched CdTe surface by evaporating 150 nm of Cu-doped ZnTe capped with 200 nm of Ni.[5]

B. Microstructural studies

The grain size of the as-grown and processed CdTe/CdS structures was determined by SEM. A beam voltage of 15 KV was used. To prevent sample charging effects, the CdTe surfaces were coated with 10 nm of gold.

C. Electrochemical surface photovoltage and spectral response measurements

Process-induced effects on bulk and junction quality were monitored by electrochemical SPV measurements, using the Polaron PN4200 electrochemical profiler with the PN4250 photovoltage spectroscopy accessory. The CdTe/CdS/SnO_2/glass structures in the as-grown state, after air anneal, and after the $CdCl_2$ dip followed by air anneal were analyzed in detail. A 0.2-M NaOH + EDTA (ethylenediaminetetraacetic acid) solution was used to form an electrochemical Schottky barrier to the CdTe surface and ohmic contact was made to the underlying SnO_2 with Indium. The samples were illuminated from the CdTe side, through the electrolyte, by chopped light in the wavelength range of 700–900 nm and the resulting photovoltage was measured under open-circuit conditions to avoid etching of the CdTe film by the electrolyte. The net open-circuit SPV signal at each wavelength is the difference between the internal photovoltages generated at the surface barrier and CdTe/CdS heterojunction.[11] To accurately compare material and junction quality of different CdTe/CdS samples, it is necessary for the CdTe film thicknesses and doping to be identical to insure that the same carrier generation profile is seen by the collecting junctions in all of the samples. Our SPV setup uses low illumination intensity such that the SPV magnitude is much less than kT. In this case, it has been shown that the photovoltage generated at the CdTe/CdS heterojunction, ignoring the presence of the electrolyte/CdTe surface barrier for now, can be approximated as[11,12]

$$\begin{aligned}\mathrm{SPV}(\lambda) &= V_{\mathrm{oc}}(\lambda)\\ &= [nkT/q]\ln(J_{\mathrm{PH}}/J_0+1)\\ &\approx [nkT/q]\,[J_{\mathrm{PH}}/J_0]\\ &= [nkT/J_0]F(\lambda)R(\lambda),\end{aligned}\tag{1}$$

where n is the heterojunction ideality factor, J_0 is the "effective" junction leakage current density, $F(\lambda)$ is the photon flux absorbed in the quasineutral CdTe bulk, and $R(\lambda)$ is the spectral response function which is comprised of contributions from the quasineutral and depletion regions of both the CdTe and CdS and reflects bulk material quality.[12] Note that the contributions from the CdS layer to $R(\lambda)$ can be ignored since the minimum wavelength (maximum energy) of the photons incident on the CdTe surface was chosen to be 700 nm (1.77 eV) which will not be absorbed by the 2.42-eV band-gap CdS layer. Hence the magnitude of the SPV signal is proportional to both the CdTe/CdS junction quality, through J_0 and n, and CdTe material quality through $R(\lambda)$. The final SPV spectrum is normalized to a calibrated photodiode to eliminate flux variations and the spectrometer response.

To support the results from the above SPV analysis, bias-dependent spectral response measurements were performed on completed CdTe/CdS cells processed with and without $CdCl_2$. ac photocurrent measurements were made with 0-V dc and −0.5-V dc reverse bias applied across the device.

D. Dark J-V-T and light J-V measurements

Dark J-V-T measurements were performed to determine the current transport mechanisms in CdTe/CdS devices fabricated with and without the $CdCl_2$ treatment. J-V data were measured in the temperature range of 180–320 K in 10-K increments using an automated J-V-T setup. The J-V characteristic at each temperature was fitted to a parallel double diode equivalent circuit model with shunt resistance, R_s, described by

$$J = J_1 + J_2 + (V - JR_s)/R_{\mathrm{sh}},\tag{2}$$

where

$$J_1 = J_{01}[\exp[(q/A_1kT)(V - JR_s)] - 1]\tag{3}$$

and

$$J_2 = J_{02}[\exp[(q/A_2kT)(V - JR_s)] - 1].\tag{4}$$

A multivariable regression analysis was used to fit the data and obtain J_{01}, J_{02}, A_1, A_2, R_s, and R_{sh} with less than 5% error in the fit over the entire voltage range. The temperature dependence of these parameters was used to deter-

Downloaded 16 Aug 2011 to 138.253.100.121. Redistribution subject to AIP license or copyright; see http://jap.aip.org/about/rights_and_permissions

mine current transport mechanisms in each device. Solar cell data were determined by lighted J-V measurements taken at 300 K under 100 mW/cm^2 AM1.5 conditions.

E. Deep level transient spectroscopy (DLTS) measurements

DLTS measurements were performed on Ni/ZnTe/CdTe/CdS/SnO_2/glass structures annealed with and without $CdCl_2$ to identify traps within the CdTe depletion region. DLTS data were taken using an automated DLTS spectrometer in a lock-in amplifier type arrangement. The output signal was integrated and analyzed using five different weighting functions from 4 to 64 ms. A pulse width of 8 ms was necessary to saturate the detectable traps. Since the CdTe doping concentration (5×10^{15} cm^{-3}, as determined by C-V measurements) is much less than that of the CdS, only the CdTe depletion region is probed. A steady reverse bias of -400 mV was used and a pulse of $+300$ mV was applied to scan the CdTe depletion region. Spatial trap distributions were measured by varying the reverse steady bias from -400 to -100 mV, but keeping the sum of the reverse steady bias and the pulse height constant at -100 mV. In this way, the edge of the depletion region is stepped toward the CdTe/CdS interface as the steady reverse bias is decreased to provide a spatial trap profile in the CdTe depletion. The temperature of each device is monitored by a thermocouple mounted directly on a glass slide of identical thickness to the glass substrate of the CdTe/CdS device which was situated adjacent to the device under test. Trap activation energies and cross sections were determined from the $\log(T^2/e_m)$ vs $1000/T$ Arrhenius plot. The trap emission rate for majority-carrier holes in the CdTe, e_{mp}, is given by

$$e_{mp}=N_v\sigma_p v_{th}\exp[(E_v-E_T)/kT], \quad (5)$$

where the terms in Eq. (5) have their usual meanings.[13]

III. RESULTS AND DISCUSSION

A. Effects of $CdCl_2$ treatment on MBE-grown polycrystalline CdTe films and solar cells

The $CdCl_2$ dip prior to postdeposition annealing of small grain CdTe films grown by electrodeposition and physical vapor deposition has been previously shown to be necessary for grain growth and cell efficiencies in excess of 10%.[2,6–9] We have found the same to be true for MBE-grown polycrystalline CdTe. The SEM photomicrographs shown in Fig. 1 indicate an estimated increase in average grain size from $\sim$0.25 μm for the as-grown and air annealed films without a $CdCl_2$ dip to $\sim$1 μm for the $CdCl_2$ treated and annealed films. Note that little or no grain growth is evident for the air annealed CdTe film without the $CdCl_2$ treatment. It is likely that the presence of $CdCl_2$ during the anneal induces a sintering mechanism within the CdTe film that acts to decrease intergrain pore size and increase average grain size.[7] The effect of this grain growth on solar cell performance is shown in Table I

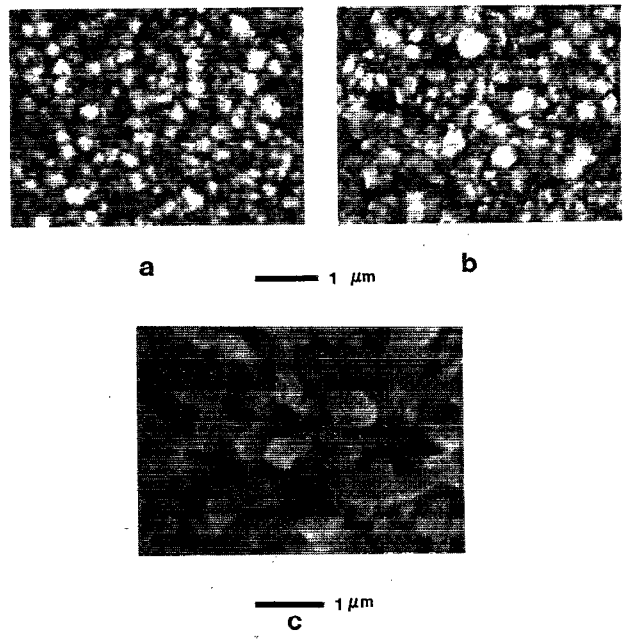


FIG. 1. SEM photomicrographs of (a) as-grown CdTe, and CdTe annealed in air at 400 °C for 35 minutes (b) without $CdCl_2$ and (c) with $CdCl_2$.

which indicates a dramatic improvement in all solar cell parameters, with the efficiency increasing from 1.3% to 8.6%.

B. Effect of $CdCl_2$ treatment on the photoresponse of CdTe/CdS structures

CdTe grain growth is expected to reduce the bulk and interface state density which tend to influence the spectral response and leakage current of the fabricated device. In order to directly assess the effects of $CdCl_2$ treatment on recombination at the CdTe/CdS junction and in the CdTe bulk, SPV measurements were performed on CdTe/CdS structures with and without the $CdCl_2$ treatment, prior to back contact (ZnTe + Ni) deposition. Samples of identical thickness from the same growth run, deposited on identical substrates, were used for the SPV analysis. Figure 2(a) shows the measured SPV spectra for (a) an as-grown sample, (b) a sample after air anneal, and (c) a sample dipped in $CdCl_2$ followed by an air anneal. The as-grown CdTe/CdS structure (curve a) yields a small and flat SPV response prior to the CdTe bandedge ($\lambda\sim850$ nm), while the air-annealed structure without the $CdCl_2$ treatment exhibits a peak near the bandedge. This peak can be attributed to the p-type conversion of CdTe[14] and subsequent

TABLE I. AM1.5 solar cell data for MBE-grown ZnTe/CdTe/CdS devices processed with and without $CdCl_2$ fluxing agent.

Treatment	V_{oc} (mV)	J_{sc} (mA cm^{-2})	FF	EFF (%)	R_s Ω cm^2
no $CdCl_2$	385	10.5	0.32	1.3	3.6
with $CdCl_2$	720	23.1	0.51	8.6	.90

Downloaded 16 Aug 2011 to 138.253.100.121. Redistribution subject to AIP license or copyright; see http://jap.aip.org/about/rights_and_permissions

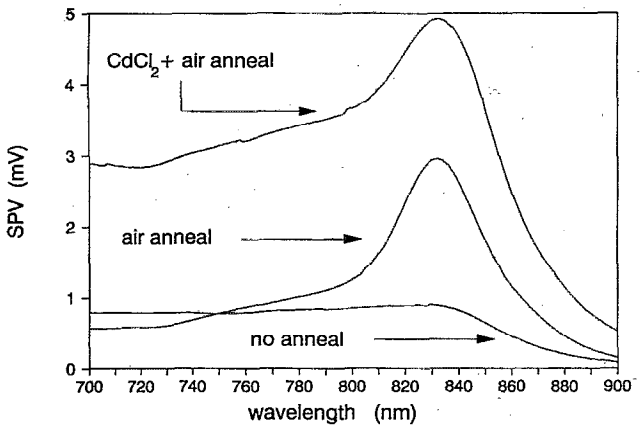


FIG. 2. SPV spectra of as-grown, air-annealed, and $CdCl_2$ + air annealed CdTe/CdS structures with light incident on the CdTe surface.

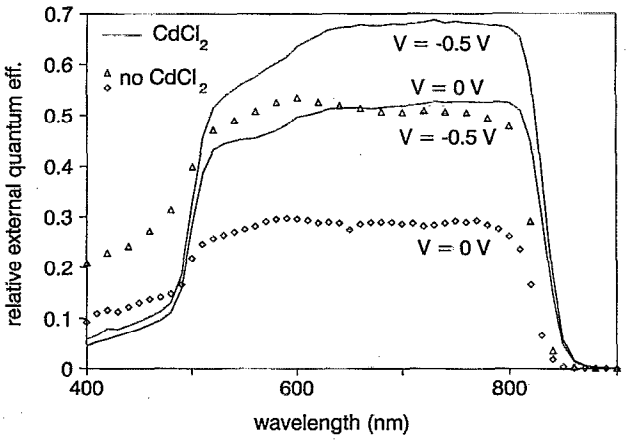


FIG. 3. Bias-dependent spectral response data of completed Ni/ZnTe/CdTe/CdS/SnO_2/glass solar cells with $CdCl_2$ (solid lines) and without $CdCl_2$ (symbols). The values of the applied reverse bias are noted.

formation of a *p*-CdTe/*n*-CdS heterojunction after air annealing which aids in the collection of carriers generated close to and within the CdTe depletion layer (recall that light is incident on the CdTe side and not the CdS). However, even though annealing in air without $CdCl_2$ aids in the formation of the CdTe/CdS junction, little or no improvement in CdTe bulk diffusion length is evident based on the similar SPV response for shorter wavelengths below the peak for both the as-grown and air-annealed samples. In contrast, the SPV response of the CdTe/CdS structure annealed after the $CdCl_2$ treatment (Fig. 2) is significantly larger at all wavelengths compared to the structure annealed without $CdCl_2$ suggesting an increase in effective carrier collection length and an improvement in CdTe bulk quality. Furthermore, the peak near the bandedge is even more pronounced after the $CdCl_2$ treatment suggesting additional improvement in the junction quality compared to CdTe/CdS annealed without the $CdCl_2$ dip. The trends in the SPV spectra are consistent with $CdCl_2$-induced grain growth shown in Fig. 1 suggesting that the SPV improvement results from a decrease in the density of grain boundary states throughout the CdTe bulk and depletion region.

To investigate the role of the $CdCl_2$ treatment on interface quality, bias-dependent spectral response measurements were performed on solar cells fabricated from films annealed with and without $CdCl_2$. Figure 3 shows the spectral responses for each sample with and without an applied reverse bias, revealing three important results. First, a significant increase in absolute spectral response with the $CdCl_2$ treatment demonstrates reduced interface recombination and increased carrier collection length. Second, while the spectral response of both samples show a wavelength-independent increase with applied reverse bias, the spectral response of the $CdCl_2$ treatment samples show a smaller bias dependence, suggesting an improved interface collection function[15] due to reduced number of defect states at or near the CdTe/CdS interface after $CdCl_2$ treatment. Both of these results are consistent with the SPV data. Finally, even after the $CdCl_2$ treatment, appreciable bias dependence in the spectral response is evident suggesting that there is still considerable interface recombination in this 8.6% efficient cell. The identification and elimination of the states responsible for this recombination is necessary to increase device performance further.

C. Effect of $CdCl_2$ treatment on CdTe/CdS junction transport properties

The dark *J-V-T* behavior of devices processed with and without the $CdCl_2$ process were analyzed to investigate the effect of the $CdCl_2$ treatment on the diode transport mechanisms in the CdTe/CdS cell. The measured and modeled dark ln *J-V* characteristics of both samples are shown in Fig. 4 as a function of temperature. Each ln *J-V* curve was fit to the double diode equivalent circuit model described by Eqs. (2)–(4), and the fitting parameters for each cell as a function of temperature are summarized in Tables II and III. The ln *J-V* characteristics are plotted with respect to the junction voltage ($= V\text{-}JR_s$) to reveal the junction transport. The deviation from linearity at higher bias voltages is due to the non-ohmic behavior of the back Ni/ZnTe/CdTe contact at larger bias voltages.[16] Figure 4 shows significant differences in the voltage dependence and magnitude of the diode current for devices processed with and without $CdCl_2$, suggesting a change in the dominant mode of current transport. To understand and quantify this difference, the dominant transport mechanisms in each cell are described in the remainder of this section.

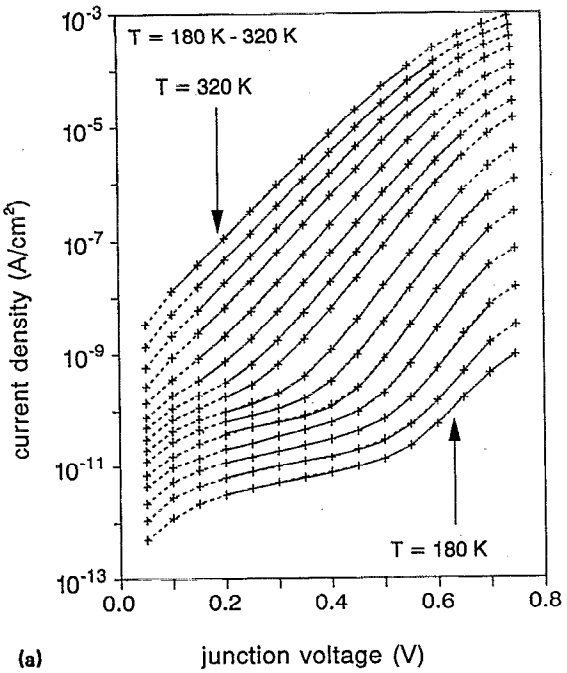
The dark current transport in the $CdCl_2$-treated cells above 220 K was best described by a single diode model, viz.,

$$J=J_{01}\{\exp[(q/A_1kT)(V-JR_s)]-1\} + (V-JR_s)/R_{sh}, \quad (6)$$

where

$$J_{01}=J_{001}\exp(-\Delta E/kT), \quad (7)$$

Downloaded 16 Aug 2011 to 138.253.100.121. Redistribution subject to AIP license or copyright; see http://jap.aip.org/about/rights_and_permissions



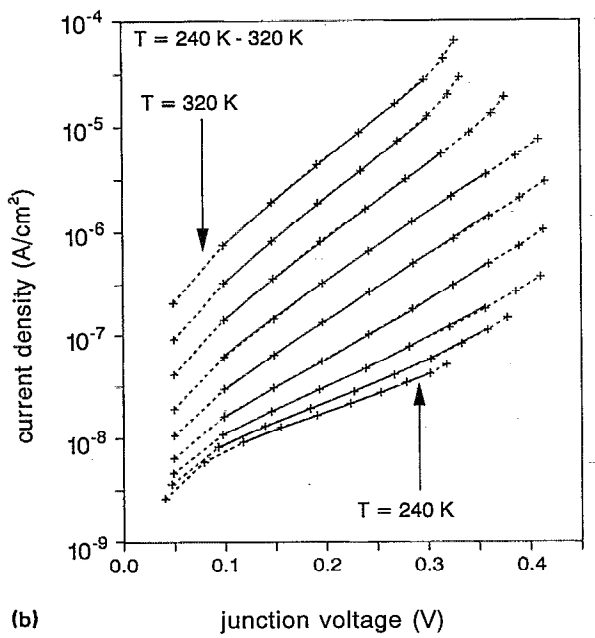


FIG. 4. Measured (symbols) and modeled (lines) J-V-T data for (a) $CdCl_2$ + air annealed and (b) air annealed without $CdCl_2$ Ni/ZnTe/CdTe/CdS/SnO_2/glass solar cells. Shown is the current behavior as a function of junction voltage (V-JR_s). The average error of each fit is less than 5%.

which is the general form for recombination-controlled current transport.[17] For interface recombination-dominated current transport, the value of A_1 should be ~ 1 for this device structure ($A_1 = 1 + (N_A \epsilon_{CdTe})/(N_D \epsilon_{CdS})$ for interface recombination) and the activation energy, ΔE, of the ln J_{01} vs $1000/T$ plot should be ~ 1.2 eV (built-in voltage of the CdS/CdTe junction).[18] Neither of these conditions were met for the $CdCl_2$-treated devices because $A_1 = 1.75$ and $\Delta E = 0.85$ eV, Fig. 5 and Table II. Hence, it is concluded that interface recombination is not the dominant transport mechanism for $CdCl_2$-treated CdTe/CdS devices. If recombination through localized states within the CdTe depletion region is dominant, then a plot of $\ln(J_{01} T^{-2.5})$ vs $1000/T$ should yield an activation energy approximately equal to half of the CdTe band gap.[17,19] Such a plot is shown in Fig. 6, yielding a ΔE value of 0.79 eV, close to half of the CdTe band gap. Hence it is likely that depletion region recombination dominates current transport in the $CdCl_2$-treated cells. Furthermore, the A_1 value of 1.75 suggests that the dominant path of recombination occurs through states displaced either above or below midgap ($A_1 = 2$ for a midgap recombination center). The presence and importance of these states will be discussed later. Note that below 220 K the J-V-T behavior exhibits temperature-independent ln J-V slopes (given by α_1 and α_2 in Table II after correction for series resistance) and weakly temperature dependent diode prefactors (J_{01} and J_{02}), as determined by further computer fitting. These transport characteristics suggest that a tunneling-type behavior is dominant at lower temperatures. Further analysis showed that the observed characteristics at low temperatures were well described by a multistep tunneling model[20] which required $\sim$40–50 tunneling steps through the CdTe depletion region to fit the experimental J-V-T behavior, similar to previously reported results for CdTe.[15] Note that two parallel diodes dictate the low-temperature transport, as indicated in Table II.

The dominant mode of dark current transport in cells processed without $CdCl_2$ was found to be significantly different than the $CdCl_2$-treated cells. Analysis of the J-V-T behavior (above 240 K) of the cells processed without the $CdCl_2$ treatment indicates thermally activated current transport, but with a much lower activation energy of 0.56 eV (Fig. 7) compared to 0.85 eV for the $CdCl_2$-treated cell. This low value of ΔE (slope of ln J_{01} vs $1000/T$) is responsible for the large diode current and J_{01} values observed for the cells processed without $CdCl_2$. Furthermore, the cur-

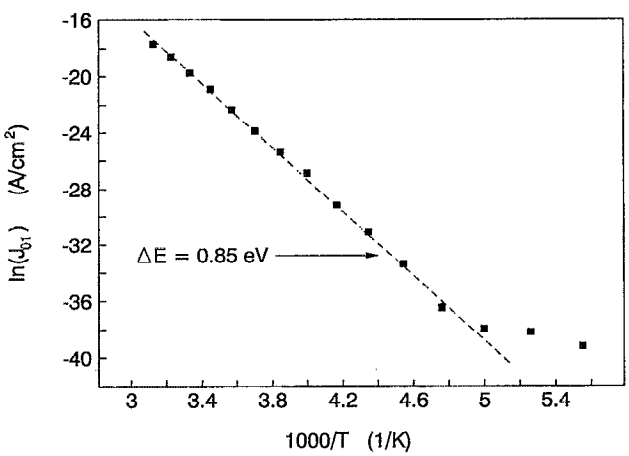


FIG. 5. Plot of ln J_{01} vs $1000/T$ for CdTe/CdS cells having undergone $CdCl_2$ + air anneal.

Downloaded 16 Aug 2011 to 138.253.100.121. Redistribution subject to AIP license or copyright; see http://jap.aip.org/about/rights_and_permissions

TABLE II. Dark J-V-T parameters extracted from fit to Eqs. (2)–(4) for MBE-grown CdTe/CdS solar cell treated with $CdCl_2$ fluxing agent. Diode 1 (subscript 1) represent the higher voltage region of the J-V-T data and diode 2 (subscript 2) represent the lower voltage region of the J-V-T curves. α_1 and α_2 represent the slopes of the ln J-V characteristics and $\alpha_2 = q/A_2kT$ in the table.

T (K)	J_{01}(A cm^{-2})	A_1	α_1 (V^{-1})	J_{02}(A cm^{-2})	α_2 (V^{-1})	R_s (Ω cm^2)
180	9.5×10^{-18}	2.16	29.8	4.3×10^{-13}	9.51	4.0×10^{6}
190	2.6×10^{-17}	2.05	29.8	7.9×10^{-13}	9.71	5.1×10^{5}
200	3.4×10^{-17}	1.90	30.5	2.5×10^{-12}	9.57	1.3×10^{5}
210	1.5×10^{-16}	1.75	31.6	6.5×10^{-12}	9.49	4.0×10^{4}
220	3.2×10^{-15}	1.78	29.6	...	...	9.8×10^{3}
230	3.2×10^{-14}	1.78	28.3	...	...	2.4×10^{3}
240	2.2×10^{-13}	1.77	27.3	...	...	9.5×10^{2}
250	2.1×10^{-12}	1.77	26.2	...	...	3.2×10^{2}
260	9.5×10^{-12}	1.77	25.2	...	...	1.8×10^{2}
270	4.4×10^{-11}	1.77	24.3	...	...	9.8×10^{1}
280	2.0×10^{-10}	1.77	23.4	...	...	6.0×10^{1}
290	8.5×10^{-10}	1.77	22.6	...	...	3.4×10^{1}
300	2.6×10^{-9}	1.75	22.1	...	...	2.4×10^{1}
310	8.1×10^{-9}	1.74	21.4	...	...	1.7×10^{1}
320	2.1×10^{-8}	1.73	21.0	...	...	1.5×10^{1}

rent transport behavior cannot be explained by depletion region recombination (in contrast to the $CdCl_2$-treated cell), interface recombination, or direct tunneling. This is evident from Table III which shows that the diode quality factor (A_1) is >2 and is temperature-dependent (recall that $A_1 = 1.75$ and was independent of temperature for the $CdCl_2$-treated cell), eliminating the possibility of simple depletion region and interface recombination. In addition, the ln J-V slope (α_1) is temperature-dependent and J_{01} is thermally activated (Fig. 7), which eliminates the possibility of direct tunneling as the dominant transport mechanism. Instead, current transport by thermally assisted tunneling of holes from CdTe into interface states followed by interface recombination was found to adequately explain the observed J-V-T behavior of the CdTe/CdS heterojunctions processed without $CdCl_2$. The J-V-T behavior is well described by the tunneling/interface recombination (T/IR) model of Miller and Olsen[21] which approximates the thermally assisted tunneling process by a series combination of direct tunneling and pure interface recombination. According to the T/IR model,[21]

$$J=J_{01}[\exp[C(V-JR_s)]-1]+(V-JR_s)/R_{sh}, \tag{8}$$

$$J_{01}=J_{001}\exp(-\Delta E/kT), \tag{9}$$

$$C=(1-f)B+f/(\xi kT), \tag{10}$$

where ΔE is the thermal activation energy shown in Fig. 7, B is a temperature-independent tunneling parameter, C is the slope of the ln J-V curves, and ξ represents the voltage division between the CdTe and CdS. The value of the f parameter quantifies the degree of tunneling in the observed J-V behavior with $f=1$ representing pure interface recombination and $f=0$ representing direct tunneling. By plotting the experimentally determined values of C ($= q/A_1kT$ in Table III) vs $1000/T$ in Fig. 8, the values of $(1-f)B$ and f/ξ in Eq. (10) were determined to be 10.3 V^{-1} and 0.266, respectively, indicating that the current transport in the cells processed without $CdCl_2$ is lim-

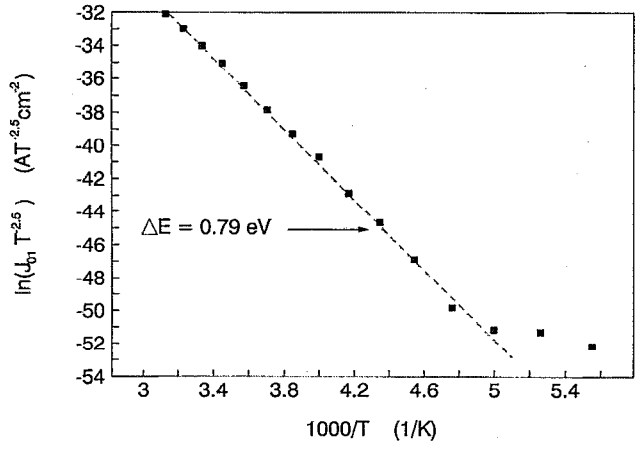


FIG. 6. Plot of $\ln(J_{01}T^{-2.5})$ vs $1000/T$ for CdTe/CdS cells that have undergone $CdCl_2$ + air anneal.

TABLE III. Dark J-V-T parameters extracted from fit to Eqs. (2)–(4) for MBE-grown CdTe/CdS solar cell not treated with $CdCl_2$ fluxing agent. J-V data below 240 K was dominated by resistance terms and are not listed.

T (K)	J_{01}(A cm^{-2})	A_1	R_s (Ω cm^2)
240	2.2×10^{-9}	3.02	3.5×10^{6}
250	4.0×10^{-9}	2.96	8.1×10^{5}
260	9.0×10^{-9}	2.92	2.4×10^{5}
270	2.4×10^{-8}	2.80	8.2×10^{4}
280	8.2×10^{-8}	2.76	2.8×10^{4}
290	2.3×10^{-7}	2.70	1.2×10^{4}
300	4.7×10^{-7}	2.63	6.6×10^{3}
310	9.8×10^{-7}	2.53	4.0×10^{3}
320	2.3×10^{-6}	2.50	1.9×10^{3}

Downloaded 16 Aug 2011 to 138.253.100.121. Redistribution subject to AIP license or copyright; see http://jap.aip.org/about/rights_and_permissions

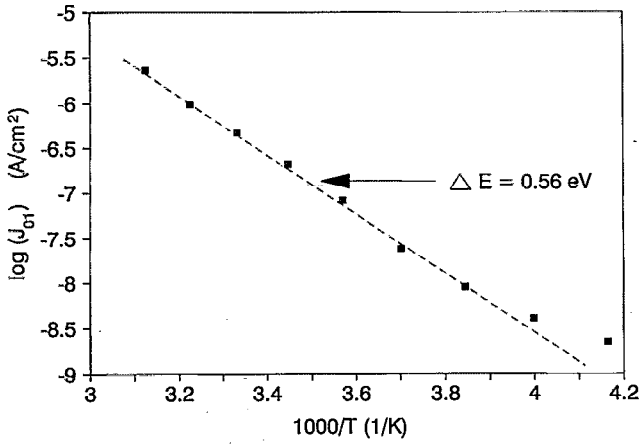


FIG. 7. Plot of $\ln J_{01}$ vs $1000/T$ for a CdTe/CdS cell annealed without $CdCl_2$.

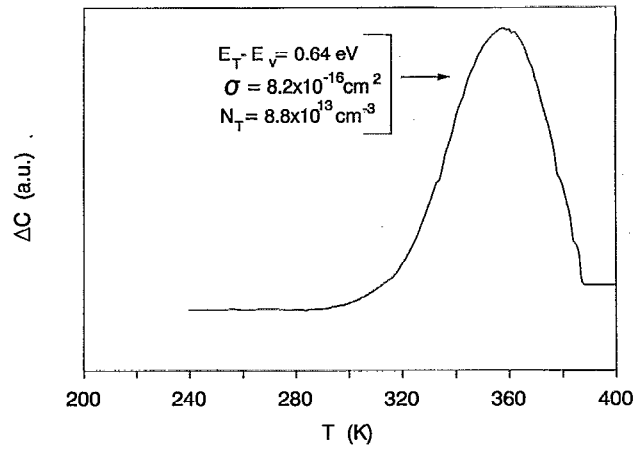


FIG. 9. Typical DLTS spectrum of a CdTe/CdS cell having undergone an air anneal with $CdCl_2$ using a steady reverse bias of -400 mV with a pulse height of 300 mV, a pulse width of 8 ms and a rectangular weighting function with a period of 4 ms.

ited by both interface recombination and tunneling, consistent with the lower barrier height observed for these devices.

Clearly, current transport via thermally assisted tunneling, as described by the T/IR model, significantly worsens cell performance of the CdTe/CdS devices in the absence of the $CdCl_2$ treatment. It is apparent that the $CdCl_2$-induced grain growth is necessary to decrease leakage current and increase V_{oc} via reduction of interface state density near the interface. However, even though the CdTe/CdS interface no longer controls the dark diode current transport after the $CdCl_2$ treatment, the bias dependence of the spectral response after $CdCl_2$ treatment (Fig. 3) indicates that interface recombination may still limit the collection of photogenerated carriers. This suggests that the $CdCl_2$ treatment removes enough interface states to alter the diode transport mechanism and reduce the diode leakage current, but is less effective in removing interface states that limit the photocurrent collection across the CdTe/CdS (recall the bias dependent spectral response, Fig. 3). To identify the origin and better understand the role of process-related defects, DLTS measurements were performed on CdTe/CdS cells processed with and without the $CdCl_2$ treatment and are discussed in the following section.

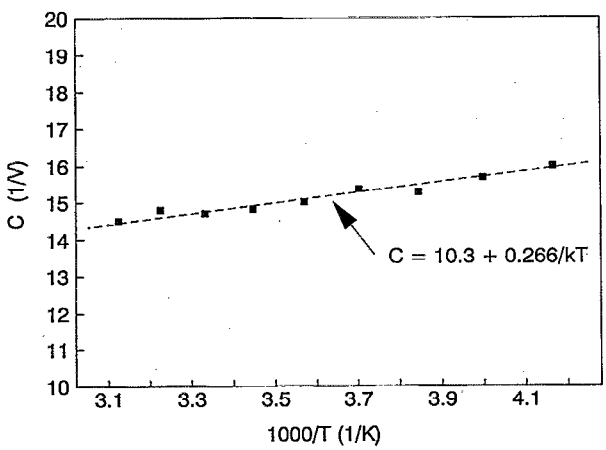


FIG. 8. Plot of the T/IR model C-factor vs $1000/T$ indicating both interface recombination and tunneling limited behavior.

D. Effect of $CdCl_2$ and heat treatment on defect generation in CdTe/CdS heterojunctions

Figure 9 shows a typical DLTS spectrum obtained for a CdTe/CdS device having undergone an air annealing step with $CdCl_2$ which revealed a hole trap peak at $\sim$330 K. DLTS measurements were also performed on CdTe/CdS devices processed without $CdCl_2$, but it was not possible to obtain useful data because of the large series resistance in these samples which dominated the DLTS response. From the Arrhenius plot of $\log(T^2/e_{mp})$ vs $1000/T$, constructed using weighting functions from 4 to 64 ms, the hole trap in the $CdCl_2$-treated device was found to be located at $E_v + 0.64$ eV (± 0.04 eV) with a cross section of 8.2×10^{-16} cm^2 and a trap density of 8×10^{13} cm^{-3} (for the trap shown in Fig. 9). This energy level agrees well with Cd vacancy-related defects such as doubly ionized cadmium vacancies, V_{Cd}^{--}, or singly ionized cadmium vacancy-halogen complexes such as $(V_{Cd}Cl)^-$, both of which have been reported to contribute acceptorlike traps in the range 0.54–0.9 eV above the valence band edge in CdTe after heat treatments.[22–28] Since halogen ions are known to readily form complexes with cadmium vacancies to give deep and shallow levels, it is likely that the $E_v + 0.64$ eV trap results from $(V_{Cd}Cl)^-$ defects.[27,28] However, further measurements are necessary to determine the exact configuration of the defect responsible for this trap.

The presence of acceptorlike traps within the CdTe depletion region was found to adversely affect the CdTe/CdS solar cell characteristics. Figure 10 shows the direct consequences of the density of this defect on the measured V_{oc} and J_{sc} of different CdTe/CdS cells that have under-

Downloaded 16 Aug 2011 to 138.253.100.121. Redistribution subject to AIP license or copyright; see http://jap.aip.org/about/rights_and_permissions

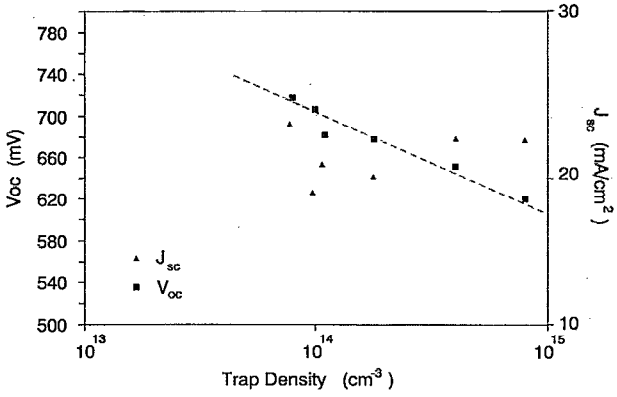


FIG. 10. Measured cell V_{oc} and J_{sc} as a function of 0.64-eV trap concentration for different CdTe/CdS solar cells that have undergone a 400 °C air anneal with $CdCl_2$ as determined by DLTS measurements.

gone the $CdCl_2$ dip followed by heat treatment. It is clear from this figure that the V_{oc} is inversely proportional to the detected trap density while there is no apparent correlation between J_{sc} and the trap density. Presently, it is not clear why the trap density shows a random spatial variation on a given sample with different cells and also from sample to sample since no intentional attempt was made to introduce a variation. It has recently been suggested that such variations can result from nonuniform drying of the $CdCl_2$-methanol solution on the CdTe surface prior to heat treatment.[29] To determine the variation in trap density as a function of depth, DLTS was performed in a multibias mode. A decrease in trap concentration from $\sim 8\times 10^{13}$ cm^{-3} to $\sim 3\times 10^{13}$ cm^{-3} was found as the CdTe/CdS interface is approached by decreasing the depletion width. This is consistent with V_{Cd} and/or Cl diffusion from the CdTe surface into the bulk as a result of the 400 °C anneal. From Fig. 10, it is evident that the variations in V_{oc} must result from the diode leakage current, which was found to increase with increasing trap density, since J_{sc} showed no such dependence. Recalling that diode current transport in the devices processed with $CdCl_2$ is dictated by recombination via deep states within the CdTe depletion region which is characterized by an A factor of 1.75, the off-center position of the trap at $E_v + 0.64$ eV suggests that this level may be responsible for the diode transport mechanism (note that an A factor of 2 represents a midgap or $E_v + 0.75$-eV trap in CdTe[17]) which in turn dictates V_{oc}. Hence, the $CdCl_2$ dip and heat treatment greatly improves the cell performance via grain growth, interface state density reduction, and transport mechanism modification, but this process also appears to limit V_{oc} by cadmium vacancy-related defect formation. Further increases in V_{oc} and efficiency can be expected if the generation of this defect can be reduced or eliminated. This may require further modification or optimization of the current cell processing schemes.

IV. CONCLUSIONS

In this paper, the beneficial and adverse effects of the standard $CdCl_2$ dip followed by a postdeposition heat treatment on the material and device properties of MBE-grown polycrystalline CdTe/CdS solar cell structures were investigated and quantified. As expected, the $CdCl_2$ treatment induced CdTe grain growth and significantly improved cell efficiency from 1.3% to 8.6%. SPV and spectral response measurements showed that the improvement in J_{sc} after $CdCl_2$ treatment was partly due to enhanced carrier collection resulting from increased carrier collection length and improved CdTe/CdS interface quality. However, even after the $CdCl_2$ treatment, the photocurrent demonstrated significant bias dependence, suggesting that J_{sc} was still limited by interface recombination, although to a lesser extent compared to cells processed without $CdCl_2$. Analysis of the dark J-V-T characteristics showed that in contrast to the photocurrent, the dark diode I-V characteristics showed a clear change in dominant transport mechanism, changing from an interface recombination/tunneling process to depletion region recombination after $CdCl_2$ treatment. The change in transport mechanism resulted in an increase in barrier height and reduced leakage current. DLTS measurements showed that depletion region recombination probably occurs through a large density of deep states at $E_v + 0.64$ eV which result from the formation of Cd-vacancy related defects during the $CdCl_2$ dip and heat treatment process that are tentatively attributed to a $(V_{Cd}Cl)^-$ defect complex resulting from the interaction between cadmium vacancies introduced by the heat treatment and chlorine from the $CdCl_2$. The cell V_{oc} was found to be inversely related to the density of this trap. Hence, even though the $CdCl_2$ treatment is very important for improving CdTe/CdS cell performance, it appears to introduce a V_{oc} and efficiency-limiting defect whose role must be studied in more detail or whose presence must be removed to achieve CdTe/CdS cell efficiencies beyond 12%–13%.

ACKNOWLEDGMENTS

The authors are grateful to R. Sudharsanan for bias-dependent spectral response measurements and useful discussions, K. S. Ringel of Kimberly-Clark Corp. and B. Bramlett for SEM measurements, and P. V. Meyers and C. H. Liu of Ametek Corp. for cell fabrication. This work was supported by SERI Contract No. XL-7-06031-1.

[1]P. V. Meyers, Solar Cells **24**, 35 (1988).
[2]R. W. Birkmire, *Proceedings of the 1989 Polycrystalline Thin Film Program Review Meeting* (1989), p. 77.
[3]T. L. Chu, S. S. Chu, S. T. Ang, K. D. Han, Y. Z. Liu, K. Zweibel, and H. S. Ullal, *Proceedings of the IEEE 19th Photovoltaic Specialists Conference* (IEEE, New York, 1987), p. 1466.
[4]Y. K. Jun and H. B. Im, J. Electrochem. Soc. **135**, 1658 (1988).
[5]A. Rohatgi, *Proceedings of the 1989 Polycrystalline Thin Film Program Review Meeting* (1989), p. 45.
[6]J. S. Lee and H. B. Im, J. Mater. Sci. **21**, 980 (1986).
[7]J. S. Roh, and H. B. Im, J. Mater. Sci. **23**, 2267 (1988).
[8]J. T. Moon, K. C. Park and H. B. Im, Solar Energy Mater. **18**, 53 (1988).

Downloaded 16 Aug 2011 to 138.253.100.121. Redistribution subject to AIP license or copyright; see http://jap.aip.org/about/rights_and_permissions

[9]P. V. Meyers, C. H. Liu, and T. J. Frey, U.S. Patent #4,710,589 (1987).
[10]S. A. Ringel, R. Sudharsanan, A. Rohatgi, and W. B. Carter, J. Electron. Mater. **19**, 259 (1990).
[11]P. Blood, J. Appl. Phys. **58**, 2288 (1985).
[12]H. J. Hovel, *Solar Cells, in Semiconductors and Semimetals, 13* (Academic, New York, 1975).
[13]A. Rohatgi, J. R. Davis, R. H. Hopkins, and P. G. McMullin, Solid State Electron. **23**, 1039 (1983).
[14]B. M. Basol, J. Appl. Phys. **58**, 3809 (1985).
[15]K. W. Mitchell, A. L. Fahrenbruch, and R. H. Bube, J. Appl. Phys. **48**, 4365 (1977).
[16]M. Roy, S. Damaskinos, and J. E. Phillips, *Proceedings of the 20th IEEE Photovoltaic Specialists Conference* (IEEE, New York, 1988), p. 1618.
[17]A. L. Fahrenbruch and R. H. Bube, *Fundamentals of Solar Cells* (Academic, New York, 1983).
[18]A. Rothwarf, IEEE Trans. Electron. Dev. **29**, 1513 (1982).
[19]J. B. Yoo, A. L. Fahrenbruch and R. H. Bube, J. Appl. Phys. **68**, 4694 (1990).
[20]A. R. Riben and D. L. Feucht, Int. J. Electron. **20**, 583 (1966).
[21]W. A. Miller and L. C. Olsen, IEEE Trans. Electron. Dev. **31**, 654 (1984).
[22]F. A. Kroger, Rev. Phys. Appl. **12**, 205 (1977).
[23]S. S. Ou, A. Bindal, O. M. Stafsudd, K. L. Wang, and B. M. Basol, J. Appl. Phys. **55**, 1020 (1984).
[24]P. Hoschl, P. Polivka, V. Prosser, M. Vanecek, and M. Skrivankova, Rev. Phys. Appl. **12**, 229 (1977).
[25]E. N. Arkadyeva and O. A. Matveev, Rev. Phys. Appl. **12**, 239 (1977).
[26]L. C. Isett, J. Appl. Phys. **56**, 3508 (1984).
[27]N. V. Agrinskaya and O. A. Matveev, Rev. Phys. Appl. **12**, 235 (1977).
[28]K. Zanio, *Cadmium Telluride*, in *Semiconductors and Semimetals*, 13 (Academic, New York, 1978).
[29]B. N. Baron, R. W. Birkmire, J. E. Phillips, W. N. Shafarman, S. S. Hegedus, and B. E. McCandless, Final Report to Solar Energy Research Institute, Contract No. XL-9-19032 (1990).

Downloaded 16 Aug 2011 to 138.253.100.121. Redistribution subject to AIP license or copyright; see http://jap.aip.org/about/rights_and_permissions