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Fabrication of ultra thin CdS/CdTe solar cells by magnetron sputtering

By

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An abstract of

Fabrication of ultra thin CdS/CdTe solar cells by magnetron sputtering

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CdTe is a nearly perfect absorber material for second generation polycrystalline solar cells because the bandgap closely matches the peak of the solar spectrum, relatively high absorption coefficient and good electronic properties in the polycrystalline phase. Fabricating high-efficiency CdS/CdTe solar cells with an ultra-thin absorber layer is a challenging yet highly desirable step in improving CdTe technology. Most of today's CdTe solar cells utilize an absorber layer which is about 2.5 μm to 8 μm thick. Thinning this layer down typically results in poorer cell performance due to shunting, incomplete photon absorption, fully depleted CdTe layer or interference between the main and the back contact junction when the CdTe layer thickness approaches a certain limit. While some of these losses are fundamental, others can be minimized by careful optimization of the fabrication steps.

In this dissertation I present the results of such optimization. Magnetron sputtered CdS/CdTe solar cells with the absorber layer thicknesses from 2.6 μm to 0.3 μm were studied. The deposition process itself and all the post-deposition parameters such as the $CdCl_2$ treatment, thickness of the Cu layer in the thermally evaporated Cu/Au back contact, and the back contact thermal activation/diffusion time for a given CdTe layer thickness were optimized to achieve the top performance for the cell of a given thickness. 13.5 % efficiency cells with 2.5 μm CdTe, 12% cells with 1 μm CdTe, 9.7% cells with 0.5 μm CdTe and 6.7% with 0.3 μm CdTe were fabricated.

Acknowledgements

I would like to thank my colleagues in the labs of the University of Toledo, graduate students, participants of the REU program, Physics and Astronomy faculty and staff members, and specifically my advisor Dr. Alvin Compaan for their help in getting this work done.

I would also like to acknowledge a very substantial contribution made by Dr. Kristopher Wieland in the form of writing the LabView applications for the temperature-dependent J-V system and very helpful discussions of the results obtained with this setup.

Table of Contents

List of Figures

List of Tables

Chapter 1: Introduction

1.1. Preface

Today the world heavily relies on the energy produced by burning fossil fuels such as oil, coal and natural gas. The world population continuously increases and so does the energy demand. At the same time, the peak supply from those conventional energy sources has already been achieved in the recent past or is about to be achieved with within the next 20 to 50 years according to different studies [1]. In addition the concentration of greenhouse gases in the Earth's atmosphere caused by emission from burning of the fossil fuels has achieved the point than it significantly impacts the climatic changes around the world, known as a global warming, and keeps on rising [2]. Therefore, we, as a society, are in need of developing and implementing an efficient and large-scale source of alternative energy.

Renewable Energy Sources as defined by the United States Department of Energy (DOE) are the sources of energy which are constantly replenished and will never run out [3]. Not only are those sources abundant, but they are also cleaner and include hydroelectric, geothermal, biomass, wind, hydrogen and solar energy. Each of these alternative solutions has its own advantages and limitations, usually in regards to geographical location, the amount of landmass required to produce enough energy and the potential environmental impact. It is the most likely scenario that all these alternative energy sources will be used in a complementary fashion and the share of each will be

defined by the state of technology present, as well as economic and environmental arguments. Further I will restrict the discussion to solar energy and more specifically – *photovoltaics* (PV) which is the field of technology and research related to the application of solar cells for energy by converting sunlight directly into electricity.

1.1. Photovoltaics

Sunlight is the most abundant and the most widely available source for power production. The energy from the sun can be used in passive heating systems in buildings which utilize materials that absorb the heat energy from the sun as well is in active *PV systems*. A typical PV system consists of a large number of individual *PV cells* packaged into a *PV module*, often electrically connected in multiples as *PV arrays* to convert the energy from the sun into electricity. PV cells and therefore PV modules and PV arrays produce *direct current* (DC) power, therefore, in most cases they are connected to the *alternate current* (AC) grid through the appropriate *power inverter*.

The PV cell or a *solar cell* is a smallest building block of a photovoltaic system. Generally it can be a semiconductor device, utilizing the physical properties of a *p-n junction*, a *dye-sensitized solar cell* which is an electrochemical system consisting of a dye-sensitized semiconductor and electrolyte, or an organic solar cell in which the active layer of the device is made of organic molecules. Currently the semiconductor based-devices are the most efficient among those categories, the dominant players in the current PV market and likely to retain this position in future as well. They in turn can be classified into three generations that indicate the order of which each became important:

First generation – single-crystalline, single junction Si cells. These cells and modules are the most highly represented in on the market, accounting for 89.6% of 2007 production.

Second generation – polycrystalline thin film or amorphous silicon devices. These devices have been developed to address energy requirements and production costs of solar cells. Several different deposition techniques such as chemical vapor deposition, sputtering, electroplating or screen printing are advantageous as they reduce the manufacturing cost significantly. Second generation technologies are expected to gain market share in 2008. The most successful second generation materials are *cadmium telluride* (CdTe) that has proven its potential for high scale manufacturing [4] and *copper indium gallium selenide* (CIGS) that although currently holding a record efficiency for the second generation laboratory scale cells, has not seen a major commercial success yet. *Amorphous silicon* and *micromorphous silicon* are also promising.

Third generation – aim to enhance mediocre electrical performance of second generation while maintaining very low production costs. There are a few approaches to improve efficiency: spectrum splitting (multijunction solar cells), modifying the incident spectrum (by using concentrators for example), multiple electron-hole pair generation by a single photon, and some others.

At present there is concurrent research into all three generations while I will be focusing specifically on CdTe PV which is a representative of the second generation technology.

1.2. Solar cell basics

Second generation PV, just like the first generation, relies on the properties of the p-n junction to separate electron-hole pairs generated by the incident light in the *absorber layer*. In the case of CdS/CdTe solar cells, the p-n junction is formed between the CdTe p-type absorber and the n-type CdS which is often called a *window layer* and heterojunction partner. Unlike crystalline solar cells where the wafer itself provides a desired mechanical support for the whole device, thin film polycrystalline solar cells are usually grown on a foreign substrate, typically glass, polymer or stainless steel. With respect to this there are two different configurations of solar cells normally referred to as *substrate* and *superstrate*.

In substrate configuration cells, the substrate underlies the cell structure while the sunlight enters the device from the other side through the window layer with a metal grid structure (Figure 1-1 a). In this case the deposition sequence is the following: substrate – back contact (BC) – absorbed layer – window layer – transparent conductive oxide (TCO) for the front contact – metal current collecting grid. The substrate configuration is the most typical for CIGS solar cells and some a-Si solar cells while CdTe devices are rarely made this way due to specifics of the back contact (BC) fabricating process which is highly temperature-dependent and therefore preferred to be the last fabrication step

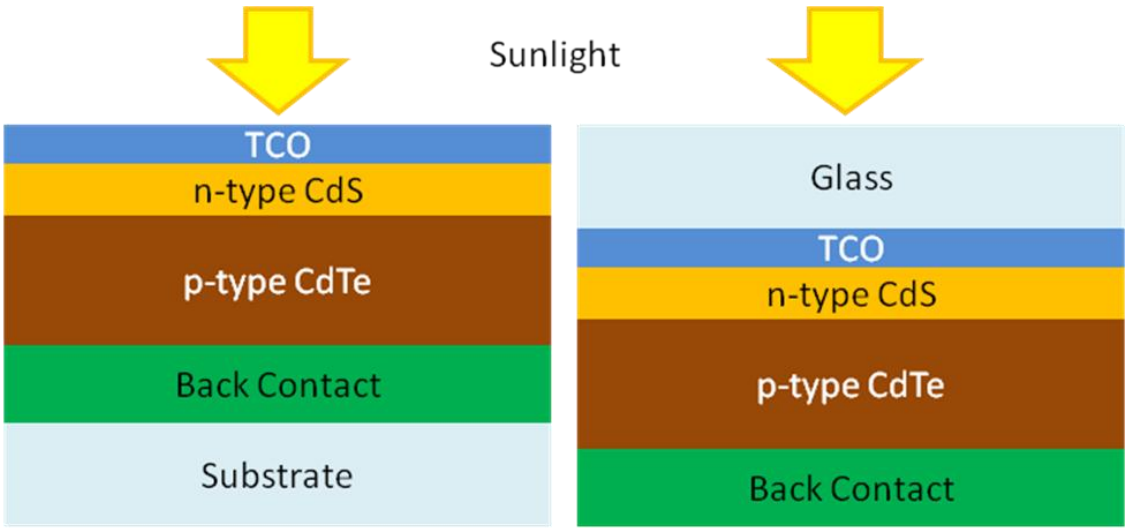

Figure 1-1. Substrate (a), and superstrate (b) configurations of a CdS/CdTe solar cell

Instead, the superstrate configuration is preferred for CdTe. In this case light enters the solar cell from the substrate side which is typically made of glass or a transparent polymer. Some commercially available glasses like Pilkington TEC glasses already have a SnO_2:F TCO coating, therefore the fabrication process may or may not include the TCO deposition, followed by CdS window layer, CdTe absorber layer and the BC layer(s) (Figure 1-1 b).

In both superstrate and substrate cases light is absorbed in the CdTe layer generating electron-hole pairs that are separated by the electric field at the p-n junction and then collected from the front (TCO) and BCs. A typical current-voltage (J-V) characteristic, along with some important numbers that can be derived from it, is shown in the Figure 1-2. The most important parameter of any solar cell, also called the first-level metric is efficiency (Eff). It is typically measured in % and represents the ratio of the electric power output of the solar cell to the total incident radiation (P_{Inc}) power

received by the cell. Power generated by a solar cell can be represented as a product of three other important figures of merit that are: the short-circuit current density (J_{SC}), the open-circuit voltage (V_{OC}) and the fill factor (FF). The FF is measured in % and represents the "squareness" of the J-V characteristics and rigorously defined as $(V_{MP} \cdot J_{MP})/(V_{OC} \cdot J_{SC})$, where V_{MP} amd J_{MP} represent the current density and voltage at the maximum power point. J_{SC}, V_{OC} and FF complete the second-level metrics of a solar cell.

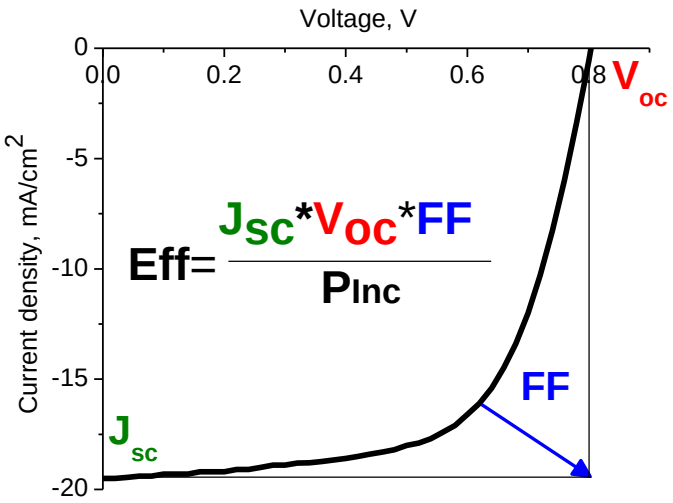

Figure 1-2. J-V characteristics of a solar cell.

Second-level metrics can be further broken down into the third-level metrics that would be losses in J_{SC} (glass reflection and absorption, TCO absorption, CdS absorption and deep penetration losses), V_{OC} (recombination) and FF (recombination, shunts, high series resistance, voltage-dependent collection).

I will use first-, second- and third-level metrics to characterize the cell performance dependence on CdTe layer thickness throughout this dissertation.

1.3. Ultra-thin CdTe challenges

One of the greatest advantages of the second generation PV over its predecessor is that the thicknesses of the semiconductor layers and therefore the amount of raw semiconductor material needed to fabricate a device is already decreased by orders of magnitude by depositing a thin active semiconductor layer on a relatively cheap and readily available substrate. Yet there is a constant driving force in CdTe-based PV to decrease the thickness of CdTe layer from 2 μm to 5 μm, typical of today's technology, to less than 1 μm by fabricating ultra-thin, high efficiency solar cells. Unfortunately, reduction of the CdTe layer thickness often leads to decrease of cell performance and a certain strategy along with some optimization techniques should be applied to the fabrication process.

From the physics point of view there are several reasons for the lower performance of the thin cells. Below I will give a brief summary of those with some comments on their relative importance for this work and their current understanding in photovoltaic community.

1. Deep penetration losses.

CdeTe is a direct band semiconductor with a relatively high absorption coefficient (Figure 1-3a). Yet, for the near-infrared light, right above the bandgap of the material (1.45 eV, or 850 nm) the absorption length becomes greater than 1 μm, and for the light with the wavelength of 600 nm it is about 0.7 μm (Figure 1-3b). Therefore, cells with absorber layer thinner than 1 μm will be semi-transparent for the long wavelength part of the solar spectrum and the losses of the photogenerated current associated with this

transparency above the bandgap of the semiconductor are known as deep penetration losses.

Deep penetration losses are well understood and depend on the absorption coefficient which is a fundamental property of the semiconductor that does not vary much except sharpening of the absorption edge that may occur during postdeposition treatment [5] and some CdS/CdTe interdiffusion that often occurs near the p-n junction [6] that will be discussed later. No specific strategies to minimize deep penetration losses are normally used in CdTe technology since cells are rarely made thin enough so the incomplete absorption becomes the major factor limiting the overall performance. Although some approaches, such as use of a back reflector [7] or textured glass substrate [8] to increase the optical path within the cells can be borrowed from amorphous silicon technology if necessary. As a matter of fact, it is likely that the rough surface of TEC glasses and gold BC are capable of making some contribution to minimization of the deep penetration losses by enhancing the optical path of the photons within

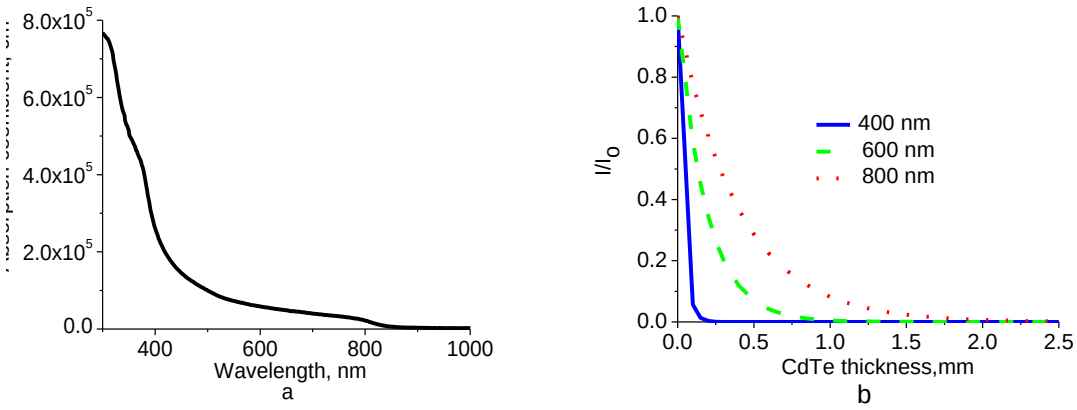

Figure 1-3. CdTe absorption coefficient (from [9]) and (b) calculated absorption profiles for the light with

2. Pinholes.

Pinholes are known to be one of the major problems for large-area devices and this problem is common for all present thin-film technologies. A pictorial view of a pinhole is shown on the Figure 1-4a along with an optical microscope image of a real defect (Figure 1-4b). If there is a pinhole in a semiconductor layer(s), the metal from the BC can fill it creating either a direct or a weak shunting of the p-n junction.

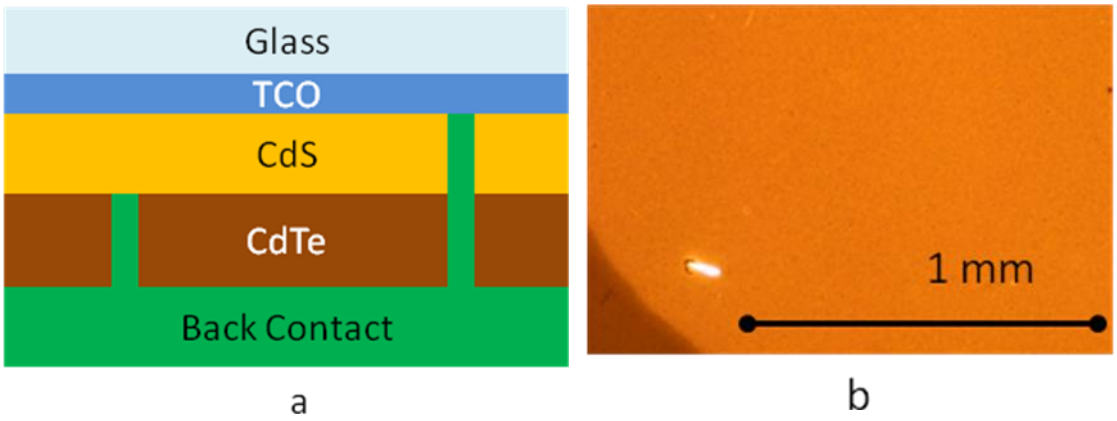

Figure 1-4. (a) sketch of two types of pinholes and (b) optical image of a real pinhole in transmitted light with some top illumination (the pinhole is very close to the edge of the gold coated, 3mm diameter dot cell).

Pinholes can be divided into subcategories: they can be present in CdS or CdTe layers separately, or can extend throughout the whole p-n structure. (See Figure 1-4a). Also they may arise during the deposition process as a result of poor substrate cleaning or dust particles accumulated on the substrate inside the deposition chamber or they can be created by inappropriate handling of the sample during the post-deposition steps. In some cases they also can be an integral part of the film nucleation and growth process or may arise during $CdCl_2$ treatment from recrystallization or local delamination.

In general, while being very specific to the particular deposition technique, pinholes are more likely to appear in very thin layers and therefore are very important to consider for this work. Even though there are established methods (e.g. use of high resistivity transparent (HRT) layer [10, 11], pinhole filling with negative photoresist) and currently researched methods (e.g. aniline treatment [12]) for pinhole passivation, understanding the reasons for their appearance and preventing it from happening is rated very high in the photovoltaic community.

In Chapter 2 I will discuss my observation of pinhole density variations correlated with sputtering chamber maintenance procedures and will give a plausible explanation for this phenomenon based on substrate self-bias measurements.

3. Weak (reach-through) diodes.

The theory of nonuniformities in large-scale PV that can be treated as random diodes arrays is presented in [13]. A weak diode is another type of imperfection in a photovoltaic device that can demonstrate a shunt-like behavior. The idea is that a large-area cell can be represented by a two-dimensional array of individual diodes wired in parallel (Figure 1-5a). Each diode is characterized with its own parameters, such as reverse saturation current which leads to variations in diode J-V curves. If the variations are small there is no huge negative effect, while if a certain diode has a very low turn-on voltage, it will find itself drawing the current in the opposite direction to the rest of the network, robbing the net photo generated current and cause a shunted-like behavior of the cell (Figure 1-5b). It is suspected that reach-through diodes are more likely to appear in ultra-thin devices and therefore should be considered as a plausible explanation for the overall poorer performance of such thin cells.

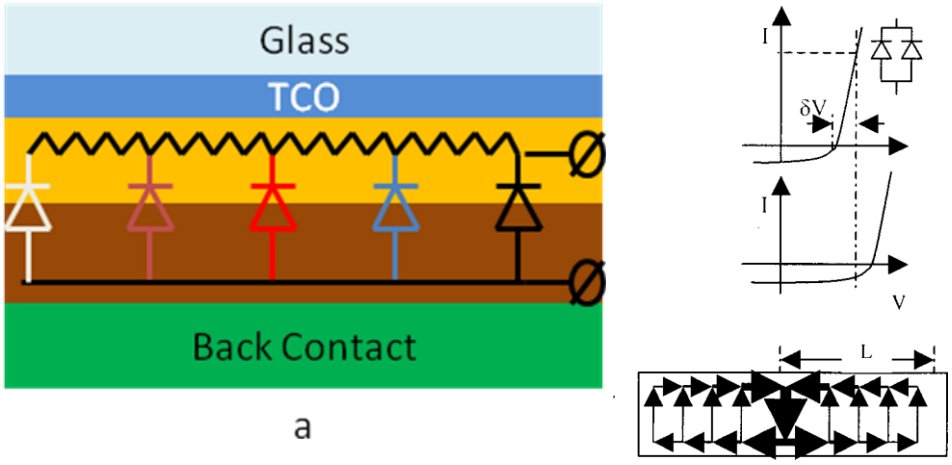

Figure 1-5. (a) random diode array; (b) mechanism of current "robbery" (from [13]).

4. Fully depleted layers.

This phenomenon is more fundamental and generally well understood in the scope of typical semiconductor physics. (See [14] for instance).

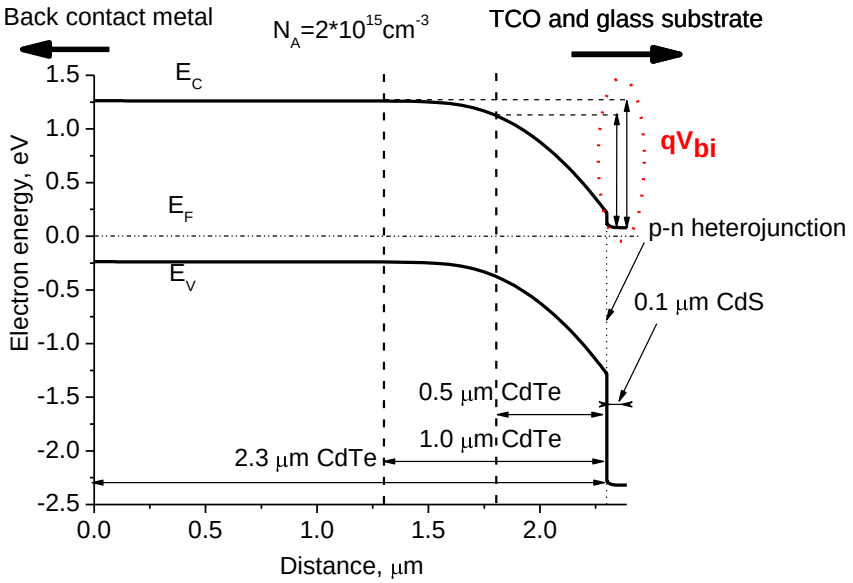

Figure 1-6. CdS/CdTe band diagram (with the influence of back contact neglected) for $N_A=2*10^{15}$ cm^{-3}. Barrier height qV_{bi} for 2.3 μm, 1.0 μm and 0.5 μm CdTe is shown in the upper right corner (modeled by SCAPS 2.5).

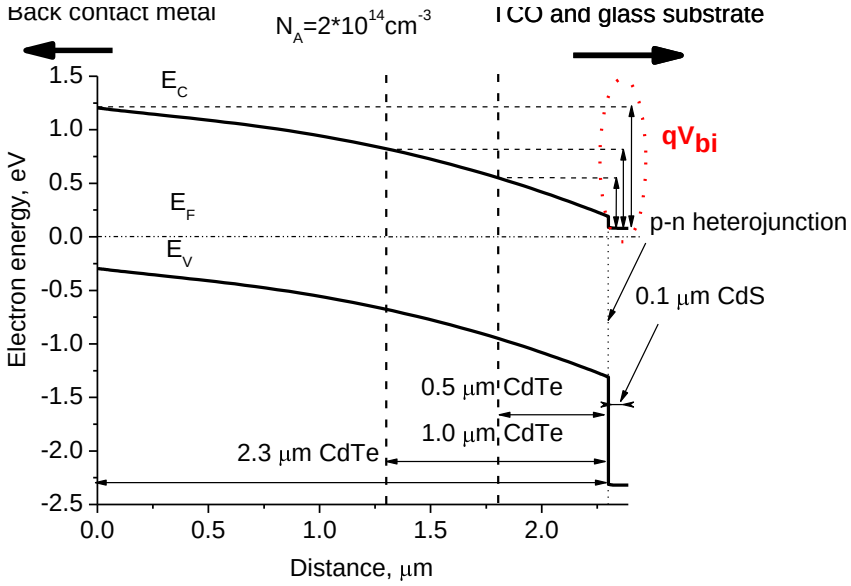

Figure 1-7. CdS/CdTe band diagram (with the influence of back contact neglected) for N_A=2*10^{14} cm^{-3}. Barrier height qV_{bi} for 2.3 μm, 1.0 μm and 0.5 μm CdTe is shown in the upper right corner (modeled by SCAPS 2.5).

Both CdS and CdTe are known to be hard to achieve high doping density, due to self-compensation mechanisms [15]. This is especially true for the case of CdTe where experimentally determined doping levels are typically in 10^{13} cm^{-3} to 10^{15} cm^{-3} range [16]. Therefore the depletion region may extend half-way through or even deeper into the CdTe layer for the case of relatively "thick" cell (2…3 μm), but a thinner layer of CdTe can be fully depleted. A similar situation may occur on the CdS side of the junction as well if the layer is made very thin in order to maximize its transparency. Figure 1-6 and Figure 1-7 show thermal equilibrium dark band diagrams (modeled with SCAPS 2.5 software [17]) for the CdS/CdTe part of the cell for two CdTe acceptor concentrations N_A=2*10^{15} cm^{-3} and N_A=2*10^{14} cm^{-3} correspondingly. The influence of the back-contact-related Schottky barrier is neglected so the depletion width for the both cases can be

determined by the valence band E_V and conduction band E_C bending. The diagrams are drawn for the case of a 2.3 μm CdTe layer, but the 1 μm and 0.5 μm cross-sections are shown for comparison. It can be seen from Figure 1-6 and Figure 1-7 that thin cells with a relatively low doping concentration will have lower V_{OC} since is proportional to the main junction barrier height qV_{bi}.

5. Proximity of the front and back junctions.

CdTe is a semiconductor with an extremely high electron affinity (5.6 eV) that makes it nearly impossible to find a metal with a workfunction high enough to provide the conditions for formation of an ohmic contact. Instead, a Schottky barrier with a typical height of about 0.4 eV normally originates at the CdTe/BC interface [18].

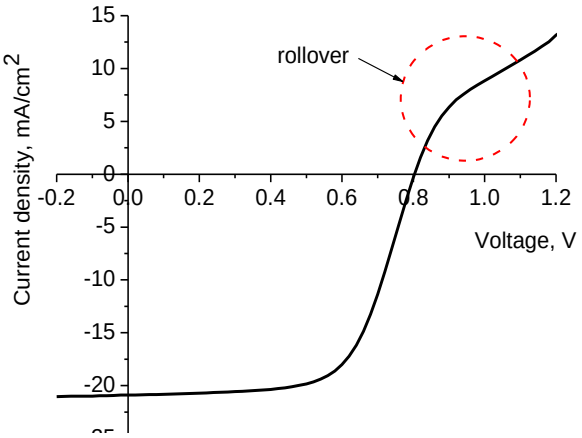

Figure 1-8. CdS/CdTe cell J-V curve with a noticeable rollover.

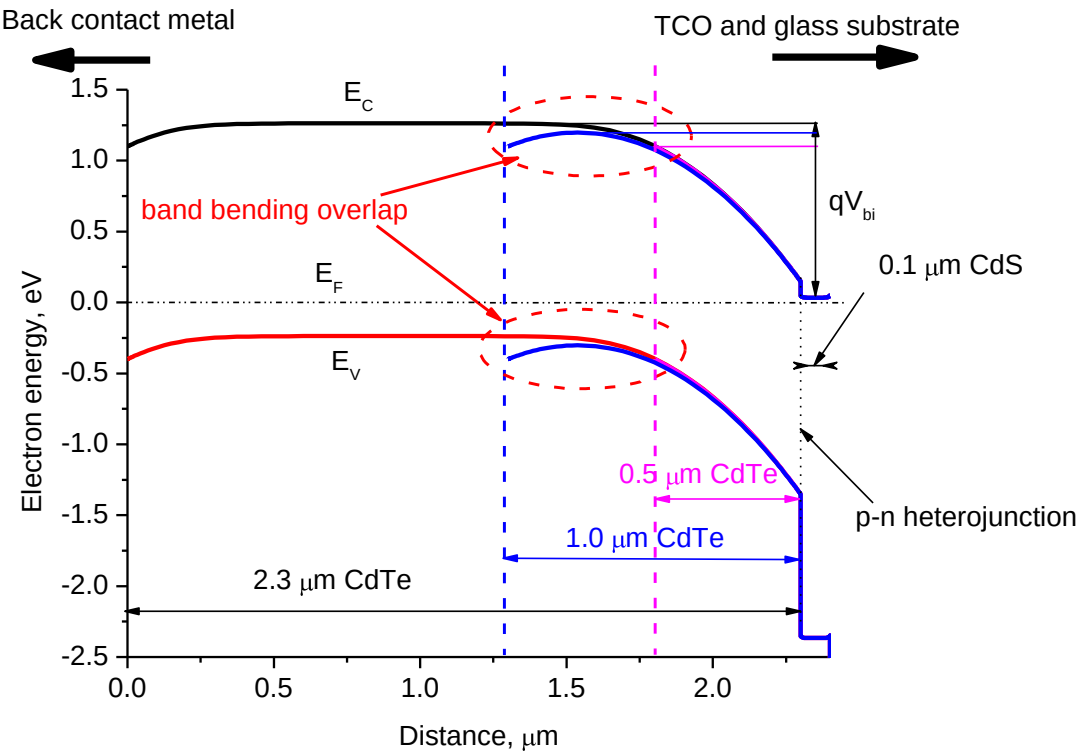

Figure 1-9. Band diagram of the CdS/CdTe cell with band bending from the main and back contact junction overlapping in 1.0 μm CdTe (modeled by SCAPS 2.5).

This Schottky diode is connected in series but in the reverse direction with the main photovoltaic CdS/CdTe junction and causes a saturation of the J-V curve in the first quadrant typically referred as a "rollover" (Figure 1-8) [19]. This effect is observed in the majority of CdTe cells, especially at low temperatures when the thermionic emission of holes over the Schottky barriers is suppressed. In the case of the ultra-thin cell, in addition to the rollover which often does not affect solar cell performance in its normal operation regime (4th quadrant of the J-V curve), another, more dramatic effect can be observed. Figure 1-9 shows the overlapping of the band bending regions in CdTe near the main and the BC junctions that are now in a close proximity to each other (SCAPS

simulation is done for 1.0 μm CdTe with $N_A=2*10^{15}$ cm^{-3}, and back barrier of 0.4 eV in dark at thermal equilibrium). This situation results in lowering of the built-in potential across the device that can be represented as the maximum difference between the CdS and CdTe conduction band minima. That in turn, leads to an additional drop in V_{OC} that is often observed in ultra-thin devices.

6. Cu shunting and accumulation in CdS layer.

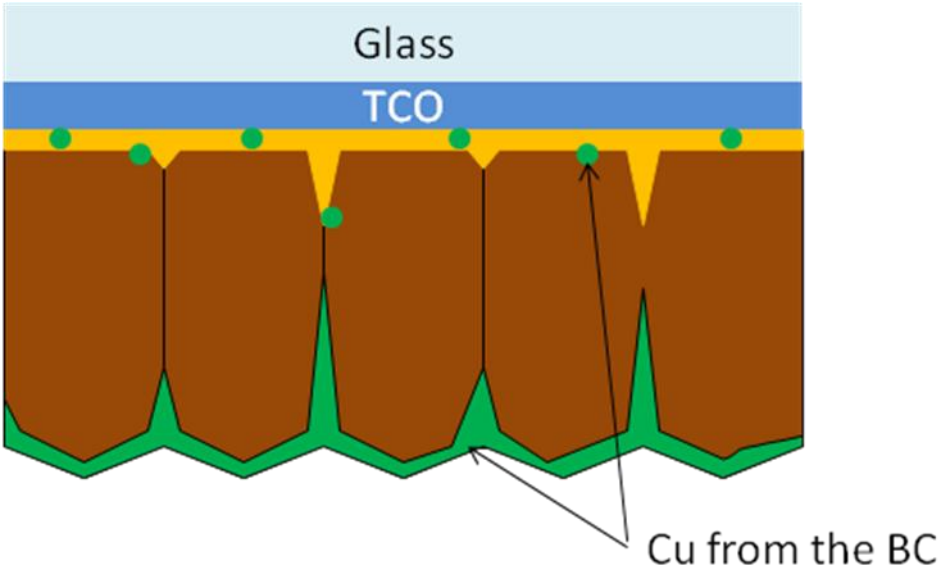

Figure 1-10. Cu diffusion along CdTe GB and accumulation in CdS.

Cu is used in the majority of successful cell fabrication schemes as a p-type dopant that helps to overcome the back-barrier problem by making the depletion width narrower and therefore changing the shape of the potential barrier and making it more suitable for holes to tunnel through. On the other hand, Cu is often blamed for the cell degradation and while it can be found in several chemical states within the device [20], and its migration kinetics are fairly complex [21, 22], it is plausible to expect that ultra-thin cells are more susceptible to the degradation associated with Cu migration from the BC. While diffusing along the grain boundaries (GB) Cu can create direct shunts of the p-

n junction, or accumulate in the CdS layer causing the reduction of V_{OC} and FF [23, 24] (see Figure 1-10).

1.4. Conclusions

Today second-generation PV and especially CdTe-based solar cells are becoming a major player on the PV market and an important component of the alternative energy portfolio for the future. Even now there is a strong interest in the PV community to decrease the thickness of CdTe layers to 1 μm and below and this issue will only become more important by the time the mass production of CdTe modules reaches the terra-watt scale. While some break-through approaches to increase ultra-thin cell efficiency are always desired and are likely yet to come in CdTe technology, I will show that careful optimization of the existing technology can lead to a considerable scaling down of the CdTe thickness (1 μm to 0.7 μm or less) with little sacrifice in efficiency. In this dissertation I will present the results of such optimization for cells with submicron thickness based on the University of Toledo "standard" 2.4 μm CdTe magnetron sputtered cell technology. The thesis is organized as follows:

In Chapter 2 I will give an overview of the magnetron sputtering process with some important results on the potential distribution inside the chamber.

In Chapter 3 I will describe the fabrication steps of the standard UT cells, present results on high-rate magnetron sputtering and describe the CdTe film structural properties dependence on the sputtering power and the sputtering gas pressure.

Chapter 4 deals with the optimization of the CdS window layer. I will present a study on the optimum CdS thickness for cells grown on SnO_2-coated soda-lime glass

substrates with and without a high resistivity transparent (HRT) layer. I will show that choosing the optimum CdS thickness leads to maximizing J_{SC} without significant decrease of V_{OC} and FF.

Chapter 5 describes the optimization of thickness-dependent $CdCl_2$ postdeposition treatment as well as the optimization of the back contact scheme that includes dependence on as-deposited Cu thickness and Cu diffusion time.

In Chapter 6 I will present some observations related to the back contact, such as Cu distribution within the CdTe layer, study of the cell performance dependence on the amount of Cu and back contact thermal activation time; and propose a novel concept of using a CdS back "buffer" layer.

Chapter 7 concludes this thesis and contains the summary of the work done along with future considerations.

Chapter 2: Potential distribution inside the magnetron sputtering plasma

2.1 Introduction

Radio frequency (RF) magnetron sputtering is a vacuum, plasma-assisted deposition process [25] used at the University of Toledo to fabricate CdS/CdTe cells. Figure 2-1 provides in-plane and cross-sectional views of a magnetron sputtering system. The RF signal is applied between the ground shroud and chamber walls that represent electrical ground and the sputtering target that contains a set of magnets as pictured. Depending on the relative strength of the magnets, the configuration of the magnetic field can vary from "balanced" when the lines start from the center magnet and end on the outer magnets or "unbalanced" when some of the lines extend closer to the substrate and end on the back side of the outer magnets. Both configurations are sketched in Figure 2-1. In the balanced configuration magnets are alternated with "blanks" made of magnetically soft Fe. The semiconductor (CdS or CdTe) target is mounted on top of the sputtering gun. The balanced magnetron configuration leads to a higher plasma density near the target surface and often allows a higher target utilization, while the unbalanced configuration increases the ion bombardment of the substrate and can be responsible for changes in the film morphology and electronic properties [26].

Ar is used as the sputtering gas and the typical deposition pressure is within the 5 mTorr to 30 mTorr range. Once the plasma is ignited after applying of the RF signal, Ar^+ ions bombard the target and sputter Cd, Te, S atoms or dimers of Te_2 or S_2 towards the

substrate held a few centimeters away from the target. Magnetron sputtering offers a wide range of tweaking opportunities to create thin films with desired physical properties. The magnetron configuration, deposition pressure, RF power, substrate temperature and the substrate bias are among the parameters that can be finely tuned and influence physical and electrical properties of the thin films [27].

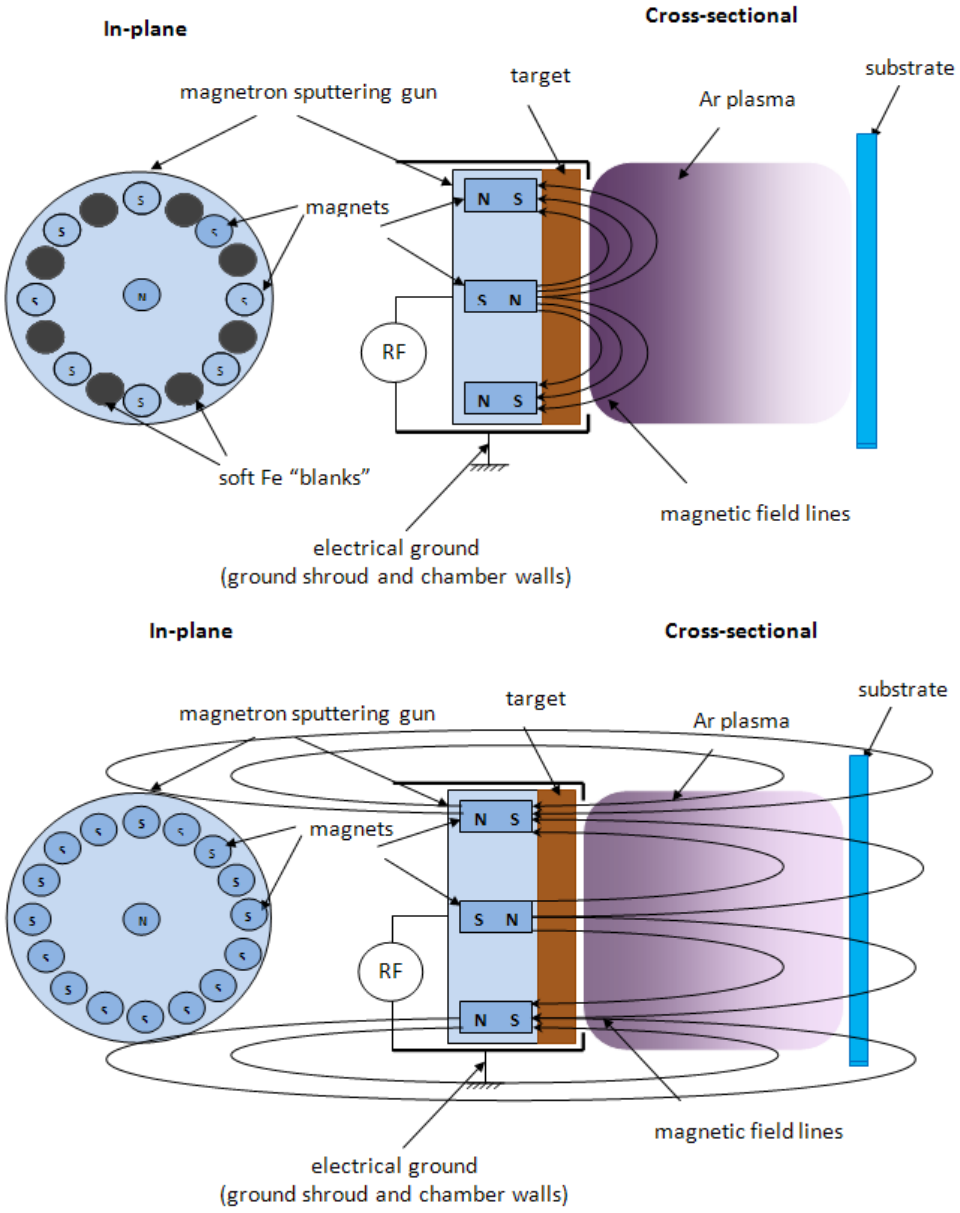

Figure 2-1. In-plane and cross-sectional views of the balanced (top) and unbalanced (bottom) magnetron sputtering system.

Without good understanding of the plasma processes though, the sputtering may become excessively complicated and produce rather confusing results. One of the ways to better characterize the plasma process is to measure in-situ the potential distribution inside the sputtering chamber. These measurements are essentially more fundamental than the typical process control data from pressure gauges and power meters and help with better understanding of the properties of the deposited films dependence on the sputtering regimes.

2.2 Experimental setup

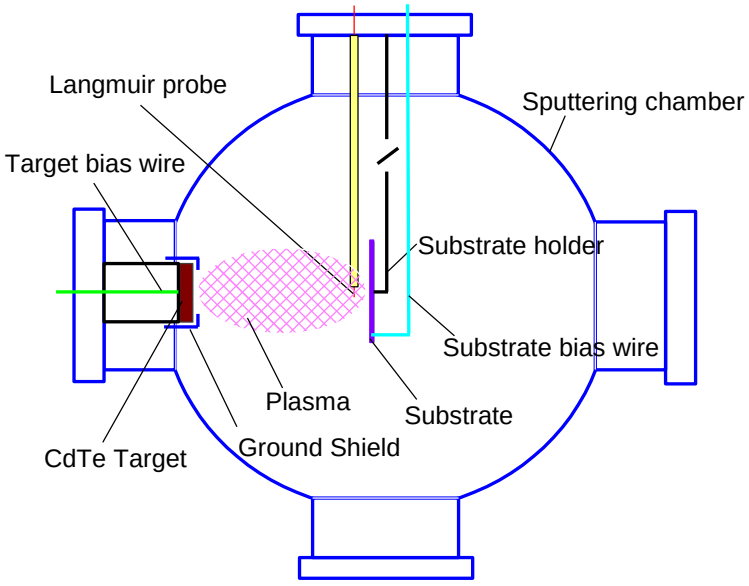

Figure 2-2. Experimental setup for potential distribution and the Langmuir probe measurements.

The experimental set up is sketched in Figure2-2. The magnetron sputter chamber has a planar geometry with an unbalanced magnetron. A turbomolecular pump is used to achieve a base pressure in the range of $\sim 10^{-6} \ldots 10^{-7}$ Torr. The distance between the 2" diameter CdTe target and the 3"x3" glass substrate is 6.5 centimeters. During the normal

deposition process the glass substrate is radiatively heated up to 250 °C. I used a Langmuir probe made of a 70 μm diameter Pt wire placed in front of the center of the substrate 10 mm towards the CdTe target. The probe consists of 10 mm of wire protruding from a glass capillary that serves as an insulator and a structural support for the probe. The other end of the probe wire is fed through the chamber wall for data readout. I used a Keithley 2400 Sourcemeter to collect the I-V data. Two other feedthroughs were used for the substrate bias wire and target self-bias wire. The substrate holder is isolated from the chamber walls with a dielectric piece, therefore during the deposition the substrate is kept at floating potential. The setup described above allowed me to measure the self-bias potential of the substrate as well as to apply a desired bias to the substrate over the range of -50 to 50 V in order to check on the corresponding changes in plasma potential.

In order to cover the most useful region in the phase space of deposition parameters I performed all the measurements for Ar pressures ranging from 5 mTorr to 50 mTorr and RF powers from 5 W to 60 W. In addition data were taken in two different configurations: with a freshly cleaned ground shroud and a ground shroud with a thick CdTe coating, equivalent to the coating that is normally builds up after about 200 hours of deposition.

2.3 Cathode DC Bias

It is known that during RF sputtering the cathode (target) develops a negative DC bias. This happens as a result of the difference in mobilities of ions and electrons in the plasma. Assuming that before plasma breakdown the cathode was at ground DC potential

with the RF signal applied to it, after the plasma is ignited the ions from the plasma bombard the target in the negative half period causing sputtering. In the positive half period the electrons are attracted instead. After a few cycles due to the higher mobility of the electrons the target is found at a certain negative bias DC V_{BIAS} (Figure 2-3).

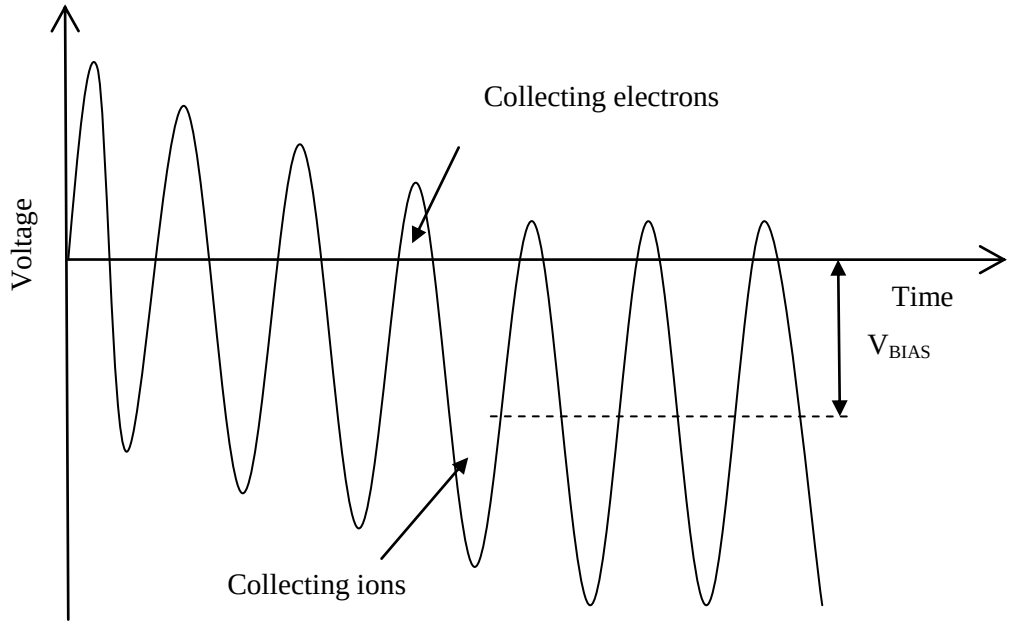

Figure 2-3.Establishing the cathode DC V_{BIAS} as a function of time for the first several cycles after the plasma ignition.

The dependence of V_{BIAS} on both sputtering pressure and applied RF power is shown in Figure 2-4. The dependence of V_{BIAS} on pressure is rather weak while it steadily becomes more and more negative when the RF power increases. Also the cathode self-bias is noticeably different between bare and coated ground shroud conditions – the cathode DC bias is always less negative for the same pressure and power conditions when the ground shroud is covered with an insulating coating of CdTe (see Figure 2-4).

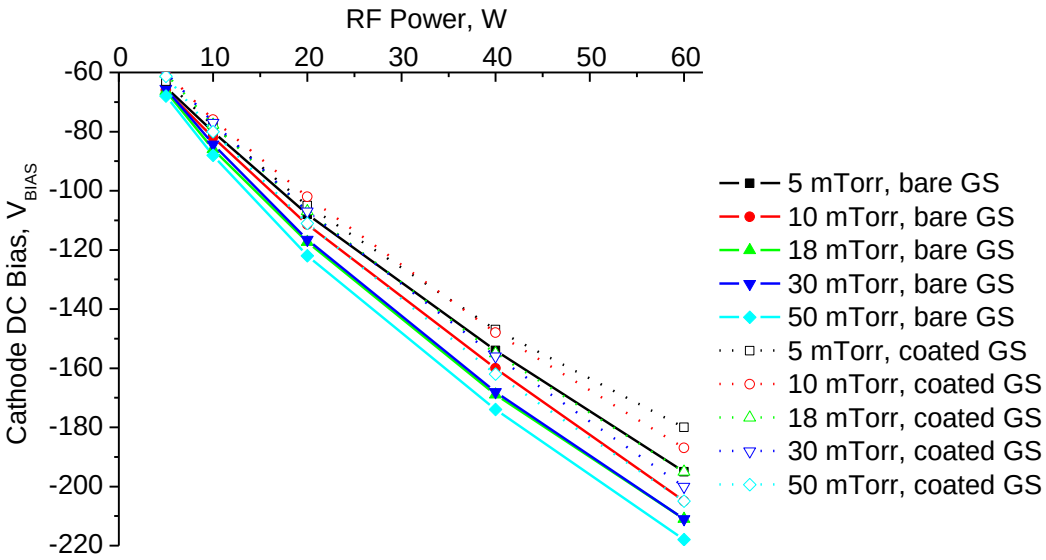

Figure 2-4. Cathode DC bias as a function of pressure and RF power. Bare ground (solid lines) and coated ground shroud (dotted lines).

2.4 Substrate Self-Bias

Our standard deposition configuration uses the substrate at floating bias. This is ensured by the dielectric insulation of the substrate holder. Therefore the substrate bias V_{SUB} can change depending on the other deposition parameters. Here I measured that change for both bare and coated grounds shroud conditions (Figure 2-5).As in the case of the cathode DC bias, the substrate self bias changes with both pressure and RF power. It becomes more positive (or less negative in some cases) when both pressure and power increase. I found the largest differences between the cases of bare and coated ground shroud. I believe that it is important that for the case of a bare ground shroud the substrate is always found under negative self-bias while it eventually becomes positive when enough CdTe coating is developed on the shroud. This is likely to be an explanation for the observed change in pinhole density – extremely high right after the

cleaning of the ground shroud and reducing later on as the total number of deposition hours increases. The hypothesis is that pinholes are caused by positively charged dust particles present inside the chamber that get attracted to the substrate when its self bias is negative and do not cause a problem otherwise.

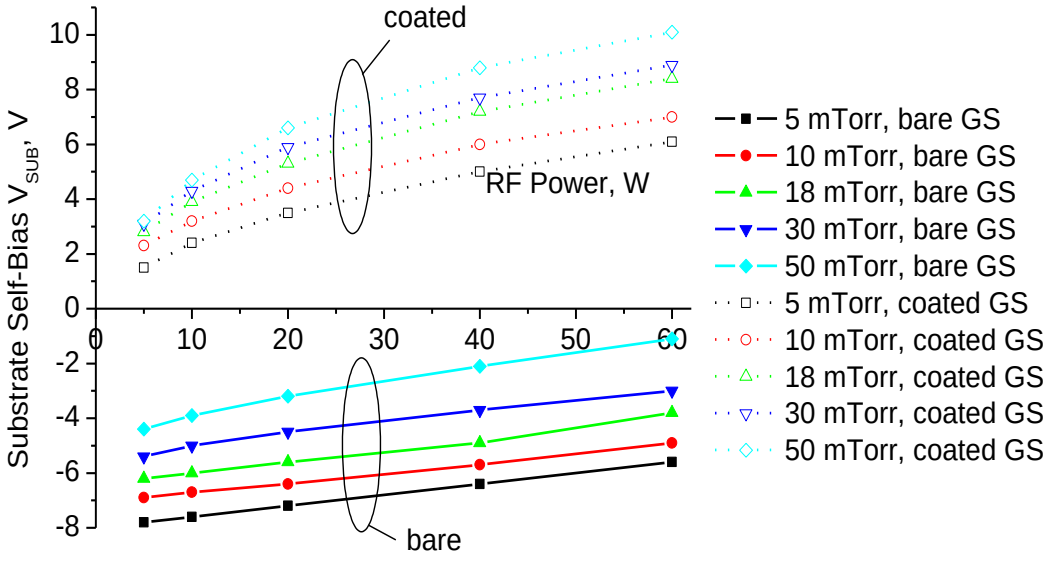

Figure 2-5. Substrate self-bias bias measured relative to chamber walls as a function of pressure and RF power. Bare ground (solid lines) and coated ground shroud (dotted lines).

2.5 Plasma Potential

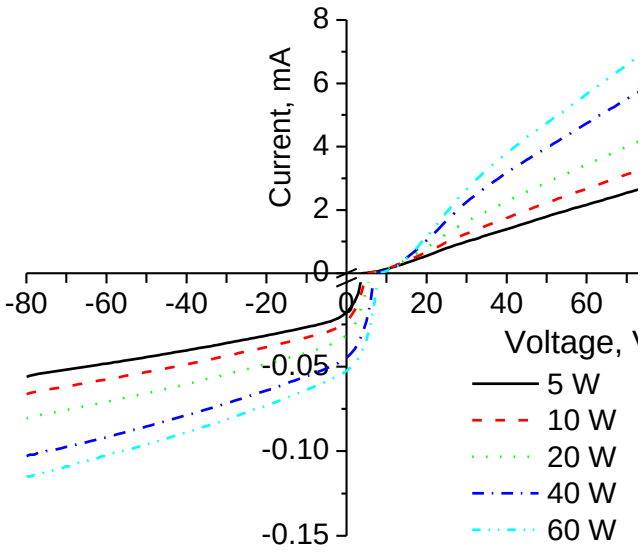

Figure 2-6. A typical set of I-V curves obtained with the Langmuir probe. Data taken with coated ground shroud at 18 mTorr.

The plasma potential was determined from the analysis of the Langmuir probe trace which technically is an I-V curve taken over the range of -80 V to 80 V. A comprehensive review of the trace evaluation is described for example in [29]. Figure2-6 shows typical I-V curves obtained as a result of the experiment while Figure 2-7 and Figure 2-8 illustrate the analysis procedure.

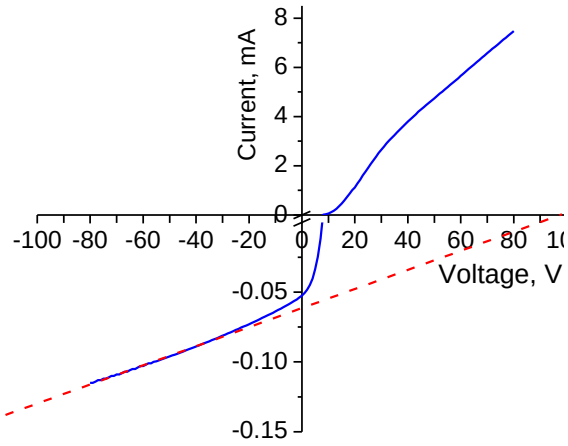

Figure 2-7. Approximation of the ion current (red dashed line) from the raw data (blue solid line).

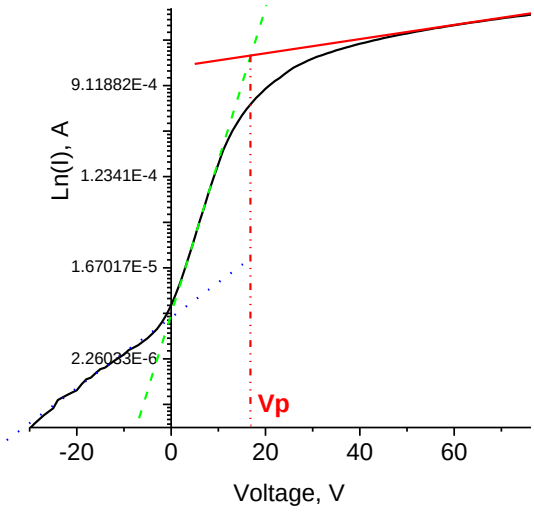

Figure 2-8. Determination of plasma potential V_P, as the knee of the Langmuir probe trace.

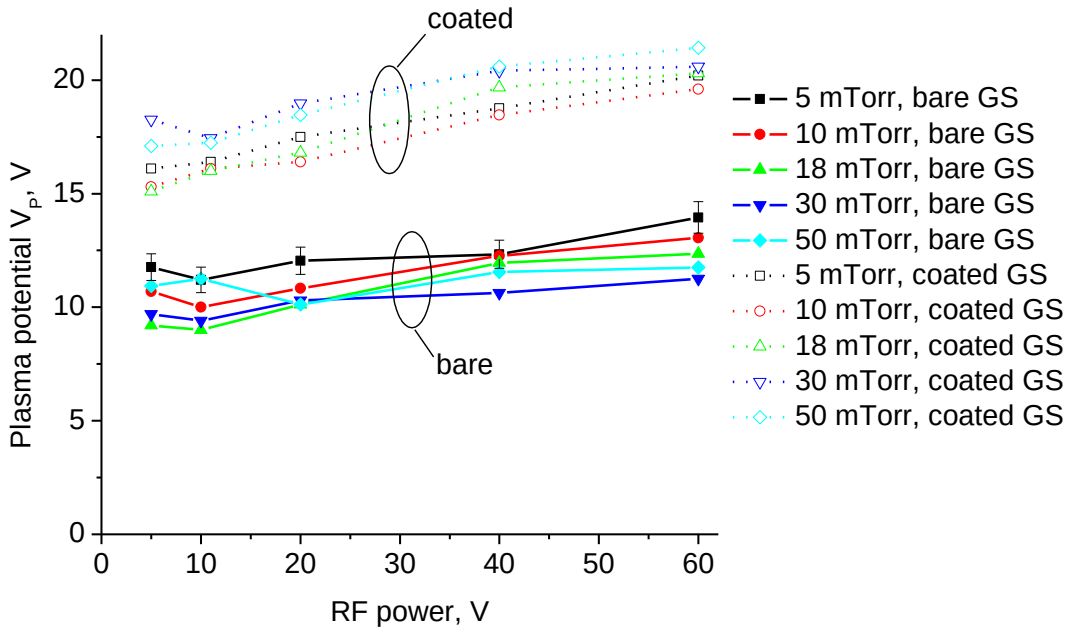

Figure 2-9. Plasma potential as a function of pressure and RF power. Bare ground (solid lines) and coated ground shroud (dotted lines). 5% error bars representing estimated experimental error are shown for one set of data.

First, a straight line approximating the ion current is subtracted from the raw data (Figure 2-7). Second, the modified data are plotted on semi-logarithmic scale and the three distinct regions are again approximated with straight lines. The red solid line in Figure 2-8 is the electron saturation current, the green dashed line represents the retardation region where the electron current increases rapidly and the blue dotted line represents the contribution from the high energy tail electrons. The plasma potential V_P was determined by the intersection of the first two lines. The results for V_P vs. RF power are shown in Figure 2-9.

It can be seen from Figure 2-9 that there is a very weak dependence of plasma potential on the RF power with a tendency to increase with increasing power while

dependence on the sputtering gas pressure is rather unclear and likely to be within the experimental error. Again the largest difference is between the cases of coated and bare ground shroud. The plasma potential is about 5 V higher in the case of the of coated ground shroud.

2.6 Plasma potential vs. substrate bias

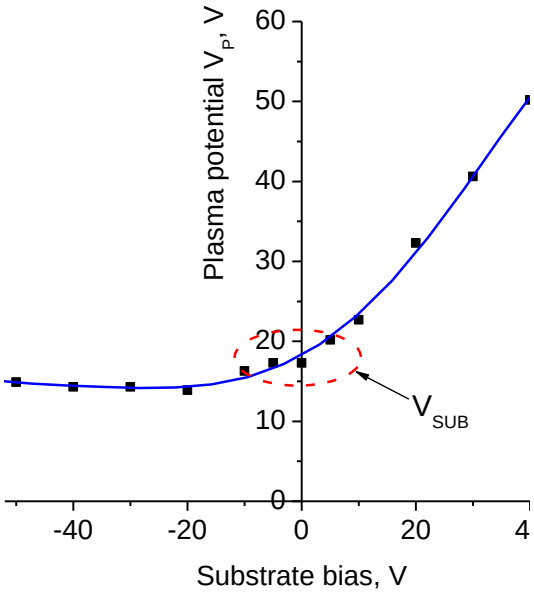

Figure 2-10. Plasma potential V_P vs. applied substrate bias. A typical range of the substrate self-bias V_{SUB} is shown.

The final measurement of plasma potential was done for the case of coated ground shroud at 18 mTorr of Ar pressure and 20 W of RF power. The variable in this case was the substrate bias that was controlled by a DC power supply connected between the substrate (3”x3” SnO2-coated soda-lime glass) and the electrical ground (chamber walls). I studied the evolution of the plasma potential while varying the substrate bias from -50 V to 50 V (Figure 2-10).

It can be seen from the Figure 2-10 that the plasma potential is less sensitive to the application of the negative bias to the substrate and very quickly reaches the constant value of about 14 V which is just slightly less than the plasma potential for the floating substrate bias condition (substrate self bias is about 4 V in this case). This can be explained by the low mobility of the ions and the fact that the plasma cannot be negative with respect to the chamber walls (0 V) regardless of the substrate bias. This limits the lowest possible potential the plasma can achieve. On the other hand, application of the positive substrate bias leads to the linear increase of the plasma potential since electrons are now easily drained from the plasma, causing an increase in plasma potential.

2.7 Conclusions

In-situ potential distribution measurements of the DC cathode bias, substrate self bias and plasma potential as functions of sputtering gas pressure and applied RF power were made.

I found that a "coated" ground shroud yields a smaller potential difference between the plasma potential V_P and the target DC bias V_{BIAS} that results in less integrated sputtering time over each RF cycle than in the case of "bare" ground shroud. This explains a gradual slowing down of the deposition rate as a function of number of depositions made since the CdTe coating is building up on the ground shroud during each deposition.

I also found a substantial difference between the substrate self-bias V_{SUB} measured with a "bare" ground shroud vs. a "coated" ground shroud. V_{SUB} is slightly negative (~ -5 V) in the case of the "bare" ground shroud and slightly positive (~ +5 V) in

the case of "coated" ground shroud for the typical sputtering conditions (18 mTorr, 20 W RF power). I believe it is the explanation for a higher density of pinholes right after the cleaning of the ground shroud originating from the electrostatic interaction between positively charged dust particles in the chamber and a negatively biased substrate.

Based on the results of these measurements I extended our typical 100 deposition hour ground shroud cleaning cycle by roughly 5 times and there were no negative effects observed other than a decrease of the deposition rate. High quality films with very low pinhole density yielding above 13% efficiency cells have been deposited consistently during this time.

Another important conclusion is that although our typical deposition parameters such as sputtering gas pressure and RF power are very useful for the process characterization and routine control, a periodic check on more fundamental plasma quantities such as measured in this study is desirable and even might be necessary in certain cases such as full performance optimization, a major change in the manufacturing process, or a transition to new sputtering equipment.

Chapter 3: UT cell fabrication process. High rate magnetron sputtering

3.1 Introduction

In this chapter I will describe the UT "standard" cell fabrication process which was used as a starting point for the ultra-thin cell optimization. Normally it involves substrate preparation, magnetron sputter deposition of CdS and CdTe layers, $CdCl_2$ post-deposition treatment, Cu/Au back contact (BC) bilayer deposition by thermal evaporation and BC activation at elevated temperature.

Optimization of the post-deposition steps will be discussed in greater detail in Chapter 5 and Chapter 6, while here I will focus mostly on fabrication of the CdTe layer. I will discuss the influence of deposition parameters such as sputter gas pressure and RF power on the deposition rate and film morphology.

3.2 UT standard cell fabrication process

As I mentioned before, the vast majority of CdTe cells are fabricated in a superstrate configuration. A typical UT cell structure is illustrated in Figure 3-1. I will go through the layers in the order they are fabricated to highlight some important details of the process.

1) Substrate. UT typical cells are made on commercially available substrates made by Pilkington. The structure of Pilkington TEC glass is shown in Figure 3-2 (from [29]). A transparent conductive oxide (TCO) stack consisting of $SnO_2/SiO_2/SnO_2$:F layers is

2) deposited on 3mm soda-lime glass. Typical sheet resistance is about 7 Ohm/□ for TEC-7 glass, 8 Ohm/□ for TEC-8, 12 Ohm/□ for TEC-12 and 15 Ohm/□ TEC 15. TEC-7 and TEC-15 are typically used for UT cells.

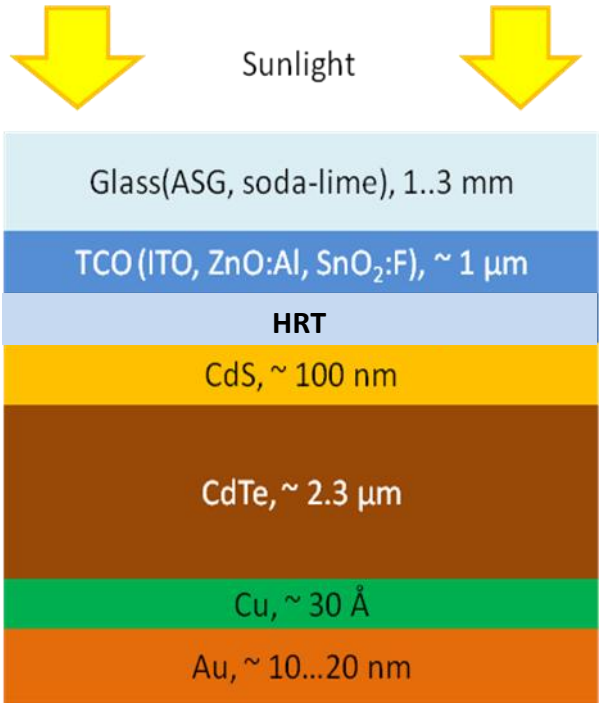

Figure 3-1. Typical UT cell structure (not to scale).

We also have a capability of making our own TCOs such as indium-doped tin oxide (ITO) or aluminum-doped zinc oxide (ZnO:Al) and therefore can use alumino-silicate Corning glass (ASG) for substrates, taking advantage of ASG's higher transmission over soda-lime glass in the visible range (see Figure 3-3). In general, using a ASG/ITO or ASG/ ZnO:Al can be advantageous over the TEC substrates due to higher transmission in the spectral range utilized by the solar cell, as can be seen from Figure 3-3. In reality though, use of TEC-7 or TEC-15 is often preferred because of convenience, higher

reproducibility of the results and a higher potential to transfer into large-scale manufacturing.

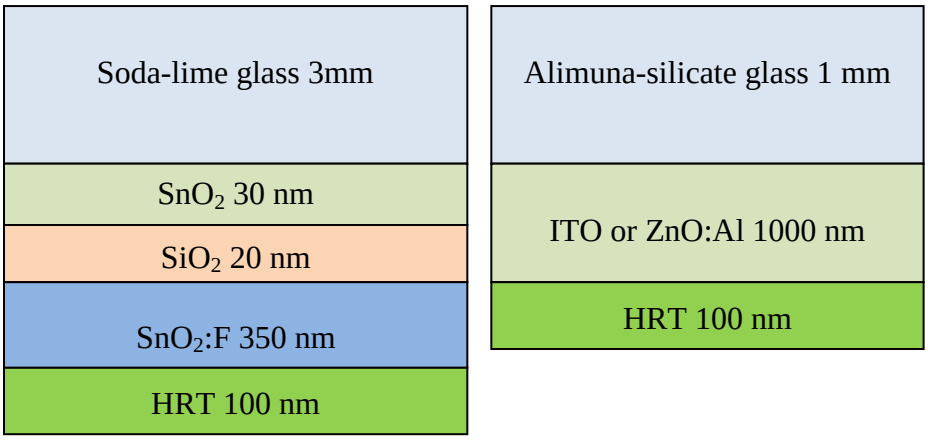

Figure 3-2. TEC glass (a) and UT ASG with ZnO:Al TCO (b) structures (not to scale). The HRT layer is optional (see discussion in the text).

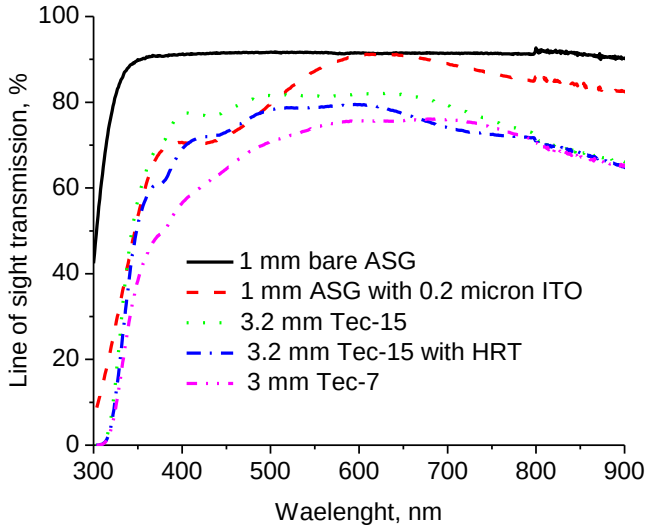

Figure 3-3. Line-of-sight transmission of different types of substrates that can be used for solar cell fabrication (bare ASG is shown for comparison).

3) HRT layer. This is the only layer in Figure 3-1 that is sometimes omitted in the real solar cell structure. Our standard cells do not have an HRT layer, although in Chapter 4 I will show that it is highly advantageous to use it when the highest efficiency is the main goal and especially for the case of ultra-thin cells. All the results for the ultra-thin cells presented in this work were obtained with the use of an HRT layer.
4) CdS layer. Typically deposited by magnetron sputtering at 18 mTorr of Ar pressure and 35 W of RF power with the substrate temperature of 250 ^{o}C. Standard thickness is around 100 nm; I will present the results of its fine optimization in Chapter 4.
5) CdTe layer. While we have a great flexibility in varying the deposition conditions and therefore, deposition rate and film morphology, as was shown in Chapter 2, our standard conditions for the CdTe layer deposition are 18 m Torr, 20 W of RF power and substrate temperature, T_S= 250 ^{o}C. The same conditions were used for fabricating the ultra thin cells, while our standard thickness is 2.5 μm.
6) $CdCl_2$ treatment. After completion of the CdS/CdTe deposition, each sample undergoes a high-temperature post-deposition treatment with $CdCl_2$ as a reactive agent. Standard conditions are 387 ^{o}C for 30 minutes. Optimization of this process will be discussed in greater detail in Chapter 5.
7) Cu layer. Cu is a part of our Cu/Au bilayer BC structure deposited by thermal evaporation. The standard thickness of the as-deposited Cu is 30 Å. I found the optimum thickness to be dependent on the thickness of the CdTe layer and report the results in Chapter 5.
8) Au layer. Provides the current collection and a contact area for the test lead during the cell measurements. Typical thickness is around 10 nm to 25 nm. Both the Cu and Au

layers are typically deposited through a mask with round holes that define the individual dot cell area (typically from 0.5 to 0.13 cm^2). If not mentioned otherwise the results reported in this thesis are for cells with 0.062 cm^2 area.

9) Cu diffusion (temperature activation). Is required to facilitate Cu diffusion into the CdTe layer. Standard conditions are: 45 minutes at 150 ^oC in a room air ambient.

Steps 1 to 9 complete the cell fabrication process. It is typically followed by J-V measurements of the individual cells (normally 35 cells per a quarter piece of the 3"x3" substrate). Measurements are done with an Oriel solar simulator at AM 1.5 conditions [30]. When needed, cells are subjected to quantum efficiency (QE), temperature-dependent current-voltage (J-V-T), x-ray diffraction (XRD), atomic force microscopy (AFM) or other tests and in this case, the measurement details will be provided.

3.3 High-rate CdTe deposition

For the maximum sputter deposition rate, deposition has to be done at an optimum pressure which is rather specific for each individual deposition chamber. In my case it has been found that the maximum rate is achieved at an argon pressure of 5 mTorr. Increase of pressure leads to decrease of the mean free path of the sputtered species and slows the deposition rate. Extremely low pressure (<5 mTorr) eventually makes the discharge unstable and decreases the sputtering rate due to decrease of the plasma density (Figure 3-4).

Further, I investigated the power dependence of the deposition rate at 5 mTorr. I found it to be slightly super linear possibly due to target heating in the racetrack (Figure 3-5). A maximum deposition rate of 140 nm/min has been achieved. This corresponds to

about 17 minutes of deposition for our standard 2.3 μm CdTe thickness or more a factor of five decrease in the time needed for fabrication of a CdTe layer in a standard 2.3- μm CdTe solar cell. Correspondingly it would take about 3.5 minutes to deposit an ultra-thin CdTe layer of 0.5 μm at this deposition rate.

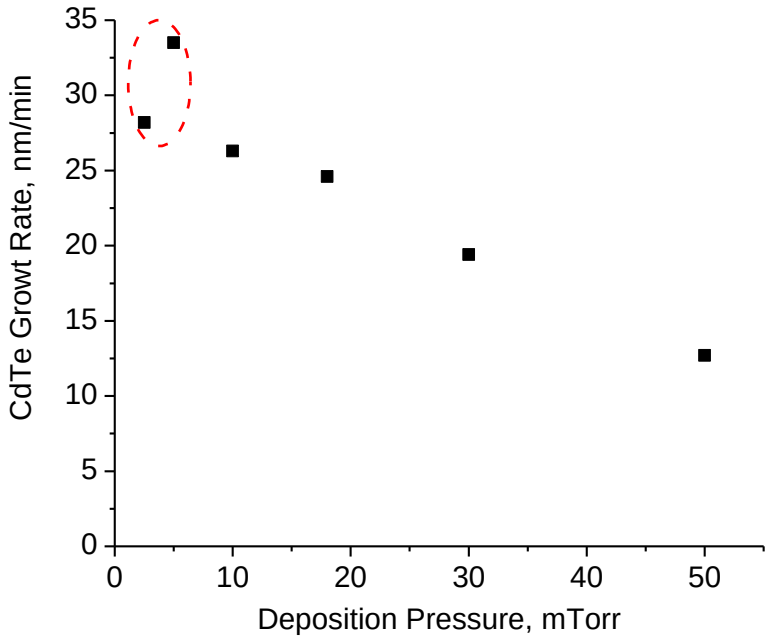

Figure 3-4. Deposition rate at 20 W of RF power as a function of Ar pressure. The region where the decrease of the deposition rate was observed is highlighted.

XRD studies revealed that, independent of deposition conditions, CdTe films grow as polycrystalline with preferred (111) orientation which becomes more random after high-temperature $CdCl_2$ treatment. Figure 3-6 shows a typical result for all the deposited films. Notice a strong (111) peak at $2\theta = 23.76^{o}$ for an as-deposited film and the appearance of a series of peaks corresponding to regrowth in different crystallographic orientations after $CdCl_2$ treatment. These crystal structure changes were independent of film growth conditions. Figure 3-7 and Figure 3-8 show that the crystal

structure of the as-grown film is virtually independent of both deposition pressure and power.

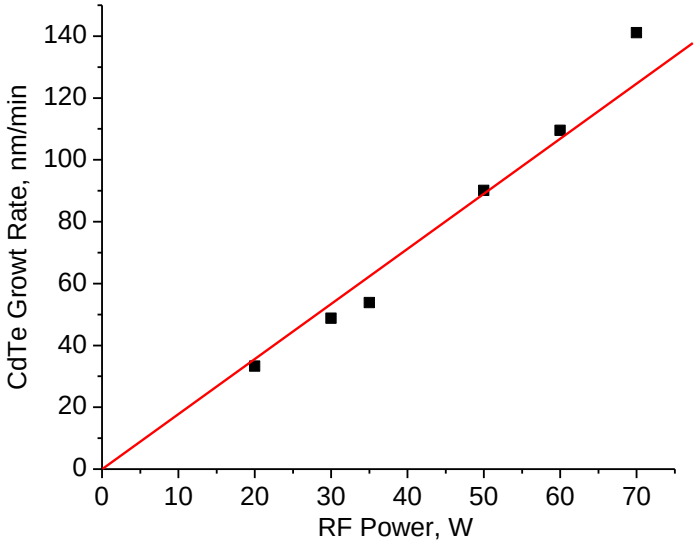

Figure 3-5. Deposition rate at 5 mTorr Ar pressure as a function of RF power (linear fit is shown).

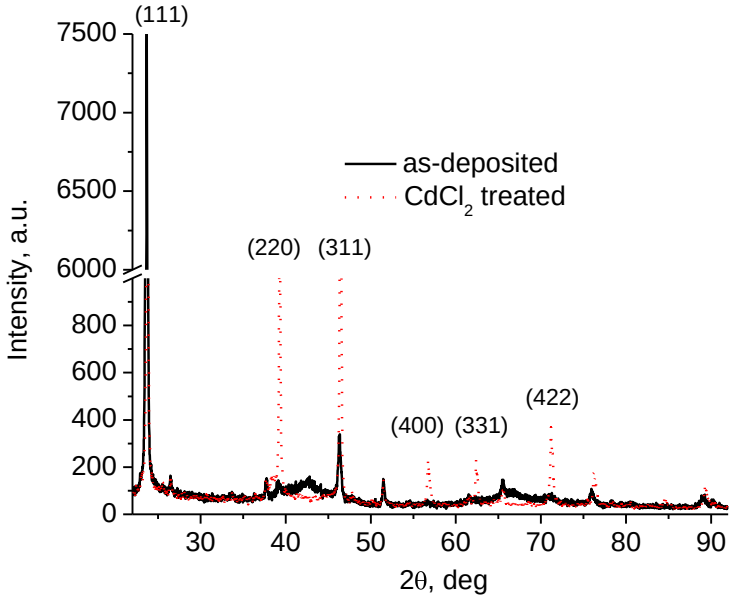

Figure 3-6. Typical XRD spectra of as-deposited and $CdCl_2$-treated films.

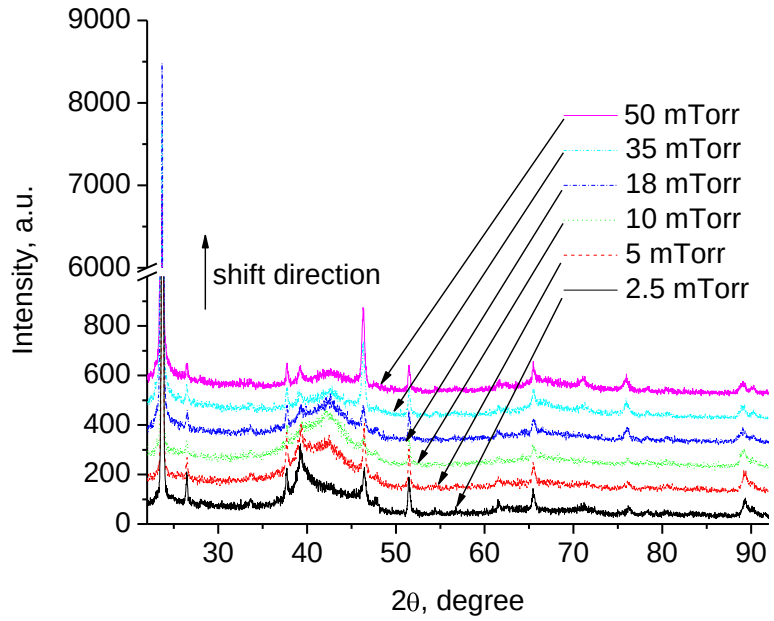

Figure 3-7. XRD spectra of the films grown at constant power of 20 W at variable pressure. Each graph is shifted upwards by 100 a. u. from the previous one for clarity.

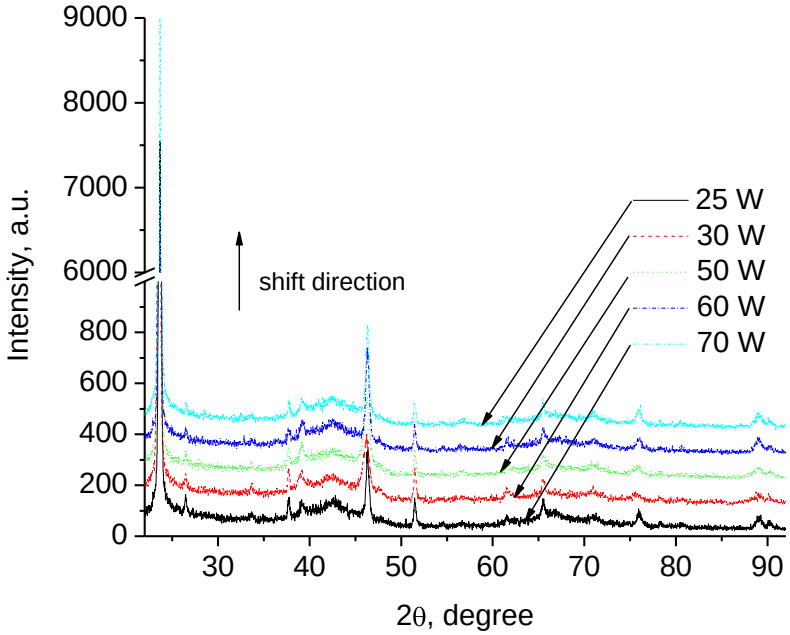

Figure 3-8. XRD spectra of the films grown at constant pressure of 5 mTorr at variable power. Each graph is shifted upwards by 100 a. u. from the previous one for clarity.

Residual strain in as-deposited films was studied by the shift of the (111) peak. Figure 3-9 and Figure 3-10 demonstrate that stress increases with lower pressure but has no clear dependence on RF power.

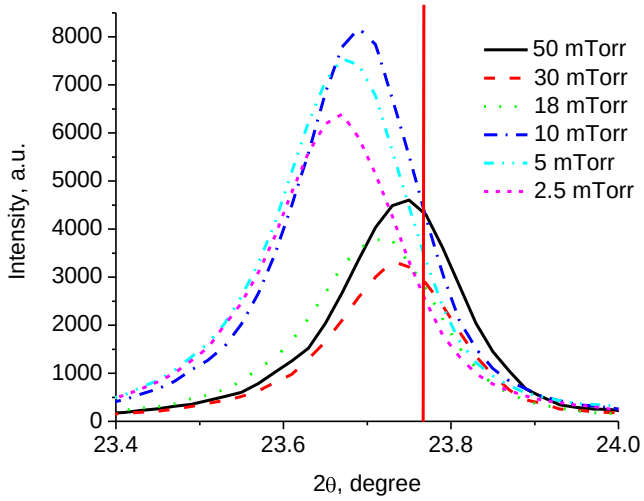

Figure 3-9. Peak shift of the films grown at constant power of 20 W at variable pressure, the red line represents the position of the peak from a powder sample.

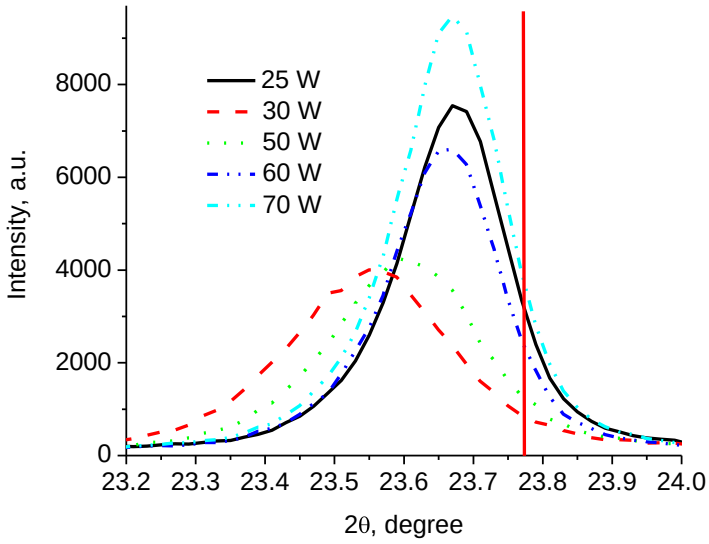

Figure 3-10. Peak shift of the films grown at constant pressure of 5 mTorr at variable power, red line represents the position of the peak from a powder sample.

Transverse strain calculated for both cases is shown in Figure 3-110 and Figure 3-12. There is a strong dependence of the residual stress on deposition rate if the changing parameter is deposition pressure, while the strain dependence on RF power is rather weak. I believe that films grown at lower pressure have higher in-plane compressive stress, because the grains are more densely packed due to a higher kinetic energy of impinging particles (Ar atoms and ions as well as Cd and Te atoms).

The remarkable result though is that strain, and consequently stress, in the film grown at the fastest rate does not necessarily achieve its highest values, which can be related to good performance of the cells made on this film as will be shown later.

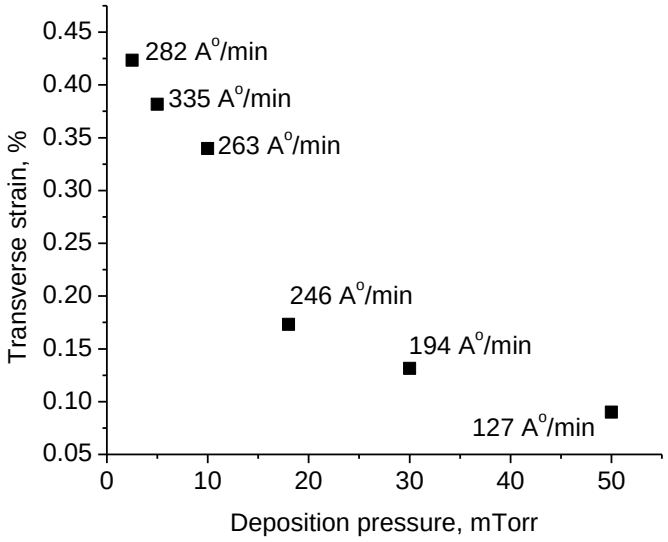

Figure 3-11. Transverse strain in the films grown at constant power of 20 W at variable pressure. Deposition rate for each case is shown.

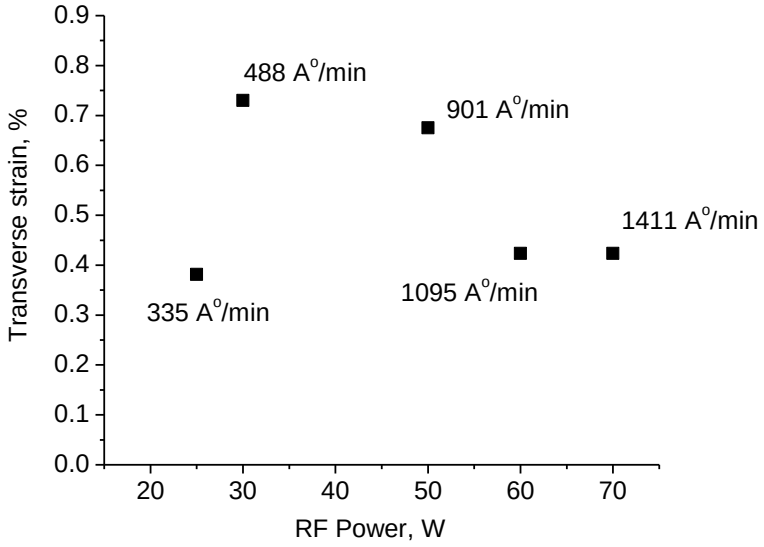

Figure 3-12. Transverse strain in the films grown at constant pressure of 5 mTorr at variable power. Deposition rate for each case is shown.

AFM shows a similar type of behavior with pressure and power. Morphology and surface roughness of the CdTe films change significantly when the deposition pressure decreases (Figure 3-13) while effect of power is rather small (Figure 3-14).

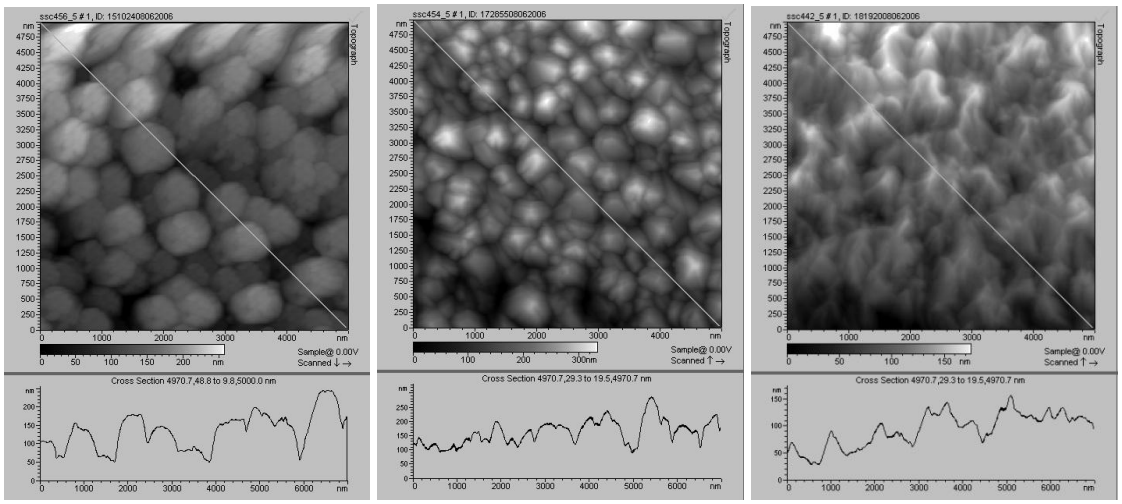

Figure 3-13. AFM images of CdTe films grown at 20W at 50 mTorr (left), 18 mTorr (middle) and 5 mTorr (right).

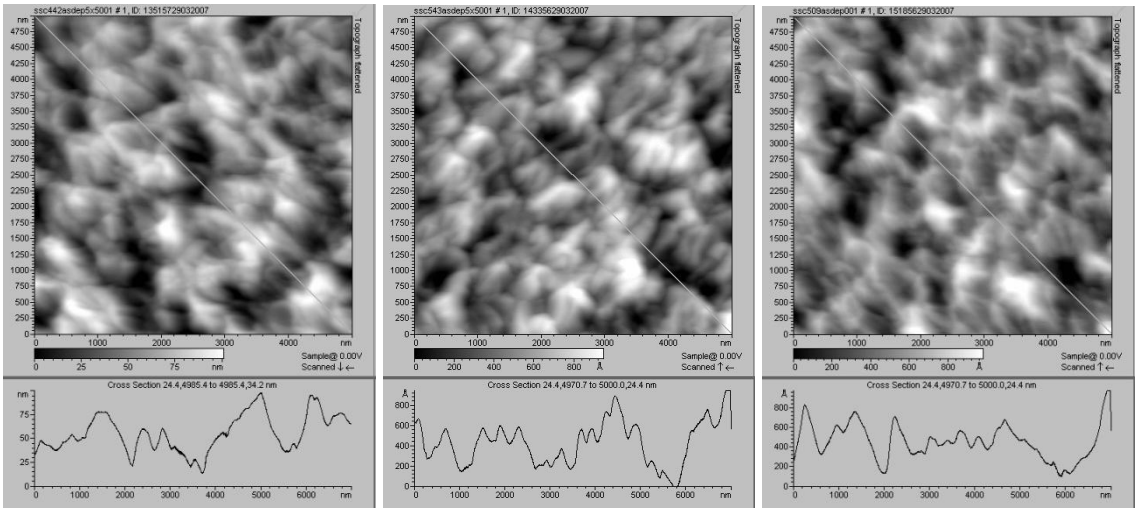

Figure 3-14. AFM images of CdTe films grown at 5 mTorr at 20 W (left), 40 W (middle) and 60 W (right).

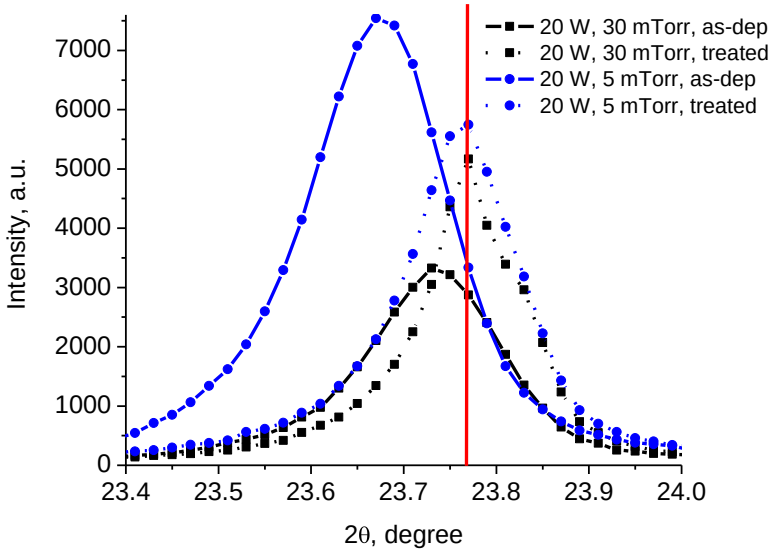

Figure 3-15. Peak shift after the $CdCl_2$ treatment for the films deposited at different pressure, red line represents the position of the peak from a reference powder sample.

$CdCl_2$ treatment is known to be one of the keys to improve the cell performance. It is remarkable that it also completely releases the residual stress independently of deposition conditions. Figure 3-15 shows the shift of the [111] peak after the $CdCl_2$

treatment for the films grown at 5 and 30 mTorr, when the difference in deposition rates is 1.5 times. In both cases almost complete relaxation is achieved.

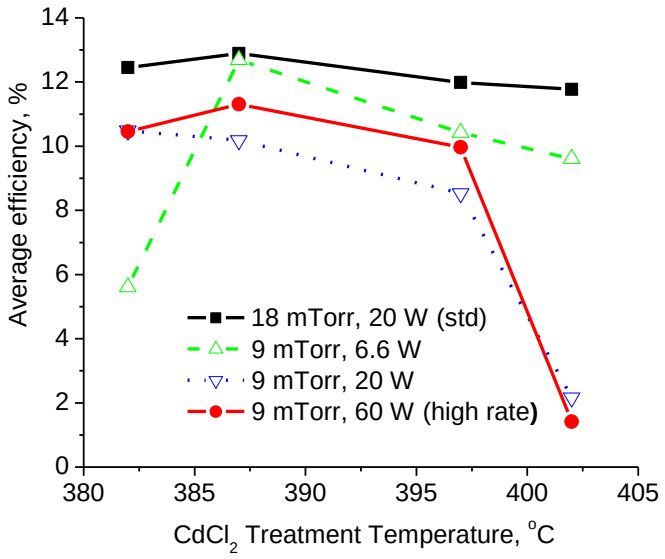

Figure 3-16. Average efficiency vs. $CdCl_2$ treatment temperature of the best 50% of cells deposited at four different conditions.

Finally, the efficiency of a set of samples grown at 10 mTorr and different RF powers (6.6 W, 20 W and 60 W) was compared with the efficiency of a cell grown at our standard conditions. Figure 3-16 shows the results obtained after $CdCl_2$ treatment at different temperatures (382 $^{\circ}$C, 387 $^{\circ}$C, 397 $^{\circ}$C , 402 $^{\circ}$C ,). In all cases a maximum efficiency of at least 7% was obtained although yield varied from excellent to rather poor, especially at the extremes of $CdCl_2$ process temperatures. In many cases, though, the yield of 0.071 and 0.126 cm^2 devices was excellent, which is represented in Figure 3-16, where the average efficiency of the best 10 out of 19 cells on each sample is plotted as a function of $CdCl_2$ temperature. It can be seen from Figure 3-16 that while devices processed at standard conditions are more forgiving in terms of $CdCl_2$ treatment

conditions, high-efficiency cells can be made on CdTe grown at different conditions, including high-rate conditions if the $CdCl_2$ treatment is optimized. For instance, our best high-deposition-rate cell to date has an efficiency of 11.8% which is typical of our standard cells on TEC-7 glass.

The QE shows evidence of slightly enhanced CdS/CdTe interdiffusion at higher chloride processing temperature (Figure 3-17,) particularly from 530-600 nm and near 850 nm). However, these changes in carrier collection at short circuit are not the key factors responsible for the efficiency and yield of the devices. J-V data (Figure 3-18) indicate that the lower efficiency of the devices deposited at lower pressure, including the high-rate deposited cells, is due to lower V_{OC} and FF. Arguably this is due to the smaller grain sizes and corresponding larger grain boundary area and thus higher recombination rates in these cells deposited at low pressure.

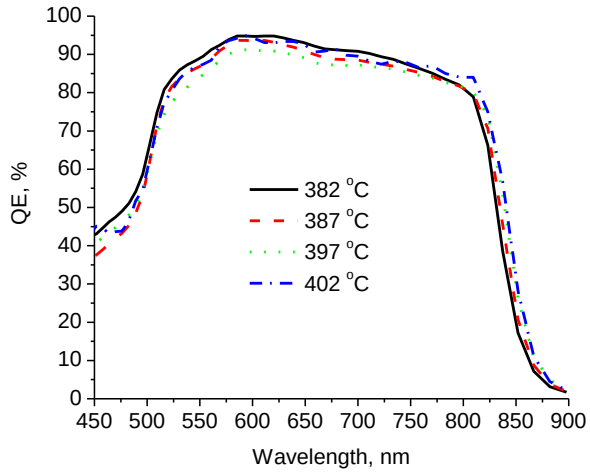

Figure 3-17. QE of the high-rate cells after $CdCl_2$ treatment at different temperatures.

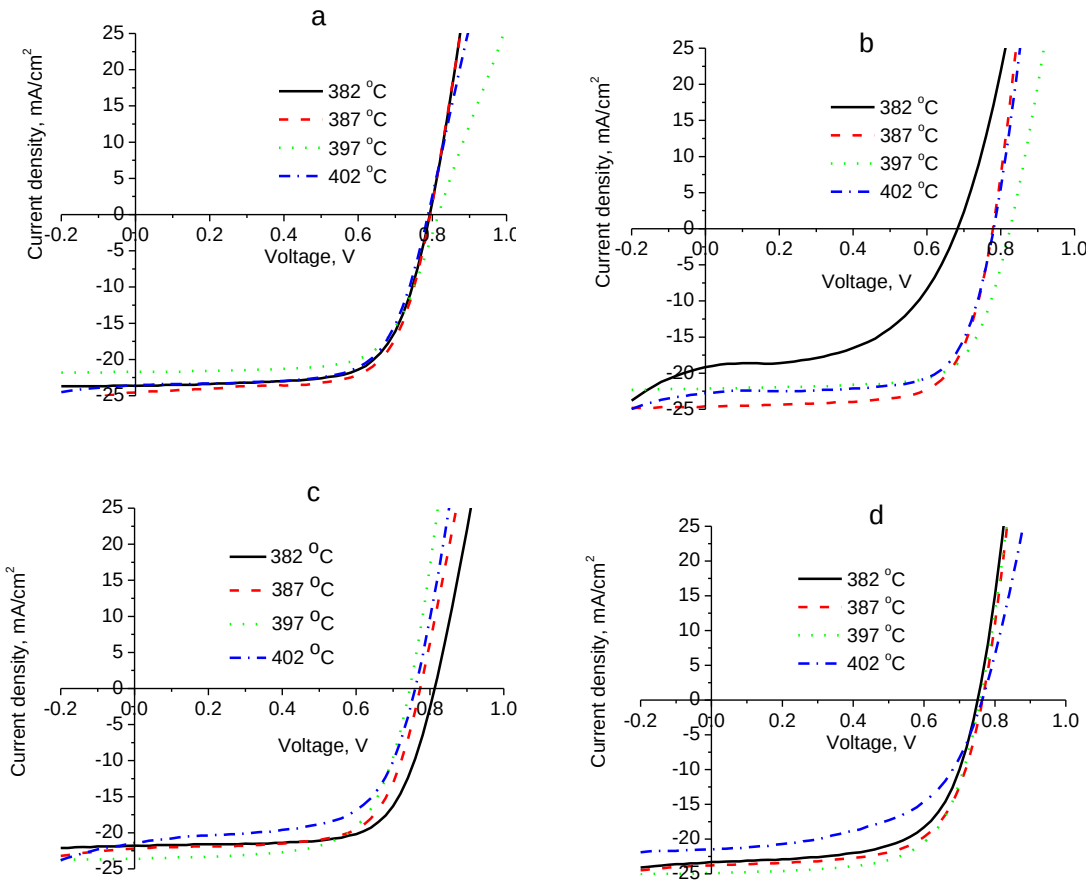

Figure 3-18. J-V curves of the best cells grown at different conditions: a) 18 mTorr, 20 W (UT standard), b) 9 mTorr, 6.6 W, c) 9 mTorr, 20 W, d) 9mTorr, 60 W (high rate) and $CdCl_2$ treated at four different temperatures.

3.4 Conclusions

I highlighted the UT standard cell fabrication process that was used as a starting point for the optimization of ultra-thin cells. In addition CdTe deposition rate dependence on sputtering gas pressure and RF power has been studied. I found that the maximum rate is achieved at 5 mTorr and the upper limit of applied power has not been identified because of concern for the integrity of the sputtering target which was not bonded to a metal backing plate. At a "safe" 60 W of RF power the deposition rate of 140 nm/min was achieved. Films were studied by means of AFM and XRD to ensure the crystalline

nature of the film and to obtain information about the grain size, orientation and residual stress in the film. I found that the morphology of the films and the residual in-plane stress in the as-deposited films has a stronger dependence on deposition pressure than power. Generally lower deposition pressure leads to more densely packed, smaller-grain-size polycrystalline films. As-deposited films have preferred (111) orientation which is randomized after $CdCl_2$ treatment just as for standard UT CdTe films. $CdCl_2$ treatment is also found to release stress in films almost completely.

High-rate deposition cells with average efficiency greater than 12% were fabricated.

Chapter 4: CdS layer thickness optimization

4.1 Introduction

CdS has been known as the best heterojunction partner for CdTe for a long period of time. Several models were developed to explain its positive effect on the cell performance as compared to other suitable n-type materials. Although, being the best known window layer so far in CdTe cells, CdS has its own challenges and limitations. One of them is the lack of carrier collection limiting the net cell efficiency.

One of the ways to overcome this problem is to keep the thickness of the CdS layer as small as possible to allow more light to pass through it and get absorbed in CdTe. The thickness cannot be reduced to zero though, because it creates a number of problems such as, for example, non-optimal electric field distribution and increasing nonuniformity of the layer.

In this chapter the results of CdS thickness optimization for sputtered cells grown on bare Tec-15/Tec-7 and HRT-coated Tec-15 will be presented.

4.2 Band diagram models and V_{OC} vs. J_{SC} tradeoff for the different thicknesses of CdS

Since the efficiency of a solar cell is determined by the product of J_{SC}, V_{OC} and FF it is equally important to maximize each of these quantities. One of the ways to do that is to optimize the thickness of the CdS layer. The problem is that there is an often

observed trade-off between V_{OC} (and FF) and J_{SC} that occurs at a certain range of CdS thickness. This is different from the well known V_{OC}-J_{SC} trade-off depending on the absorber layer bandgap width [31, 32] and is solely related to the properties of the CdS window layer. The term "window layer" describes the role of CdS very well since the lack of carrier collection from CdTe layer is well-recognized but still poorly understood [31, 33, 34]. Therefore from the point of optical analysis it can be treated as a filter with a cut-off frequency corresponding to the bandgap of the material (2.4 eV or 520 nm). A typical quantum efficiency (QE) graph of the CdS/CdTe cells shown in Figure 4-1 illustrates this effect. The graphs represent two extreme cases of a very thick (230 nm) and very thin (30 nm) CdS layer so the difference can be clearly seen. Since the J_{SC} of the cell can be represented as the area under the QE curve it is obvious that the cell with 30 nm CdS will have a much higher J_{SC} due to enhanced blue response. Therefore, making the CdS layer as thin as possible is one of the major strategies to improve the overall cell efficiency [35, 36].

This approach, of thinning the CdS, should be taken with care though, since making the CdS layer too thin often results in reduction of V_{OC} and FF as will be shown later in this chapter. Once again the exact mechanism of this process is debatable but one can think about its being caused by the nonuniformities in the very thin film or this layer becoming fully depleted and therefore weakening the main photovoltaic junction.

Later on in this chapter I will present the results of CdS thickness optimization for the cells grown on Pilkington Tec-7 and Tec-15 substrates, and on Tec-15 substrates covered with high resistivity transparent (HRT) layer which is known to improve thin CdS performance.

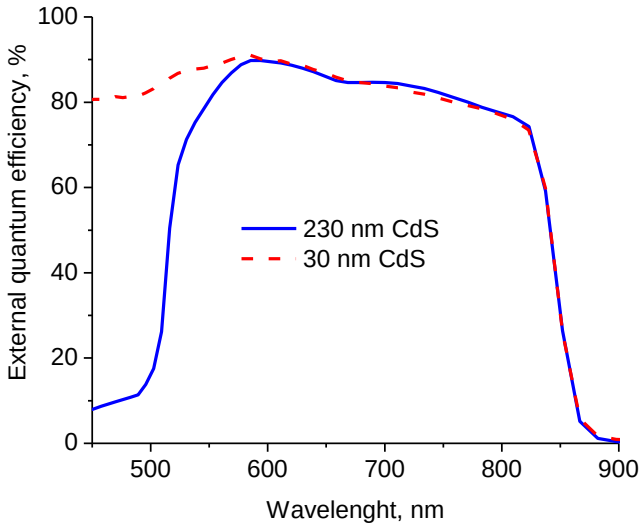

Figure 4-1. External QE of the cells with 230 nm (solid) and 30 nm (dot) CdS window layer.

4.3 Experimental results

CdS/CdTe solar cells were made by the standard UT fabrication process:

1. Ultrasonic cleaning of the substrate using Micro-90 soap solution
2. Deposition of CdS by magnetron sputtering (variable thickness)
3. Deposition of 2.3 μm CdTe by magnetron sputtering
4. 25 minutes $CdCl_2$ treatment at 387 ^{o}C
5. 30 Å Cu/ 200 Å Au back contact deposition by thermal evaporation
6. 45 minutes Cu "activation" treatment in air at 150 ^{o}C to facilitate Cu diffusion at the back contact

We chose the thickness of the CdS layers to be 230 nm, 160 nm, 80 nm, 45 nm, 30 nm and 0 (no CdS) in order to cover a reasonably broad range of practically important cases. The samples prepared were first tested with QE measurements in order to verify

the change in CdS thickness and the presence of an interdiffusion layer in all cases except the zero CdS thickness. The results shown in Figure 4-2 are for the cells on Tec-7 substrates. The QE for the cells on Tec-7, Tec-15 and HRT Tec-15 are essentially identical for a given CdS thickness.

These samples behave as expected showing increasing transmission for $\lambda < 500$ nm as the thickness of the CdS layer increased. There are typical signs of an interdiffusion layer in the 500-560 nm, as well as 810-840 nm parts of the QE plots, for all the samples but the one with no CdS layer. The explanation is that there is an interdiffusion layer with the thickness of about 30-40 nm formed during the $CdCl_2$ treatment. The optical properties of this layer are different from both the stoichiometric CdS and CdTe (see for example [37, 38, 39]). Figure 4-3 shows a pseudobinary phase diagram of the CdTe-CdS system (left) and experimental data for the bandgap of the $CdTe_{1-x}S_x$ alloy showing a strong bowing behavior (Figure 4-3, right).

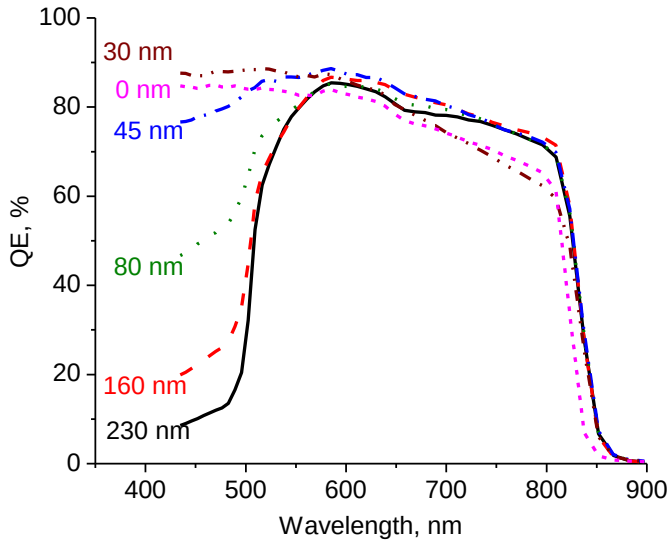

Figure 4-2. QE data for the cells with variable CdS thickness

A thermodynamically stable (at the temperature of $CdCl_2$ treatment (around 400 ^oC)) mix of $CdTe_{0.94}S_{0.06}$ and $CdS_{0.96}Te_{0.04}$ alloys has enough difference in the bandgap widths translating into shifts of the absorption edges (see Figure 4-3, right) to be observable by the QE measurements. That is why the QE extends deeper into the infrared region (presence of $CdTe_{0.94}S_{0.06}$ with the bandgap lower than a pure CdTe) and often has a "rounded" knee in the 500-560 nm region ($CdS_{0.96}Te_{0.04}$ with the bandgap lower than pure CdS) for the samples with CdS/ $CdTe_{1-x}S_x$ /CdTe structure. Interdiffusion is a also a reason why samples look more transparent in the CdS "window" than the as-deposited CdS thickness suggests – about 20 nm to 30 nm of CdS is typically consumed by the interdiffusion layer during the $CdCl_2$ treatment process [6, 40].

Interestingly, the sample with 30 nm of as-deposited CdS has significant deep penetration losses (see Figure 4-2 again). I believe this can be due to the very thin n-type CdS that is left after the $CdCl_2$ processing being fully depleted and therefore lowering the electric field at the junction which results in poorer collection efficiency for the long-wavelength photons absorbed farther away from the junction.

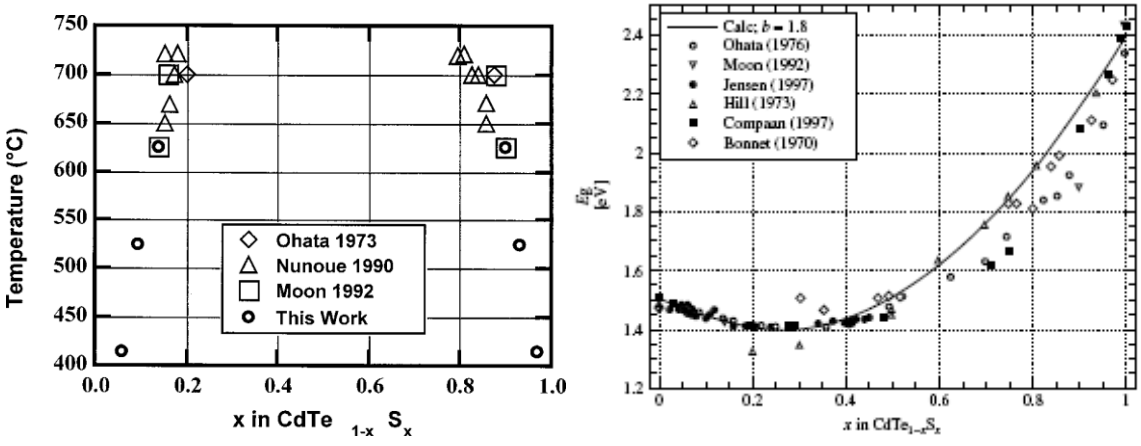

Figure 4-3. Left - CdTe-CdS pseudobinary phase diagram; right – optical bandgap bowing of the $CdTe_{1-x}S_x$ alloy (both from [31])

The J-V data presented in Figure 4-4 support the QE observations. The change in open-circuit voltage becomes very noticeable when the thickness of the as-deposited CdS layer goes below 80 nm. A simultaneous increase of the short circuit current does not quite make up for the V_{OC} drop and the average cell performance decreases. On the other hand, making CdS much thicker than 100 nm is not very beneficial either. The very slight, increase of Voc and FF cannot compensate for the gradual decrease of Jsc. These points can be better illustrated by the statistical analysis of the J-V parameters given on the Figure 4-5. Statistics are given for 23 individual cells of each type with 13 of them having an area of 0.126 cm^2 and the other 10 with area of 0.071 cm^2.

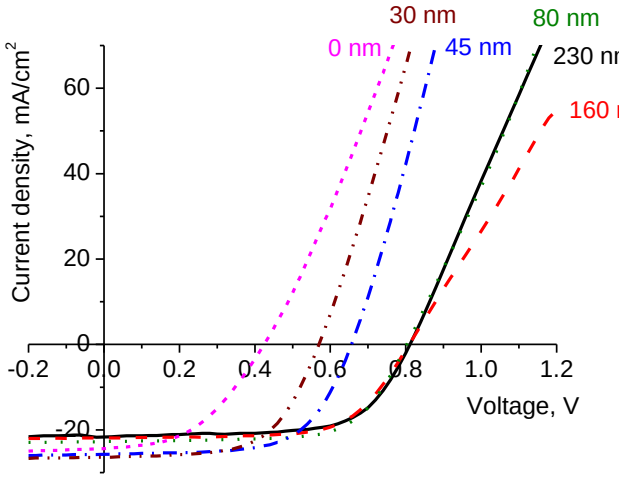

Figure 4-4. J-V data for the cells with variable CdS thickness. Tec-7 substrate with no HRT layer

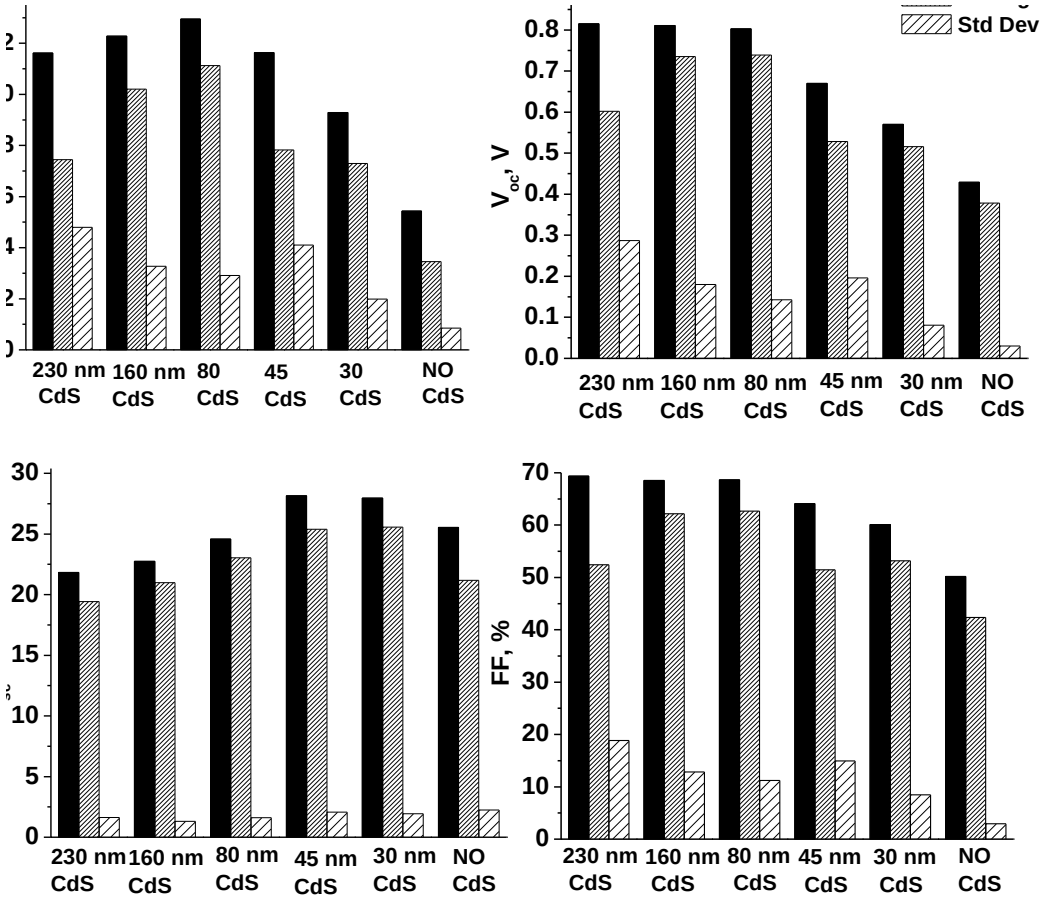

Figure 4-5. J-V parameters of the cells with variable CdS Thickness. Bare Tec-7 substrate

As seen from the histograms, a CdS thickness of about 80 nm appears to yield optimum efficiency for the UT standard cells with a 2.3 μm CdTe layer deposited on bare Tec-7 or Tec-15 substrates.

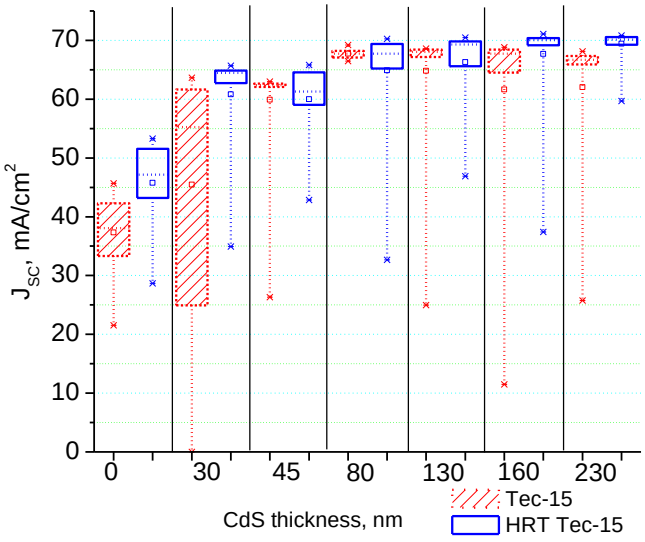

Figure 4-6. Short-circuit current dependence on CdS thickness for cells deposited on bare Tec-15 and HRT-coated Tec-15 substrates.

The situation is significantly different for cells deposited on HRT-coated Tec-15 substrates. While the photocarrier collection and therefore the J_{SC} dependence on CdTe thickness is very similar to the samples grown on bare substrates (Figure 4-6), no significant decrease in Voc (Figure 4-7), and FF (Figure 4-8) was observed down to CdS thickness as small as 30 nm for the cells on HRT-coated substrates. As a result, 30 nm CdS cells with efficiency above 12% were fabricated (Figure 4-9). [For all the "box-and-whiskers" plots in this chapter, the line inside the box is the median (second quartile), the symbol inside the box is the average value, the top and the bottom of the box are the third and first quartiles correspondingly, and the symbols at the ends of the whiskers represent the best and the worst cells. The number of cells for each box-and-whisker data point is 35 and the area of each cell is 0.062 cm^2.]

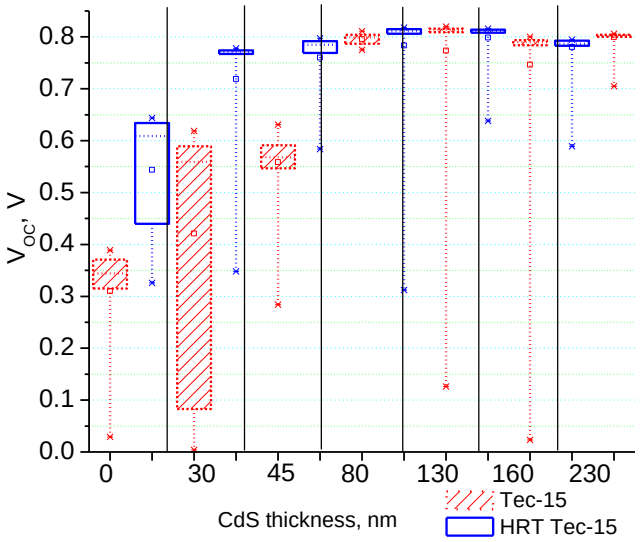

Figure 4-7. Open-circuit voltage dependence on CdS thickness for the cells deposited on bare Tec-15 and HRT-coated Tec-15 substrates.

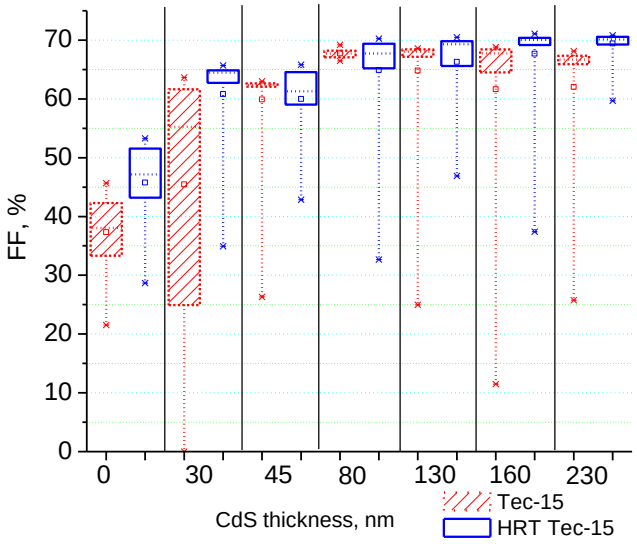

Figure 4-8. Fill-factor dependence on CdS thickness for the cells deposited on bare Tec-15 and HRT-coated Tec-15 substrates.

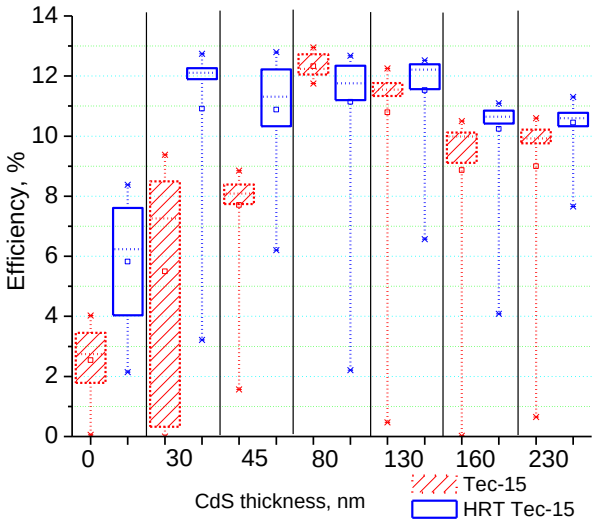

Figure 4-9. Efficiency dependence on CdS thickness for the cells deposited on bare Tec-15 and HRT-coated Tec-15 substrates.

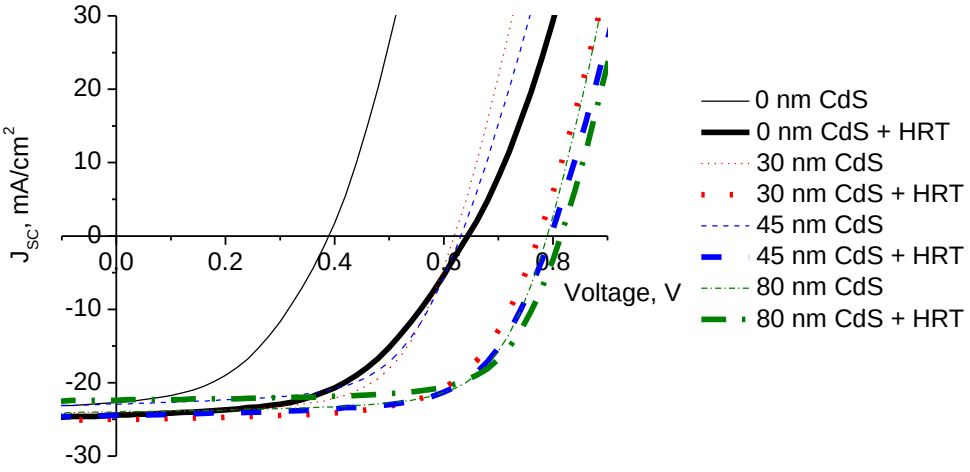

Figure 4-10. J-V curves of the best cells on bare Tec-15 and HRT-coated Tec-15 substrates for four CdS thicknesses

Figure 4-10 illustrates the difference in light J-V curves of cells on bare Tec-15 and HRT-coated Tec-15 substrates. Note a relatively high (about 650 mV) V_{OC} for the

cell without a CdS layer on HRT-coated substrate. We believe that fabricating such no-CdS structures (TCO/HRT/CdTe/BC) can be used as a simple method for evaluating the quality of the HRT layer. Our results suggest that if the HRT layer is "good" then the addition of a very thin layer of CdS (30 nm in our case) pushes Voc to 780 nm range yielding high efficiency cells.

4.4 Conclusions

The optimum thickness of the CdS layer in UT sputtered cells on substrates without HRT has been found based on the results obtained from J-V and QE. We find the optimum to be about 80nm to 100nm of as-deposited CdS that reduces to about 50nm to 70 nm after the standard $CdCl_2$ treatment. The statistical uniformity of the cells with different CdS thickness is comparable; therefore the main criterion for choosing the optimum thickness was Jsc – Voc trade-off.

The effect of using an HRT layer on Tec-15 glass from Pilkington has been investigated as well. It is found to make a dramatic difference on the performance of the cells with very thin (30 nm to 80 nm) CdS layers. Cells with efficiency above 12% were fabricated using a 30 nm CdS / 2.5 μm CdTe structure owing to enhanced blue photocurrent collection while maintaining good V_{OC} and FF. This strategy (using an ultra-thin CdS layer) was successfully applied later for fabrication of high-efficiency ultra-thin CdTe cells (see Chapter 5).

Chapter 5: Optimization of the post-deposition steps for the cells with variable CdTe thickness

5.1 Introduction

In this chapter I will present the strategy and the results of the post-deposition steps for optimization of the cells with variable CdTe thickness. It is known that once the thickness of the CdTe layer approaches a certain minimum, the cells start to suffer significantly from losses in all three important figures of merit (i.e. J_{SC}, V_{OC} and FF). While a loss in J_{SC} with thin CdTe is fairly well understood as arising mainly from the deep penetration loss in the IR part of the spectrum, losses in V_{OC} and FF are more complex. These two parameters can be affected in general by six variables: 1) the substrate details, 2) the CdS thickness, 3) the CdTe thickness, 4) the $CdCl_2$ treatment parameters, 5) the amount of copper used in the back contact, and 6) the duration/temperature of the final back contact diffusion. I will use the results presented in the previous chapters by briefly recalling the conclusions, while the post-deposition part of the cell fabrication cycle will be discussed in greater details in this chapter.

5.2 Substrate choice

It has been shown in Chapter 4 that adding a high resistivity transparent (HRT) layer between the CdS and the conventional high conductivity SnO_2:F coated glass is beneficial, because it allows us to use an ultra-thin and therefore highly transparent CdS

window layer without much reduction of V_{OC} and FF. Thus Pilkington Tec15 glass with HRT coating was my choice of substrate for this optimization experiment.

5.3 CdS thickness

Even though results presented in the Chapter 3 suggest that the minimum CdS thickness can be as small as 30 nm, I chose it to be 60 nm for all of the samples studied in this chapter independent of the CdTe thickness. This approach has almost certainly decreased the maximum efficiency due to a slight loss in Jsc caused by the excessive absorption in CdS, but on the other hand it gave me extra assurance that the n-side of the photovoltaic junction is robust and not likely to influence the observed V_{OC} and FF changes. For all the samples the CdS layer was deposited at 18 mTorr of Ar pressure with 35 W of applied RF power.

5.4 CdTe thickness.

CdTe thickness is an independent variable in this study. It is expected that once the thickness of the absorber layer is reduced, the cell performance is going to drop. As was shown in Chapter 1, this can be caused by losses in J_{SC}, V_{OC} and FF.

I prepared a set of samples with the following CdTe thicknesses: 0.38 μm, 0.5 μm, 0.65 μm, 0.8 μm, 1.1 μm, 1.45 μm, 1.85 μm, 2.2 μm and 2.6 μm. Thickness was measured by a DEKTAK profilometer and represents a mean thickness of the sample averaged over 35 small area (0.062 cm^2) cells on each sample (a quarter piece of UT's typical 3"x3" substrate, see Figure 5-1). For all the samples, CdTe layers were deposited at 18 mTorr of Ar pressure with 20 W of applied RF power.

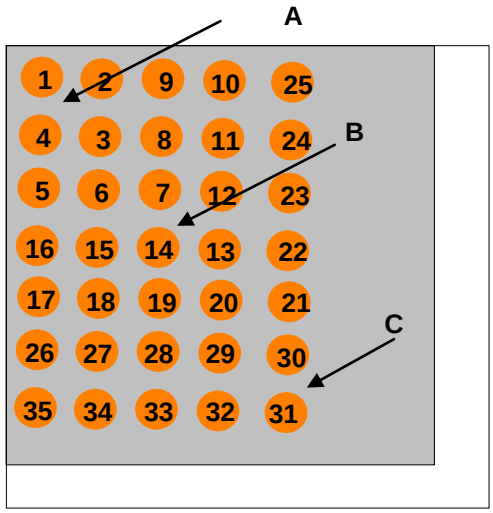

Figure 5-1. A sketch of a sample with individual dot cells. Numeration starts from the upper left which was near the center of the full substrate. Dot cells with lower numbers thus typically have slightly thicker CdS and CdTe layers. Letters A, B and C indicate the approximate places where the thickness was measured.

5.5 $CdCl_2$ treatment.

I have observed previously some dependence of cell parameters on all the variables associated with $CdCl_2$ treatment such as the treatment type ("vapor" or "wet"), treatment temperature and treatment duration. In this study I used a "wet treatment" which means that a room temperature saturated $CdCl_2$-methanol solution was applied directly to the CdTe surface and allowed to dry forming a relatively uniform coating on the sample. In contrast, "vapor treatment" stands for a variation of a "proximity cap" technique when a sample is placed 3mm to 4mm above the "source plate" which consists of a piece of alumino-silicate glass with a roughened (usually by sandblasting) surface coated with the $CdCl_2$ powder applied by vaporization of $CdCl_2$-methanol solution. In both cases of wet and vapor treatment the sample is enclosed between two SiC-coated graphite blocks with thermal masses large compared to that of the sample. The graphite

blocks are radiatively heated and feedback to the heating lamps is provided through thermocouples inserted into the blocks so a constant temperature can be maintained during the treatment.

It has been my experience that while vapor treatment is capable of producing high-efficiency cells and arguably is more suitable for large-scale-manufacturing, it also requires a very tight control over the quality of the source plate that "ages" after a few treatments. The number of treatments before the source plate turns "bad" seems to depend on a number of variables, such as the amount of room air exposure, relative humidity of the room air, roughness of the glass plate, and likely some other factors that have not been clearly identified yet. Therefore I used wet treatment for this experiment to ensure better consistency of the results.

After application of the $CdCl_2$ solution and drying, samples were annealed in dry air (from a cylinder with < 10 ppm H_2O) for variable times at 387 ^oC. A typical temperature profile for the treatment is shown in Figure 5-2. The flat regions of the two curves represent the nominal treatment time as it would be entered into the computer program that controls the system. In reality the cells undergo some treatment during the ramp-up and ramp-down time as well (Figure 5-2 and Figure 5-3).

While there are some relatively in-depth studies of the $CdCl_2$-tratment process kinetics, the analysis gets very complicated quickly if the problem is approached rigorously (see [6, 40] for example. Here I present a very simplified approach that does not constitute a full quantitative analysis, but can serve as a starting point for a more precise analysis. Here I assume that the total amount of treatment that a sample receives is an integral value of both ramp-up and constant temperature treatment times and can be

represented as the area below the curve in Figure 5-3 if the Arrhenius-like behavior of the different processes that form a core of $CdCl_2$ treatment is also taken into account. There is no coordinate dependence such a CdTe thickness in this approach, which is of cause a very crude assumption. Instead the CdTe film is treated as if it is of infinitesimal thickness and in direct contact with a semi-infinite source of diffusion ($CdCl_2$ coating on the CdTe surface).

Figure 5-4 represents the temperature dependence of bulk diffusion coefficients for Cd ($D_{Cd(Bulk)}$) and Cl ($D_{CL(BULK)}$), and the grain boundary diffusion coefficient for Cd ($D_{Cd(GB)}$). Cd self-diffusion coefficients are taken from [40], and the Cl diffusion coefficient in CdTe single crystal is taken from [41]. From data of Figure 5-3 and Figure 5-4 one can estimate a relative contribution of the treatment during the ramp-up and ramp-down time to the entire treatment and adjust to a nominal treatment time with a step function temperature-time profile.

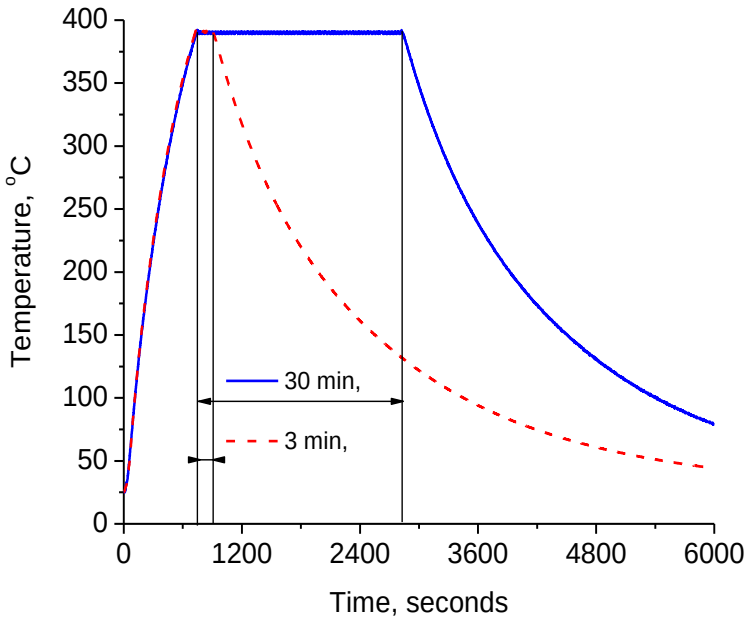

Figure 5-2. $CdCl_2$ treatment temperature profiles for nominal 3 minute and 30 minute treatment times.

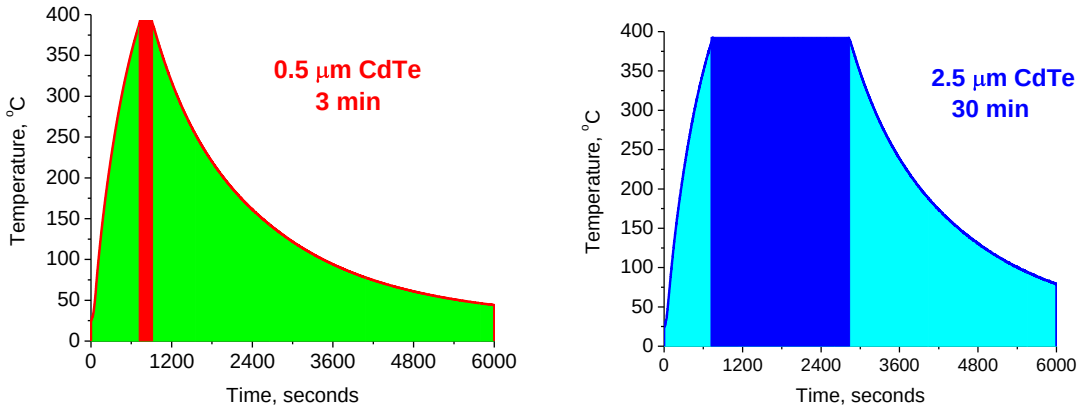

Figure 5-3. A schematic representation of "nominal" (square areas on the graphs) vs. "actual" (the whole area under the curve) treatment time.

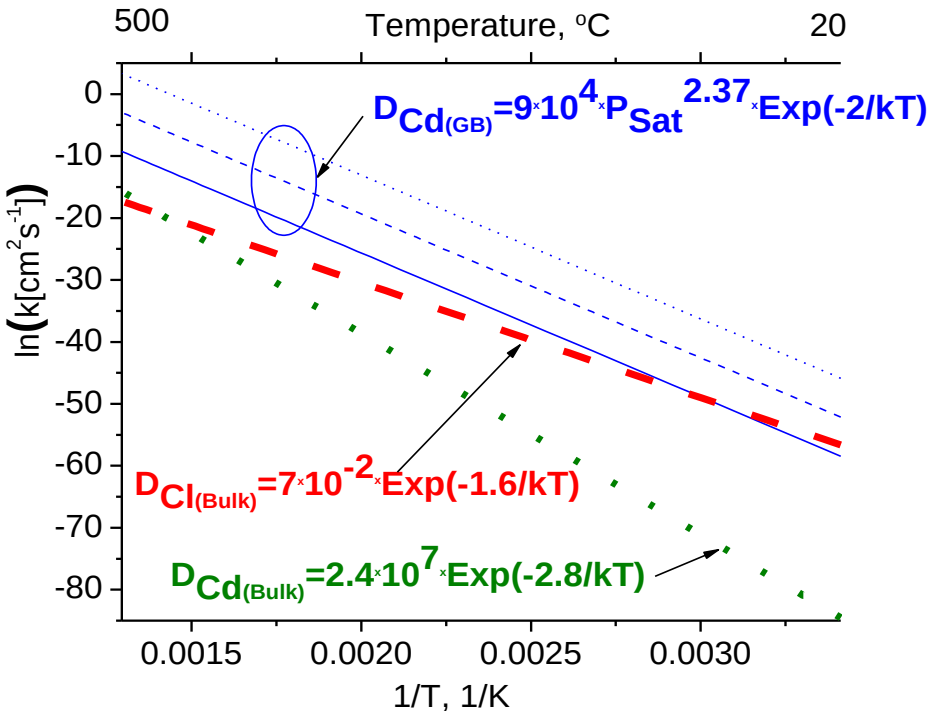

Figure 5-4. Arrhenius plots of diffusion coefficients for Cl in bulk CdTe ($D_{Cl(Bulk)}$ –thick red dashed line), Cd self-diffusion in bulk CdTe ($D_{Cd(Bulk)}$ – thick green dotted line), and Cd diffusion along grain boundaries in CdTe ($D_{Cd(GB)}$ – thin blue lines). The three different curves are for 1 mTorr (solid), 10 mTorr (dashed) and 100 mTorr (dotted) partial pressures of $CdCl_2$).

Figure 5-5 shows the values for three different processes for a 30 minute treatment and Figure 5-6 – for a three-minute one. Once again, this estimation should not be taken as a full quantitative analysis but I believe that it provides useful guidelines for choosing $CdCl_2$ treatment times for the cells with different CdTe thicknesses.

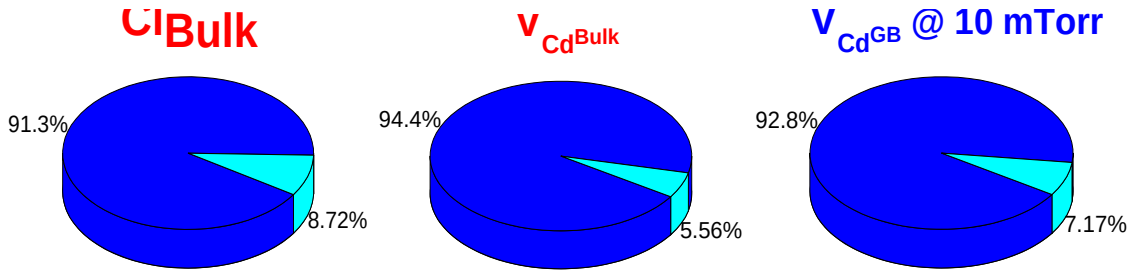

Figure 5-5. Relative contribution of the ramp-up and ramp-down time (light blue segment) calculated for the three different processes from Figure 5-4 for the case of a 30-minute treatment at 387 ^{o}C.

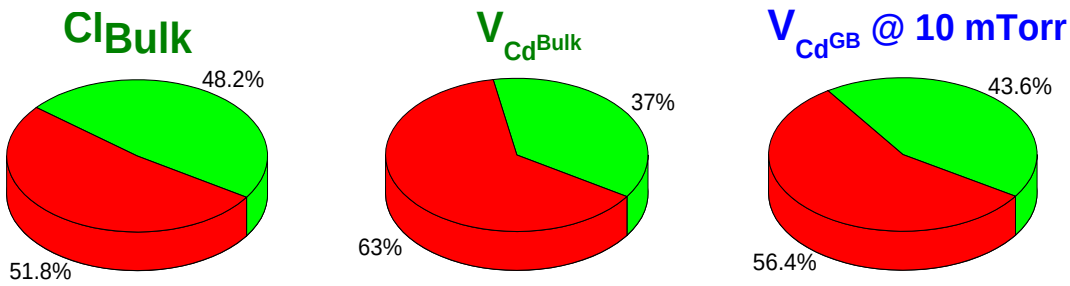

Figure 5-6. Relative contribution of the ramp-up plus ramp-down time (green segment) calculated for the three different processes from Figure 5-4 for the case of a three-minute treatment at 387 ^{o}C.

As an example of this correction for ramp-up and ramp-down, I was able to reanalyze UT's previously established benchmarks that are proven to give reasonably good results in terms of cell performance (Table 5-1 – "nominal" treatment time column). If treatment time is plotted against CdTe thickness (Figure 5-7, open squares) it does not intercept the origin, while if you consider the ramp-up plus ramp-down contribution to be equivalent to approximately 3 minutes of treatment at constant temperature (387 ^{o}C) (see Figure 5-6) and correct the time correspondingly ("actual" treatment time in the Table 7-1) then the results can be easily approximated by a straight line passing through the origin (Figure 5-7, round dots).

Table 5-1. Benchmarks for $CdCl_2$ treatment time of the samples with different CdTe thickness and corresponding best cell efficiency.

CdTe Thickness	**$CdCl_2$ treatment nominal time at 387 ^oC**	**$CdCl_2$ treatment equivalent time at 387 ^oC**	**Best cell efficiency**
2.5	30	33	14%
2.25	25	28	13.7%
1.32	15	18	11%
0.97	10	13	12%
0.75	5	8	8%
0.5	3	6	10%
0.3	1	4	6 %

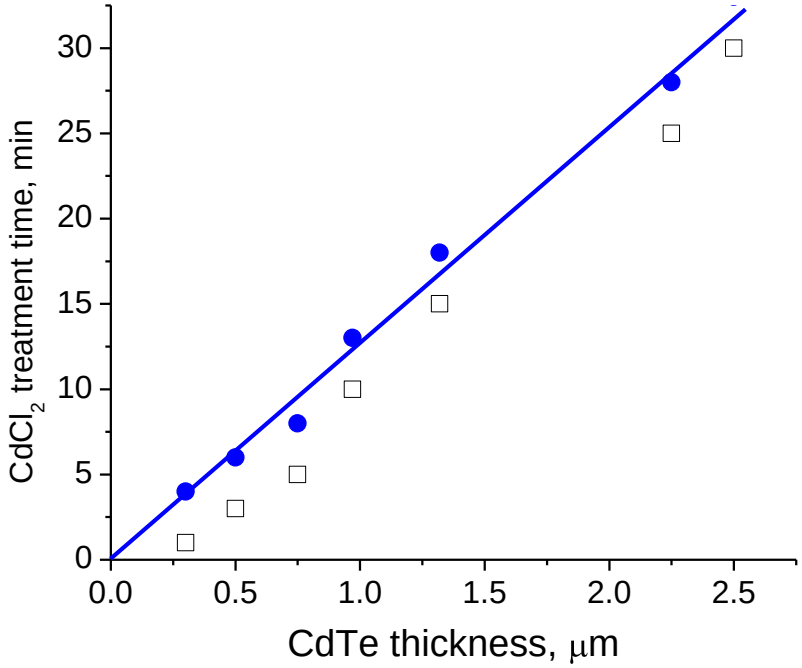

Figure 5-7. CdCl2 treatment time ("nominal" – open squares and "actual" - blue dots) vs. CdTe thickness and the linear fit for the "actual" time.

This dependence was used as a reference when I prepared a set of samples with different CdTe thicknesses as stated above and treated them with times that would approximately follow the straight line from the Figure 5-7 but with a small variation such that each sample of a certain thickness was treated for two different times closely spaced

along the time axis. Figure 5-8 illustrates this approach. The x-axis is CdTe layer thickness. Two separate sets of values at the y-axis correspond to "nominal" and "actual" treatment time. Nine samples (ssc32, ssc34, ssc31, ssc33, ssc37, ssc35, ssc30, ssc38, ssc28) are plotted according to the average CdTe thickness over the sample area. The number in parentheses represents CdTe thickness at the points A, B and C (see Figure 5-1) correspondingly. Arrows to the time axis indicate the treatment times that sister pieces of each sample received (see Table 5-2 for more information).

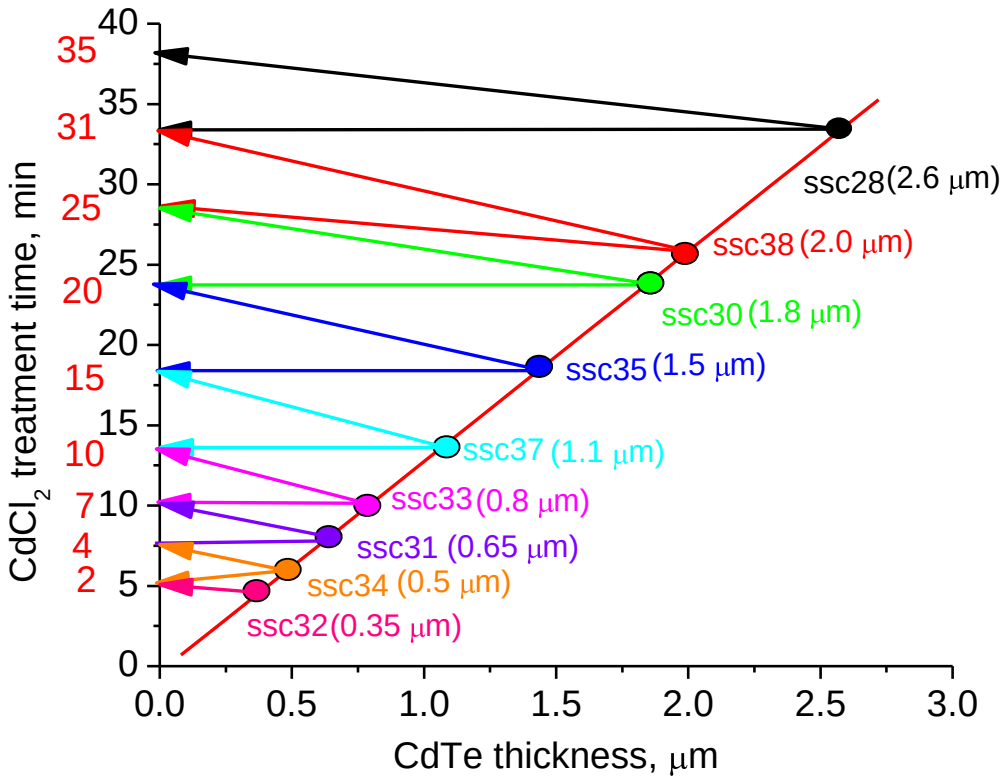

Figure 5-8. Treatment time chosen for samples of different thickness. Arrows indicate the two different treatment times chosen. Values on the time axis are "actual" (black) and "nominal" (red) treatment times.

5.6 Thickness of the as-deposited Cu layer.

A Cu/Au bilayer back contact deposited by thermal evaporation was used in this experiment. Since I have previously found some dependence of cell efficiency on the as-deposited Cu layer thickness as the CdTe thickness is changed, this parameter was included in the study in addition to the $CdCl_2$ treatment time variation. As described before, two sister quarter pieces from each sample of a certain thickness were treated for a longer time than the two others. After that, one sample with a longer treatment time was completed with a back contact having a Cu layer thinner than the other one. Samples with shorter $CdCl_2$ treatment time were processed similarly (Figure 5-9). For the samples with CdTe layer thicker than 1.5 μm, 10 Å Cu / 200 Å Au and 30 Å Cu / 200 Å Au back contacts were used and for the thinner ones the 10 Å Cu / 200 Å Au and 20 Å Cu / 200 Å Au combination was chosen. See Table 5-2 for detailed information about each sample.

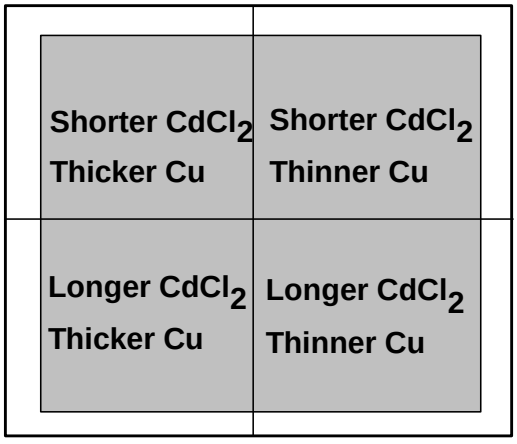

Figure 5-9. A typical sample used in this study. Each quarter-piece receives a certain combination of $CdCl_2$ treatment and back contact.

5.7 Cu diffusion time.

Table 5-2. Sample fabrication details.

Sample ID		Substrate	CdS, nm	CdTe, µm	$CdCl_2$ treatment, min		Cu, Å	Au, Å	Cu diff, min
					minal	actual			
SSC28	A	HRT Tec 15	60	2.84, 2.5, 2.15	35	38	10	200	45
	B						30		
	C				31	34	10		
	D						30		
SSC38	A			2.24, 2.0, 1.85			10		
	B						30		
	C				25	28	10		
	D						30		
SSC30	A			2.0, 1.83, 1.53			10		
	B						30		
	C				20	23	10		
	D						30		
SSC35	A			1.6, 1.35, 1.25			10		30
	B						30		
	C				15	18	10		
	D						20		
SSC37	A			1.1, 1.1, 0,95			10		20
	B						20		
	C				10	13	10		
	D						20		
SSC33	A			0.83. 0.75, 0.65			10		15
	B						20		
	C				7	10	10		
	D						20		
SSC31	A			0.68, 0.65, 0.6			10		10
	B						20		
	C				4	7	10		
	D						20		
SSC34	A			0.52, 0.46, 0.4			10		7
	B						20		
	D				2	5	10		
	C						20		
SSC32	B			0.37, 0.35, 0.3			10		5
	A						20		

Again, my previous experience suggested that Cu diffusion time should progressively get shorter as the thickness of the CdTe layer decreases. The optimum conditions for all the different thicknesses of CdTe are yet to be determined, especially on the thinnest side of the series presented here, but I followed UT's previous benchmarks that were proven to be useful (see Table 5-2 for more information).

The back contact area of 0.062 cm^2 was defined by a mask with 35 dots per quarter piece sample as pictured in Figure 5-1. Individual cells are indexed in such a way that cells with smaller numbers are closer to the middle of the sample and the larger number is closer to the outer regions. Since these cells normally have a thickness gradient from the center to the edge as reflected in the CdTe thickness column in the Table 5-2 (three values correspond to the thickness measured close to the cells #1, #9 and #25 correspondingly) this sometimes provides valuable information about fine structure in the variance of the cell performance vs. CdTe thickness.

Normally I try to obtain statistical results for the whole ensemble of 35 cells for each sample, but in this particular case I had to take a different approach. This is a consequence of an unusually large pinhole density in all the samples regardless of CdTe thickness. (We recently found the high pinhole density was a result of a particular step in our sample handling procedure that has now been changed. Although normally we keep our samples in plastic boxes without anything being in contact with the film, in this case they were stored in polyethylene bags that proved to be detrimental for the cells. We have observed that pinholes appear after the sample has been stored in the bag even for a short

period of time [42]. Electrostatic interactions between the plastic and the sample surface is the plausible cause, but further investigation is needed.)

As a result of film damage presumably caused by the plastic bags, the statistics for 35 cells ended up being greatly affected and not representative of a proper fabrication process. Therefore I had to restrict my analysis to the best 10 out of 35 cells on the each sample. I believe that this approach is more appropriate in this particular case and the results presented below nicely represent the CdTe thickness dependence that was actually sought.

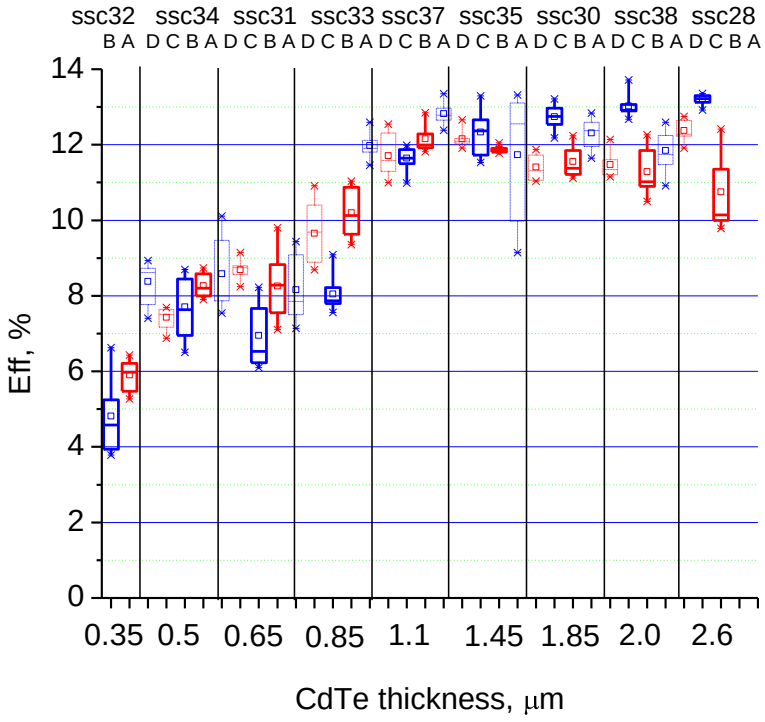

Figure 5-10. Box-and-whisker plot of the efficiency of the 10 best cells from each set. See Table 5-2 for each sample fabrication details.

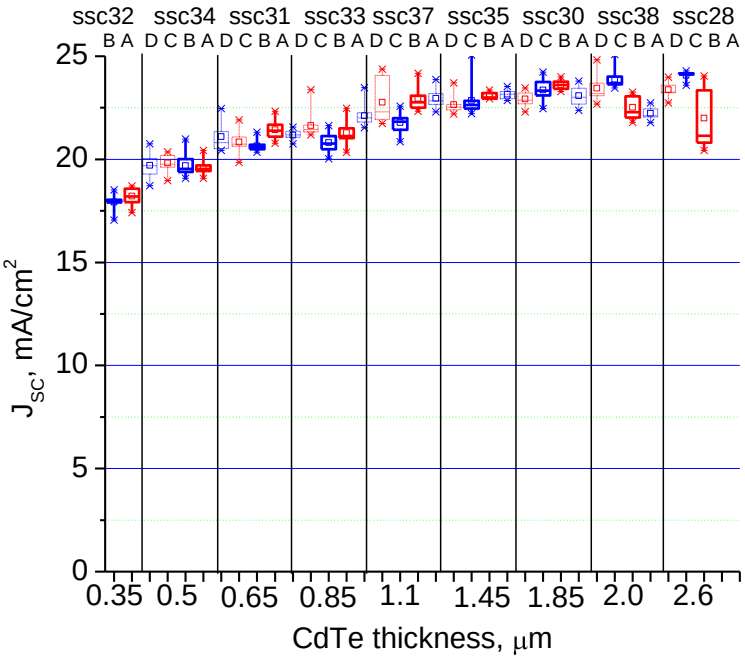

Figure 5-11. Short-circuit current of the 10 best cells from each sample. See Table 5-2 for each sample fabrication details.

Figure 5-10 represents the efficiency dependence on CdTe thickness. Box-and whisker plots represent the smallest observation, lower quartile, median, upper quartile, the largest observation, and the average value (square square dot). This applies to all the "box and whisker" plots in this dissertation. Following the recipes presented in Table 5-2 I have been able to fabricate cells with an average efficiency greater than 12 % for all the thicknesses above 1 μm. It looks from my data that this thickness represents the first tipping point below which a significant efficiency drop is observed. The second critical value appears to be around 0.5 μm below which a more rapid efficiency drop begins. It also can be seen from the figure that variations in as-deposited Cu (red vs. blue symbols) have a stronger effect on efficiency than variations in $CdCl_2$ treatment time (solid vs. dashed).

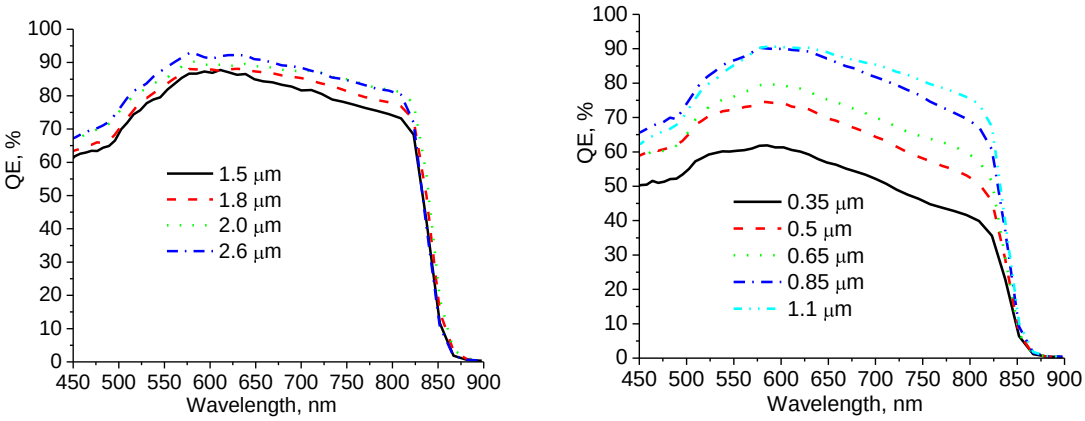

Figure 5-12. Quantum efficiency at zero bias

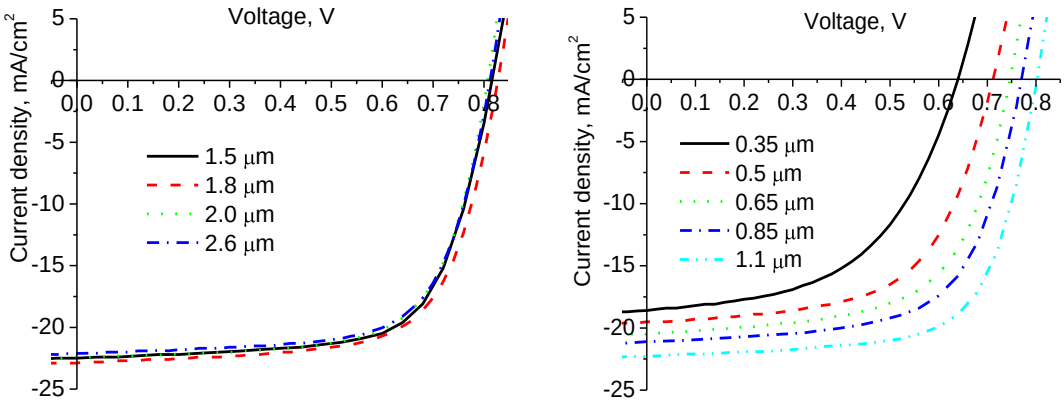

Figure 5-13, J-V characteristics of the cells from the Figure 5-11.

Figure 5-11, Figure 5-13 and Figure 5-14 represent the second order metrics for the same sets of cells. The short-circuit current (Figure 5-11) starts to decrease gradually when the thickness of the CdTe layer is less than one μm due to deep penetration loss first and more dramatically due to weaker collection which appears to be wavelength independent as can be seen from the QE graphs in Figure 5-12. On top of that there are slight variations in transmission of the CdS layer that can be attributed either to the position of the cell on the sample (CdS thickness gradient, similar to that of CdTe), or to

nominal as-deposited CdS thickness fluctuations from sample to sample, or to the amount of CdTe consumed by interdiffusion during the $CdCl_2$ treatment process.

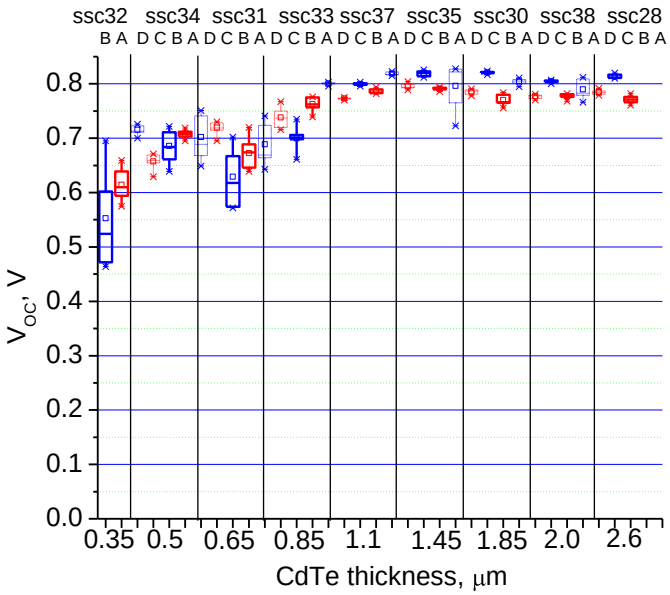

Figure 5-14. Open-circuit voltage of the 10 best cells from each sample. See Table 5-2 for each sample fabrication details.

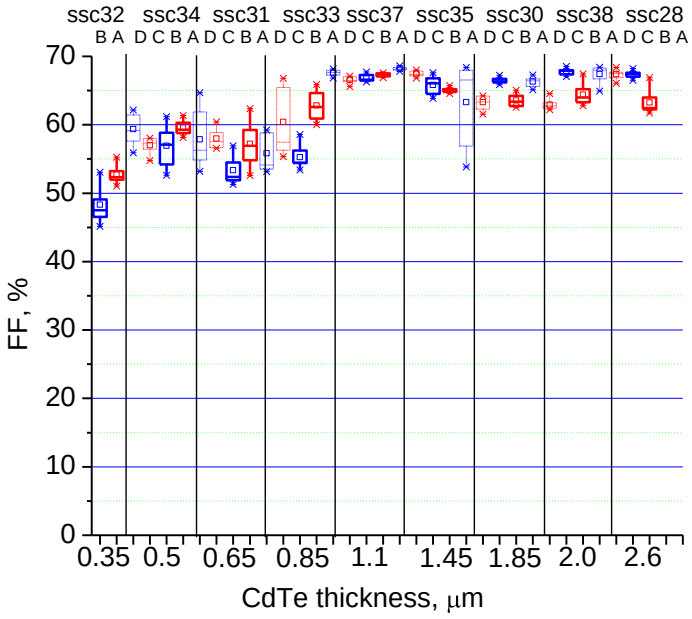

Figure 5-15. Fill factor of the 10 best cells from each sample. See Table 5-2 for each sample fabrication details.

Open-circuit voltage (Figure 5-14) follows approximately the same dependence on CdTe thickness as does J_{SC} – remaining virtually the same for all the samples thicker than one μm and gradually decreasing for the thinner ones. This is consistent with the collection problems of the thin samples observed in the J_{SC} graphs. One interesting observation is the prominent effect of Cu on the cells with thicker CdTe layers (one μm and above) - an additional 20 Å of as-deposited Cu can increase the average V_{OC} by as much as 50 mV in some cases (1.85 μm sample on the Figure 5-14). A similar dependence was observed in the fill factor as well (Figure 5-15).

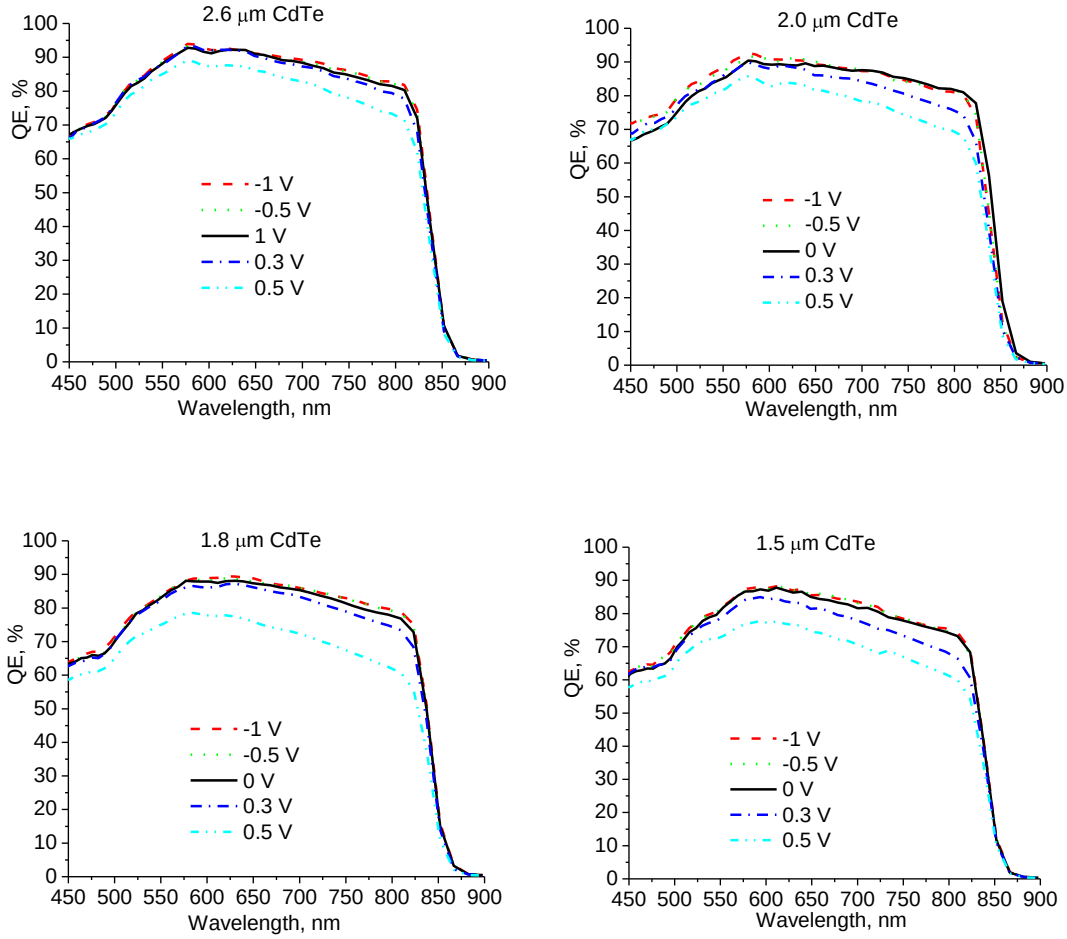

Figure 5-16. Quantum efficiency at variable bias. Thicker cells.

I obtained bias-dependent QE measurements on one of the best samples from each thickness point to investigate further the issue of carrier collection. It is remarkable that there is virtually no difference between the QE curve taken at zero bias and at reverse bias (-0.5 V and -1 V) for all the samples with CdTe layer thicker than 1 μm. There is also a very little change in the overall QE shape, for thicknesses above 1μm, except for a slight hint of deep penetration loss (Figure 5-16 and the top left graph on the Figure 5-17).

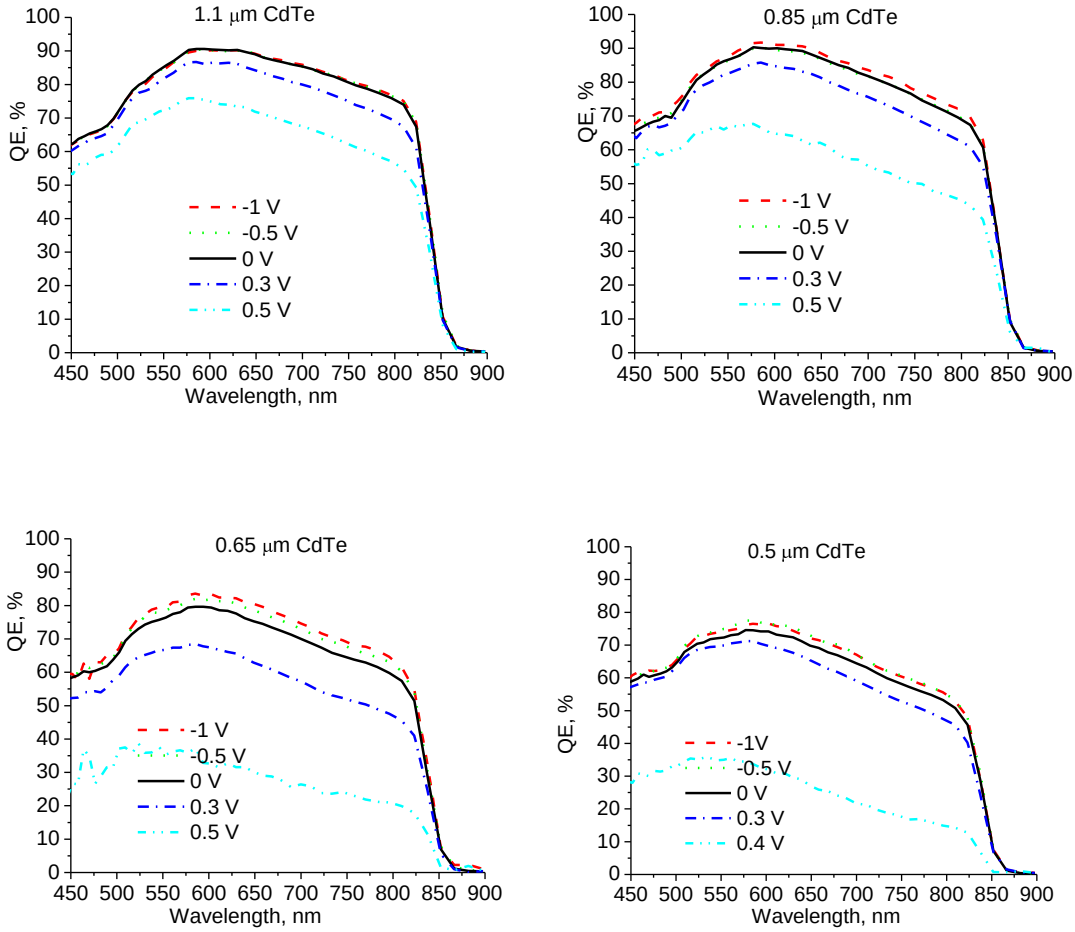

Figure 5-17. Quantum efficiency at variable bias. Thinner cells.

The results change significantly when the CdTe layer thickness decreases below one μm. The difference between zero-bias QE and reverse-bias QE becomes more apparent and shows no wavelength dependence below the CdS absorption edge. The QE also shows an overall decrease that is not compensated even by application of a strong negative bias and therefore cannot be attributed solely to a weaker electric field at the junction. I believe that it indicates some yet unidentified recombination mechanisms within the space charge region that are not present in the thicker cells. Plausible explanations can range from imperfections at the CdS/CdTe interface that are not fully

cured because of the shorter $CdCl_2$ treatment of the thinner cells, higher grain boundary surface to the volume ratio in the thinner cells due to smaller average grain size, or proximity of the CdTe/back contact junction with a high surface recombination velocity.

5.8 Conclusions

I investigated the dependence of the cell performance over a wide range of CdTe thicknesses (0.35μm…2.6μm). I found that that an average efficiency of greater than 12% can be achieved for cells as thin as 1 μm with the appropriate post-deposition treatment and optimized back contact scheme. Over CdTe thicknesses of one μm and above, I found the effect of the back-contact scheme (as-deposited Cu thickness) to be more dramatic than variation in $CdCl_2$ treatment time. Insufficient Cu caused average V_{OC} reduction of as much as 50 mV in some cases, while the use of adequate amounts of Cu yielded V_{OC} greater than 800 mV consistently for all samples within this thickness range.

I also found that further reduction of CdTe thickness leads to a gradual decrease in performance although 10% efficiency can be obtained with 0.5 μm CdTe. I established some benchmarks for $CdCl_2$ treatment and back contact processing for these samples with CdTe thickness less than one μm that yield reasonably good results although more comprehensive studies need to be done to resolve the issue of V_{OC} and FF losses.

Chapter 6: Back contact related issues

6.1 Introduction

Back contact (BC) related issues in CdTe solar cells have been studied very actively by a number of research groups [43-46]. These include optimizing initial cell performance or studying cell degradation modes depending on the amount of Cu in the back contact. While there is a lot of information available on this subject from different sources it is very difficult to summarize these results or draw a solid conclusion from them because of the use of a variety of different deposition techniques (chemical vapor deposition, closed space sublimation, magnetron sputtering for CdTe) and BC recipes (Cu-rich graphite paste, ZnTe:C, Cu/Au). Moreover, there is very little data available on back contacts for ultra-thin CdTe cells, since there has been a very limited number of successful attempts to fabricate these devices in general. In this chapter I will present some observations related to the Cu/Au thermally activated back contact often used in UT cells. I will start from a Cu X-ray fluorescence study indicating the presence of different chemical states of Cu near the CdTe/BC interface after thermal activation in an O_2-containing environment, then present results on optimizing the Cu layer thickness for the standard 2.3 μm CdTe cells. This experiment along with the study of the activation time required for the BCs with different Cu thickness, led to important guidelines for the BC recipes for ultra-thin CdTe cells. Finally I will present preliminary results on theGlass/TCO/HRT/Cds/CdTe/CdS/Cu/Au structure where an additional thin (about 20

to 50 nm) layer of CdS between CdTe and back is believed to operate as a back contact "buffer" similar to the HRT layer in the front part of the cell.

6.2 Back contact peel-off and Cu X-ray fluorescence

The first indication that, contrary to many models, the majority of Cu used for the back contact activation stays on the CdTe/back-contact (BC) interface was found during EXAFS studies of fused silica/CdS/CdTe/Cu/Au structures [20]. This experiment was done at Argonne National Lab in collaboration with Dr. Xianxin Liu (The University of Toledo) and Dr. Jeff Terry (Argonne National Lab and Illinois Institute of Technology) and its objective was to explore the chemical state of Cu in a structure which is as close to the real cell as possible.

The only difference between the structures studied and a typical working UT cell was the substrate used. Instead of using TCO-coated glass, a pure quartz substrate was used. This way we had extra assurance that there would be no residual elements in the substrate and therefore no undesired background obscuring the Cu signal. For the same reason we avoided using a ZnO TCO coating, especially taking into account the proximity of Cu K-α and Zn K-α edges.

Furthermore, we wanted to remove the upper Au layer to prevent undesired distortion in data extraction because of signal attenuation. We applied a modified version "peel-off" sample preparation technique that was used before by T. Kahle and N. Reiter [47] and can be described as follows:

1. Standard ultrasonic cleaning of 1mm quartz substrate using Micro-90 soap solution

2. Deposition of 0.13 µm CdS by magnetron sputtering
3. Deposition of 2.3 µm CdTe by magnetron sputtering
4. 30 minutes $CdCl_2$ treatment at 387 $^{\circ}$C
5. 30Å Cu/ 200Å Au back contact deposition by thermal evaporation
6. 45 minutes Cu "activation" treatment in air at 150 $^{\circ}$C to facilitate Cu diffusion at the back contact
7. Application of LOCTITE ® Quick SET™ Epoxy over the cell area
8. Full cure of the epoxy
9. Heating up the sample for 2 minutes to about 50 $^{\circ}$C
10. Pealing off the epoxy layer with Au back contact film adhered to it using tweezers

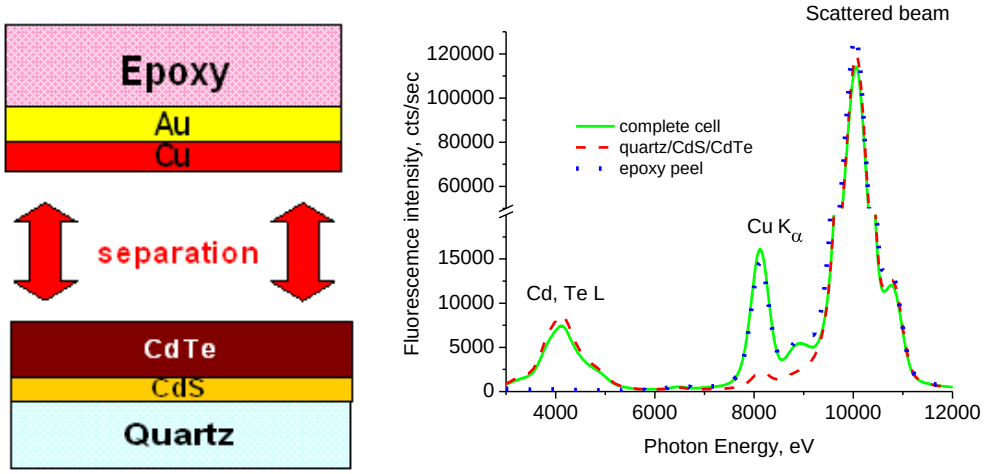

Figure 6-1. A sketch of the "peel-off" procedure (left), and corresponding X-ray fluorescence spectra of the complete cell, Quartz/CdS/CdTe part and the back contact peel (right).

It was found that careful removal of the epoxy with the back contact layer does not damage the underlying structure and in many cases a new back contact can be redeposited on the top of it to form a working cell.

The "peel-off" technique described above allowed us to compare the Cu x-ray fluorescence spectra of the full quartz/CdS/CdTe/Cu/Au with the spectra of the parts separated after peeling, namely, quartz/Cds/CdTe and the epoxy peel with metal layers adhered to it. The results along with the sketch of the peeled off structure is illustrated in Figure 6-1. Fluorescence was excited by a monochromatic x-ray beam of the Argonne APS synchrotron with energy of 10 keV. Elastic scattering of the incident beam is responsible for the most intense peak shown in Fig 1 with that energy. The two other denoted peaks are the 8.1 keV Cu K-α and closely spaced Cd and Te L-α and L-β peaks that appear to be one a single broad one at the energy about 4.2 keV. It is remarkable that while the spectrum of the complete structure exhibits both Cu and Cd/Te fluorescence peaks, after the separation the peeled-off contact has very little Cd or Te and the quartz/CdS/CdTe has very little Cu (see Figure 6-1).

The Cd and Te L fluorescence peak only appears in the spectra of the complete structure and quartz/CdS/CdTe sample. The lower intensity of the Cd/Te peak of the complete structure is likely due to attenuation by the overlying Au layer. The spectrum of the delaminated metal layer on the other hand does not have a detectable peak of these heavy elements which indicates that peeling occurs very cleanly and abruptly at the CdTe / back contact interface. The situation with the Cu K-α peak is completely opposite. The peak in the spectrum of the complete cell appears to be a superposition of the peaks of the other two. A quantitative estimation suggests that the intensity of the Cu peak from the quartz/CdS/CdTe part of the cell is roughly 10 times less intense than from the peeled off part of it. This suggests that during a standard UT cell fabrication process the majority (about 90%) of the copper remains on the CdTe/BC contact interface even after the

thermal diffusion/activation treatment at 150 ^{o}C for 45 minutes in air. EXAFS and TEM studies done by Liu et al [20, 48] have shown that this Cu is primarily in the form of oxides, while the other 10% is likely to be diffused into the structure, including along the grain boundaries, and into the CdTe and cannot be removed by physical separation along the interface as in case of the interfacial oxide layer removal during the "peel-off" process.

This result suggests that Cu in CdS/CdTe cells exists in two different forms both of which can potentially contribute both to enhanced cell performance and to Cu-associated cell degradation.

6.3 Performance of the recontacted cells

The next step was to fabricate a cell that would not have any interfacial Cu, but at the same time had a p-type back contact region formed as a result of Cu diffusion. To achieve this goal I implemented the same "peel-off" technique described previously followed by the deposition of a new Cu-free back contact on top of the area from there the old one was peeled off.

I started from TEC-7/0.13 μm CdS/2.3 μm CdTe/30Å Cu/200Å Au structures that were $CdCl_2$ treated. The efficiency of these cells was measured twice and the data were used for comparison later on. The first measurement was before Cu thermal activation, and the second time after diffusion was completed. In addition a set of samples with TEC-7/0.13 μm CdS/2.3 μm CdTe/200Å Au (i.e. without Cu) was made. These cells were also measured, but kept intact afterwards.

Therefore at the end of the first stage of this "recontact" experiment I had J-V data for the following sets of cells:

a) Tec-7/0.13 μm CdS/2.3 μm CdTe/30Å Cu/200Å Au without Cu diffusion
b) Tec-7/0.13 μm CdS/2.3 μm CdTe/30Å Cu/200Å Au after Cu diffusion
c) Tec-7/0.13 μm CdS/2.3 μm CdTe/200Å Au (no heat treatment after back contact deposition)

After the second J-V characterization, the back contacts of Cu-containing cells were lifted off and another back contact was redeposited on top of the original contact areas using a carefully aligned mask with dots of slightly smaller size. The secondary back contact schemes were applied as:

d) 30Å Cu/ 200Å Au "recontact" without second diffusion;
e) 30Å Cu/ 200Å Au "recontact" after second diffusion; and
f) 200Å Au "recontact" without secondary heat treatment.

Finally I had six different categories of cells with different back contact schemes to compare and analyze with the main question to ask - "do we need to have an interfacial layer of Cu/Cu_2O that contains about 90% of the total amount of Cu in the cell? Or can it be removed without a significant drop of cell performance?" Figure 6-2 and the following discussion answer this question:

a) The thin solid line, a, is a J-V characteristic of a typical UT cell and should be considered a "reference" one in this case. All other curves should be compared to it, which is relatively easy in three of five other cases illustrated on Figure 6-3.

b) The thin dashed line, b, corresponds to the cell with pure gold back contact. It shows an often seen J-V curve with low V_{oc} and vicious rollover indicating a large back barrier.

c) The thin dotted line, c, is for a Cu/Au back contact without thermal activation treatment. The V_{oc} is slightly higher than in the previous case and the rollover is a little less dramatic. However, it is a poor cell overall.

d) The thick dotted line, d, is the first of the "recontacted" cells – a Cu/Au recontact *without diffusion*. In general it is similar to the previous case and needs some more explanation considering the next situation.

e) The thick dashed line, e, is a Cu/Au "recontact" *after diffusion*. It shows a substantial increase of device performance over the previous case. It is not as good as the "reference" cell due to a poorer Jsc, but the Voc is just as high and there is no obvious back barrier indication. At the same time this cell contains even more Cu than the standard cell does, but secondary diffusion did not lead to increase of the performance as compared to the "reference" cell.

f) The thick solid line, f, is the last and the most interesting case – a pure Au recontact. Its J-V curve is almost identical to the previous case and still inferior to the "reference" again due to the loss of Jsc. On the other hand this cell contains about 10% of the amount of Cu that the UT reference cell does.

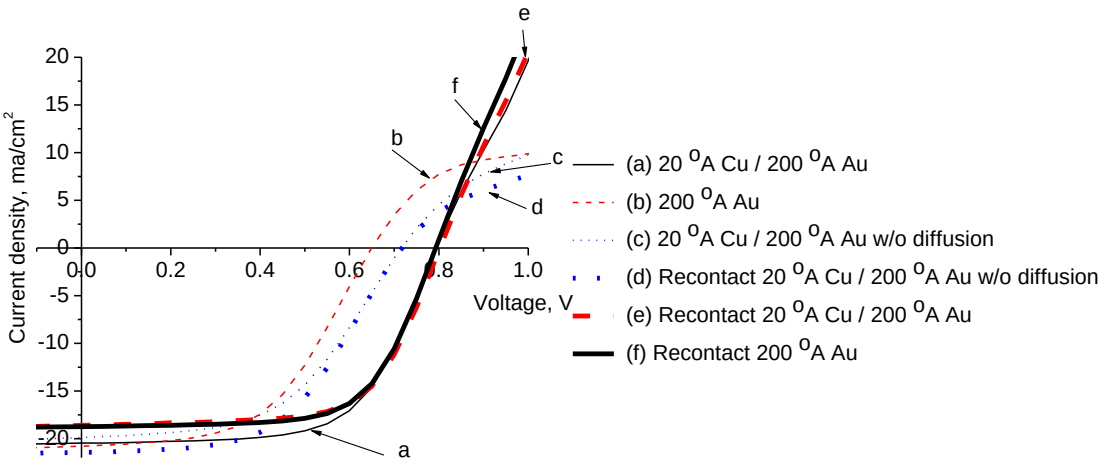

Figure 6-2. Typical J-V characteristics for the cells with different back contact structures. Letters correspond to the cases discussed in the text.

Figure 6-3 supports these observations from individual cell J-V curves in the form of statistics for first and second level metrics—efficiency, V_{OC}, J_{SC}, and FF. The data represent 8 cell ensembles for each case except "e" (4 cells). Cell area is 0.177 cm^2 for the cells "a", "b", and "c"; and 0.126 cm^2 for the cells "d", "e" and "f". Error bars represent standard deviation.

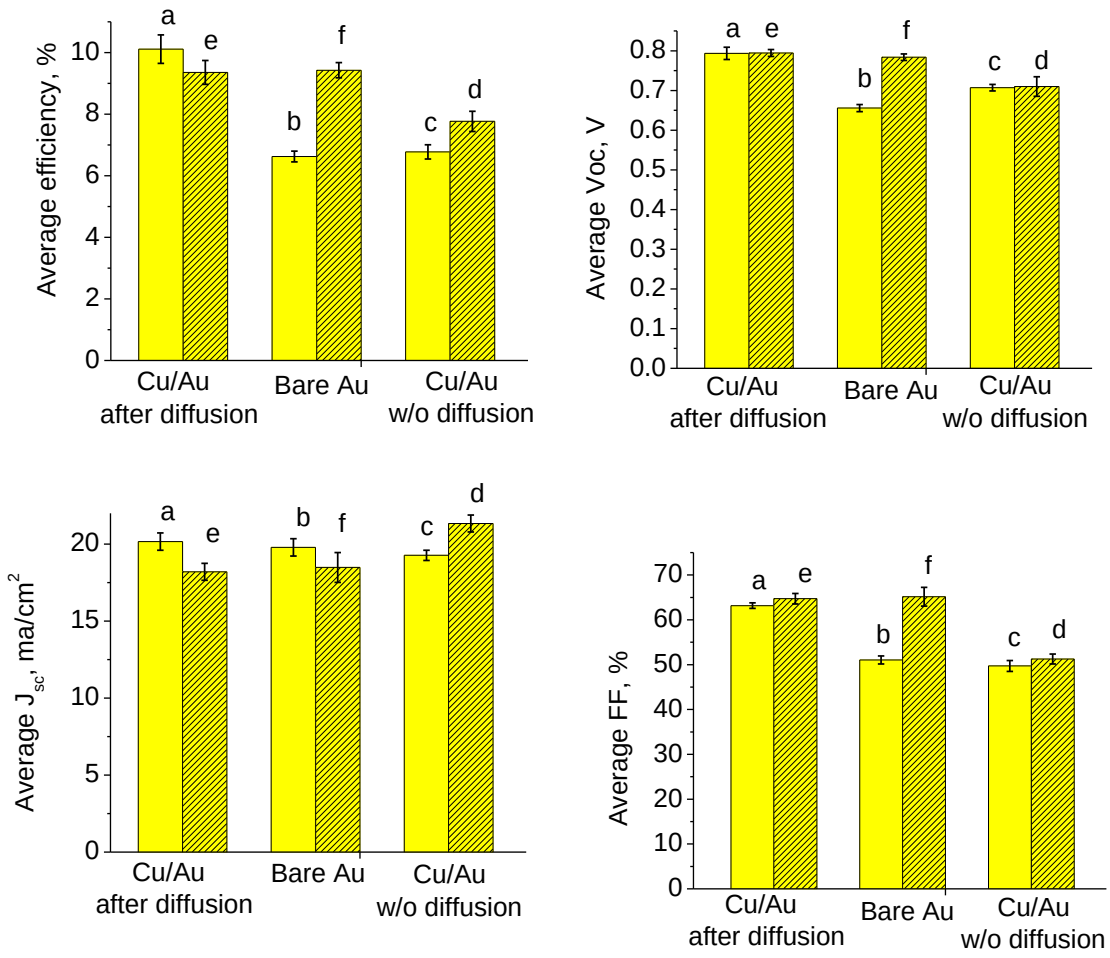

Figure 6-3. J-V parameters for cell with different back contacts. Solid colors represent regular cells and crossed ones are cells with that were "recontacted." Letters on top correspond to the letters of Figure 6-2 and have explanation in the text.

6.4 Cu activation time

UT standard 2.4 µm CdTe cells with 30 Å Cu/ 150 Å Au normally require about 45 minutes of thermal activation (150 ^{o}C, room air ambient) and have a relatively high tolerance to small variations of thermal activation time. While 45 minutes is our standard time, efficient cells with high yield can be made with 30 minutes or 60 minutes of activation time. The same is true for the thickness of the as-deposited Cu layer. The

thickness of 30 Å is considered a sweet spot, and small (within ±5 Å) fluctuations, that are typical for our Cu evaporation process, do not have a large affect on cell performance.

In order to study the interrelation between the thickness of the as-deposited Cu layer and the activation time I deliberately varied the different thicknesses of as-deposited Cu layer ranging from 3Å (approximately 10 times thinner that UT's standard for 2.5 μm CdTe cell) to 120 Å and activation time from 0 to 45 minutes with 15 minute increments. The results are shown in Figure 6-4. I found that for 2.4 μm CdTe cells to achieve maximum efficiency it is essential to have a fairly thick (30 Å to 60 Å) as-deposited Cu layer, such a layer needs a longer activation time. On the other hand, thinner Cu layer provides higher starting (no thermal activation) activation efficiency that ramps up quickly within first 15 minutes of the thermal activation process (same 150 ^{o}C, room air ambient conditions).

It was my previous observation that for the ultra-thin cells (about 0.5 μm CdTe) the diffusion time should not surpass an approximate 10 minute limit (see Figure 6-5). Therefore, it was very important to determine the optimum Cu layer thickness that provides maximum cell efficiency given that relatively short activation time. The diffusion time interval suitable for the ultra-thin cells is circled in all the graphs from Figure 6-4 and a linear fit for the average cell efficiency within this interval is shown. It can be seen from the figure that the best results for the short activation treatment can be obtained when the thickness of the as-deposited Cu layer is around 10 Å. Cell efficiency has a maximum at around 7 minutes of Cu activation time for both 3 min and 6 minute $CdCl_2$ treated cells and decreases if the activation time is too long (Figure 6-5).

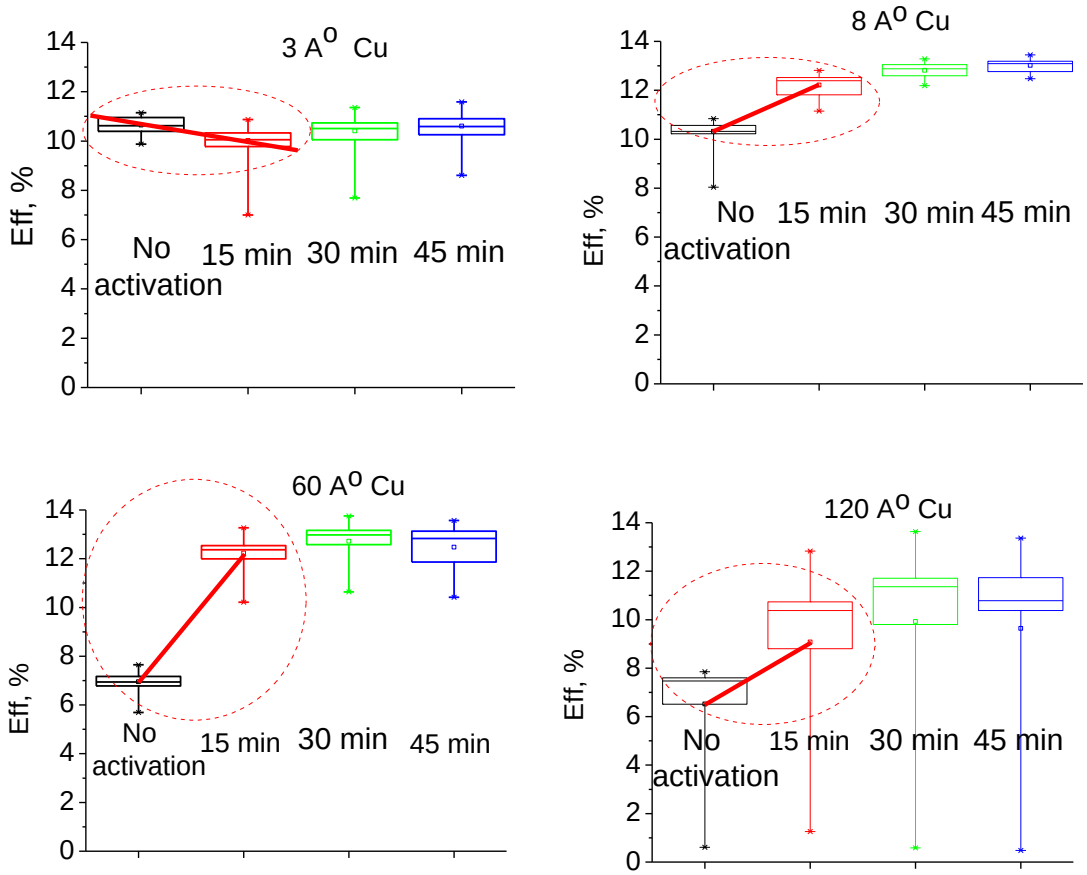

Figure 6-4. Cell efficiency dependence on the thickness of as-deposited Cu layer and heat treatment activation time. All the cells are 30nm CdS/ 2.4 µm CdTe. Change in performance after first 15 minutes of activation treatment is highlighted.

Figure 6-6 shows a different efficiency dynamic that is, in my opinion, a sign of insufficient amount of as-deposited Cu. In this case the Cu thickness was 5 Å and the maximum cell efficiency, as well as the average value, observed after 5 minutes of Cu diffusion is approximately 2% absolute percent lower that for the case of thicker (10 Å) Cu layer (compare with Figure 6-5). Additional diffusion time with 5 min increments decreases cell performance, but the drop was relatively small, compared to the case of 10 Å Cu back contact, the performance did not change much even after 25 minutes of Cu diffusion

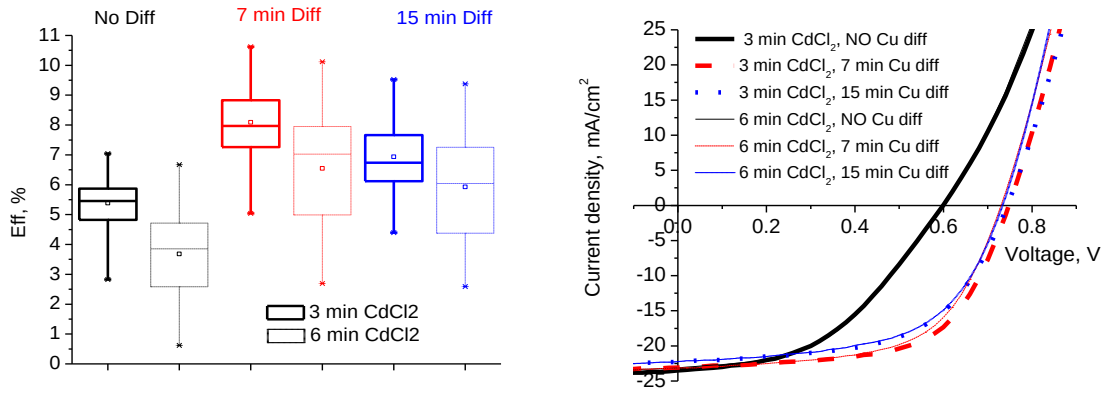

Figure 6-5. 0.5 µm CdTe cell efficiency dependence on the back contact heat treatment activation time. Statistics for 35 cells (left), and J-V curves for the best cell (right). Two sets of cells are shown –one is 3 min $CdCl_2$ treatment time and the other is 6 min $CdCl_2$ treatment time. In both cases the thickness of the Cu layer is 10 Å.

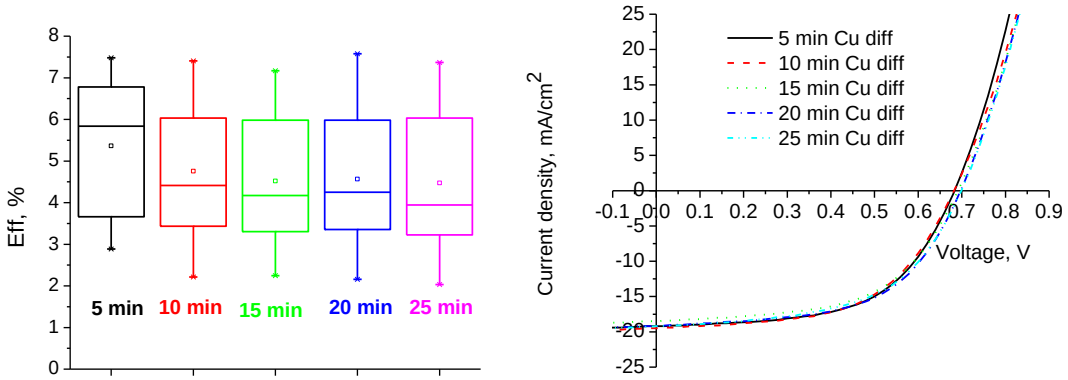

Figure 6-6. 0.5 µm CdTe, 5 Å Cu cell efficiency dependence on the back contact heat treatment activation time. Statistics for 35 cells (left) and J-V curves for the best cell (right.)

6.5 Back contact "buffer" CdS layer

6.5.1 Back contact with CdTe thickness ≥ 0.5 µm

Application of a "buffer" layer such as HRT (high-resistivity transparent) coating has been proven to be a winning strategy to increase cells performance [36, 49].

Typically this layer is applied to the front (glass) side of the CdS/CdTe solar cell,

between the TCO (transparent conductive oxide) and CdS layer. Several materials, including Cd_2SnO_4 [50], Zn_2SnO_4 [51], ZnO [52], SnO_2 [53] or oxygenated CdS [54] have been successfully used for this purpose. Pure CdS, if made sufficiently thick, also serves as a shunt passivation layer effectively [35, 36]. The main limitation with using thick CdS is the J_{SC} loss due to the absorption in the CdS layer that was described thoroughly in Chapter 4. Therefore, recently there has been a lot of interest in shunt passivation from the back contact side. It is typically done after the completion of the $CdCl_2$ treatment, but before the application of the back contact [55].

In this work I decided to use a different approach, namely sandwiching the CdTe between two layers of thin (about 30 nm) CdS (Figure 6-7). The CdS and CdTe layer can deposited in the same chamber with or without vacuum break (see discussion below) and the $CdCl_2$ treatment is done after the whole CdS/CdTe/CdS stack is completed. Cells were finished with Cu/Au back contacts. In this case the front CdS layer is acting similar to those in a normal cell configuration, providing the formation of a strong photovoltaic junction and mild shunt passivation, while allowing for a good transmission in the blue region. The back CdS layer does not alter the photocarrier generation since the short wavelength photons are already absorbed even in the ultra-thin (0.3 μm to 0.5 μm) CdTe layer. However the back CdS is still expected to exhibit shunt passivation properties. The band diagram of a cell with such configuration is undetermined at this time, but it is plausible to expect that the back CdS is p-type due to Cu doping after the Cu/Au back contact thermal activation. I also expect an extensive CdS_xTe_{1-x} alloy formation near the back contact.

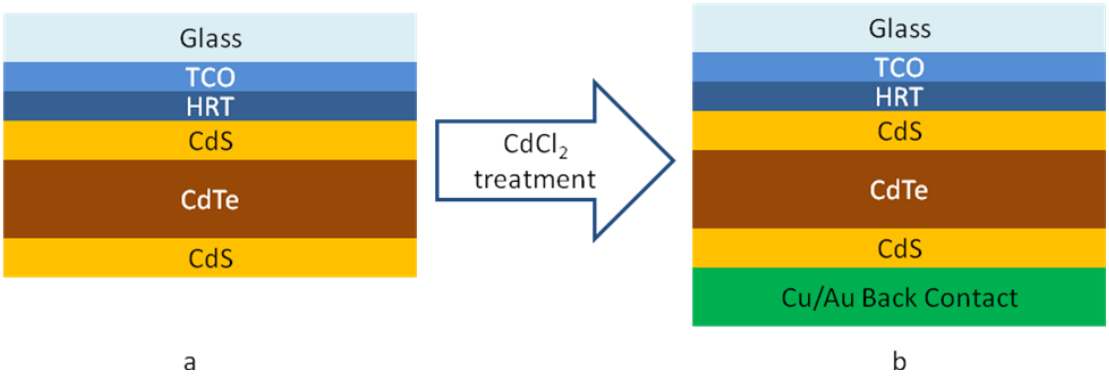

Figure 6- 7. CdS/CdTe/CdS call fabrication process. Cell structure after the magnetron sputtering (a) and after CdCl2 treatment (b)

The result of CdS back buffer layer application for 0.5 µm CdTe cells is shown in Figure 6-8. The 30 nm CdS/0.5 µm CdTe/ 30 nm CdS cells are compared to conventional 30 nm CdS/0.5 µm CdTe cells without back buffer. There are two sets of conventional (CdS/CdTe) cells with a difference in CdTe layer deposition parameters. One is our standard 18 mTorr, 20 W RF power CdTe and the other is a high-rate (see Chapter 3) 9 mTorr, 40 W RF power sample. The CdTe of the cells with back buffer (CdS/CdTe/CdS) is a conventional 18 mTorr, 20 W RF power layer. Both front and back CdS layers in all the cells are deposited using 18 mTorr, 35 W RF power conditions.

My conclusion from Figure 6-8 is that while the CdS/CdTe/CdS structure is inferior to the conventional CdS/CdTe structure in terms of the maximum cell efficiency, the efficiency distribution for the cells with the back CdS layer is much tighter and suggests that the second CdS layer acts as a buffer as expected. Overall, even though it seems like the back buffer CdS layer benefits the yield and the average efficiency; I would not describe the difference in performance as a dramatic. It has been shown in

Chapter 5 and earlier in this chapter that about 10% efficient 0.5 µm CdTe cells can be successfully fabricated with just the front HRT buffer layer.

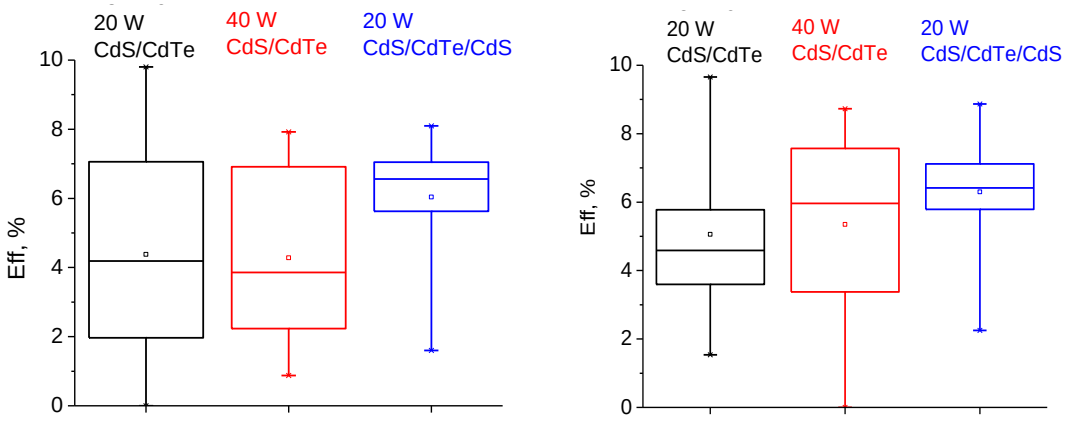

Figure 6-8. 0.5 µm CdTe cells with and without back CdS buffer layer. 2 min CdCl2 treatment (left) and 3 min $CdCl_2$ treatment (right). Statistics is shown for 35 0.06 cm^2 cells of each type.

6.5.2 Back contact with CdTe thickness ≤ 0.5 µm

On the other hand, earlier, I had considerably less success with the cells thinner than 0.5 µm and the conventional CdS/CdTe structure (see Chapter 5 again). Thus I decided to try the back contact CdS buffer approach to the cells with the CdTe layer of 0.3 µm and below. Figure 6-9 shows the thickness profiles across samples ssc21 (originally without back CdS buffer) and ssc22 (with back CdS buffer), deposited during two consecutive depositions. The deposition time and parameters for the both cells were exactly the same (18 mTorr, 35 W CdS. 18 mTorr, 20 W CdTe) and it translated into nearly identical thickness. The slightly thicker profile of the cell ssc22 can be attributed to the back CdS layer of 30 nm nominal thickness added to the cell structure without the vacuum break.

Figure 6-10 illustrates the combinatorial approach used for this experiment. Both samples were divided in halves and the parts ssc21a and ssc22a were used in the first run of the post-deposition processing which consisted of 3 minutes of $CdCl_2$ treatment at 387 ^oC and application of 13 Å Cu/ 150 Å Au, followed by 5 minute thermal activation (150 ^oC, room air ambient). Cell performance results (represented statistically in Figure 6-11) indicated a huge difference between the cells with and without back CdS buffer (6 % vs.3.5% maximum efficiency and 3.5 % average efficiency vs. 1.5% average efficiency correspondingly).

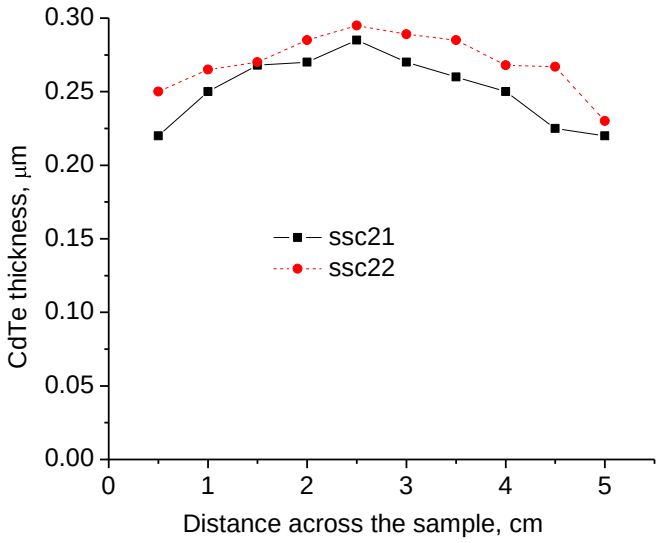

Figure 6-9. Thickness profiles of the samples ssc21 and ssc22

In order to confirm these results I decided to complete the ssc21b piece by adding a 30 nm back CdS layer and repeat the post-deposition process identical to the one applied to the samples ssc21a and ssc22a. After the deposition of the back CdS layer, sample ssc21b was treated together with the sample ssc22b, so I ended up with 1 sample with conventional CdS/CdTe structure and 3 samples with CdS/CdTe/CdS sandwich

structure with 70 0.06 cm^2 individual cells on each. The results are summarized in Figure 6-11.

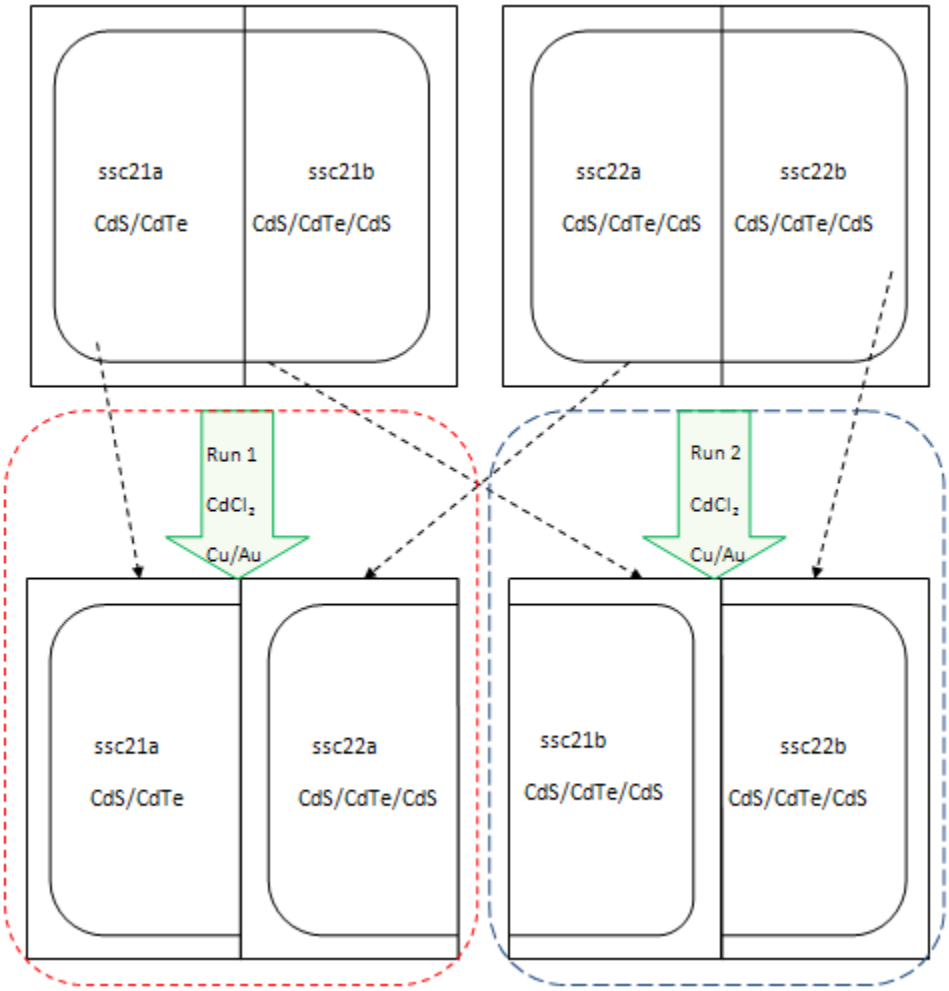

Figure 6-10. Combinatorial approach used for the samples ssc21 and ssc22. Parts ssc21a and ssc22a were processed together during the post-deposition run 1. Sample ssc21b was completed with CdS back buffer and then combined with the sample ssc22b for the post-deposition run 2. $CdCl_2$ treatment and Cu/Au back contact parameters are nominally identical for the both runs.

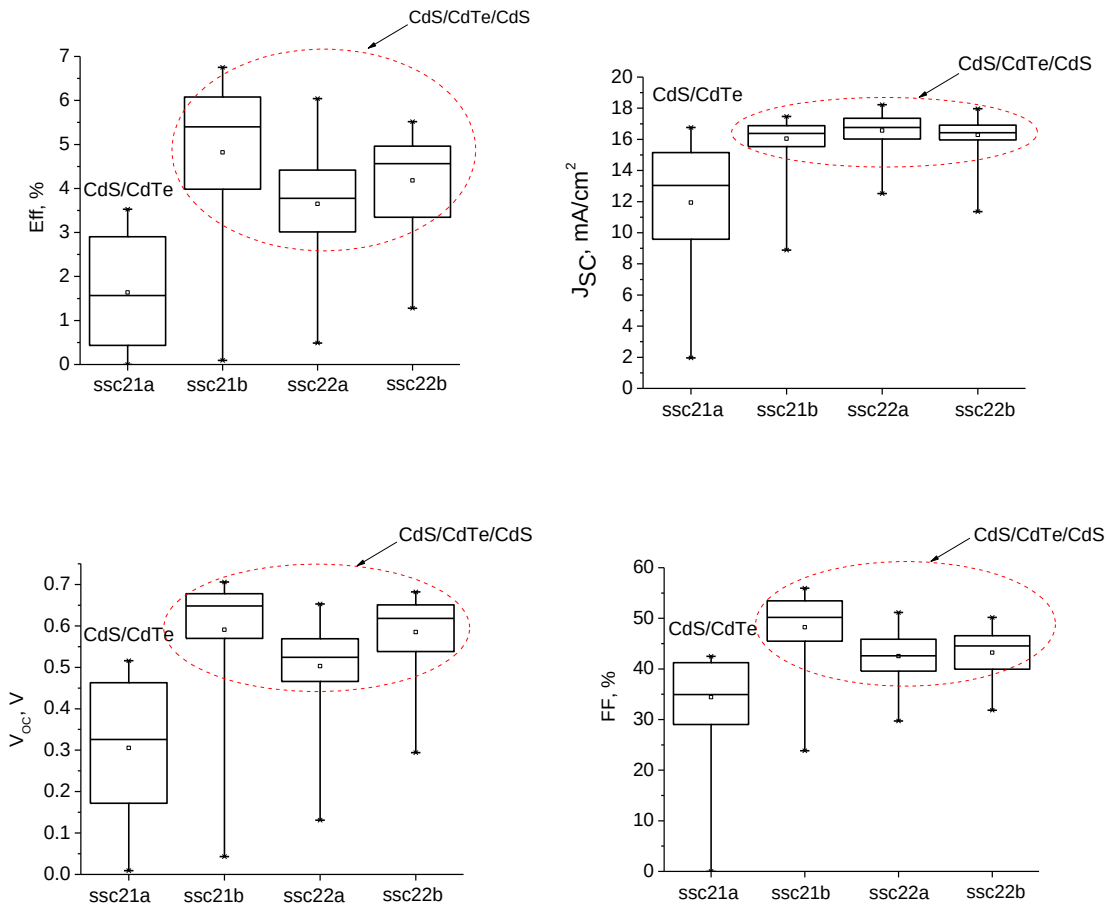

Figure 6-11. First and second order metrics for the samples ss21a, ssc21b, ssc22a and ssc22b.

Sample ssc21b has shown the best performance out of the four samples measured. Maximum cell efficiency was 6.7 % with the V_{OC} of 707 mV and FF of 56%. These numbers indicate a great difference in cell performance between the sister piece (ssc21a) that does not have the back CdS layer. Sample ssc21b is the best sample with the CdTe thickness below 0.3 µm that I have made to date. I believe that the key feature to achieve

this result was the application of the CdS back buffer that should be optimized and studied in greater detail later.

6.6. Conclusions

In this chapter I summarized a number of observations related to the back contact of the CdS/CdTe solar cells, that were done by me over an extended period of time and ranging from Cu distribution in the CdTe and back-contact layer, through the dependence of cell performance on the amount of Cu in the back contact, to the effect of back buffer CdS layer. Some of these results are specific to the ultra-thin devices, while others were obtained on conventional 2.4 μm CdTe cells and still benefited from the optimization process.

I studied the dependence of the standard (2.4 μm CdTe) cell performance on the Cu thickness and the heat treatment (at 150 ^{o}C) activation time over the wide range of Cu thickness (from 5 A to 120 Å). There were 3 main observations made:

1) Unless the Cu layer thickness is extremely small (below 5 Å) a specific diffusion time is required to achieve optimum cell performance.

2) The thicker the as-deposited Cu layer the lower is the efficiency of the cells that did not receive any Cu activation treatment at all. A plausible explanation for this phenomenon is that if sufficiently thick, as-deposited metallic Cu imposes boundary conditions that are different from those of Au on the CdTe/ back contact interface. The Cu workfunction of 4.5 eV is less than that of Au (5.1 eV), therefore it is plausible to expect the formation of a higher Schottky barrier at the CdTe/back contact interface for the cells with a thick Cu layer. Increase of cell

performance after heat treatment in O_2-containing ambient can be attributed to conversion at least some of the metallic Cu into the Cu_2O phase and much of the rest interdiffusing with Au [48], along with well-known CdTe p-type doping and corresponding changes in band alignment and carrier transport mechanisms. In contrast, if the Cu layer is thin enough to begin with, its influence on the back barrier height is less noticeable and allows for higher performance of the cells without any back contact heat activation treatment.

3) The thicker the Cu layer, the steeper is the slope of the efficiency vs. activation time curve for the first 15 to 30 minutes of activation.
4) If the Cu layer is extremely thin (below or about 5 Å) there was no significant change in efficiency as a function of activation time observed.

These results, along with our previous studies indicate that ultra-thin cells require shortened activation time of about 5 to 10 minutes, and lead to the conclusion that the optimum Cu thickness for the ultra-thin devices should be about 10 Å. This has been taken into account for the optimization process and yielded good results with ultra-thin cells later (see also Chapter 5).

Finally, I presented some results on the back buffer CdS layer that helps to significantly improve the performance of 0.3 μm CdTe cells. Maximum efficiency of 6.7 % and V_{OC} of 707 mV have been observed for such devices. Even though this approach needs to be studied further, it looks like a promising alternative to other shunt passivation schemes, since it can be completed with the existing deposition equipment without a vacuum break, does not introduce any other element besides those already used in the fabrication process, does not require a wet processing or other chemical treatment.

Chapter 7: Conclusion

7.1 Summary

This dissertation is focused on the thinning down of the absorber layer in CdS/CdTe solar cells fabricated by magnetron sputtering. During the first phase of this work, as a result of some slight revisions of the UT standard fabrication procedures, a robust 12.5% baseline for conventional 2.4 μm CdTe cells was established. The second phase consisted of determining the optimum fabrication conditions for the cells with reduced CdTe thickness. For instance, 12% efficiency cells with 1 μm CdTe, 10 % cells with 0.5 μm CdTe and 6.5% with 0.3 μm CdTe were fabricated.

The major challenges in ultra-thin cell fabrication, such as deep penetration losses, pinholes, nonuniformities (weak diodes), fully depleted layers, interaction between closely spaced front and back junctions, and cell degradation/shunting caused by Cu migration were described in Chapter 1. Many of these issues were successfully addressed later. For example, Chapter 2 gives an overview of the magnetron sputtering process and contains results on the potential distribution in the sputtering system plasma. One of the major findings that came from this study, besides the more in-depth characterization of the deposition process, was the realization that the substrate self-bias plays an extremely important role in pinhole formation during CdTe deposition. A sudden increase in pinhole density after cleaning of the magnetron gun ground shroud was successfully traced down to the change in substrate self-bias caused by the lowering

of the plasma potential for the case of the bare ground shroud. I opted for the mild cleaning of the loose particles instead of complete stripping down of the CdTe coating from the ground shroud, and this led to much improved consistency in device yield that played a major role in establishing a solid baseline for conventional cells.

Two other important methods of pinhole passivation which are also very effective for curing of other nonuniformities, such as weak diodes, are described in Chapter 4 and Chapter 6. Chapter 4 emphasizes the role of the high resistivity transparent (HRT) coating and concludes that the thickness of CdS layer can be reduced to 30 nm to 45 nm in case the good quality HRT layer is applied. Chapter 6 introduces an alternative method for "buffering" nonuniformities by sandwiching a CdTe between two thin (about 30 nm) layers of CdS. This approach needs to be studied further, but it has already shown its potential for ultra-thin cells with CdTe thickness below 0.5 μm.

Achieving high CdTe doping concentration still remains an issue for the thin cells, but I believe I had a big improvement in cell performance and especially the consistency of the results after switching to the wet $CdCl_2$ treatment described in Chapter 5. I achieved a maximum Voc of 840 mV for a conventional 2.4 μm cell, and an impressive 747 mV for 0.5 μm cell by using this technique.

7.2 Future considerations

One of the most challenging areas in ultra-thin CdTe cell fabrication that certainly requires more in-depth studies is the back contact. My research has shown that Cu is an essential element for high performance ultra-thin cells, much like it is for the thicker devices. On the other hand, it is also evident that the amount of Cu should be reduced for

the ultra-thin cells. I achieved best results using a 10 Å as-deposited Cu layer, but the exact interrelation between the CdTe thickness, amount of Cu and duration of the optimum heat activation treatment still needs better understanding.

Another challenging issue is the yield of the ultra-thin devices which is typically lower than that of the thicker cells. In this regard, front and possibly back buffer layers seem to be almost inevitable for successful fabrication of the ultra-thin cells. While the front HRT layer has received considerable of attention, prior to this work, the concept of the back CdS buffer layer introduced in this dissertation may serve as an alternative, or better yet, supplemental shunt passivation treatment for the ultra-thin devices.

Lastly, I would like to mention explicitly that the issue of the deep penetration losses was acknowledged but not fully addressed by any means in this work. Partially this is due to the dual nature of this phenomenon with respect to the ultra-thin cells. On one hand, the cell performance can certainly benefit if these losses are minimized. I expect the known techniques such as use of the back reflector or coarsely textured TCO layer that enhance the optical path and provide better absorption of the red photons within the cell to be fully applicable in the CdTe ultra-thin cell technology. On the other hand, cells with the CdTe layer of 0.5 μm and thinner can be specifically designed for semitransparent applications, such as architectural glass or top cells in tandem devices. In this case, a higher transparency below and slightly above the CdTe absorption edge is actually beneficial, and the main effort should be focused on developing a stable, highly efficient transparent back contact.

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