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16.5%-Efficient CdS/CdTe POLYCRYSTALLINE THIN-FILM SOLAR CELL

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ABSTRACT: Cadmium telluride is a promising photovoltaic material for thin-film solar cells. However, the performance and reproducibility of devices has been limited by the conventional SnO_2/CdS/CdTe device structure used for more than 30 years. In this paper, we report that the device performance and reproducibility of CdTe cells can be improved by using a modified CTO/ZTO/CdS/CdTe device structure developed at NREL. We achieved high FF of 77.34% and high J_{sc} of near 26 mA/cm^2, and fabricated a CdS/CdTe polycrystalline thin-film solar cell demonstrating an NREL-confirmed, total-area efficiency of 16.5%. This is the highest efficiency ever reported for CdTe solar cells.
Keywords: CdTe – 1: High-Efficiency – 2: Polycrystalline - 3

1. INTRODUCTION

Cadmium telluride has been recognized as a promising photovoltaic material for thin-film solar cells because of its near-optimum bandgap of ~1.5 eV and its high absorption coefficient. Small-area CdTe cells with efficiencies of more than 15% [1,2] and commercial-scale modules with efficiencies of >10% [3-5] have been demonstrated. However, the performance and reproducibility of CdTe cells have been limited by the conventional SnO_2/CdS/CdTe device structure that has been used for more than 30 years. For example, conventional transparent conductive oxides, primarily SnO_2 films, have an average transmission of only 80% when a sheet resistivity of ~10 Ω/sq is used. This does not provide adequate design latitude when trying to optimize either device performance or manufacturing cost. The CdS window layer has a low bandgap (~2.4 eV) that causes absorption in the short-wavelength region. The CdS film with 0.1-μm thickness can absorb about 63% of the incident radiation with energy greater than the bandgap energy [6]. Higher short-circuit current densities (J_{sc}) can be achieved by reducing the CdS thickness to improve the blue response in the conventional CdS/CdTe device structure [1,2]. However, reducing the CdS thickness can adversely impact device open-circuit voltage (V_{oc}) and fill factor (FF) [7-9]. Finally, it is well known that the $CdCl_2$ treatment is important for making high-efficiency CdTe devices and offers several substantial benefits such as: increased grain size, grain-boundary passivation, increased CdS/CdTe interface alloying, and reduced lattice mismatch between the CdS and CdTe layers. However, one disadvantage of the $CdCl_2$-treatment is that over-treatment can result in loss of adhesion. The adhesion problems can limit the optimal $CdCl_2$ treatment process, as well as device performance.

In the last five years, we have tried to understand and solve these issues related to the conventional SnO_2/CdS/CdTe device structure. We developed several novel materials and a modified CdTe device structure. First, we developed a novel process to prepare high-quality cadmium stannate (Cd_2SnO_4, or CTO) transparent conductive oxide (TCO) films, which have lower resistivity, higher transmittance, and smoother surfaces than conventional SnO_2 TCO films [10-12]. By replacing the SnO_2 TCO film with a Cd_2SnO_4 film in a CdTe cell, J_{sc} and FF of CdTe cells can both be improved [13-15]. Second, we developed and integrated a high-resistivity zinc stannate (Zn_2SnO_4, or ZTO) buffer layer into CdTe cells, which improved device performance and reproducibility [16-18]. Third, we developed and integrated modified CdS films, with a higher optical bandgap into our CdTe devices. This improved the quantum efficiency in the blue and the J_{sc}. Fourth, we developed a modified CTO/ZTO/CdS/CdTe device structure and made high-efficiency CdS/CdTe polycrystalline thin-film solar cells [19]. Finally, we developed a novel manufacturing process for fabricating high-efficiency CTO/ZTO/CdS/CdTe solar cells with the potential for low cost and high throughput [20,21].

In this paper, we present the updated high-efficiency device results and give some examples to explain how the modified CTO/ZTO/CdS/CdTe device structure achieves the high performance and good reproducibility.

2. EXPERIMENTAL

Figure 1 shows the modified CTO/ZTO/CdS/CdTe device structure. In this device structure, a cadmium stannate TCO film replaces the conventional SnO_2 TCO film as a front contact, and a zinc stannate film is integrated as a buffer layer located between the CTO and CdS layers.

Both CTO and ZTO films were deposited by rf magnetron sputtering at room temperature in pure oxygen using commercial hot-pressed oxide targets with 99.99% purity. The cleaned Corning 7059 glass substrate (for CTO film deposition) or the CTO film on the glass (for ZTO film deposition) was placed on a sample holder parallel to the target surface. The sputter system was evacuated to a base pressure of ~2 x10^{-6} torr, and then backfilled to 10-20 x10^{-3} torr with pure oxygen gas. The distance between the substrate and the target was varied from 6 to 9 cm. An Inficon XTC quartz-crystal monitor measured the film thickness and deposition rate. Prior to each deposition, the

target was pre-sputtered for ~5 minutes while the substrate was covered by a shutter. Subsequently, the CTO film was treated at 580°-660°C for 10-20 minutes in a CdS/Ar atmosphere. The thickness of both CTO and ZTO films was varied from 100 to 300 nm. The CdS film was prepared by a chemical-bath deposition (CBD) technique [22], using cadmium acetate [$Cd(C_2H_3O_2)_2$], ammonium acetate ($NH_4C_2H_3O_2$), ammonia hydroxide (NH_4OH), and thiourea [$CS(NH_2)_2$] in an aqueous solution. The CdTe films were prepared by the close-spaced sublimation (CSS) technique and were deposited at 570°-625°C for 3-5 minutes in O_2/He atmosphere. After CdTe deposition, samples received a vapor $CdCl_2$ treatment at 400°-430°C for 15 minutes. HgTe:CuTe-doped graphite paste annealed at ~270°C for 30 minutes, followed by a layer of Ag paste, was then applied to the devices as the back-contact layer. An ~1000Å MgF_2 antireflection (AR) coating was deposited on some of the cells.

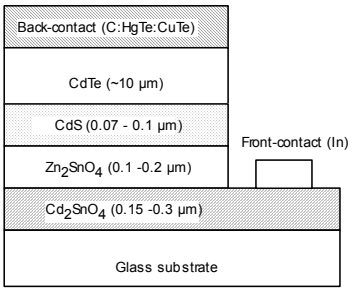


Figure 1. A modified CTO/ZTO/CdS/CdTe device structure.

3. DEVICE RESULTS AND DISCUSSION

Using the modified CTO/ZTO/CdS/CdTe device structure, we have achieved a high FF of 77.34%, a high J_{sc} of near 26 mA/cm^2, and an efficiency of 16.5%.

3.1 High fill factor

Table 1 lists current-voltage parameters of two high-efficiency CdTe cells with FF of more than 77%. These are the highest FF values ever reported for CdS/CdTe polycrystalline thin-film solar cells. Device analyses from NREL and the Colorado State University [23] indicate that these cells with a high FF have a lower series resistivity R_s (~1 Ω cm^2), a higher shunt resistivity R_{sh} (3-5x10^3 Ω cm^2), and better diode quality factor A (1.6-2).

Table 1. High-efficiency CdTe cells with high fill factor.

Cell #	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	Area (cm^2)
1	842.1	24.12	**77.26**	15.7	1.001
2	848.1	23.97	**77.34**	15.7	0.976

3.1.1 Reduced series resitivity R_s by replacing SnO_2 with CTO film

It is well known that reducing TCO resistivity is essential for reducing R_s and improving FF in superstrate devices. The cadmium stannate TCO films have electrical resistivities (ρ ~1.5x10^{-4} Ω cm) two times and six times lower than SnO_2 films produced using $Sn(CH_3)_4$ (TMT) and $SnCl_4$ chemistries, respectively (see Table 2). The high conductivity of the Cd_2SnO_4 films is attributed to its high mobility (μ) with high carrier concentration (n). The high mobility of CTO films results from their near defect-free microstructure [19]. It is thus obvious that by replacing the SnO_2 with a Cd_2SnO_4 TCO film, the series resistivity R_s of a cell can be reduced. At present, the width of sub-cells in CdTe module design is mainly limited by the conductivity of the TCO film. Therefore, the low-resistivity Cd_2SnO_4 films will allow us to increase the width of the sub-cells, thereby increasing the total-area module efficiency.

Table 2. Comparison of electrical properties between the Cd_2SnO_4 and SnO_2 films.

Sample	Thick-ness (Å)	n (cm^{-3})	μ cm^2/Vs	ρ (Ω cm)	R_s Ω/Sq
Cd_2SnO_4	5100	8.94 x10^{20}	54.5	1.28 x10^{-4}	2.6
SnO_2 ($SnCl_4$)	~10000	4.95 x10^{20}	15.4	8.18 x10^{-4}	8.6
SnO_2 (TMT)	~10000	4.52 x10^{20}	42.0	3.29 x10^{-4}	3.3

3.1.2 Increased shunt resistivity R_{sh} by integrating ZTO buffer layer

In the modified CTO/ZTO/CdS/CdTe device structure, the shunt resistivity R_{sh} can be improved in two ways by integrating a ZTO buffer layer.

First, the ZTO buffer layer can reduce the probability of forming localized TCO/CdTe junctions when the CdS film is thinned. In the conventional SnO_2/CdS/CdTe device structure, high J_{sc} is achieved by reducing the CdS thickness to improve the blue spectral response. However, reducing the CdS thickness can adversely impact device V_{oc} and FF. As the CdS thickness is thinned, the probability of pinhole formation increases, causing localized TCO/CdTe junctions with inferior device parameters (V_{oc} and FF). But the addition of a ZTO buffer layer located between the CTO and the CdS layers minimizes the probability of forming localized TCO/CdTe junctions, because the ZTO film has both high optical bandgap (~3.6 eV) and high resistivity that roughly matches that of the CdS film.

Second, the ZTO buffer layer can act as an "etch-stop" layer during the back-contact formation process and greatly reduce shunting problems. It is well known that the polycrystalline CdTe film is very difficult to dope heavily p-type, and therefore, to make a low-resistance back-contact. Thus, a wet-chemical etch (such as a nitric/phosphoric-based acid etchant) is typically used to form a p^+ surface region. Although this p^+ surface layer facilitates ohmic contact formation, this etch can also preferentially etch boundaries, leaving highly conductive shunt paths that degrade the device shunt resistivity, thereby reducing device

FF and V_{oc}. Figure 2 shows an over-etched CdTe film, in which there are a number of shunt paths along grain boundaries. Because the ZTO film resists the etchant used for back-contact formation (i.e., serving as an "etch-stop" layer), these devices are less susceptible to over-etching, which greatly reduces shunting problems.

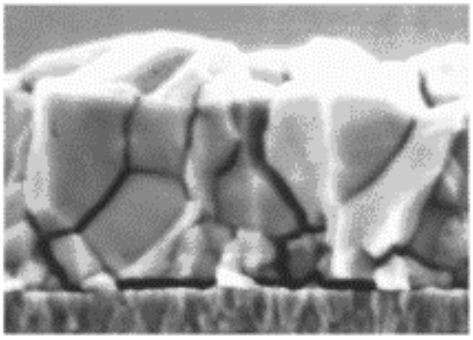


Figure 2. An "over-etch" CdTe film with a number of shunt paths along grain boundaries (SEM data).

3.2 High short-circuit current density

Table 3 lists current-voltage parameters of two high-efficiency CdTe cells with J_{sc} of nearly 26 mA/cm^2. In this work, high J_{sc}'s have been achieved in three ways: reducing J_{sc} loss due to TCO absorption; reducing J_{sc} loss due to CdS absorption; and reducing J_{sc} loss due to recombination in the junction and CdTe regions.

Table 3. High-efficiency CdTe cells with high J_{sc}.

Cell #	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	Area (cm^2)
1	847.5	**25.86**	74.45	16.4	1.131
2	845.0	**25.88**	75.51	16.5	1.032

3.2.1 Reduced J_{sc} loss due to TCO absorption

Cd_2SnO_4 films have significantly better optical properties than conventional SnO_2 films. This is, in part, due to the lower resistivities, which allow thinner film to be used. Figure 3 shows the transmittance and absorbance of both Cd_2SnO_4 and SnO_2 films with similar sheet resistivities (~10 Ω/sq). It can be seen that the Cd_2SnO_4 film has a higher transmittance and a lower absorbance than the SnO_2 film. Our results have demonstrated that the J_{sc} can be improved by replacing the SnO_2 film with a Cd_2SnO_4 TCO film in CdTe devices.

Table 4 lists the J_{sc} loss due to TCO absorption for four different TCO films that are all deposited on Corning 7059 glass. It can be seen that the CTO film has the lowest J_{sc} loss (~0.6 mA/cm^2) – two to four times lower than SnO_2 films prepared by TMT and $SnCl_4$ precursors, respectively. Also, we can see from comparison of the CTO and the CTO/ZTO samples in Table 4 that integrating a ZTO buffer layer into a CdTe cell results in a J_{sc} loss of <0.1 mA/cm^2 due to its high optical bandgap and low absorption.

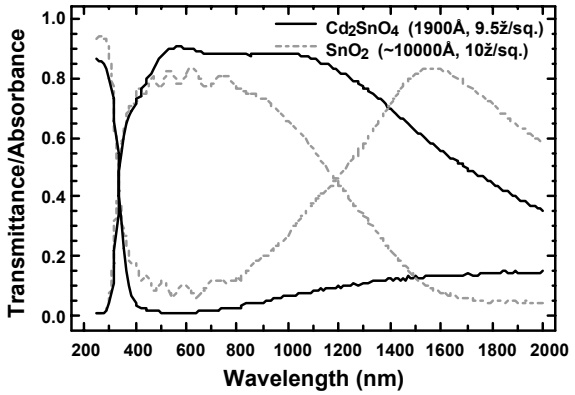


Figure 3. Transmittance and absorbance of a Cd_2SnO_4 and a SnO_2 film with a similar sheet resistivity of ~10 Ω/sq.

Table 4. The J_{sc} loss due to TCO absorption for four different TCO films.

TCO	R_s (Ω/sq)	J_{sc} loss due to TCO absorption
SnO_2 ($SnCl_4$)	8-10	2.8
SnO_2 (TMT)	7-8	1.3
Cd_2SnO_4	7-8	0.62
CTO/ZTO	7-8/~10^5-10^6	0.68

3.2.2 Reduced J_{sc} loss due to CdS absorption

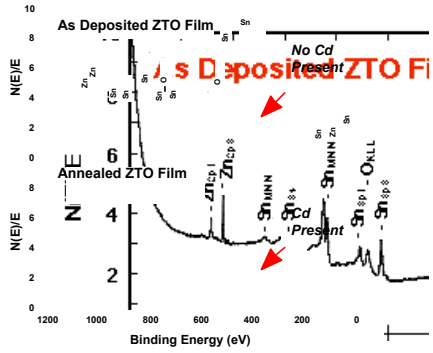
In conventional SnO_2/CdS/CdTe devices, improved blue spectral response can be achieved by reducing the CdS thickness. However, reducing CdS thickness can impact device V_{oc}, FF, and reproducibility. In the modified CTO/ZTO/CdS/CdTe devices, interdiffusion between the CdS and ZTO films can "consume" part of the CdS film during device fabrication. This interdiffusion can occur either at higher temperature (570°-650°C) in Ar or He, or at lower temperature (400°-430°C) in a $CdCl_2$ atmosphere.

(1) Interdiffusion at high temperature.

In this study, two test samples were prepared. A CdS film and a ZTO film were deposited on separate 7059 Corning glass substrates by CBD technique and rf magnetron sputtering, respectively. X-ray photoelectron spectroscopy (XPS) was used to measure the changes of film composition before and after these films were annealed face to face at 600°C.

Figure 4(a) shows XPS spectra surveys taken from the ZTO film both before and after annealing, and Figure 4(b) is a similar set of surveys from the CdS film. Figure 4(a) indicates an absence of Cd in the ZTO film before annealing, within the detection limits of XPS. However, after annealing, about 3-5 at.% Cd diffuses into the ZTO film from the CdS film. Similarly, as shown in Figure 4(b), we cannot detect any Zn in the CdS film before annealing, whereas we detect about 2-3 at.% Zn in the CdS film.

(a) ZTO film



(b) CdS film

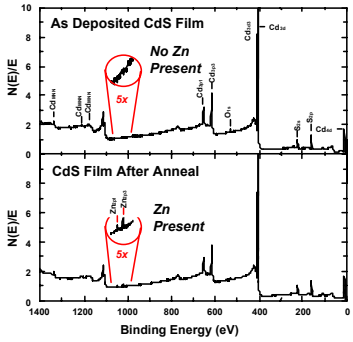


Figure 4. XPS survey spectra of the ZTO film (a) and the CdS film (b) before and after annealing.

(2) Interdiffusion at lower temperature in $CdCl_2$ atmosphere.

A test sample with ZTO/CdS/glass structure was prepared and annealed at 420°C for 15 minutes in a $CdCl_2$ atmosphere. Secondary-ion mass spectroscopy (SIMS) depth profiling was used to determine the extent of interdiffusion at the ZTO/CdS interface. SIMS data (Fig. 5) also indicate a considerable amount of Cd and Zn diffusion into the ZTO and the CdS films, respectively.

Therefore, we can control CdS "consumption" by optimizing CdTe deposition and $CdCl_2$ treatment process. In addition to XPS and SIMS techniques used in this study, two research groups have developed two non-destructive techniques: Angular Dependence of X-Ray Fluorescence (ADXRF) and Variable-Angle Spectroscopic Ellipsometry (VASE), to determine, quantitatively, the compositional depth profile and the extent of CdS "consumption" [24,25]. Thus far, we can conclude that CdS interdiffusion into both the ZTO and the CdTe reduces J_{sc} losses due to CdS absorption. Using this technique resulted in internal quantum efficiencies of >75% at 400 nm (Figure 6) and reduced J_{sc} loss due to CdS absorption to 1.0-1.3 mA/cm^2, while retaining both high V_{oc} and FF. This property may also be exploited in production by using thicker CdS films, thereby enhancing yield without reducing J_{sc}.

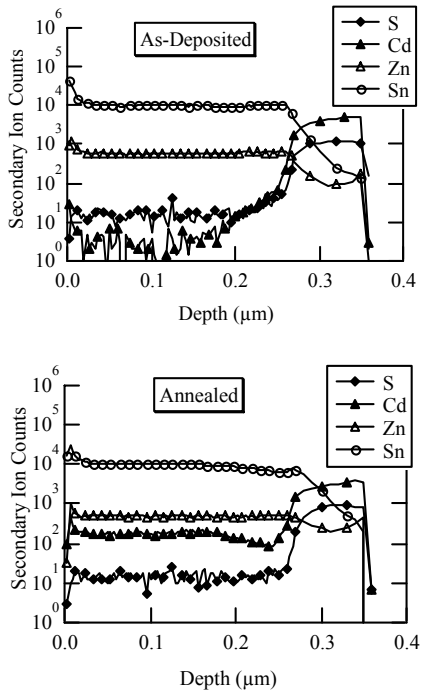


Figure 5. Interdiffusion of ZTO and CdS films at 420°C in a $CdCl_2$ atmosphere (SIMS data).

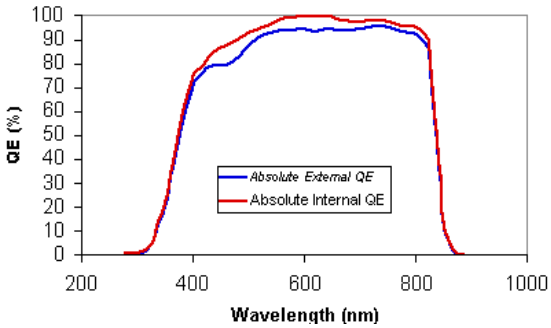


Figure 6. Absolute external and internal quantum efficiency of a CTO/ZTO/CdS/CdTe cell.

3.2.3 Reduced J_{sc} loss due to recombination in junction and CdTe regions

It is well known that the $CdCl_2$ treatment is a very important process for making high-efficiency CdTe cells. Performance and reproducibility of CdTe cells are significantly influenced by the $CdCl_2$ treatment, which is used by all CdTe module manufacturers. However, $CdCl_2$ over-treatment can result in adhesion-loss problems. Grain growth of the CdS film, which occurs during the $CdCl_2$ treatment, may introduce stress at the TCO/CdS interface, resulting in film blistering or peeling. The interdiffusion of the CdS and ZTO layers may relieve the stress at the

CdS/ZTO interface, thereby improving device adhesion. We have previously reported experimental results demonstrating that integrating the ZTO buffer layer into CdTe devices could significantly improve the adhesion after the $CdCl_2$ treatment [19]. The adhesion improvement not only improves the device reproducibility, but also provides greater latitude in optimizing the $CdCl_2$ treatment process. The optimally $CdCl_2$-treated CdTe cell has better quality of CdTe film and junction, which is confirmed by time-resolved photoluminescence (TRPL) measurements.

Figure 7 shows TRPL results of three cells with different $CdCl_2$ treatments. It can be seen that an optimally $CdCl_2$-treated device (W380-A) has the longest TRPL lifetime (2.2 ns), which is three times higher than the device (W380-D) with a normal $CdCl_2$ treatment, and more than 10 times higher than the device (W380-C) without $CdCl_2$ treatment. The CdTe cells with long TRPL lifetime have better junction properties and a well-passivated CdTe film. This is confirmed by measurements of saturated dark current density J_0 and diode quality factor A. The J_0 and A of the optimally $CdCl_2$-treated CdTe cells are in the range of 10^{-11} – 10^{-9} A/cm^2 and 1.6-2.0, respectively. In contrast, the J_0 and A of the conventional $CdCl_2$-treated cells are >10^{-9} A/cm^2 and >2, respectively. This is also confirmed by measurements of device quantum efficiency. We can see that in Figure 6, the optimally $CdCl_2$-treated CTO/ZTO/CdS/CdTe cell has excellent internal quantum efficiency in the long-wavelength region of 580-840 nm. Indeed, J_{sc} loss due to recombination in the junction and CdTe region was reduced to ~0.5 mA/cm^2.

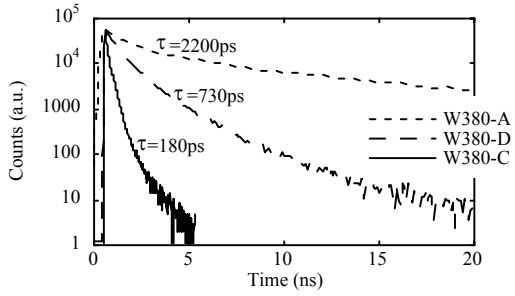


Figure 7. TRPL decay curves of three CdTe cells with different $CdCl_2$ treatment.

3.3 High-efficiency CdTe cells

A number of CTO/ZTO/CdS/CdTe cells with NREL-confirmed efficiencies of more than 15.8% have been fabricated (see Table 5). These results also indicate that the modified CTO/ZTO/CdS/CdTe device structure provides better reproducibility.

In Figure 8, we show a CTO/ZTO/CdS/CdTe polycrystalline thin-film solar cell with an NREL-confirmed total-area efficiency of 16.5% (V_{oc}=845.0 mV, J_{sc}=25.88 mA/cm^2, FF=75.51%, and area=1.032 cm^2). We believe that this is the highest efficiency ever reported for a CdTe-based solar cell.

Table 5. High-efficiency CTO/ZTO/CdS/CdTe cells.

Cell #	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)	Area (cm^2)
1	844.0	25.21	74.41	**15.9**	1.004
2	848.2	25.55	73.55	**15.9**	1.040
3	846.3	25.43	74.24	**16.0**	1.130
4	849.9	25.50	74.07	**16.1**	1.029
5	835.6	25.25	76.52	**16.1**	0.961
6	842.2	25.65	74.67	**16.1**	0.948
7	842.7	25.24	76.04	**16.2**	1.116
8	847.5	25.86	74.45	**16.4**	1.131
9	845.0	25.88	75.51	**16.5**	1.032

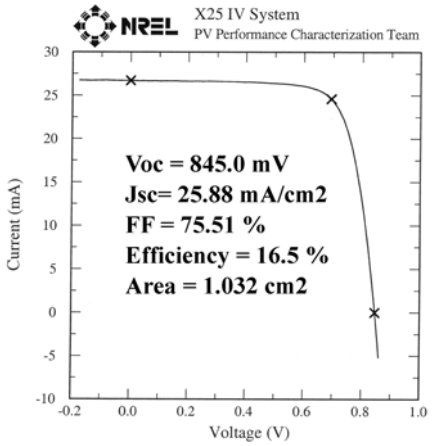


Figure 8. Current-voltage characteristics of a polycrystalline CTO/ZTO/CdS/CdTe thin-film solar cell.

3.4 Future work

The best photovoltaic parameters achieved in our work are V_{oc} = 858 mV (~58% of the CdTe bandgap E_g of ~1.48 eV for NREL CdTe film), J_{sc} = 25.9 mA/cm^2 (~87.7% of the theoretical J_{sc} of 29.5 mA/cm^2), and FF = 77.3%. In the short term, a conversion efficiency of 17% can be expected by optimizing the device J_{sc} to ~90% of theoretical and the FF to 78%-80%. To achieve higher-efficiency CdTe cells (18%-19%), research should focus on improving the ratio of V_{oc}/E_g to at least 60%. This could be achieved in two ways: (1) Improve the built-in potential by minimizing compensation and increasing doping of CdTe film; and (2) Improve the diode quality factor A by minimizing the recombination-center density.

4. CONCLUSIONS

The use of a modified CTO/ZTO/CdS/CdTe device structure can minimize some issues that are significant in conventional SnO_2/CdS/CdTe cells and can improve device performance and reproducibility. A CTO/ZTO/CdS/CdTe polycrystalline thin-film solar cell with an NREL-confirmed total-area efficiency of 16.5% has been achieved, which is the highest efficiency ever reported for CdS/CdTe solar cells.

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