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Towards ultra-thin CdTe solar cells using MOCVD

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ABSTRACT

A study was made on very thin CdTe absorber <1 μm layers to investigate limitations in CdTe collection efficiency. Metal organic chemical vapour deposition (MOCVD) was used to deposit cadmium sulfide (CdS), cadmium zinc sulfide ($Cd_{0.9}Zn_{0.1}S$) and cadmium telluride (CdTe). Improvements in photon collection in the blue, where the absorption length is shorter, have been achieved using a wider band gap $Cd_{0.9}Zn_{0.1}S$ ternary alloy to replace CdS as the window layer. Solar cell capacitance simulator (SCAPS) modelling software [M. Burgelman, P. Nollet, S. Degrave, Thin Solid Films, 361–362 (2000) 527–532] has been used to calculate device parameters as a function of the absorber layer thickness (controlled by *in situ* using laser reflectometry). One feature of the MOCVD grown devices is the apparent absence of pin-holes, demonstrated by growth of an ultra-thin absorber (200 nm) with conversion efficiency of nearly 4%.

1. Introduction

In order to reduce material usage and to address carrier recombination loss throughout the absorber layer, the CdTe absorber thickness has been decreased below the absorption limit of 1 μm. The absorber layer thickness for thin film CdTe solar cells is normally between 2 and 10 μm. Thicker absorber layers are generally used to avoid pinholes reaching through to the window layer, which may lead to shorting from the back contact. The CSER group previously [2] studied planar CdTe solar cell structures with extremely thin absorbers gaining insights into the relationship of the device to the materials characteristics. Comparison of TCO/CdS/CdTe devices showed an increasing tendency for shorting in the structures with thinner CdTe. However, it was concluded that with comprehensive cleaning of the substrates, very thin absorber devices without pinhole shorting could be achieved.

Not only does the reduction of the absorber layer offer an insight into the device physics and capability of the deposition technique, but can provide flexibility in device designs including; (i) its usage in tandem solar cells (with transparent back contacts (e.g. ZnTe) [3]; and (ii) as potential PV glazing devices given their increased transparency.

The use of a (ZnO) buffer layer [4] as an insulating layer between the transparent conducting layer (TCO) and the window layer, has resulted in device improvements, with the benefits of adding a physical barrier for any migrating dopants/impurities; and decreasing the probability of pinhole related problems as the absorber layer thickness is reduced. In very thin PV devices, where the photon absorption length can be considerably greater than the absorber layer thickness, the photo-generation of electron-hole pairs will be reduced. The use of a wider band-gap window layer, ($Cd_{0.9}Zn_{0.1}S$), has been investigated and the upcoming paper reports on its successful incorporation into thinner absorber devices with an absorber layer thickness of, or below, 1 μm.

The need to push cell absorber thickness toward the absolute absorption limit requires the use of a fully controllable growth process producing very high quality material. Until recently, the only CdTe deposition technologies proven for utilizing thin CdTe layers, less than 4 μm, were electrodeposition [5,6], or physical vapour deposition (PVD) [7] such as sputter deposition [8] and close-space sublimation (CSS) [9]. These techniques are still prone to pinhole and other non-uniformity defects often limiting the thickness requirement, rather than being caused by fundamental absorption. The MOCVD process is well suited for studying very thin absorber layers due to its ability to attain high quality material, and can be grown with excellent controllability over extended growth parameters.

Theoretical calculated carrier generation has been shown by Amin et al [10], to be at its highest in the vicinity of the CdS/CdTe junction, reducing by two orders of magnitude within the first 1 μm. This indicates the importance of the quality of the CdTe within the first 1 μm interfacing with the window layer near the depletion region, as most of the carriers are generated and collected in this region.

This paper will address device limitations and potential enhancements with very thin absorbers which includes;

(1) The lower photocurrent (J_L) due to reduced photon absorption,
(2) Enhanced collection of more highly absorbing blue photons by using a wider band gap window layer, increasing J_{sc}.

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(3) Investigating issues related to CdTe device uniformity and potential pinhole formation due to surface coverage.

These studies were carried out using MOCVD to grow very thin absorber layers within complete CdS/CdTe device structures. The *J–V* characteristics of these devices were compared with a simple model constructed using the SCAPS model in an attempt to explain observed devices behaviour.

2. Experimental

2.1. Growth of PV devices

CdTe based solar cell structures were grown by horizontal MOCVD at atmospheric pressure, using H_2 carrier gas, on indium tin oxide (ITO) coated glass substrates (supplied by delta technologies). Full device growth comprised of;

i. Deposition of the window layer: 240 nm of CdS or (CdZnS at 360 °C) at 315 °C on ITO/glass substrates, using dimethylcadmium (DMCd) and ditertiarybutylsulphide (DtBS) (and diethylzinc (DEZn) for CdZnS) as the organo-metallic (OM) precursors.
ii. Deposition of the absorber layer: CdTe at 390 °C using dimethylcadmium (DMCd), and diisopropyltelluride (DiPTe) which is doped *in situ* with tris-dimethylaminoarsine (tDMAAs) yielding an arsenic (As) doping concentration of 2×10^{18} atoms cm^{-3} in the bulk CdTe layer.
iii. Selection of the back contact process:
Forming a good ohmic contact with back contact due to the very large work function (Φm) of CdTe has long been a challenge in the PV community. As no common metals have an adequate work function, gold, as in CSER group's case, is usually chosen in laboratory devices owing to its high work function. Additional difficulty is encountered when planning to etch such thin absorber layers with a standard bromine/methanol etch, where it is inherently difficult to control the end absorber thickness and uniformity. Thus there exists a need to eliminate wet etching, if not all wet processing steps, during full PV device growth.
Currently two main approaches are investigated to decrease the back barrier height (1) to increasingly dope a thin layer of absorber near the back contact effectively creating a p^+ layer enabling the majority carriers to tunnel through the Schottky barrier (and lower the surface carrier recombination); and/or (2) reduce the valence band offset at the back contact, by depositing a p-type ZnTe [1] intermediate layer, so that the barrier is effectively reduced.

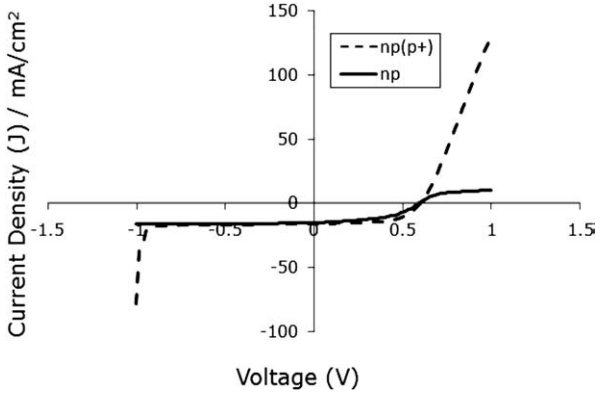

Fig. 1. Light *J–V* curves of CdS(240 nm)/CdTe (2 μm) showing improved back contact response after the deposition of the highly doped back contact layer affording a npp^+ type structure. (npp^+ (Rs=2.8 Ω cm^2), (np Rs=13.3 Ω cm^2).

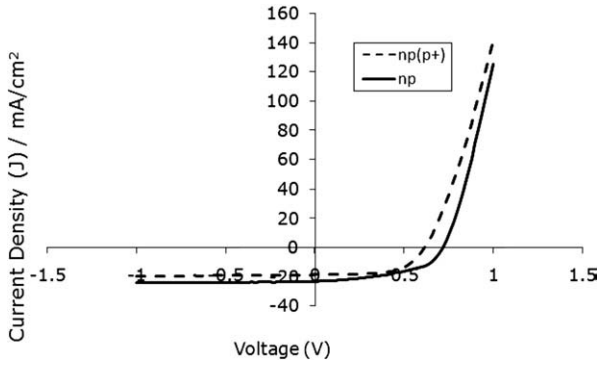

Fig. 2. Light *J–V* curves of thinner absorber (1 μm) device with and without the highly doped back contact layer. Showing little or no benefit of the npp^+ back contact layer for thinner absorber devices. (npp^+ (Rs=2.1 Ω cm^2), (np Rs=2.2 Ω cm^2).

Although CdTe is known to be a self-compensating material, being difficult to dope at high active acceptor concentrations, the authors have previously proposed [11] to simplify the back contact design by heavily doping the last part of the CdTe absorber layer. The approach uses the same dopant as in the absorber itself, to create an npp^+ type structure where directly after the deposition of the CdTe:As absorber layer, a highly As-doped CdTe layer "back contact layer" was deposited at the same substrate temperature of 390 °C,

iv. The entire structure was then subjected to an *in situ* $CdCl_2$ treatment (using DMCd and tertiarybutylchloride (tBuCl)) to passivate grain boundaries, effectively growing a $CdCl_2$ layer on top of the CdTe absorber, followed by an anneal at or over 400 °C for 10 min.

Growth rates were monitored, *in situ*, using a triple wavelength laser interferometer supplied by ORS Ltd. All precursor (provided by SAFC Hitech) concentrations were measured using an Epison gas concentration monitor. Full experimental procedure has been described elsewhere [12]. The group has previously reported [11] an all-MOCVD grown CdS/CdTe PV cell, able to grow all required layers in one chamber in an all dry process with no wet chemical etch required.

2.2. J–V and C–V measurements

The *J–V* measurements were carried out using a class-A Xenon lamp (450 W). The light power density of 100 mW cm^{-2} over a 2.5 cm^2 area was measured using a broadband thermopile power meter and regularly adjusted using a calibrated mono-FZ-Si reference cell from ISE/S Brachmann. In addition, the calibration was cross-correlated with a CdTe reference cell from NREL with known *J–V* parameters

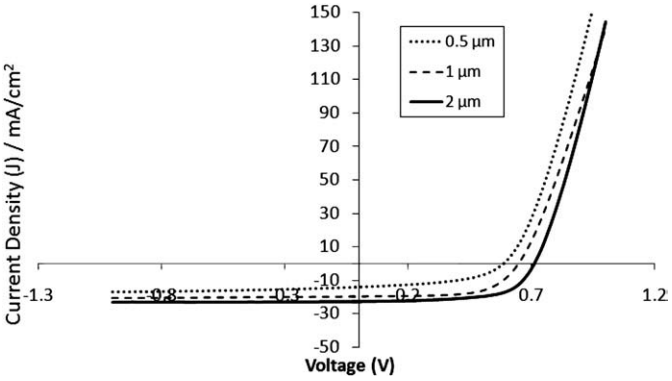

Fig. 3. Light *J–V* curves (under 100 mW/cm^2 xenon lamp illumination) for i) 0.5 μm, ii) 1 μm and iii) 2 μm absorber thicknesses.

Table 1
Shunt and series resistance values for a) standard (2 μm), b) thin (1 μm), and c) ultra thin (500 nm) absorbers

Absorber thickness (nm)	Series resitance Ω·cm^2	Shunt resistance Ω·cm^2
2000	1.9	2688
1000	2.3	1062
500	2.0	315

measured under AM1.5, where its short-circuit current density (J_{sc}), directly related to the photon absorption, was taken as a reference point to the AM1.5 spectrum. The device temperature during measurement was 25 °C.

Dark capacitance–voltage (*C–V*) measurements were taken from −1.2 to 1.2 V, at a frequency of 150 kHz and room temperature. Using this frequency avoids contributions from deep states, which can be ignored at frequencies higher than 120 kHz. The samples investigated at absorber thicknesses from 2 μm, down to 500 nm. Cells are biased from −1.40 V to 0.6 V as this represents transition to a regime dominated by capacitance at the back-contacts [13].

3. Results and discussion

3.1. J–V curves

The back contact layer has been optimized for the baseline process having a back contact layer of 250 nm. Since this thickness will represent a larger proportion of thinner devices it has been decided to reduce the thickness of the back contact layer down to 100 nm.

Growths were carried out of devices which (i) had a npp$^+$ type structure (with back contact layer), and (ii) had a standard np structure (no back contact layer) to measure the effect of the npp$^+$ type structure on thinner films. Fig. 1 shows the effect such a structure has on the baseline (2 μm) thick devices, the np device shows a large rollover behaviour associated with a poor back contact, whereas the npp$^+$ device shows a linear *J–V* at high forward bias, suggesting an improved back contact region for baseline (2 μm) thicknesses.

This improvement appears not to be necessary when the absorber layer is reduced. Fig. 2 shows that no rollover is seen for the structure without the p$^+$ layer and only a small decrease in series resistance is seen by the addition of a p$^+$ layer near the back contact. This suggests that the thinner layers have a higher effective doping concentration.

J–V measurements of thin and ultra thin absorbers can be used to investigate voltage dependent collection in devices. From the work of McMahon and Fahrenbruch [14], it is suggested that the reduction of the absorber layer thickness increases the voltage dependent collection at high forward bias. Fig. 3 shows the light *J–V* curves for different absorber layer devices. The open circuit voltage (V_{oc}) is seen to

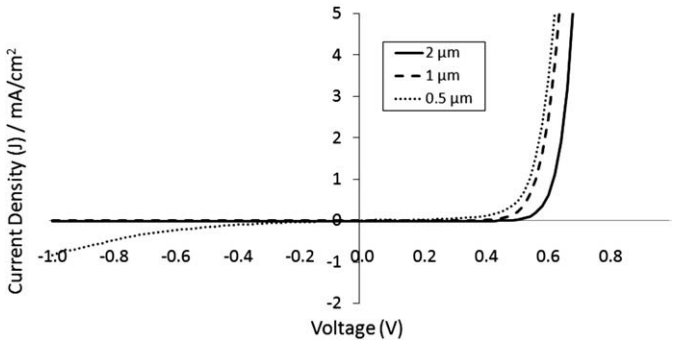

Fig. 4. Dark *J–V* curves of cells with different absorber thickness showing increased recombination for the thinner cells.

Table 2
Parameters used in baseline modelling

Layer	CdTe	CdS
Thickness (μm)	2	0.24
Bandgap (eV)	1.5	2.4
Electron affinity (eV)	3.9	4
Dielectric permittivity (relative)	9.4	10
CB effective density of states (cm^{-3})	8.00×10^{17}	2.20×10^{18}
VB effective density of states (cm^{-3})	1.80×10^{19}	1.80×10^{19}
Electron thermal velocity (cm/s)	1.00×10^{7}	1.00×10^{7}
Hole thermal velocity (cm/s)	1.00×10^{7}	1.00×10^{7}
Electron mobility (cm^2/Vs)	1.05×10^{3}	1.00×10^{2}
Hole mobility (cm^2/Vs)	4.00×10^{1}	2.50×10^{1}
Shallow donor density (cm^{-3})	0	1.10×10^{18}
Shallow acceptor density (cm^{-3})	5.00×10^{14}	0

increase with absorber thickness, due to an increase in the photogenerated current (J_L) as the absorption volume is increased. None of the grown devices display rollover features in light *J–V*, indicating good back contact formation. Evolution of series resistances with absorber thickness (Table 1.), shows minimal change in series resistance, demonstrating that the back contact barrier is unaffected by the close proximity of the pn junction, even down to 200 nm absorber thickness. A large decrease in shunt resistance (approximated from *J–V* curves) with decreasing absorber thickness is observed. Such increase in shunting is possibly caused by leakage currents around the edges of the cell, as the layers are so thin, but it could also be due to extended lattice defects (grain boundaries, dislocations, etc …) in the depletion region of the device.

Dark *J–V* (Fig. 4) have also been measured and show recombination effects are increased for the 500 nm thick CdTe layer in the reverse bias region. The dark *J–V* curves shows that when the absorber

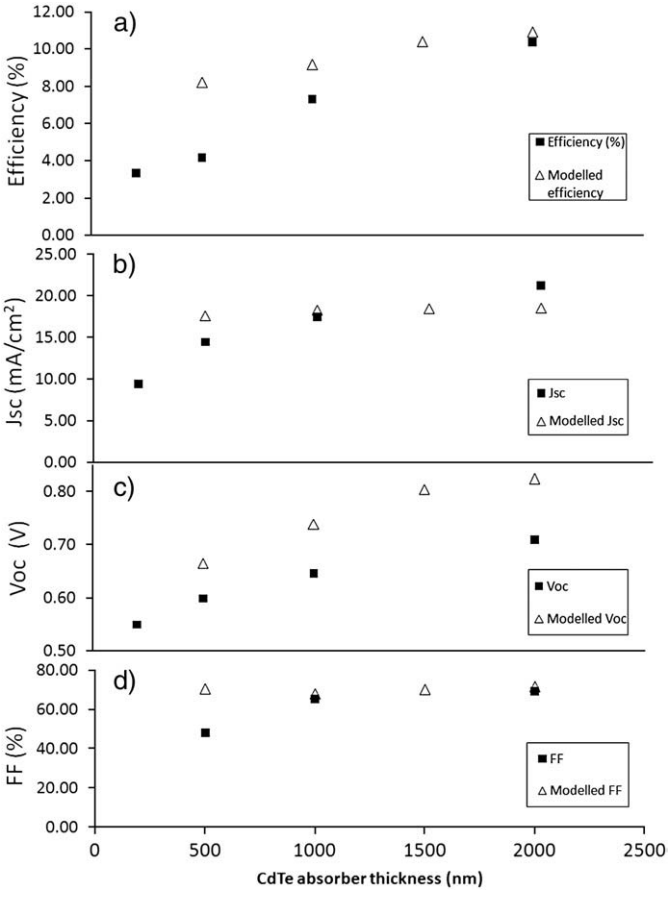

Fig. 5. Measured and modelled device parameters as a function of absorber thickness.

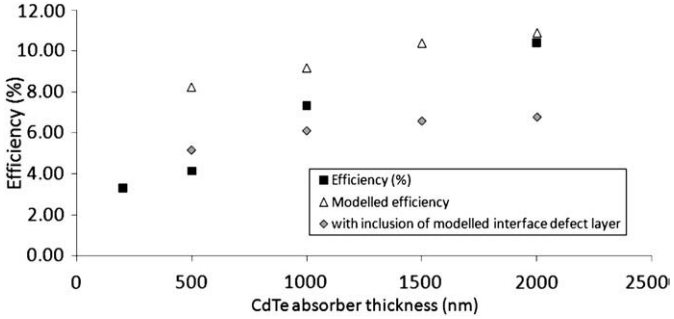

Fig. 6. Efficiency vs. absorber thickness for a (i) measured, (ii) modelled, and (iii) introduction of a acceptor defect at the CdS/CdTe interface.

thickness is reduced below the CdTe absorption thickness (~1 μm), recombination effects increase and dominate device characteristics. The recombination current is limited by diffusion across the field free region, which should be smaller for thinner cells affording less recombination current at the back contact. Such effect consequently results in a decrease of series resistance (Rs), which could explain the inherently lower series resistance of the thinner cells. It may also be, and the reason, why no appreciable benefit is gained with the inclusion of the back contact layer.

3.2. Forming a model of the CdS/CdTe junction

The SCAPS modelling program developed by Burgelman et al. [15,16] can be used for modelling, in 1D, basic TCO/CdS/CdTe structures at normal working conditions.

To simplify the simulation of the MOCVD devices, the highly doped CdTe (p^+ back contact layer) has been omitted and a series resistance value of 2 Ω·cm^2 was assumed. Data from *C–V* [12] of baseline MOCVD devices were also entered into the model with acceptor concentration of 5×10^{14} cm^{-3} and minority carrier diffusion lifetime of 1 μs (Table 2.). The need for large number of input parameters (50–100) makes convenient modelling difficult. With the need for a consistent set of parameters, with parameters depending on deposition technique and even differing with each sample, suggest, only limited modelling can be achieved. However, comparing modelled results with real experimental data, however basic, can be useful. The authors took the approach [17] of selecting a baseline parameter set, and only one parameter was varied at a time (thickness in this case).

3.3. Measured and modelled device results

A three layered model (ITO 120–160 nm, CdS 240 nm, and CdTe 2 μm) agreed well with calculated conversion efficiencies of baseline MOCVD cells, decreasing the absorber thickness from 2 μm down to 200 nm (Fig. 5a). One can observe a decrease in efficiency as a result of decreased absorption volume, decreasing more rapidly as the absorber thickness is decreased below 1 μm.

Table 3
Device results of a thin absorber (1 μm) with a) a CdS or b) a high band gap $Cd_{0.9}Zn_{0.1}S$ layer

Window layer (240 nm)	Efficiency (%)	J_{sc} (mA/cm^2)	FF (%)	V_{oc} (mV)
CdS	7.31	17.4	65.1	640
$Cd_{0.9}Zn_{0.1}S$	11.42	20.6	74.1	750

Overall, the measured device efficiency decreases at a faster rate than predicted by the basic model. Analysis of the device parameters showed that J_{sc} (Fig. 5b) and V_{oc} (despite being overestimated by the model, Fig. 5c) agreed well at thicker absorber thicknesses but decreased more rapidly at <1 μm. The smaller values of V_{oc} of thinner absorber layer devices suggests the saturation current increases dramatically, as the J_L is expected to decrease with decreasing absorber thickness. The Fill factor (FF), Fig. 5d) contrarily to the model, decreased at thicknesses below 1 μm, demonstrating a larger increase in shunts, as the shunt resistance is decreased.

To closer represent the large discrepancy in V_{oc} values, an acceptor defect layer (10^{14} cm^{-2}) at the CdS/CdTe interface was added, and produced improved agreement with measured devices with thicknesses below the absorption limit (Fig. 6).

3.4. C–V measurements

The *C–V* curve (Fig. 7) shows a large increase in the capacitance with decreasing absorber thickness, suggesting increased carrier density in the measurement region. In reverse bias, for bias voltage (V_b) lower than −0.2 V, the capacitance in all cases saturates, where the samples are fully depleted of majority carriers. The thickest sample (i.e. 2 μm CdTe) shows a noticeably weaker increase of capacitance with increasing voltage as compared to other samples despite all having the same arsenic doping conditions, which indicates a transition to a regime dominated by capacitance at the back-contacts [13].

3.5. Wider band gap window layer

It is inherent that when the thickness of the absorber is decreased (less absorption volume), a lower J_{sc} will be achieved. It is vital to understand and gain insights into device physics of thin CdTe devices; therefore there exists a need to eliminate photo-generated losses. These losses are due to a) absorption volume decrease or, b) materials quality limitations.

The $Cd_{0.9}Zn_{0.1}S$ (e.g. ~2.7 eV) ternary alloy can be used to increase the window layer band gap and to reduce the usual blue absorption faced using CdS window layers. Table 3 shows the results of thin absorber (1 μm) devices, with and without the wider band gap

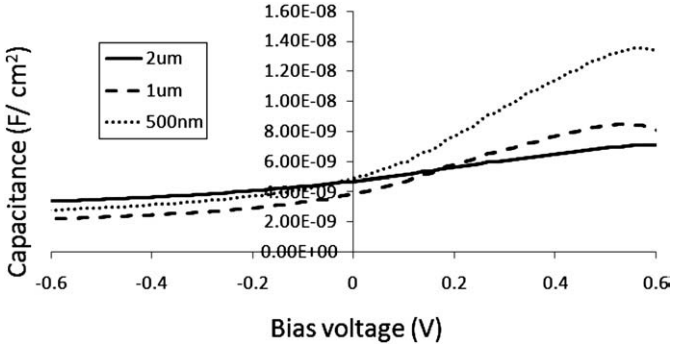

Fig. 7. Dark *C–V* curve of CdS/CdTe junction devices with differing CdTe absorber thicknesses.

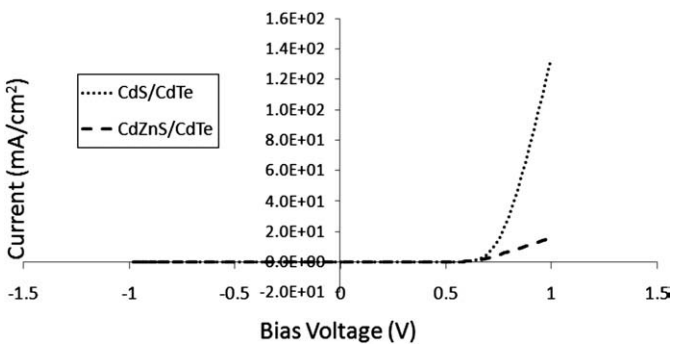

Fig. 8. Dark *J–V* curves for standard (i) CdS/CdTe junction and (ii) an extended band gap CdZnS/CdTe junction.

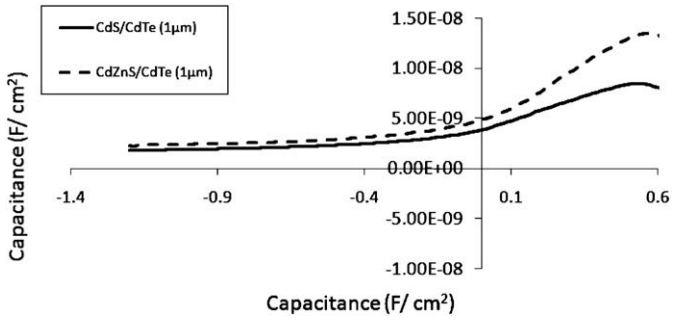

Fig. 9. CV curves of ultra thin cells with (i) standard CdS/CdTe junction and (ii) CdZnS/CdTe junction.

window layer. All device parameters are improved, with conversion efficiency increasing by 50%. The large increase in V_{oc} would suggest a decrease in the interface defect density as the V_{oc} is higher than would be expected simply from the increase in the blue photon capture. Dark *J–V* curve response measurements (Fig. 8) show a poor forward bias characteristic suggesting increased series resistance for CdZnS/CdTe junction compared to CdS/CdTe.

The observed increase in J_{sc} can be attributed to a shift in the optical band of the window layer form 2.4 eV to 2.7 eV, improving the blue-region response, and shifting the absorption edge from 500 nm to 400 nm for the wider band gap ternary alloy window layer devices. The absorption edge is effectively shifted by 100 nm towards the high energy region of the AM1.5 spectrum by only 10% Zn inclusion in the CdS. Details of the window layer characteristics are part of an ongoing study and will be published elsewhere.

C–V response curves of CdTe devices with the wider band gap layer ($Cd_{(0.9)}Zn_{(0.1)}S$) (Fig. 9) demonstrate an increased capacitance of the wider band gap window layer device ($Cd_{(0.9)}Zn_{(0.1)}S$/CdTe) cell, symptomatic of a superior pn junction over the standard CdS/CdTe junction.

4. Conclusions

The large decrease in device parameters with decreasing absorber thickness (below 1 μm) suggests the cells are limited not only by optical issues but also interface and possibly back contact proximity. By the basic addition of an acceptor defect between the CdS and CdTe, the agreement of the basic model with measured results improved, particularly when ultra thin absorbers were employed, possibly signifying an increase in the interface defect density with thinner absorbers. Further investigation of the effect of the back contact will need to be carried out to establish any contribution with the pn junction of ultra thin layers. This could be facilitated using bifacial analysis, where the light is shone from both sides, separating the effects of the back contact and the pn junction.

C–V analysis confirms the presence of a larger increased built-in field with thinner CdTe cells, having a larger capacitance value at forward bias. This should in theory be beneficial to the device, but could also be detrimental to the cell since the probability of impurity migration is also increased, thus a long term stability study of thinner cells should be investigated.

Basic modelling has been employed and gives some basic insights into the device. Further detailed analysis on MOCVD grown CdTe needs to be done in order to obtain the 50–100 parameters needed for accurate device modelling. Using limited parameter set, the decrease of the absorber thickness does imply an increasing contribution from the interface.

Unexpectedly the doping of the devices seems to be improved affording an improved back contact, making possible the deposition of the back contact (gold) without any prior surface treatment avoiding further complicating the production process.

Work on a wider band gap window layer (CdZnS) has shown that it is possible to increase the generated photocurrent, currently lost using thinner absorber layers as a results of reduced absorber volume, by extending the optical band gap via the alloying of Zn in CdS. Device efficiencies over 10% with 1 μm thick absorber layers have been shown to be possible using MOCVD, due to the high quality of material produced.

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