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The Effect of High-Resistance SnO_2 on CdS/CdTe Device Performance

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Abstract: In this paper, we have studied the effect of high-resistance SnO_2 buffer layers, deposited by low-pressure chemical-vapor deposition, on CdS/CdTe device performance. Our results indicate that when CdS/CdTe devices have a very thin layer of CdS or no CdS at all, the i- SnO_2 buffer layer helps to increase device efficiency. When the CdS layer is thicker than 600Å, the device performance is dominated by CdS thickness, not the i- SnO_2 layer. If a very thin CdS layer is to be used to enhance device performance, we conclude that a better SnO_2 buffer layer is needed.

INTRODUCTION

High-resistance transparent (HRT) layers have been used as a buffer layer between the transparent conducting oxide (TCO) and the CdS layer to help maintain CdS/CdTe device performance when thin CdS films are used or there is a high density of pinholes. Several HRT materials have been used as a buffer layer, including undoped SnO_2 , TiO_2 , and Golden Photon's (GPI) proprietary HRT layer.

In our group, a sputter-deposited intrinsic SnO_2 (i- SnO_2) was used as a buffer layer in baseline process. Previous experiments incorporating this layer have yielded mixed results. In some instances, the buffer layer helped to maintain high device open-circuit voltages (V_{oc}) and fill factors (FF), thereby improving reproducibility. However, the device efficiency (η) did not always improve with the addition of the buffer layer. We found that, in part, this could be explained by the thermal instability of the buffer layer, which was deposited at room temperature.¹

Recently, we installed a low-pressure chemical-vapor deposition (LPCVD) system for TCO research, which has yielded better quality SnO_2 films. With this ability, we investigated the effect of high resistance SnO_2 on CdS/CdTe device performance and its interaction with CdS layer thickness.

EXPERIMENTAL

In this study, both high resistance i- SnO_2 and conductive SnO_2 ($\text{SnO}_2\text{:F}$) films were deposited by LPCVD with growth temperatures of 500°C. The precursors for tin, oxygen, and fluorine dopant were tetramethyltin (TMT), ultrahigh purity oxygen gas, and CBrF_3 , respectively. The resistivities of the $\text{SnO}_2\text{:F}$ and i- SnO_2 films were

approximately $5 \times 10^{-4} \Omega\text{-cm}$ and $1 \Omega\text{-cm}$, respectively. A bilayer structure with an i-SnO₂ buffer layer on the top of the SnO₂:F was used as a front electrode for CdS/CdTe device fabrication. The total bilayer thickness was kept around 6000 Å, with the i-SnO₂ thickness varied from zero to 2000 Å. The sheet resistance of the bilayer-SnO₂ film used in this study ranged from $\sim 8 \Omega/\text{sq}$ ($\sim 6000 \text{ Å}$ SnO₂:F and zero Å of i-SnO₂) to $\sim 12 \Omega/\text{sq}$ ($\sim 4000 \text{ Å}$ SnO₂:F and $\sim 2000 \text{ Å}$ of i-SnO₂). Later in this paper, we will see that the sheet resistance of bilayer TCO does not affect the device performance under our experiment of conditions.

The CdS films were then deposited by chemical-bath deposition (CBD) and CdTe films were deposited by close-spaced sublimation (CSS). A source temperature of 660°C and a substrate temperature of 620°C were used in the CSS deposition. A vapor CdCl₂ treatment was chosen as a post-deposition treatment. The source-plate temperature varied between 395°-405°C, and the substrate temperature varied between 390°-400°C. After the vapor CdCl₂ treatment, all the samples were finished with a nitric-phosphoric acid etch and a Cu doped HgTe/graphite back-contact. Finally, the device was isolated by physically removing the material around the back-contact area. The width of the device was carefully controlled to about 3 mm to limit the loss caused by the TCO sheet resistance. Moreover, by keeping the constant device width, we can assess the effect of sheet resistance on the device performance.

EXPERIMENTAL RESULTS

The Temperature Stability of SnO₂ Film

We have compared the temperature stability of the three types of SnO₂ films that were deposited by LPCVD using a TMT precursor, room-temperature (RT) sputtering, and high-temperature CVD using a SnCl₄ precursor. All the samples were annealed at 500°C for 15 minutes in a H₂ ambient. The TMT-formed SnO₂ did not show any reduction of either optical or electronic properties. The SnCl₄-formed SnO₂ film had a low optical transmission as formed and did not show a reduction after annealing. However its resistance increased by about one order of magnitude after annealing. The sputtered-formed SnO₂ film showed a dramatic reduction in quality. Fig. 1 shows that after annealing, the absorption of sputtered SnO₂ increased from an average of 10% to over 30%, and the absorption of LPCVD-formed SnO₂ did not change at all. The X-ray results indicate that the optical reductions may be due to free tin resulting from the reduction of the SnO₂.¹ Because after annealing, a tin diffraction pattern was seen in the sputtered SnO₂ sample, but not in LPCVD-formed SnO₂ sample. We conclude that the SnO₂ film made by the high-temperature LPCVD process and TMT precursor is very stable thermally.

The Effect of Morphology of SnO₂ Film

For the front-wall structure CdS/CdTe device, the mechanical properties of the front TCO electrode could affect the CdS and CdTe layers that grow on it.² The film crystallite orientation was studied using X-ray diffraction (XRD). Fig. 2 is a plot of two XRD patterns obtained from SnO₂:F (1.25 μm thick) and i-SnO₂ (1.11 μm thick) films. The SnO₂:F film shows a strong (200) orientation, and the i-SnO₂ film shows a random orientation compared to the doped one. Because the two samples have a similar thickness, we believe the difference in crystallite orientation is due to the doping of the films not the film thickness.³ For the bilayer SnO₂ structure, the XRD pattern is a composite of both the doped and undoped diffraction patterns. The atomic force microscopy image showed that the surface roughness (R_{rms}) of both the i-SnO₂ and SnO₂:F films depended strongly on the growth temperature and the film thickness. With a growth temperature of 500°C and a film thickness of 6000Å, the surface roughness of SnO₂ films was about 60 nm.

The preliminary device results indicated that adding a i-SnO₂ layer, which has different crystallite orientation than SnO₂:F, did not affect the adhesion of CdS/CdTe on the SnO₂ layer. The adhesion loss of CdS/CdTe films from the TCO substrate mainly depends on the CdS thickness and the strength of vapor CdCl₂ treatment.

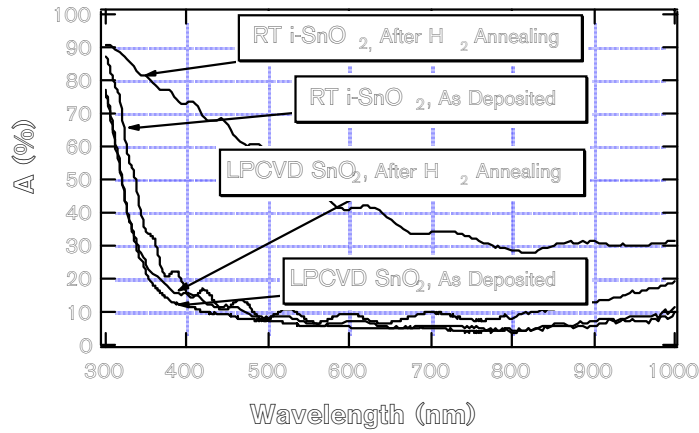


FIGURE 1. The annealing effect on the absorption of SnO₂ film made by LPCVD and by RT sputtering. Both films were annealed at 500°C in a H₂ ambient for 15 minutes. The solid lines are for as-deposited samples and the dotted line are for samples after annealing.

The Effect of i-SnO₂ Film Thickness

Three groups of samples were studied to understand the relationship between the i-SnO₂ ($t_{\text{i-SnO}_2}$) and the CdS/CdTe device performance. Each group of samples had a range of CdS thicknesses (300Å, 600Å, and 900Å), and a range of i-SnO₂ thicknesses (0Å, 600Å, 1200Å, and 1800Å). The device parameters were then studied as a

function of $t_{\text{i-SnO}_2}$. Fig. 3 shows that for the first group of samples ($t_{\text{CdS}} = 300 \text{ \AA}$), V_{oc} depended on the $t_{\text{i-SnO}_2}$ thickness. When $t_{\text{i-SnO}_2}$ increased from zero to 1800 \AA , the V_{oc} increased from $\sim 500 \text{ mV}$ to over 700 mV . For the second and third groups of devices, which have moderate CdS thicknesses ($t_{\text{CdS}} = 600 \text{ \AA}$ and 900 \AA), the V_{oc} was almost unchanged over the range of $t_{\text{i-SnO}_2}$.

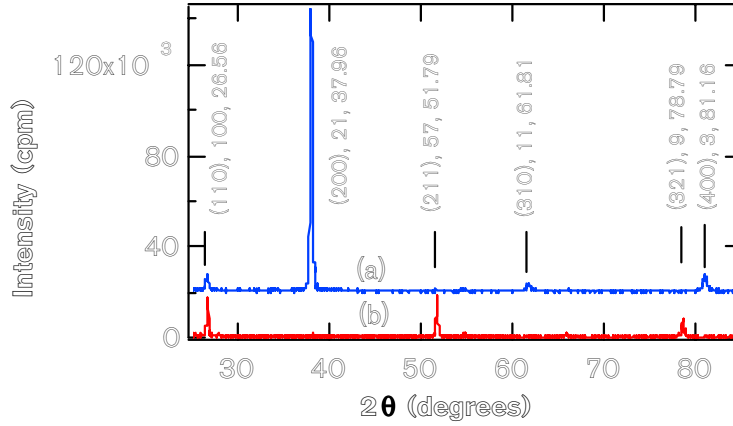


FIGURE 2. The X-ray diffraction patterns of fluorine-doped and undoped SnO_2 . (a) $\text{SnO}_2\text{:F}$, (b) intrinsic SnO_2 .

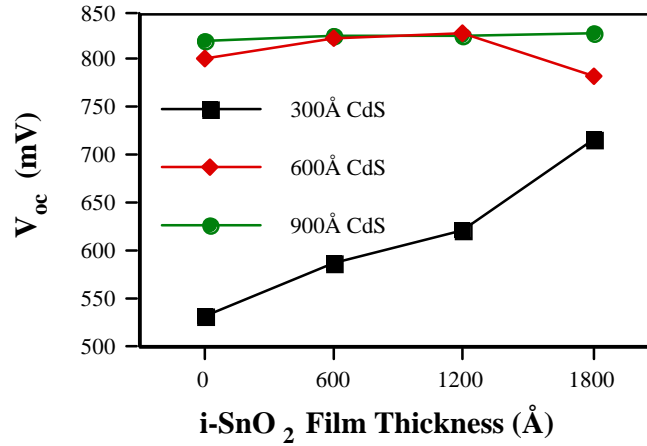


FIGURE 3. The relationship of V_{oc} to i-SnO_2 buffer-layer thickness for those devices made on different CdS and i-SnO_2 films thickness.

We did not observe changes in the short-circuit current density (J_{sc}) as t_{i-SnO_2} was varied. This is likely because the transmission of the i-SnO₂ film is as good as the SnO₂:F film. The device series resistance (R_{s0}) and shunt resistance (R_{sh0}) were plotted as a function of bilayer sheet resistivity (R_{sq}). We did not observe a consistent relationship between R_{sq} and R_{s0} or R_{sh0} . Similarly, no clear trend was observed between the FF and t_{i-SnO_2} . As a result, the η exhibits a pattern similar to that observed in figure 3 for V_{oc} . The devices made with a very thin CdS layer ($t_{CdS} = 300\text{\AA}$) gained over 30% in η as t_{i-SnO_2} increased from zero to 1800 \AA .

The Effect of Buffer Layer Resistance

GPI's proprietary HRT layer has a resistivity in the $10^4 \Omega\text{-cm}$ range, about four orders of magnitude higher than for the i-SnO₂ buffer layer made by LPCVD using a TMT precursor. To study the effect of buffer layer resistance, both buffer-layer thickness (t) and resistivity (ρ) must be considered. Several SnO₂ samples with a similar thickness to GPI's HRT were made. The V_{oc} , obtained from both types of samples was plotted as a function of $\rho \times t$. Fig. 4 shows that when $\rho \times t$ is less than $10^4 \Omega\text{-cm}^2$, V_{oc} varied from 300 mV (with no CdS film) to 800 mV (with a CdS film thickness of over 300 \AA). When $\rho \times t$ is greater than $10^4 \Omega\text{-cm}^2$, like GPI's HRT film, the V_{oc} was not significantly affected by the CdS thickness. Whether there was a 900- \AA -thick CdS film or no CdS at all, the V_{oc} values were about 800 mV (three data points are present in this range in figure 4). Because there was composition difference in between LPCVD-formed i-SnO₂ and GPI's high resistance SnO₂, we do not know yet whether the GPI buffer-layer works mainly because of its high resistance, or its chemical composition, or both. Further study in this area is needed.

SUMMARY

LPCVD-deposited SnO₂ films are very stable under a high-temperature condition. The optical and electronic properties of i-SnO₂ remains the same after a thermal annealing in H₂ ambient. The i-SnO₂ film has a different crystal orientation than the SnO₂:F film. However, we have not observed that the difference in crystal orientation affects the adhesion of the CdS film to the TCO substrate.

In varying the i-SnO₂ thickness from zero to 1800 \AA and the CdS thickness from zero to 900 \AA , we observe the following: for thin CdS films, the CdS/CdTe device performance (mainly V_{oc}) depends on the i-SnO₂ buffer-layer thickness. About a 30% gain in device efficiency can be obtained for a 300 \AA CdS by increasing the i-SnO₂ layer thickness from 0 to 1800 \AA . For moderate and thick CdS films, the CdS/CdTe device parameters were dominated by the CdS thickness and were not sensitive to the i-SnO₂ thickness.

Compared to GPI's HRT buffer layer, the LPCVD formed i-SnO₂ film has less of an effect on the CdS/CdTe device performance. Differences in buffer-layer resistivity and surface properties may contribute to the results. We are planning further study in this area.

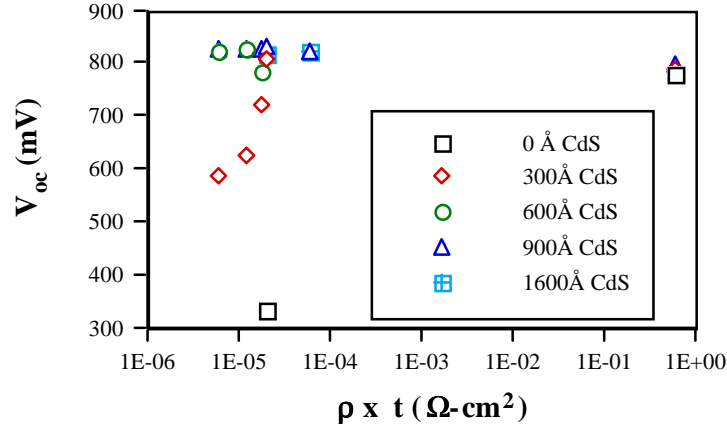


FIGURE 4. V_{oc} as a function of the product of resistance and thickness of high-resistance SnO₂ film.

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