Reach-through band bending in semiconductor thin films

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We describe a phenomenon of reach-through band bending in thin film semiconductors. It occurs through generation of defects that change the semiconductor work function. This translates the effect of the metal presence through the semiconductor film and induces a Schottky barrier in another semiconductor tangent to the film on the opposite side (reach-through band bending). We have found experimental evidence of this effect in CdTe photovoltaics. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1803950]

The phenomenon of Schottky barrier formation is well known from standard junction theory. Here we introduce a scenario of junction formation for semiconductor thin films where the Schottky barrier is absent or strongly suppressed. The underlying idea is that in a thin film semiconductor the Fermi level (F) can be shifted by generating a limited number of defects. Such a scenario becomes impossible for a thick semiconductor where F is fixed by the bulk.

We consider a three-component system of a thin n-type semiconductor film sandwiched between a metal and p-type semiconductor. Both system interfaces can have interfacial states. In our experimental verification this is represented by an n-type CdS film between a conductive electrode and p-type CdTe, which combination has important photovoltaic applications.[1] Its band diagram is shown in Fig. 1 for a particular case where the Fermi energies F_F and F_B in the film and bulk semiconductor components are close, while being significantly different from that of the metal (F_M). We assume that the screening length in the n-type semiconductor forming the film is considerably shorter than the film thickness, $L \ll l$. For such a system, the standard junction theory predicts a weak p- n junction between bulk and thin film semiconductors and a strong Schottky barrier between the metal and the film [Fig. 1(b)].

A conceivable effect of lowering F_F shown next in Fig. 1(c) is due to acceptor defect generation. As a result, the film becomes depleted and strongly increases its screening length, $L \gg 1$. The metal and bulk semiconductor then interact across the film similar to metal-insulator-semiconductor (MIS) structures, and align their Fermi levels, $F_B = F_M$. In particular, the band bending appears at the film interface opposite to the metal as though the latter was in direct contact with the bulk semiconductor. We call this phenomenon a reach-through band bending. When strong, it results in an inverse layer in the bulk semiconductor.

Phenomenologically, the film depletion corresponds to a potential barrier in the band diagram. The barrier is needed to separate the conduction band from the Fermi level and thus to self-consistently maintain the film insulating properties [as schematically shown in Fig. 1(c)]. Such a barrier is achieved by shifting up the entire thin-film energy spectrum in the process of the aligning of its lowered Fermi level with F_M.

As usual, the barrier in the electric potential corresponds to a certain electric charge distribution related to the defect and interfacial state parameters. In turns, the latter determine the barrier shape and height. As a conceivable example, we note that lowering F_F empties interfacial states thus making interfaces charged positively. This results in the dipole layer type of charge distribution shown in Fig. 1(c). The CdS interior region can pick some electric charge too, which depends on the material density of states and will not be further discussed here.

As a numerical example related to the data below, we assume a typical interfacial state density $\sigma \sim 10^{11}$ 10^{12} cm^{-2} and film thickness $l \sim 10^{-5}$ cm. This results in the barrier height $V_B \sim (4\pi/\epsilon)\sigma q^2 l \sim 0.1-1$ eV, where q is the electron charge and ϵ is the dielectric constant.

Consider more quantitatively the energy balance for the diagram in Fig. 1(c). The nL electrons per unit area move to the bulk semiconductor gaining the energy $\Delta F_{MB} \equiv F_M - F_B$ each, amid occupying the region of width L with screening charge density n in the bulk semiconductor. This increases the electrostatic energy in both the film and bulk semicon-

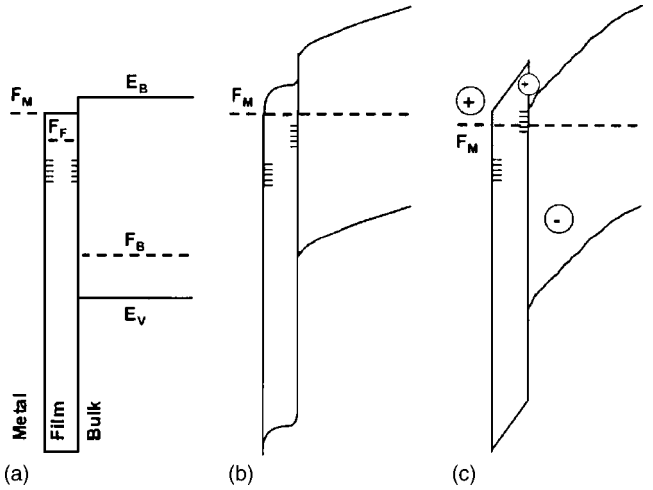

FIG. 1. Energy-band diagrams for a system of metal, semiconductor thin-film, bulk semiconductor (a) before contact, (b) after contact as predicted by the standard Schottky barrier formation scenario, (c) after contact accompanied by acceptor defect generation.

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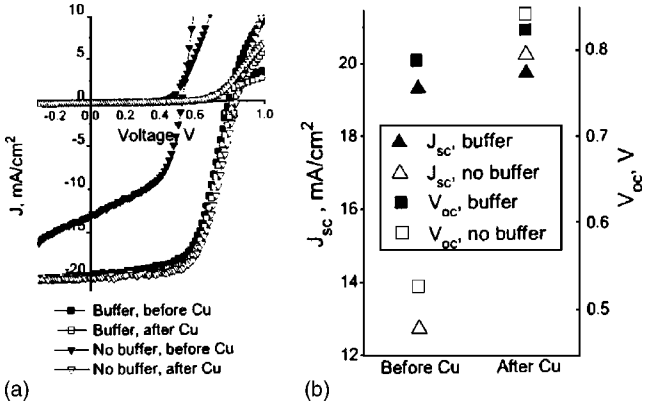

FIG. 2. $J-V$ curves (a) and open circuit voltage (V_{oc}) and short-circuit current (J_{sc}) (b) for Cu-doped and undoped CdS/CdTe structures with and without buffer layer.

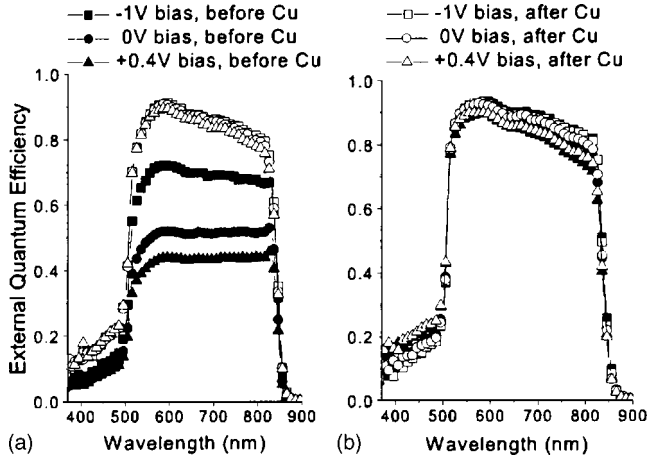

FIG. 3. QE characteristics of CdS/CdTe structures without (a) and with (b) buffer layer for different voltages before and after Cu diffusion.

ductor second and third terms on the right hand side of Eq. (1) below. Also, we add the defect generation energy W_d that depends on defect chemistry in the film and semiconductor. Optimizing the total energy

$$W(L) = nL\Delta F_{MB} + \frac{2\pi n^2 q^2 L^3}{3\epsilon} + \frac{2\pi n^2 q^2 L^2 l}{\epsilon} + W_d \qquad (1)$$

yields the the barrier width L_l and energy gain $W(L_l)$

$$L_l = \sqrt{L_0^2 + l^2} - l, \quad L_0 \equiv \sqrt{\frac{\epsilon \Delta F_{MB}}{2\pi n q^2}}; \qquad (2)$$

$$W(L_l) = -\frac{2nL_l \Delta F_{MB}}{3}\left(1 - \frac{lL_l}{2L_0^2}\right) + W_d. \qquad (3)$$

For the case of $l=0$ our consideration reproduces the well-known result[2] for a Schottky barrier. The scenario of Fig. 1(c) becomes energetically favorable when $W(L_l)$ is lower than the energy $W(L_0)$ calculated with the parameters corresponding to the thin film (with $\Delta F_{MB} \rightarrow \Delta F_{MF} \equiv F_M - F_F$). As is seen from Eq. (3), such a scenario is more likely when $l \ll L_0$.

As exposed to the absorbed light, a strong reach-through band bending can generate a high open-circuit voltage, thus paving a way to efficient photovoltaics. A related conceivable effect is that shifting up the thin film energy spectrum can affect the electron-hole recombination and further improve the system characteristics.

We now turn to the experimental verification of the above scenario and note preliminarily that the suggested defects can be introduced through either surface states on the interface between the thin film and the metal or by chemical doping. Our experiments were aimed at revealing similarities between the effects of surface modification and doping.

As an implementation of a structure in Fig. 1, we used a 0.25-μm-thick n-type CdS and 3.5-μm-thick p-type CdTe deposited on a glass substrate by close-space sublimation (see Ref. 3). Their respective charge carrier concentrations,[4] $n \sim 10^{17}/\mathrm{cm}^{-3}$ and $p \sim 10^{14}/\mathrm{cm}^{-3}$, were such that the CdS film thickness $l=0.25$ μm was much smaller than the screening length in CdTe and much larger than that in CdS ($L_0 \sim 3$ μm and $L_0 \sim 0.1$ μm, respectively, assuming a built-in voltage ~ 1 V).[2] The transparent conductive oxide (TCO) layer of sheet resistance 15 $\Omega/\square$ on a glass substrate underlying the CdS was used as a conductor. The structures underwent the standard anneal in the presence of $CdCl_2$ vapors known to improve electrical characteristics.[5]

To affect the CdS interface, we additionally deposited on the TCO a 0.1-μm-thick tin-oxide based buffer layer.[6,7] Its sheet resistance ($\approx 1.2 \times 10^4 \Omega/\square$) was much higher than that of the TCO, yet low enough to consider it a metal in the sense that its Fermi level is above that of the CdS film (as assumed in Fig. 1 where the leftmost parts of the diagrams can represent either the TCO or the buffer layer).

For the alternative CdS modification by doping, Cu was introduced at the metal semiconductor junction through an anneal step.[8] The latter procedure promotes the movement of Cu to the CdS film where it accumulates in high concentrations.[9]

We have measured current–voltage ($J-V$), quantum efficiency (QE) and capacitance–voltage ($C-V$) characteristics that constitute the basic diagnostics for CdS/CdTe photovoltaics.[2] The $J-V$ results in Fig. 2 represent the averages of ten to 1.1 cm area cells. QE (measured with white bias light, Fig. 3) and $C-V$ (at 75 kHz, Fig. 4) measurement were taken on two cells for each condition.

Both the open-circuit voltage and short-circuit current (under one-sun light intensity) in Fig. 2 are almost the same in the range of practically significant values for the undoped

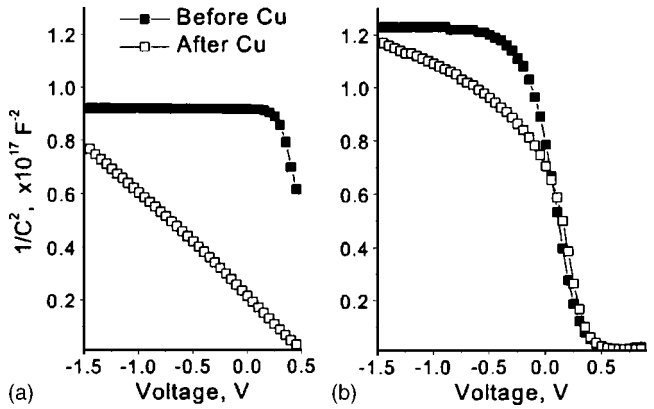

FIG. 4. $C-V$ characteristics of CdS/CdTe structures without (a) and with (b) buffer layer before and after Cu diffusion. In the graph (a) the data are truncated to $V<0.5$ V to avoid the conduction contribution indicated by the phase angle between the real and imaginary parts of the measured admittance.

devices with buffer layer and for doped devices without buffer layer. However, these parameters are much lower when neither buffer layer nor Cu doping are present. This shows that either the buffer layer application or Cu doping lead to a well developed junction where the built-in field is strong enough to provide efficient current collection.

Furthermore, the close numerical coincidence between the two recipe results suggest that Cu and the buffer layer have a similar effect on the CdS layer. Since Cu is known to act as an acceptor CdS, [10] Fig. 1(c) seems to represent a plausible band diagram for either the Cu-doped or the buffer-layer-containing structure. This choice is additionally supported by the observation [Fig. 2(a)] that the dark $J-V$ curves are abnormally flat thus showing extremely high series resistance. We attribute the latter to a barrier V_B in Fig. 1(c) (which is photoconductive, similar to Ref. 11). The undoped devices without buffer layer are better described by the diagram in Fig. 1(b), which predicts a poorly developed junction and thus low V_{oc} and J_{sc}.

QE data (Fig. 3) confirm our interpretation. Since QE represents the number of electron-hole pairs collected per photon, we conclude that carrier collection is equally improved by doping or applying a buffer layer. In addition, the QEs of undoped structures without buffer layer are strongly bias dependent. This means, again in agreement with Fig. 1(b), that the junction is not well developed and thus carrier collection can be considerably improved by reverse bias. Disappearance of such bias dependence after Cu diffusion can be attributed to the formation of a well developed junction. A strong junction consistent with the diagram in Fig. 1(c) is also evident from the QE data for the structures with buffer layer. Similarly the $J-V$ characteristics, the QEs remain practically insensitive to Cu doping for the buffer layer containing structures, meaning that the junction once developed by the buffer layer effect remains practically insensitive to further material compensation, consistent with the above understanding.

$C-V$ data (Fig. 4) add specificity to the above interpretation. Samples without buffer layer and Cu show voltage-independent geometrical capacitance. Cu doping creates a space charge region, which, in accordance with the standard interpretation,[2] is responsible for the slope of C^{-2} vs V. However, with the $J-V$ data in mind, that region does not seem to contribute much to the device barrier height (close similarity between the Cu and buffer layer effects). Finally, the buffer-layer-containing devices exhibit $C-V$ characteristics typical of MIS structures with C varying between two limiting geometrically related values,[2] which, again, is consistent with the diagram in Fig. 1(c). Also, the latter is consistent with the observed potential drop between the CdS and buffer layer in the buffer/CdS/CdTe structure studied with the Kelvin probe technique.[12]

We conclude that the above data confirm the hypothesis of Schottky barrier suppression in a semiconductor thin film and show that the metal can act through the film causing reach- through band bending. More specifically, our findings suggest that surface treatments can dramatically change the dielectric properties of a thin film and thus affect the electric field distribution in the entire system. For example, the CdS deposition method (sublimation or sputtering) and temperature can affect the device V_{oc}, a prediction that can be verified experimentally.

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