SUBCONTRACT TITLE: ***ADVANCED PROCESSING OF CdTe- AND $CuIn_{1-X}Ga_XSe_2$- BASED SOLAR CELLS***

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1.0 INTRODUCTION

This is the final report for the 3-year project with subcontract # NDJ-2-30630-18. The CdTe section of the report is organized in 2 major sections: (a) a summary of the activities and major results obtained during the first two 2 years (covered in Annual Reports I & II), and (b) activities for year 3. Additional details will be provided within the subsequent sections.

2.0 SUMMARY OF FABRICATION PROCEDURES

The CdTe portion of the project utilizes a set of tools, materials, and processes previously developed and/or under study during this project. These are summarized in table 1; more specific details for the various materials/processes will be provided within the results/discussion sections that follow.

Table 1. Summary of processes and materials utilized for the fabrication of CdTe solar cells

	Materials	COMMENTS
Substr.	7059 Borosilicate Glass; Soda lime glass (TEC 15)	Borosilicate glass cleaned in dilute HF solution (1:10) and rinsed with DI water
Transparent Contact	SnO_2:F†	by MOCVD (Tetramethyltin, O_2, F-source: Halocarbon 13B1)
	Cd_2SnO_4	by co-sputtering of CdO and SnO_2
	$CdIn_2O_4$	by reactive co-sputtering of Cd and In
	ITO	by sputtering of In_2O_3:Sn @ T_{SUB}=300°C
Buffer Layer (high-ρ)	SnO_2†	by MOCVD (as above; undoped)
	SnO_2	by sputtering of Sn (reactive) or SnO_2 targets
	Zn_2SnO_4	by co-sputtering of ZnO and SnO_2
	$ZnIn_2O_4$	by reactive co-sputtering of Zn and In
	In_2O_3	by reactive sputtering of In
CdS		by: (a) Chemical Bath Deposition (CBD)† and (b) Close-spaced sublimation (CSS)
CdTe		by CSS: (a) small area reactor for baseline devices†; (b) large area (10 x 10 cm^2) deposition with substrate motion
$CdCl_2$ HT		(a) Direct application of $CdCl_2$ by evaporation followed by HT†; (b) Exposure of CdTe surface to $CdCl_2$ vapors
Back Contact	Graphite	(a) doped with HgTe:Cu†; (b) undoped (used as received)
	Mo	by RF sputtering
	Sb_2Te_3/Mo	by RF sputtering
	Cu_XTe/Mo	by RF sputtering
	Cu/back electrode	Cu deposited by sputtering; back electrode: undoped graphite or Mo

† Baseline material/process

3.0 HIGHLIGHTS FROM PHASES I AND II

This section is only a summary of work that was carried out during the first two years of the project. Additional details can be found in the annual reports submitted previously [1,2]

3.1 Conductive Oxides and Buffers (low-ρ/high-ρ Bi-layers)

3.1.1 Conductive Oxides Investigated During this Project

Various oxides (high ρ and low ρ) deposited by RF sputtering were investigated during this project. The only exception is SnO_2:F which serves as the baseline conductive front contact and is prepared by CVD (see table 1). Table 2 summarizes the (optimized) properties obtained for the conductive oxides.

Table 2. Transparent oxide properties obtained for materials used during this project

Material	T_{DEP} [°C]	T_{ANN} [°C]	Sheet ρ [Ω/□]	ρ [Ω-cm]	μ [cm^2/(Vs)]	n [cm^{-3}]	E_G [eV]
Cd_2SnO_4	RT	600	10.57	$2.01X10^{-4}$	29.2	$8.47X10^{20}$	3.15
$CdIn_2O_4$	RT	600	9.14	$2.90X10^{-4}$	30.9	$5.50X10^{20}$	3.43
SnO_2:F	480	None	9.50	$4.00X10^{-4}$	38.0	$4.00X10^{20}$	3.85

3.1.2 CdTe Solar Cells on Various Bi-layer Oxides as Front Contacts

In an effort to identify alternative front contact materials a major component of this project focused on fabricating devices using the various conductive oxides studied. Solar cells were fabricated using baseline processing on substrates coated with the conductive oxides listed in table 2, in combination with a high-ρ (or buffer) oxide (i.e. the front contacts were low-ρ/high-ρ bi-layers). Table 3 lists representative "best" devices fabricated during phases I & II. High-ρ oxides used were: SnO_2 by CVD or sputtering, Zn_2SnO_4, and In_2O_3.

Among the devices of table 3, the Cd_2SnO_4/Zn_2SnO_4 cell is superior with respect to J_{SC}. This improvement is directly related to the blue response for this cell (see Fig. 1); based on the starting thickness of the CdS, it was not expected that blue QE would be as high as shown in Fig. 1. It is therefore speculated that the CdS was consumed from both sides (i.e. it interdiffused with both the CdTe and Zn_2SnO_4 films). Clearly, as previously demonstrated by the group at NREL, this particular bi-layer structure is best suitable for "thin CdS" devices. More on the effect of Zn_2SnO_4 will be discussed later.

Table 3. Representative devices fabricated on the various bi-layer transparent contacts

Front Contact	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]
Cd_2SnO_4	821	23.10	69.6
Cd_2SnO_4/SnO_2(CVD)	849	23.90	68.9
Cd_2SnO_4/SnO_2(RF Sput.)	825	23.60	69.7
Cd_2SnO_4/Zn_2SnO_4	830	24.93	67.5
$CdIn_2O_4/SnO_2$(CVD)	837	23.80	70.4
$CdIn_2O_4/In_2O_3$	825	23.30	69.3

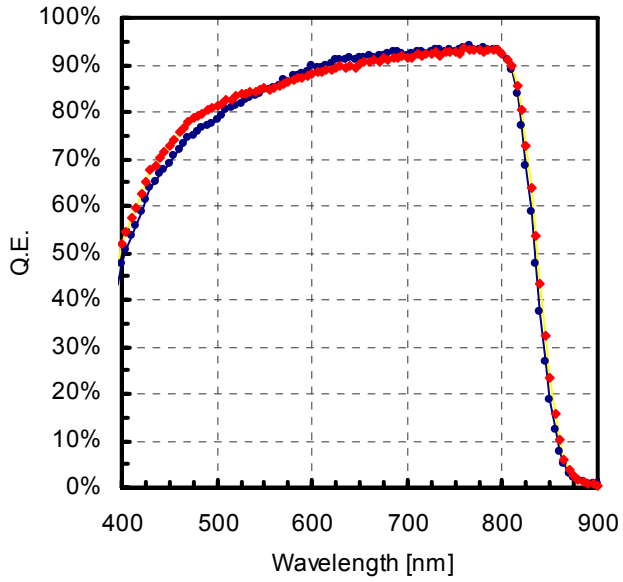


Figure 1. Spectral response of CdTe solar cells fabricated on Cd_2SnO_4/Zn_2SnO_4 bi-layers

3.1.3 CdTe Solar Cells Fabricated Directly on Cd_2SnO_4

One of the interesting findings of the front-contact related work was the performance of CdTe cells fabricated directly on Cd_2SnO_4 (for example the first device in table 3). The performance of these cells was comparable to devices fabricated on low-ρ/high-ρ bi-layers (i.e. V_{OC} > 800 mV & FF in the high 60's). Table 4 lists a series of devices fabricated directly on Cd_2SnO_4 of various thicknesses. As indicted in a previous report, the as-deposited Cd_2SnO_4 films are amorphous and require annealing (T_{ANN}>575°C) in order to crystallize. Although no buffer was used for the devices listed in table 4, it is possible that the surface of Cd_2SnO_4 is still defective enough (possibly not fully crystallized) and can therefore have a similar effect as a buffer layer; this is only a speculation at this time, however, the potential of utilizing Cd_2SnO_4 without a buffer clearly exists as suggested by the solar cell results in table 4.

Table 4. Solar cell performance for cells fabricated on Cd_2SnO_4 without a buffer layer

Cd_2SnO_4 thickness [Å]	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]
1000	825	23.56	68.3
1500	808	23.48	67.3
2000	821	23.10	69.6

3.1.4 ITO/In_2O_3 Bi-layers

In addition to the conductive oxides listed in table 2, ITO (In_2O_3:Sn) was also used for cell fabrication in bi-layer front contacts with In_2O_3 as the buffer, (realizing that there are material issues related to indium which may place such a bi-layer structure at a disadvantage for large scale manufacturing).

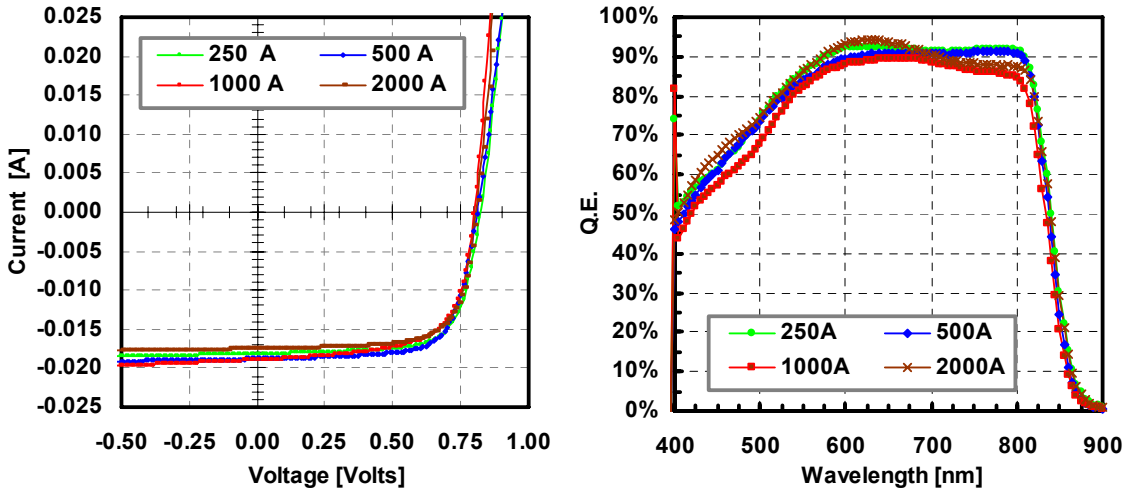


Figure 2. Light J-V and SR for CdTe cells fabricated on ITO/In_2O_3 bi-layers; the starting CdS thickness is approximately 600 Å

The results obtained on CdTe cells fabricated in ITO/In_2O_3 bi-layers are summarized in Figs. 2 and 3; Figure 2 shows J-V and SR data from devices fabricated with a starting CdS thickness of approx. 600 Å, and varying In_2O_3 thickness (from 250 to 2000 Å). The results shown in these two figures clearly demonstrate the reproducibility of device performance obtained for this bi-layer configuration (even at these relatively small CdS thickness). The blue SR @ 450 nm is approximately 60 % or higher, suggesting that this combination is an effective front contact for devices with "thin" CdS. It is also apparent that the thickness of the buffer (In_2O_3) does not seem to have a significant impact on device performance over a large range. Most importantly, a thickness of only 250 Å is sufficient to improve device performance. As indicated in a previous report, devices fabricated directly in ITO suggested that a barrier was present at the front of the device (i.e. between CdS and transparent contact). Figure 3 summarizes the performance of several sets of devices as a function of the CdS and In_2O_3 thicknesses. In general, as is often typical behavior for CdTe cells, thinner CdS results in lower V_{OC} and FF, with the effect of the In_2O_3 being minimal or non-existent, as mentioned above.

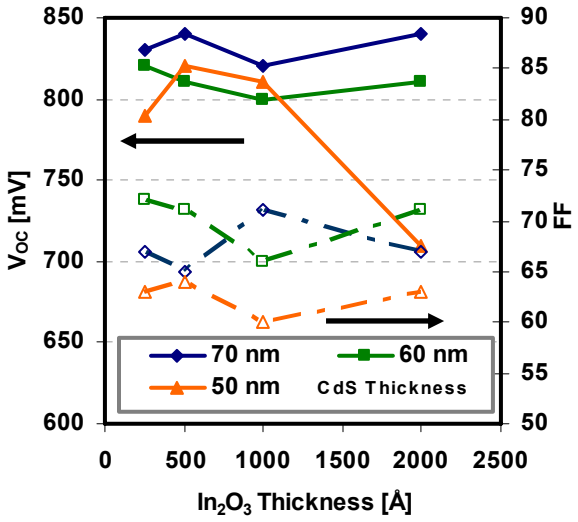


Figure 3. The V_{OC} and FF for CdTe cells fabricated on ITO/In_2O_3, as a function of the thickness of In_2O_3 and CdS

3.1.5 Zn-Sn-O(ZTO)-based Devices

Work on ZTO films and the use of these as buffers in CdTe cells, has continued during the final phase of this project, and most results will be presented in a subsequent section. The only highlight presented here is the effect of annealing temperature (which directly affects the films' structural properties) on device performance. As indicated in a previous report the ZTO films (similar to Cd_2SnO_4) begin to crystallize at temperatures around 575°C; this effect seems to correlate very well with device performance as indicated in Fig. 4, where solar cell performance is shown as a function of ZTO annealing temperature. It should also be noted that when ZTO is used as-deposited (i.e. amorphous) the consumption of CdS is enhanced (presumably due to additional interdiffusion with ZTO).

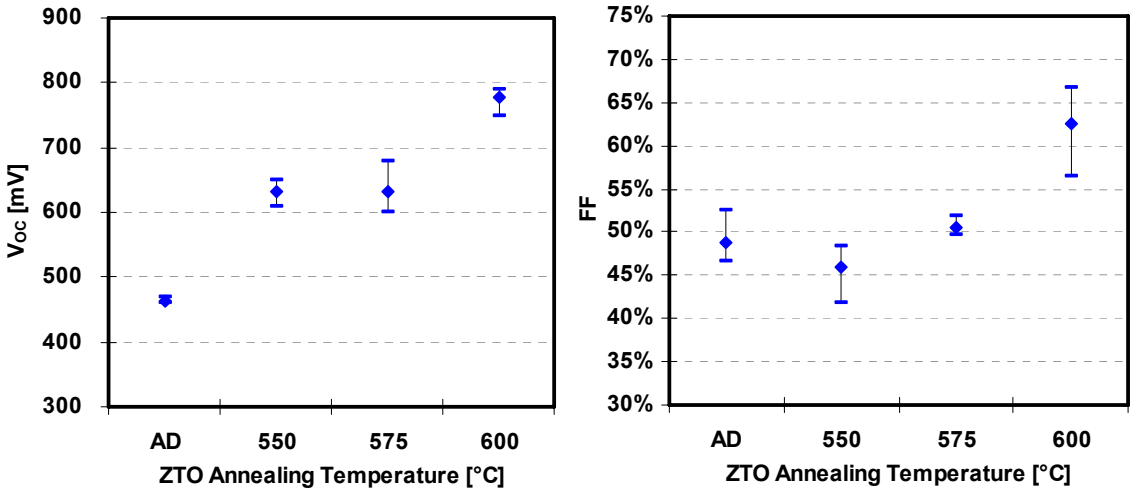


Figure 4. The V_{OC} and FF for CdTe cells fabricated on ZTO buffers annealed at various temperatures

3.2 Improving Process Manufacturability

A major objective of this project was to seek ways to simplify device processing in such a way that it would ultimately improve the manufacturability of CdTe cells and modules and therefore provide solutions for further lowering the manufacturing costs of this technology. Three issues addressed during phases I and II were: (a) decreasing the time of the $CdCl_2$ heat-treatment, an obvious bottleneck in CdTe manufacturing; (b) investigating the effect of a dry CdTe surface treatment prior to the formation of the back contact, and (c) investigating the performance of CdTe cells fabricated using a process scheme that simulates real manufacturing conditions, such as deposition of the semiconductors on moving substrates.

3.2.1 Vapor $CdCl_2$ Heat Treatment

The $CdCl_2$ heat-treatment is a common feature among all CdTe cell technologies. In general this process requires temperatures in the range of 380-420C for durations of 20-30 minutes. During this project a vapor $CdCl_2$ treatment was investigated and state-of-the-art device performance characteristics were demonstrated. Subsequent work in this area focused on reducing the $CdCl_2$ treatment duration below 5 minutes, in order to improve the throughput of the technology. The key results from these efforts are summarized in Figs. 5 and 6. Figure 5 shows a set of light J-V for devices heat-treated for 1, 2, and 5 minutes; it should also be noted

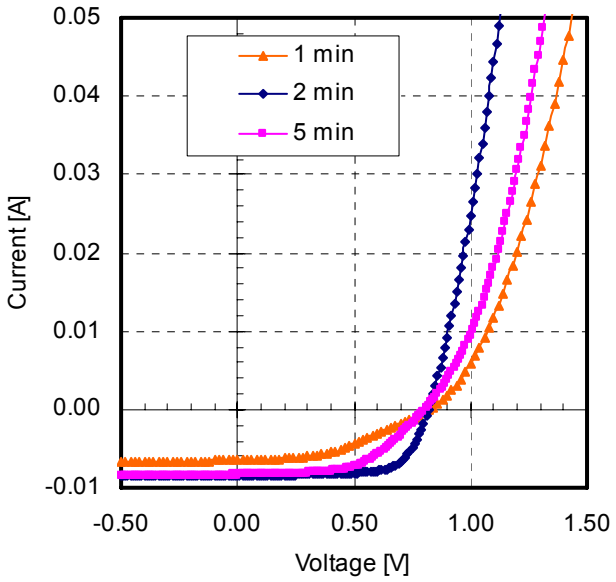


Figure 5. Light J-V for CdTe cells $CdCl_2$ heat-treated at 500ºC for times of 5 mins or less

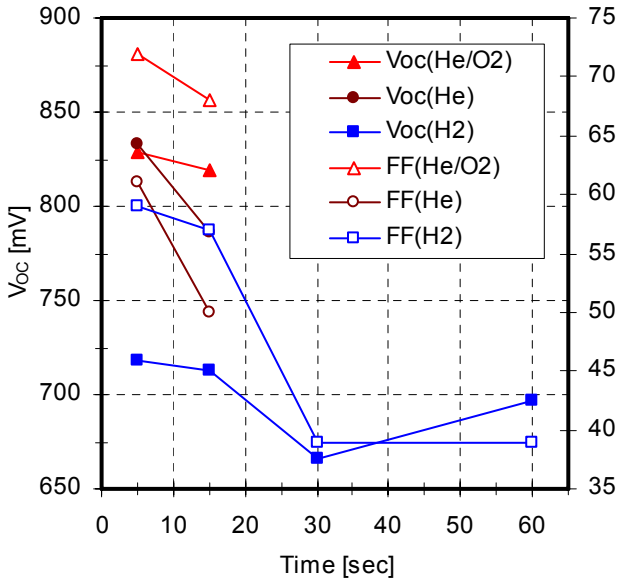


Figure 6. V_{OC} and FF for cells vapor treated for times less than 1 minute

that all devices described in this section did not receive the baseline Br_2/methanol etch; rather, they were contacted immediately following the $CdCl_2$ heat treatment. The cells in Fig. 5 exhibit similar V_{OC}'s (around 820^+ mV), however two of the devices also exhibit limited FF's due to an apparent back contact barrier. This behavior, which was not uncommon, points to the difficulty of controlling the surface of CdTe during the accelerated $CdCl_2$ heat-treatment. Since the heat-treatment is carried out in the presence of O_2 it is reasonable to expect the formation of oxides on the surface of CdTe, which can lead to FF losses similar to what is depicted in Fig. 5; it is believed that had the devices in Fig. 5 undergone the standard Br_2 etch, that they would all behave as the device heat-treated for 2 mins. Therefore, these results not only demonstrate that the duration of the $CdCl_2$ heat-treatment can be significantly reduced by simply using higher annealing temperatures, but they also suggest that improved control of this process to minimize the formation of surface oxides can lead to elimination of the wet etch prior to the application of the back contact, further improving the manufacturability of the technology. Figure 6 offers further evidence of the potential of reducing the $CdCl_2$ heat-treatment time. The device performance depicted in Fig. 6 is for cells that were heat-treated for a few seconds; it should be noted that the time required to reach the annealing temperature, was on the order of 2-3 minutes, therefore the actual annealing time (i.e. within a certain ΔT around the annealing temperature) is longer than what is depicted in Fig. 6. Nevertheless, the results shown here clearly demonstrate that the $CdCl_2$ heat-treatment need not be a bottleneck for CdTe module manufacturing.

3.2.2 Dry Back Contact Process

As mentioned above, the devices described in the previous section did not undergo the standard Br_2 etch prior to the application of the back contact. However, in the event that a CdTe surface treatment will be necessary, it would be desirable to have a vacuum-based dry process to replace the wet etch. To that end a dry etch plasma process was investigated. A summary of results obtained from this study is depicted in Fig. 7, where solar cell performance is shown as a function of the RF power and etch time (N_2 was used as the sputter gas). These results show that state-of-the-art V_{OC}'s with little dependence on the sputter etch process characteristics, can be achieved. On the other hand the FF seems to degrade significantly

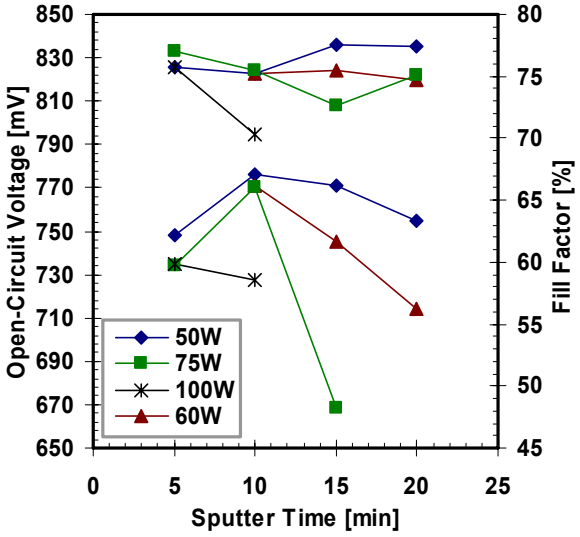


Figure 7. The V_{OC} and FF for CdTe cells sputter etched under different conditions of rf-power and sputter time (sputter gas: N_2)

depending on the process parameters. It is therefore possible to develop an all-dry process for the fabrication of CdTe cells, avoiding issues associated with handling and disposing of solutions generated from wet-based processes.

3.3 Stability

Device stability is another major component of this project. During the first two phases the effect of the $CdCl_2$ heat-treatment on device performance was studied. A brief summary of this work is provided here.

3.3.1 Devices Studied – Stress Conditions

The devices studied had the typical superstarate configuration and were fabricated using baseline processes:

- 7059/SnO_2:F/SnO_2/CdS(CBD:70-80nm)/CdTe(CSS:4-5 µm)/Graphite:HgTe:Cu

The main variation was the temperature used for the $CdCl_2$ heat treatment:

- $CdCl_2$ heat treated at 360, 380, 390, and 400°C

The stress conditions were:

- T: 60-70°C
- Inert Ambient
- Light/Dark Cycles (4 hrs ON/4 hours OFF)
- Cells kept at OC and SC

3.3.2 Summary of Observations

Additional details of this work can be found in previous reports [2], the key observations and findings are described here:

- In all cases performance degraded; ***the samples processed under optimum $CdCl_2$ conditions degraded less***
- Short-circuit conditions lead to smaller changes/degradation (vs. OC)
- In some cases the observed changes – in particular the increase in the dark current – were "delayed". However, after 1000 hours of light soaking the device characteristics were essentially indistinguishable.

Figure 8 below shows J-V data for cells processed at non-optimum conditions (left and center) and cells processed at optimum conditions (right). The key devices changes are marked with circles and labeled as A, B, C, and D

- "A": this area marks dark shunting, that was not observed in devices processed under "optimum conditions", i.e. the devices whose J-V characteristics are shown in the far right.
- "B": this area marks a region affected by R_S, back contact (roll-over), or changes in the photoconductivity of CdS; these differences/changes can be seen in the linear J-V (region "C"), where in some cases the slope clearly decreases while in others the entire J-V simply shifts to lower voltages; this points to two potential mechanisms present: (a) a simple increase in resistivity in one of the semiconductors (most likely CdS), and (b) a change in the photoconductivity of CdS, or the formation of a secondary barrier at the front junction that further delays the device turn-on.
- "D": in all cases the light R_S increased
- All devices exhibited an increase in the dark current due to increased recombination

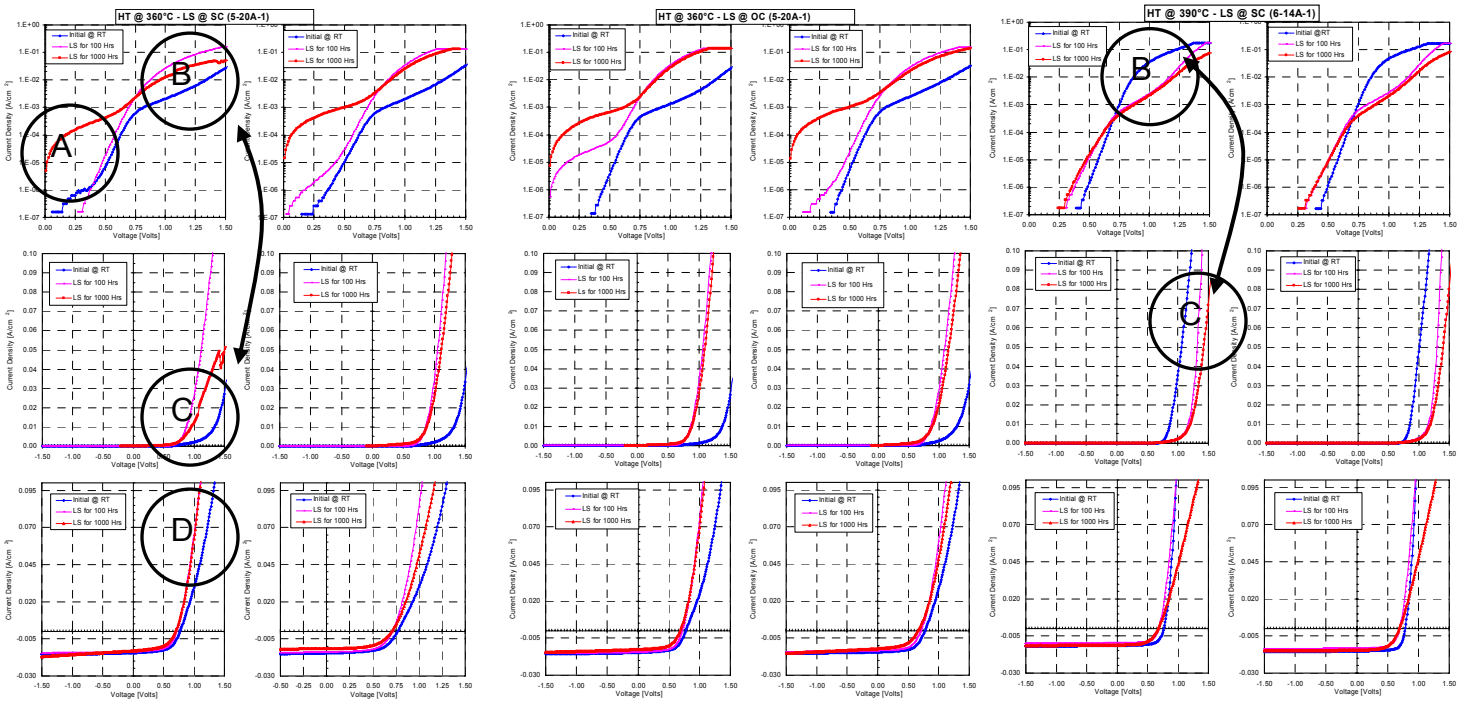


Figure 8. Dark and Light J-V for light soaked CdTe cells: left – sample $CdCl_2$ HT at 360°C kept at SC; center – sample $CdCl_2$ HT at 360°C kept at OC; right - sample $CdCl_2$ HT at 390°C (optimum) kept at SC.

4.0 PHASE III – FINAL YEAR

4.1 Zn-Sn-O(ZTO) Buffers and Their Effect on Device Performance

The effectiveness of bi-layer front contacts in CdTe has been demonstrated by several groups, including the CdTe Group at NREL that has achieved the current record efficiency of 16.5% using zinc stannate (ZTO) as the high resistivity (buffer) layer in their CdTe devices; zinc stannate refers to two types of oxides depending on the film stoichiometry: (a) Zn_2SnO_4 has a cubic spinel structure, and (b) $ZnSnO_3$ has an orthorhombic structure.

During the 3rd Phase of this project work on ZTO films and solar cells continued in order to improve our understanding of their effect on device performance. The films are being deposited by co-sputtering from ZnO and SnO_2 targets (4N), a process that allows variation and control of film stoichiometry. The main focus for this work has been to study the effect of film stoichiometry (i.e. Zn/Sn ratio) on film and device properties; the term "Zn/Sn ratio" refers to the as-deposited film ratio determined through calibration runs using EDS; to-date the Zn/Sn ratio was varied from 1.5 to 3.0, with most experiments focusing on the ratio of 2.0 (in order to obtain the Zn_2SnO_4 phase of zinc stannate). In order to maintain control of the Zn/Sn ratio, the process was recalibrated every 4-5 depositions. In addition to the effect of the Zn/Sn ratio, the effect of the deposition and annealing temperatures of the ZTO films was also studied. Since the main effect of ZTO films is that they are effective in devices with "thin" CdS, the thickness of the CdS was also varied; this was done primarily by adjusting the conditions of the $CdCl_2$ heat treatment (i.e. temperature) to promote the consumption of CdS. Additional information on the ZTO process has been included in previous reports. Solar cells were fabricated using "baseline" procedures: these include CBD CdS, CSS CdTe, and doped graphite contact; the device structure was: SnO_2:F/ZTO/CdS(CBD)/CdTe(CSS)/graphite-HgTe:Cu.

4.1.1 Resistivity

The resistivity of the ZTO films was measured using the 4-point probe method. The results of these measurements are summarized in Fig. 9; all films shown were deposited at room temperature and annealed in inert ambient; the resistivity of as-deposited films was in most cases too high to measure with the 4-point probe method (no resistivities for as-deposited films are shown in Fig. 9).

The results in Fig. 9 suggest the following:

- Although the resistivity of films annealed at 550°C is lower than that of the as-deposited films, it is still the highest in this set of samples; this could be due to their structural properties. Since as indicated previously, films annealed at 550°C remained amorphous, their mobility may be too low resulting in these high resistivity values.
- In general, the resistivity decreases with increasing annealing temperature; again this could be due to improvements in the film microstructure (i.e. films become polycrystalline) as indicated by XRD analysis [3]. One exception to this trend is the resistivity of the films deposited at a ratio of 1.0; to the extent that this behavior is related to the particular phases formed in these films (Zn/Sn=1.0) it is not clear at this time, since no XRD data are available on these films as of yet.
- The resistivity increases with Zn content; a similar trend in resitivity was observed by others and it was attributed to the phase(s) of the ZTO films formed for the different Zn/Sn ratios [4]. Since based on the XRD data obtained during this work essentially all annealed ZTO films contained both ZTO phases (Zn_2SnO_4 and $ZnSnO_3$), the resistivity is believed to be determined by the relative amount of each phase (and the overall film crystallinity)

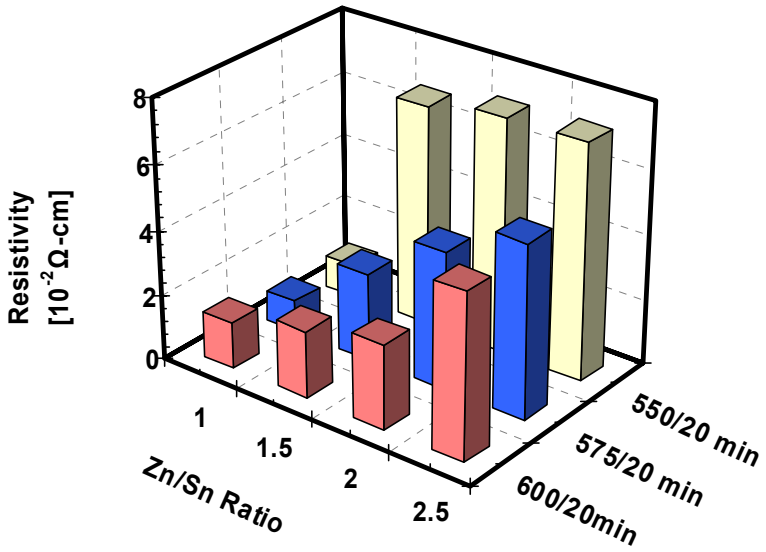


Figure 9. The resistivity of ZTO films as a function of the Zn/Sn ratio and annealing conditions

4.1.2 Structural Properties

The co-deposition process used for this project offers the option to vary the film stoichiometry. A series of films were deposited at different Zn/Sn ratios (1.5-2.5). Figure 10 shows the XRD spectra of the ZTO films deposited over this range; (all spectra shown are for films deposited on glass/SnO_2 substrates and have been annealed in inert ambient at 600°C; the major peaks located at 26.63, 51.80, and 54.78° are originating from the substrate and it is not possible to identify the formation of SnO_2 with the ZTO film itself). Table 5 lists the various planes (and phases) identified from these data. These results suggest that:

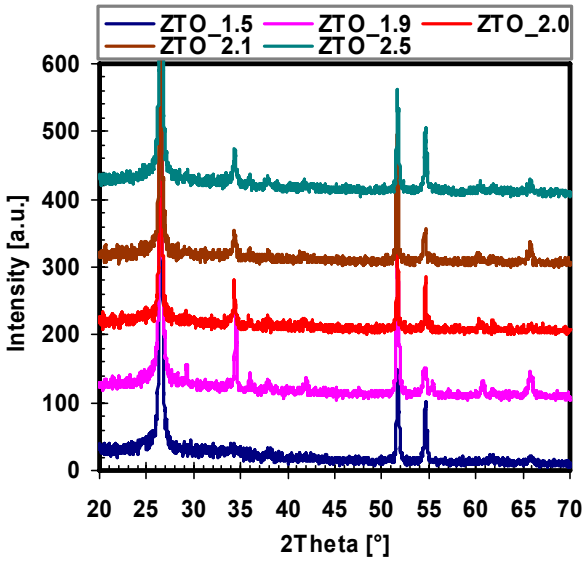


Table 5. XRD peaks identified for the films shown in Fig. 10

Zn/Sn	Zn_2SnO_4	$ZnSnO_3$
1.5	None	(006)
1.9	(220), (311), (222), (400), (440)	(006)
2.0	(311), (222), (400), (440)	(006)
2.1	(311), (222)	None
2.5	(311), (222)	(006)

Figure 10. XRD spectra for ZTO films deposited at different Zn/Sn ratios; annealed at 600°C

- For Zn-rich and near stoichiometric films (Zn/Sn=1.9-2.5) the Zn_2SnO_4 phase dominates
- For Zn-poor films (Zn/Sn=1.5), the Zn_2SnO_4 phase is not detected; only weak reflections from the $ZnSnO_3$ are found

Another process parameter varied was the substrate temperature. The two films shown in Fig. 11 were deposited with a Zn/Sn ratio of 2.0 at a substrate temperature of 400ºC; one of these was subsequently heat treated at 600ºC. A key difference between these ZTO films and the ones discussed above (all of which were deposited at room temperature) is the relatively low intensity of the Zn_2SnO_4 peaks. Instead, the highest intensity peaks (excluding those from the SnO_2 substrate) correspond to the $ZnSnO_3$ and ZnO_2 phases. This is the only case (i.e. high deposition temperature) where a binary oxide phase was identified. Table 6 summarizes the results of the XRD measurements.

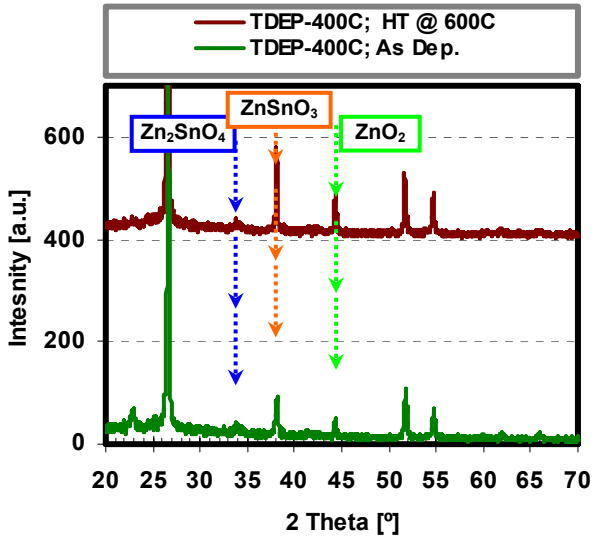


Figure 11. XRD spectra for ZTO films deposited at 400ºC; bottom: as-deposited; top: heat-treated

Table 6. List of peaks identified in the ZTO films shown in Fig. 11 (deposited at T_{SUB}=400°C)

	Zn_2SnO_4	$ZnSnO_3$	ZnO_2
AD.	(311)	(006)	(211)
AD/HT @ 600C	(311)	(012), (006)	(211)

4.1.3 ZTO-Based Solar Cells

Solar cells were fabricated on glass/SnO_2:F/ZTO substrates using baseline procedures i.e. CBD CdS, CSS CdTe, $CdCl_2$ HT, doped graphite back contact. Most ZTO films used for the solar cells discussed in this section, originated from the same deposition runs as the films shown in Figs 9 and 10 that describe their XRD characteristics.

4.1.3.1 Zn/Sn=2.0 – Effect of Annealing Temperature

One batch of devices whose SR and J-V characteristics are shown in Figs. 12 and 13, were fabricated on ZTO films deposited with a Zn/Sn ratio of 2.0 and were utilized for solar cell fabrication either as-deposited or after a heat-treatment in inert ambient. The results in Fig. 12 demonstrate a finding described in a previous report: when ZTO films are amorphous they tend to enhance CdS consumption. The devices shown in Fig. 12 had their CdS films deposited at the same time (i.e. same CBD CdS deposition), therefore the starting CdS thickness was the same for all these cells, yet the blue response clearly shows that in two of these the CdS is significantly thinner; the highest blue SR, and therefore thinner CdS, are associated with the two devices fabricated on amorphous ZTO (i.e. as-deposited or annealed at 550°C). The dark J-V of the same devices are shown in Fig. 13, where higher dark currents are evident for the two devices fabricated on amorphous ZTO. The solar cell characteristics of the devices described in Figs. 12 and 13 are listed in table 7. The two cells fabricated on amorphous ZTO (thinner CdS and higher dark currents) exhibit the lowest V_{OC}'s and FF's, suggesting that amorphous ZTO films are not effective buffers (since the V_{OC} and FF decrease significantly with decreasing CdS thickness).

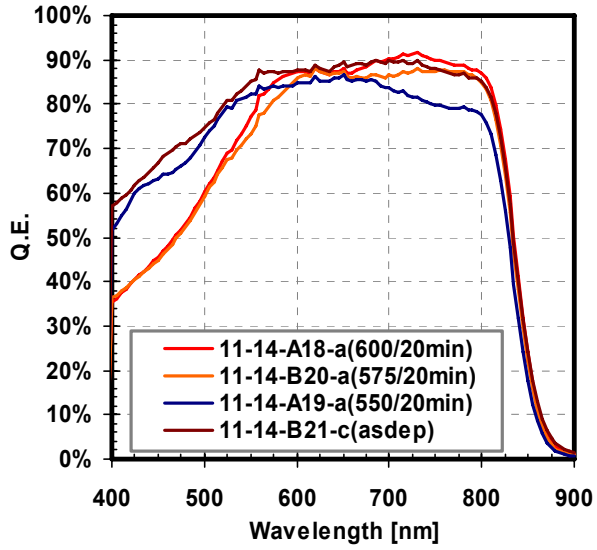


Figure 12. SR of cells fabricated on as-deposited and annealed ZTO films (Zn/Sn=2.0)

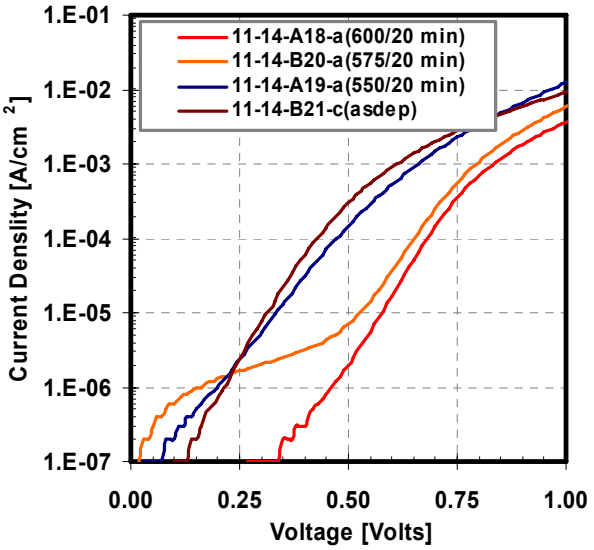


Figure 13. Dark Ln(J)-V for the cells shown in Fig. 12

Table 7. Solar cell performance characteristics for the cells shown in Figs 12 & 13

ZTO	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]	R_S (L) [Ω-cm^2]	R_{SH} (L) [Ω-cm^2]
AD	730	58.0	23.40	2.05	1100
HT 550 ºC	730	55.0	22.00	2.10	1000
HT 575 ºC	820	68.0	21.40	1.55	1170
HT 600 ºC	830	69.0	22.00	0.96	900

4.1.3.2 Effect of Zn/Sn Ratio

The effect of the Zn/Sn ratio in ZTO films was studied by depositing the films at ratios from 1.5 to 2.5 and subsequently annealing them at 600°C; this annealing temperature was chosen as "optimum" primarily based on solar cell results such as the one described in the previous section(s). The characteristics of cells fabricated on ZTO films with ratios from 1.5 to 2.5 are summarized in Figs 14 and 15, and table 8. All CdS films had the same initial thickness and all cells were exposed to the same $CdCl_2$ heat treatment, therefore, the only remaining difference that could influence the CdS thickness is the ZTO buffer. The blue response suggests that the cells for which the Zn/Sn ratios were 2.1 and 2.5 (i.e. excess Zn) end up with the thickest CdS (after completing the cell fabrication process); the cells with Zn/Sn ratios below 2.0 show an increased blue response, therefore thinner CdS. These results seem to suggest that CdS consumption also depends on the Zn-content (i.e. composition) of the ZTO films in addition to their structural characteristics (amorphous vs. polycrystalline) as discussed in the previous section. As noted for the cells discussed in the previous section, solar cell performance continues to degrade with decreasing CdS thickness, with the FF decreasing to a greater extent than V_{OC} as shown in table 8. The dark J-V for these devices do not offer a completely consistent correlation with device performance, primarily due to the fact that dark shunting and series resistance effects seem to dominate some of these devices; nevertheless, the best devices (Zn/Sn=2.1 & 2.5) do exhibit the lowest dark currents. It is reasonable to expect that extensive interdiffusion at the main junction would eventually lead to high dark (recombination) currents due to the formation of interfacial states. Based on the SR data of Fig. 14, ZTO films

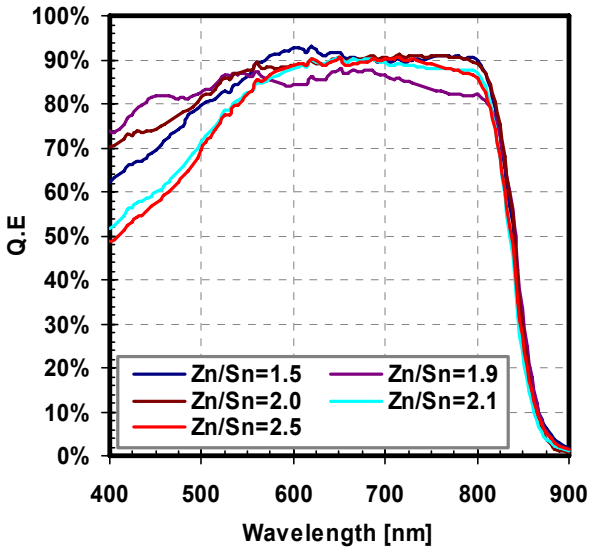


Figure 14. SR of cells fabricated with ZTO films deposited with different Zn/Sn ratios - annealed at 600°C

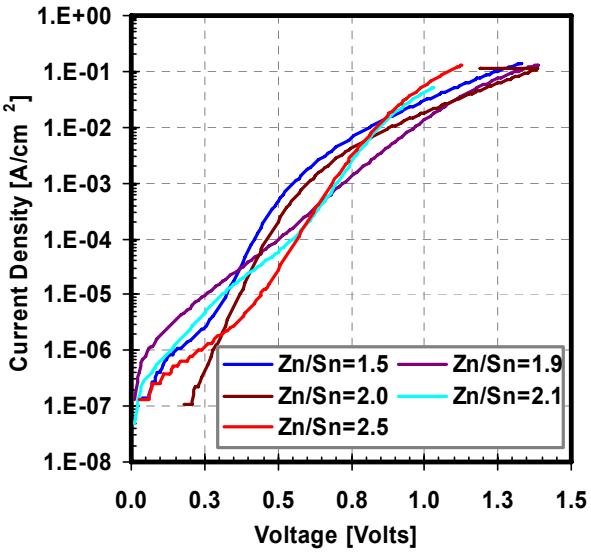


Figure 15. Dark Ln(J)-V characteristics of the cells shown in Fig. 14

Table 8. Solar cell performance characteristics for the cells shown in Figs 14 & 15

Zn/Sn Ratio	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]
1.5	710	54.6	24.40	2.32	500
1.9	770	44.3	24.00	2.34	730
2.0	780	58.2	24.50	2.30	800
2.1	810	66.6	23.10	2.50	800
2.5	790	66.7	23.00	1.40	900

with ratios equal to or less than 2.0 seem to consume CdS extensively. It is possible that in these devices Zn, Sn, and/or O can also diffuse into the CdTe junction region leading to the high currents shown in Fig. 15.

4.1.3.3 Effect of ZTO Deposition Temperature

As discussed in the "structural properties" section, ZTO films deposited at higher substrate temperatures (400°C; Zn/Sn=2.0) were found to contain ZnO_2 in addition to the zinc stannate phases. Several of these ZTO films with different thicknesses were used for cell fabrication. Spectral response data and device performance are summarized in Figs. 16 and 17, and table 9. Clearly in all cases the blue response of these cells is relatively high (greater than 60% for wavelengths below 500 nm), high enough that one would expect solar cell performance (V_{OC} and FF) to degrade. However, as indicated in table 9 all these devices exhibit high V_{OC}s and FFs; these cells also exhibit the highest shunt resistances of all the cells discussed in this report, suggesting that the buffer properties (and in general the CdS/buffer interface) are critical to improving this device parameter; R_{SH}). Subtle differences in the SRs shown in Figs 16 and 17 could be related to the duration of the ZTO annealing, which as indicated in the figures was carried out for 5 and 20 minutes respectively.

Clearly the results obtained for CdTe cells fabricated on ZTO buffers suggest that this material can be effective in utilizing thin CdS films while maintaining high V_{OC}'s and FF's. Nevertheless,

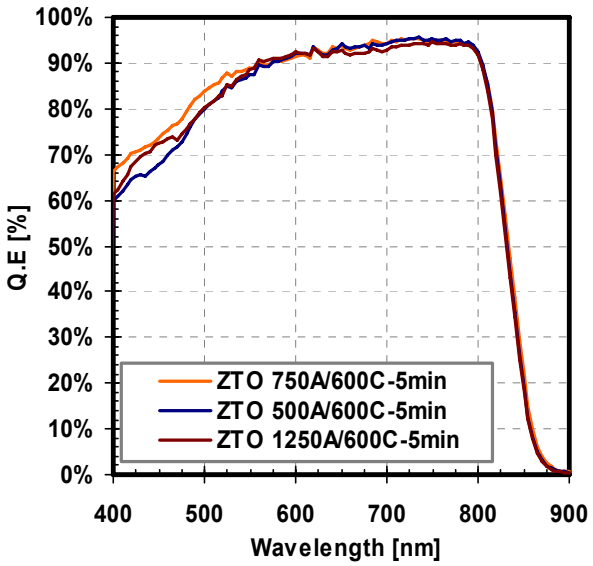


Figure 16. SR of cells fabricated with ZTO films deposited at 400°C; annealed at 600°C/5 mins

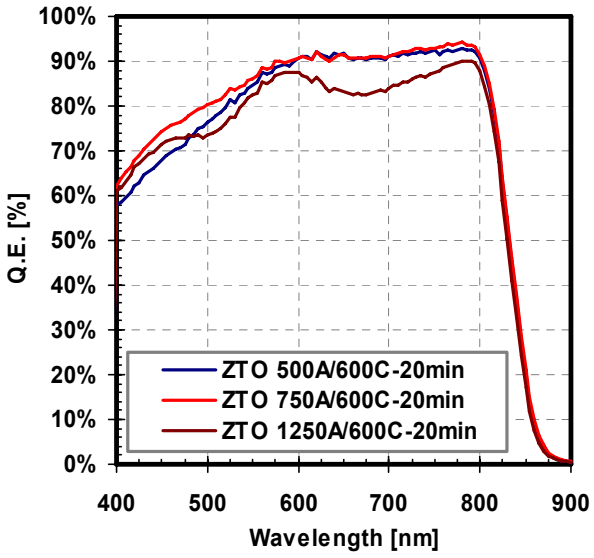


Figure 17. SR of cells fabricated with ZTO films deposited at 400°C; annealed at 600°C/20 mins

Table 9. Solar cell performance characteristics for cells fabricated with ZTO films deposited at 400°C (from Figs. 15 and 16)

Zn-Sn-O Thickness. [Å]	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]
500	840	68.2	24.40	1.64	1700
500	830	71.0	23.80	1.44	1700
500	830	69.3	24.74	1.33	1900
750	830	68.2	24.84	1.75	1900
1250	820	69.1	24.39	1.47	2000

the properties of ZTO must be closely monitored and controlled in order to achieve optimum performance, and both the composition and crystallinity of ZTO are critical. Although a Zn/Sn ratio of 2.0 yielded devices with “optimum” performance, it should be noted that the ZTO films were not single phase Zn_2SnO_4; rather the XRD analysis revealed that both zinc stannate phases (Zn_2SnO_4 and $ZnSnO_3$) and the binary ZnO_2 were all present (see table 6). The Zn-Sn-O system is certainly an interesting buffer that will require further studies in order to fully understand its impact on the junction composition and device performance. Such studies should include material phase identification, compositional depth profiles of the junction, and cross sectional analysis to determine the extent to which the CdS is fully converted into a different phase.

5.0 STABILITY STUDIES

The effort to correlate long term device stability to certain process parameters/characteristics continued during the 3rd phase of this program. This report summarizes results from a stability study that focused on devices fabricated with varying amounts of Cu in the back contact, in an effort to determine the role of this element on device stability and long term performance. In addition, a second set of devices without intentional Cu introduced during the back contact formation process was also fabricated and light soaked. In these cells Cu was introduced immediately following the CdS(CSS), deposition.

5.1 Devices with Varying Amounts of Cu in the Back Contact

The devices utilized in this study were fabricated with baseline procedures *excluding* the back contact fabrication step: following the $CdCl_2$ heat treatment the structures were rinsed in methanol and etched in a Br_2 solution (0.1% vol. in methanol). Subsequently, a thin Cu film (thickness varied) was deposited by sputtering; following the Cu deposition a graphite electrode was applied and heat treated in inert ambient. No intentional dopant was included in the graphite (used as-received); it is possible that the overall fabrication process could be re-optimized around this particular contact process for better initial performance, something that was not attempted for this work.

Figure 18 shows the initial performance characteristics of the solar cells used in this study; these were fabricated with different amounts of Cu in the back contact and heat treated at 240°C. The V_{OC}'s are reproducible and appear to improve with decreasing Cu thickness; however the FF's exhibit significant dispersion for the two larger Cu thicknesses, the cause of which is not clear at this time. Light soaking of the cells was carried out in a vacuum oven under N_2 ambient (the experimental set up was described in a previous report); the cells were exposed to light (within ±15% of AM1.5) during a 4 hour interval (ON), and subsequently stored in the dark for another 4 hours (OFF). Typically, four identical cells were stressed; two at open-

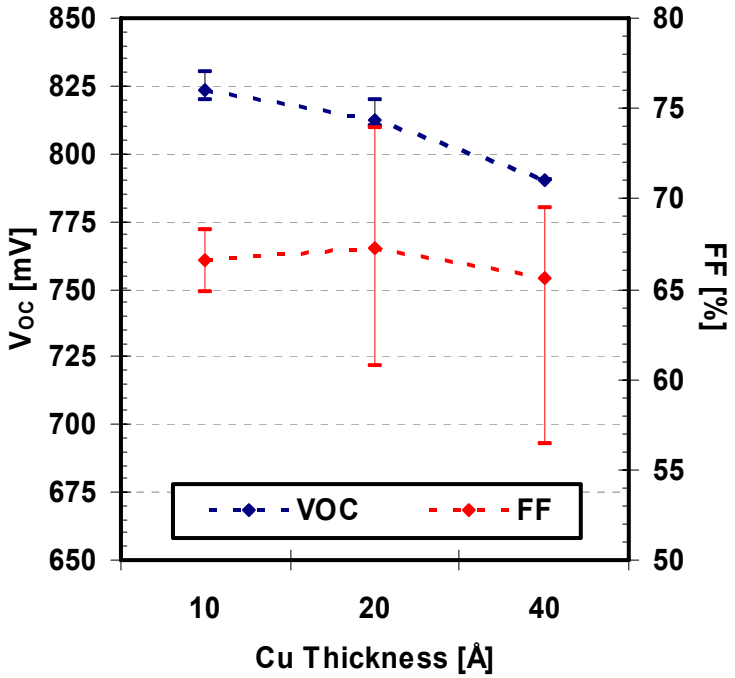


Figure 18. Initial V_{OC} and FF of CdTe cells used for light soaking

circuit (OC) and two at short-circuit (SC) conditions; the cell arrangement is shown in Fig 19. Dark and light J-V were measured at regular intervals during the ON and OFF cycles (typically 8 measurements were taken during the ON cycle); light J-V measurements were taken at operating temperatures – which reached the 60-70°C range.

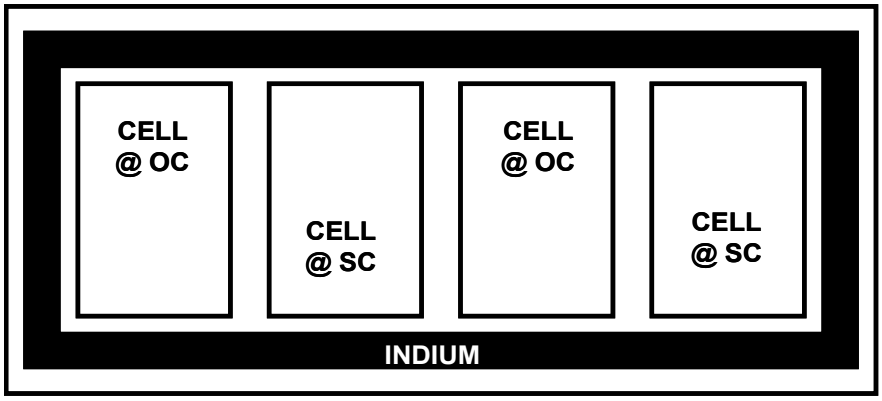


Figure 19. Substrate schematic showing the cell arrangement and bias conditions

5.1.1 General Trends

Figure 20 shows the general trends for V_{OC} and FF for devices light-soaked for over 700 hours at OC and SC conditions (two devices at each condition); missing data indicates that the particular device most likely experienced a catastrophic failure; in some cases the soldered contact to the cell failed and had to be reconnected, which resulted in missing data over short periods of the light soaking process. It should also be noted that the apparent "spread" in the values of the V_{OC} and FF is to first order associated with the cell temperature rising during the ON cycle; as indicted above up to 8 measurements were taken during the ON cycle, during which the sample temperature increased. Additional discussion on this variation will be provided below. The time axis in Fig. 20 is the total light soaking time (i.e. the time the cells were kept in the dark is not included).

5.1.1.1 Open Circuit Voltage – V_{OC}

As the data in Fig. 20 indicates cell performance decreased in all cases, however, there appear to be distinct differences among the three sets of devices as well as between the two bias conditions. The V_{OC} of the devices with the *smallest amount of Cu* (top/left) appears to have decreased slightly more for the devices held at OC but the difference is small, and since the number of devices tested is very small, it is considered to be statistically insignificant at this time. However, an examination of the two other sets of devices fabricated with increased Cu (left: middle and bottom), suggests that increasing the amount of Cu leads to two distinct changes: (a) *the **initial** (i.e. within the first 10-20 hours) decrease in V_{OC} increases with Cu*, and (b) the apparent "spread" in the values also seems to increase with Cu but only for the cells held at SC; more discussion on this "spread" will follow below. Therefore this set of data clearly suggests that higher Cu concentration is detrimental to V_{OC}, and the bias conditions influence the observed degradation; these observations are consistent with results obtained by other groups.

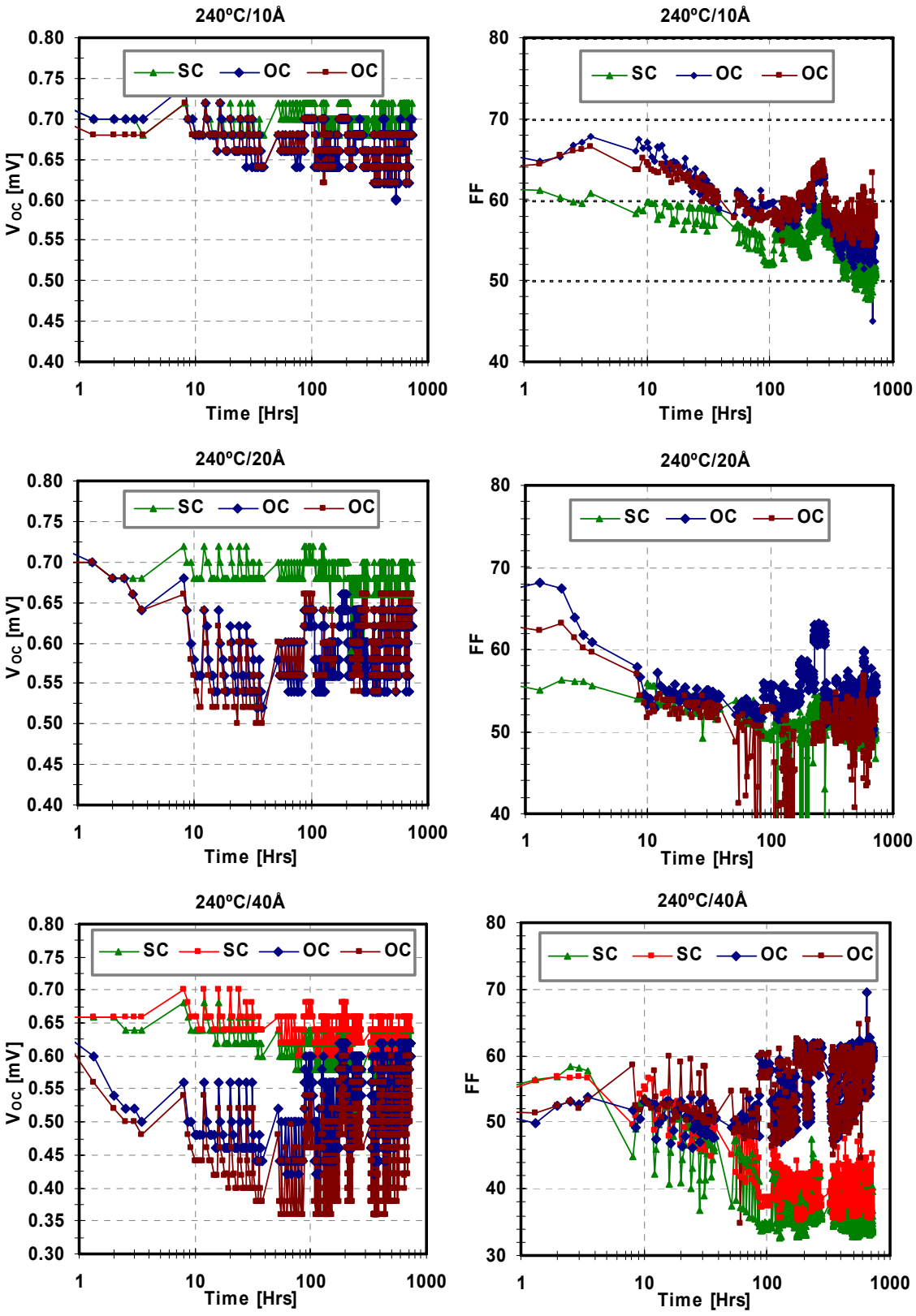
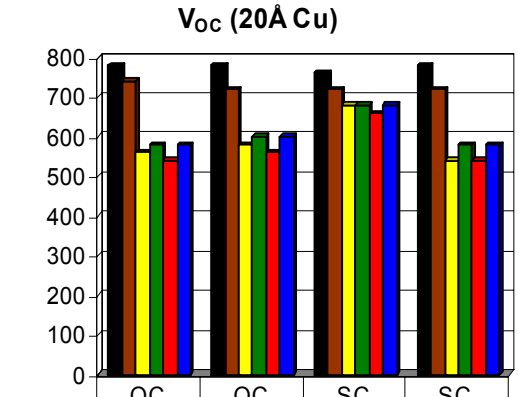
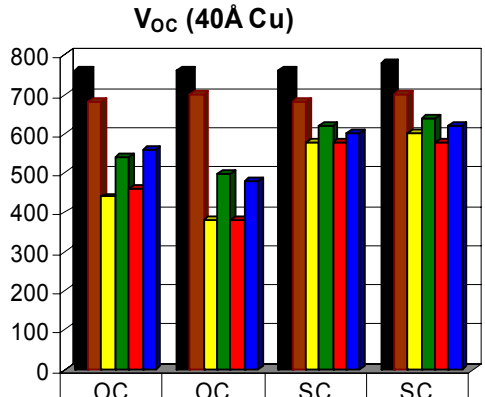


Figure 20. The V_{OC} and FF of CdTe cells during approximately 700 hours of light soaking; the back contact was formed using different amounts of Cu: top – 10Å; middle – 20 Å; bottom - 40 Å.

Some of the data of Fig. 20 are re-plotted in Fig. 21 to demonstrate two of the key general observations with respect to V_{OC}: (a) there is a large initial decrease, and (b) the overall decrease is larger for cells held at OC.



	OC	OC	SC	SC
initial	779.947	779.954	759.938	779.959
0.08	739.979	719.985	719.983	719.986
150	559.982	579.888	680.056	539.935
350	579.981	600	680.053	579.979
450	539.941	559.966	660.057	539.947
650	579.979	600.01	680.059	579.981



	OC	OC	SC	SC
INITIAL	759.935	759.935	759.93	779.957
0.08	680.025	700.013	680.025	700.015
150	440.022	380.061	579.978	599.996
350	539.942	499.98	620.021	640.042
450	460.015	380.067	579.991	579.982
650	559.962	480.001	600.001	620.01

Figure 21. V_{OC} (in mV) for cells fabricated with 20 Å and 40 Å of Cu; (the left column shows the total hours)

5.1.1.2 Fill Factor – FF

The general trend in the FF behavior varies significantly from that observed for V_{OC}. For the cell with the smallest amount of Cu (top/right), the initial and final (after 700 hours) values appear to be in the same range. However for cells held at OC there is an initial increase in the FF which is not uncommon for CdTe cells; this is consistent with findings of others who have observed an initial increase *in performance* during stability studies. As the Cu amount is increased (middle/right), the overall FF behavior appears to be very similar for both bias conditions (i.e. at OC and SC). Further increase in the amount of Cu leads to distinctly different trends for the FF of cells held at OC vs. SC; cells held at OC show an increase in the FF while those held at SC exhibit a decrease. As indicated earlier, from a performance point of view the devices fabricated with the largest amount of Cu exhibited the lowest performance, with the spread in the values of FF being significantly large.

The behavior of both the V_{OC} and FF suggests that the cells are undergoing changes that are not linear with time, and which can be quite complex; the higher Cu amounts clearly seem to lead to increased degradation as well as more complex behavior. From J-V data it is apparent that part of the FF losses can be attributed to increases in the series resistance, while losses in V_{OC} can be due to higher dark currents and collection losses.

5.1.1.3 Transients

In the previous section the presence of a "spread" in the V_{OC} values (to be referred to as a "transient" from this point onward) was attributed to the change in cell operating temperature. As already mentioned above, up to 8 measurements were taken during the ON cycles. During the ON cycle one would expect the cell temperature to rise, and initial calibrations of the sample stage suggested that the temperature of the cells could reach 60-70°C. It should be noted that only limited temperature data were collected during the light soaking process. Figure 22 shows smaller "regions" of the data shown previously in Fig. 20 (around 200 and 600 hours). The V_{OC} in all cases decreases during the duration of the ON cycle. When this "transient" behavior was first recorded it was attributed to the cell temperature rising and no further analysis was planned. However, as the light soaking process continued certain changes in the transient behavior seemed to suggest that this may not be simply a temperature effect, and the data suggests that a correlation exists between the transient and the amount of Cu and bias condition. The magnitude of the V_{OC} *change* increases as one moves to higher Cu concentrations (it is highest for cells held at OC), and seems to decrease with time. Each plot in Fig. 22 (and Fig. 20) contains data from cells fabricated on the same substrate, and as indicated in Fig. 19 the bias conditions were alternated (i.e. the 1st and 3rd devices were held at OC and 2nd and 4th were held at SC); therefore the temperature of the four devices should be essentially identical. Nevertheless, the magnitude of this V_{OC} transient for the 40 Å devices (bottom) is clearly at least 2 times higher for the cells light soaked at OC. To further demonstrate that this transient is not simply a temperature effect Fig. 23 shows the FF for the 40 Å. The FF behavior is again more complex. Around 200 hours the FF for the device held at OC decreases, while for the device held at SC it decreases and then recovers. At the 600 hour interval the device held at SC no longer shows any transient behavior, while the time constant of the transient of the device held at OC appears to be short.

In general the transient behavior can be generically attributed to trapping (and detrapping) of carriers through Cu-related (or possibly other impurity) complexes. Although the limited set of data collected in this case suggests a correlation with Cu, further targeted studies will be needed to possibly identify the complexes and their location across the device structure; it is also possible that these transients can be used to predict module long term stability.

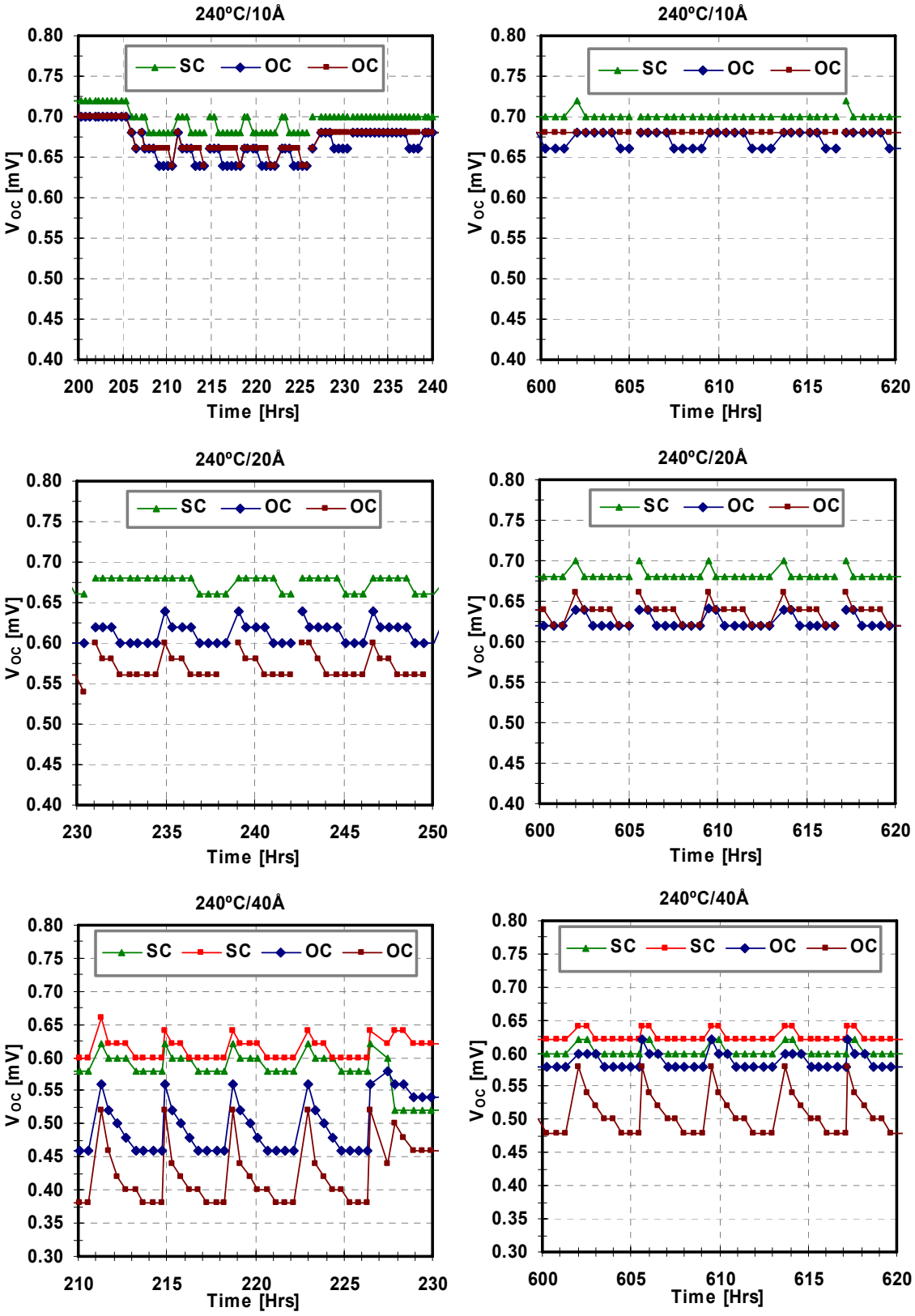


Figure 22. The data shown in this figure are expanded portions of the V_{OC} plots shown in Fig. 20, to show the variation of V_{OC} during the ON Cycle; data from 210-230 hours for the 20 Å cell were lost due to a break in the connection to the data acquisition system.

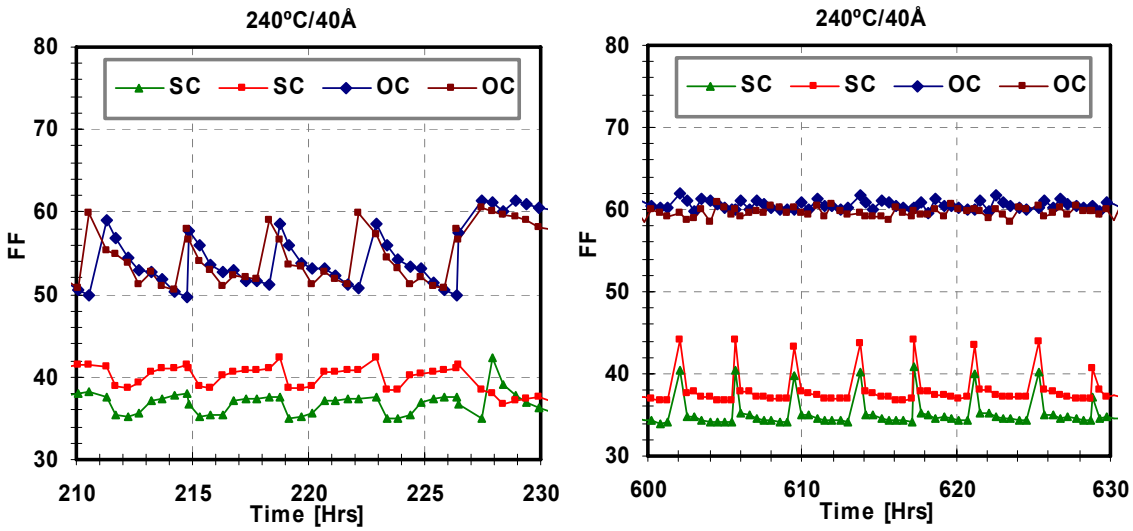


Figure 23. The FF for the 40 Å devices around the 200 and 600 hour

5.2 Devices with No Intentional Cu in the Back Contact

In the previous sections the light soaking/stability related work focused on devices fabricated with varying amounts of Cu in the back contact. The devices to be discussed in this section differ in the way Cu was introduced in the cell. Figure 24 shows the distinction in the fabrication process between the devices discussed above (left) and the devices to be discussed in this section (right).

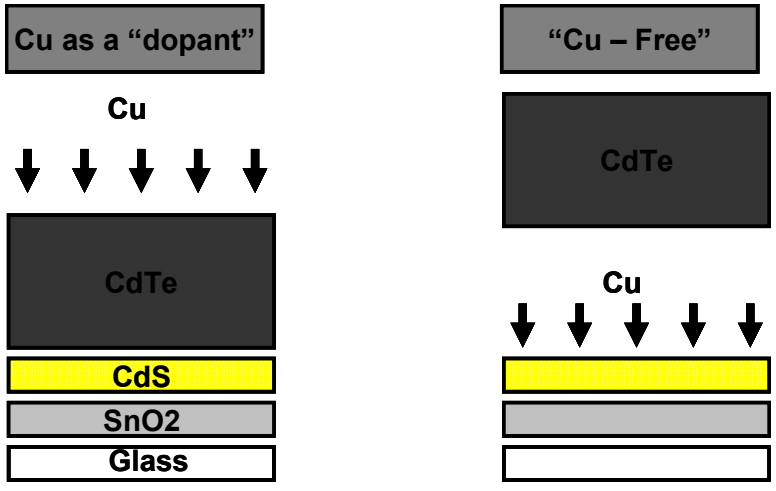


Figure 24. The baseline cell fabrication sequence (left) where Cu is added during the back contact process (devices discussed in section 5.1), and the approach utilized for the devices discussed in this section 5.2 (right)

It is now well known that Cu seems to accumulate at the CdTe/CdS interface, and light soaking (or other type of stress) leads to an increase of the Cu levels at the interface and not necessarily in CdTe (bulk). In an effort to further understand the role of Cu a process where Cu is introduced near the device interface has been developed [5]. Following the CdS deposition by CSS, the films (glass/SnO_2:F/SnO_2/CdS) are dipped in a warm aqueous solution of CuCl (of a certain concentration); from this point on this process will be will be referred to as a "Cu-treatment". With more details available elsewhere, tables 10 and 11 list some of the device characteristics obtained for cells processed using the Cu-treatment process (Fig.24 – right).

Table 10. The effect CuCl solution concentration on solar cell performance

CuCl Concentration [M]	V_{OC} [mV]	FF [%]
6.0×10^{-9}	766	60.1
3.0×10^{-7}	772	59.8
6.0×10^{-8}	830	67.4
6.0×10^{-7}	733	53.0

Table 11. The effect CuCl-treatment time on solar cell performance

Time [min]	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]
5	710	55.5	23.9
10	830	66.3	23.4
15	830	65.3	23.9
20	650	48.0	19.6

Using this Cu-treatment approach, a series of CdTe cells were fabricated (the back electrode was sputtered Mo) and put through a light-soaking process. The light soaking conditions were the same as those described in the previous section. The only difference is that these cells were only light soaked at open-circuit (OC) conditions.

Table 12 lists initial and final performance data for the Cu-treated devices; the measurements were taken at room temperature before and after light soaking the cells for approximately 700 hours. Each performance value in table 12 represents the average from 3 cells; the information in the second column refers to the amount of concentrated "stock" solution used and treatment time. All final solution concentrations were in the *mid 10^{-8} M range*, very close to the "optimum" conditions listed in table 10. Some of these devices exhibited a significant drop in performance which is associated primarily with losses occurring at the back contact (i.e. back contact barrier formation). Figure 25 shows the light J-V around V_{OC} of a representative (degraded) cell; clearly the curvature in this region of the light J-V characteristics suggests degradation of the back contact properties.

Table 12. Initial and final performance of Cu-treated CdTe solar cells following light soaking of approximately 700 hours

		V_{OC} [mV]		**FF [%]**	
Sample ID	**cc/min**	**Initial**	**Final**	**Initial**	**Final**
1-8-A17	10/10	807.5	755.0	55.0	34.0
3-23-A1	***12/8***	***807.5***	***807.5***	***64.5***	***62.0***
1-8-B11	10/10	812.5	785.0	62.9	38.2
4-2-B8	12/10	815.0	690.0	44.2	43.2
2-26-A7	10/10	816.7	793.3	63.6	50.0

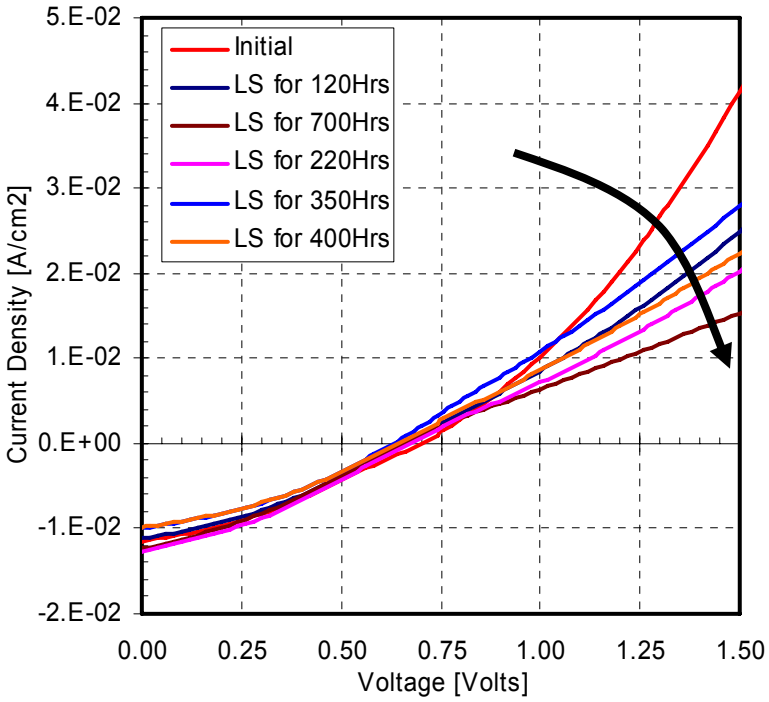


Figure 25. Light J-V around V_{OC} for a degraded CdTe cell

Nevertheless one set of devices (3-23-A1) show no losses in V_{OC} and only a 2% drop in their FF (as indicated above the values in table 12 are averages from 3 cells, therefore there are 3 devices that exhibited essentially no change in performance). These results provide existence proof that stable CdTe devices can be fabricated, with Cu intentionally introduced at the junction of the cells. The fact that the degradation in these cells was dominated by back contact losses, suggests that this device region remains a key to achieving long term stability. Assuming that Cu is essential in CdTe cells to achieve a certain level of performance, there appears to exist an "optimum" amount and "location" for this element in order to also achieve long term stability. Clearly these results suggest that work on the role of Cu in CdTe cells must continue.

PART II – CIGS

1.0 INTRODUCTION

CIGS solar cell technology has been on the threshold of commercial success for several years. The two predominant types of deposition have been the two-step metallization followed by selenization with hydrogen selenide process, and the co-evaporation process. Each of these clearly has merit, but there are also shortcomings. Co-evaporation is from a purely technology perspective the ideal process in that atoms can be placed exactly where they are needed. It is not surprising then that the highest efficiencies are achieved with this process, and the high degree of control is conducive to building a base of understanding of the relationships among deposition, film properties and performance. The technical prowess of this technology, however, is also the source of its shortcomings on the manufacturing floor. The exacting control that it provides and thus requires turns into a premium in manufacturing cost. The two-step process allows for depositing atoms in layers which is less costly but then depends upon both the kindness of nature and as much cleverness as we can conjure up to have the atoms reassemble into favorable locations and phases. Consequently it enjoys a lower manufacturing cost but gives up some performance relative to co-evaporation. Another shortcoming of the two-step process is that it uses hydrogen selenide gas which is hazardous and thus detracts from the otherwise good manufacturability profile. It is too early to draw conclusions about which of these may nevertheless succeed as a major commercial player. However, it has been, and still is the case that improved processes for CIGS are desired, if not needed.

The primary objective of this project was to develop improved processing techniques for CIGS solar cells. The approach has been a modification of the two-step process in which selenization is accomplished by use of selenium instead of hydrogen selenide. This is clearly a less hazardous approach, and it was hoped that throughput would also be increased. An equally important objective was to contribute to the understanding among growth, film properties and performance, particularly with respect to the similar hydrogen selenide two-step process. Throughout the project contributions have been made to this understanding through both experimental results and interpretations with AMPS based simulations. To a large extent these contributions have been generic and not unique to our process. This is particularly true for the identification and influence of defects. Early on in the project a fundamental CIGS model was developed based upon the identification of the key defects and formation energies by the NREL theory group. This model has been successful in guiding interpretation of the behavior of our devices and has helped understand the origins of defect formation for our process. These defects are present in all devices, though to different extents depending upon the processing details. Their influence on performance is the same, and thus that part of the understanding is generic. Those results have been presented on an ongoing basis in reports, publications and Thin-Film Partnership meetings.

In this final report we will focus upon a few topics that have been ongoing and have been furthered with recent results. Of greatest importance is new insights we have gained regarding performance limitations in our devices. This has resulted from combining simulations with experimental results related to Na and substrate effects. Before presenting these results we will first present our findings on performance versus CIGS thickness. As we all know, the supply and cost of Indium as become a key factor in the prospects for large scale CIGS manufacture. Most CIGS devices are about two microns thick which is about twice the thickness needed for effective light absorption. Thus cutting the CIGS thickness in half would significantly impact the use of Indium as well as increase the throughput. Consequently most of us in the CIGS community have taken up the challenge to reduce thickness but maintain performance.

Following presentation of CIGS thickness results we will provide results on our efforts to alter the doping profile of ZnO. ZnO is normally doped with Al or Boron and is typically degenerate n-type. It serves well as the transparent contact, but that contact also involves use of an undoped layer. Many studies have demonstrated that the properties of the undoped ZnO layer affect performance, and this is especially true for devices that avoid use of CdS. In earlier projects we worked explicitly on ZnO/CIGS devices and achieved record current densities. However, Voc's and FF were always lower than devices with CdS, and this was apparently due to the superior interface with CdS. Reports of the development of p-type ZnO suggested new possibilities. We undertook development of p-type ZnO using our processing approach with the thought that the ability to systematically move the fermi level might provide new opportunities for device improvement. There is also an overriding need for good p contacts for other devices. As will be discussed below, we did produce p-type ZnO but did not pursue studies in CIGS devices because of funding limitations.

2.0 CIGS THICKNESS STUDIES

2.1 Background

CIGS solar cells have demonstrated their capabilities as a promising thin-film technology. CIGS modules are in production and are commercially available using the leading deposition technologies, and others are working behind the scenes to develop improvements in those technologies as well to develop other approaches. An issue that has arisen is the potential high cost of the Group III components, particularly In. To help mitigate this issue it is desirable to reduce the thickness of devices from their typical value of 2-3 microns down below 1 micron. In this section we report results from our efforts to contribute to this endeavor. Our devices are fabricated from an all-solid-state two-step process that is similar to the hydrogen selenide-based two-step process. Details have been provided elsewhere[6] and briefly below. A key aspect of the process is that CIGS formation depends upon both the kinetics and thermodynamics of the layered precursor films. The constituents need to diffuse together and then react to form single phase CIGS, particularly in the space charge region. An important consideration is minimizing the formation of secondary phases. We have optimized our process for thicknesses of two microns; however, reduction of the thickness upsets the balance we have achieved and requires retuning. Our best devices have bandgaps of about 1 eV. As will be discussed below, the bandgap becomes an important parameter in efforts to reduce device thickness.

2.2 Experimental

Our substrate is soda lime glass, which we purchase from the local hardware store. A standard glass cleaning procedure is used, and the glass substrate is heated in vacuum prior to Mo deposition by sputtering. Varying combinations of metal or metal selenide layers are deposited by evaporation. These precursor layers are then annealed in a selenium flux through a temperature profile with a maximum temperature of 550 °C. Several process recipes are presently under development, and each involves specific precursor layers and anneal profiles. All of what is presented in the following discussion is for our baseline process. In this process the order of deposition of the precursors is Cu/Ga/(In + Se). Formation of the semiconductor layer takes about one-half hour. The substrate is finally turned into a device using standard procedures for CBD CdS followed by sputter deposition of high ρ/ low ρ ZnO. The elemental sources are located to give rise to compositional gradients to enrich the data base. To get as much mileage as possible out of a run we fabricate 5 x 5 arrays of 0.1 cm2 devices by using a shadow mask for the ZnO deposition. The arrangement of sources around the substrate is shown in Fig. 1.

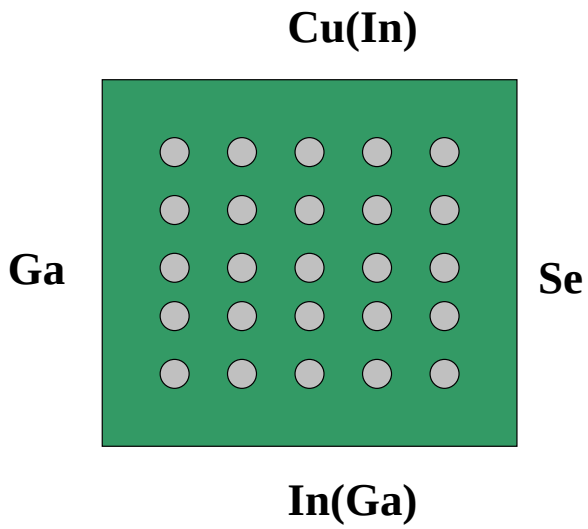


Figure 1. Arrangement of sources around the 2" x 2" substrate for the original chamber. For the new chamber Cu and Se are uniform, and the sides of highest In and Ga composition are shown in parentheses.

2.3 Results and Discussion

For the initial runs in this study we reduced the thickness by reducing the deposition times of the metal precursors. We expect, based on past experience, that when we change the run parameters to reduce the thickness it will be necessary to retune the entire structure to accommodate the change. In particular we have shown that the Na level has a profound effect on performance [7] and that some adjustment of the back contact to compensate for the reduced CIGS thickness will be needed. Nevertheless for the devices used in this study we have left the rest of the device steps fixed. In Fig. 2 we show (the two data curves) the effect on QE of reducing the CIGS thickness from our standard thickness of 2.0 microns to 0.65 microns. As can be seen, there is a downward shift in the overall spectrum and additional loss in the red that we will argue is a shift in band gap and not simply transmission loss. The downward shift we have shown previously to be attributed to interface states [6,7]. To help interpret these results we have also included AMPS simulated QE spectra for three CIGS thicknesses. The parameters we use in our AMPS simulations contain a complete set of defect parameters and have been shown to match experimental performance of our devices [6]. In Table 1 we show the AMPS simulated performance parameters for our standard 2.0 micron devices and what happens if all that we change is the thickness. As can be seen in Fig. 3, there is some tradeoff in the red and blue regions of the simulated spectra in dropping to 1.0 microns, and additional absorption loss in the red at 0.65 microns. However, the change in the red for the 0.65 eV data is much larger, and we attribute this to a band gap shift. The device data is below that of the simulations in the red because this series of devices has somewhat poorer collection than the experimental device used as the basis for simulations, but that does not detract from the observations and interpretation. In Fig. 3 we show additional data for thicknesses of 1.5 and 1.0 microns. The 1.5 micron spectrum (CO25-056) shows the downward shift which is seen to diminish in the red because the carriers are generated away from the recombination interface at the front and the bandgap shift is small. The 1.0 micron device (CO26-11) has the same downshift, but significantly reduced red response. When comparing with the simulation loss for

absorption in Fig. 2, which is minimal, it must be concluded that the change in the red is due to a bandgap shift in the 1.0 micron device.

Table 1. AMPS simulated performance for 2.0, 1.0 and 0.65 microns CIGS thickness.

Parameter/Thickness	2.0	1.0	0.65
Voc	.496	.509	.518
Jsc	37.8	37.1	35.1
FF	0.68	0.72	0.74
η	13.4	14.3	14.2

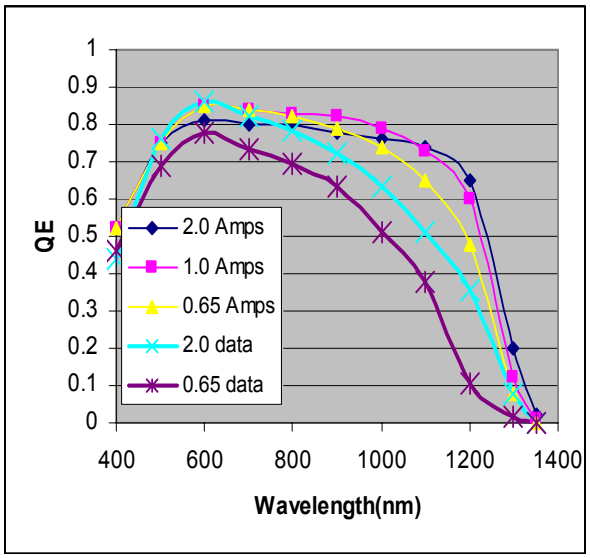


Figure 2. Experimental spectra for 0.65 and 2.0 micron thick CIGS and AMPS simulated QE spectra for 2.0, 1.0, and 0,65 microns.

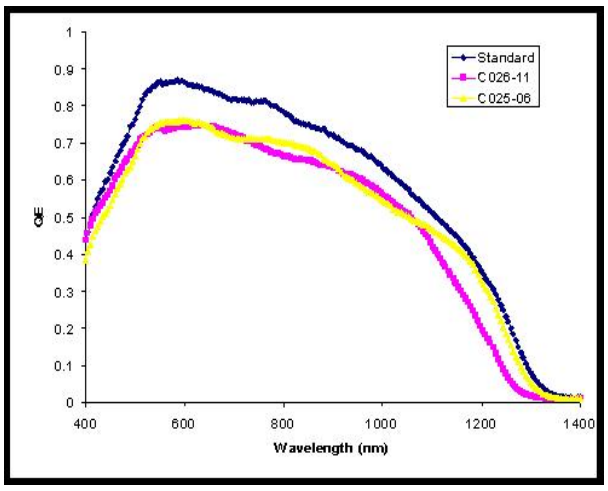


Figure 3. Experimental QE spectra for 2.0(Standard), 1.5(CO25) and 1.0(CO26) micron thick CIGS devices.

We attribute the apparent bandgap shift to the fabrication procedure and resulting structure of our devices. The precursor layers are deposited in the order Cu, Ga, In/Se. Most of the Ga that we deposit ends up outside of the space charge region and contributes to bandgap widening at the rear. We speculate then that as we decrease the CIGS thickness, although the Ga level has been reduced proportionately as well, more of the Ga is "forced into" the space charge layer. This increases the bandgap there which of course results in shifting of the QE spectrum. In our standard two micron thick devices we are able to increase the band gap by depositing more Ga. The effect on Jsc that results from increasing the Ga level and hence the bandgap is shown in Fig. 4. The curve labeled "Ideal" represents the ideal case for which Jsc is only affected by bandgap changes. The additional losses in Jsc over and above band gap induced losses are due to recombination. Increasing recombination with increasing Ga level is due to improperly bonded Ga that produces defects. Others have also reported shifts in bandgap with reduced thickness, although different mechanisms may be operable [8]. Whether such shifts occur depends upon all details of the fabrication process.

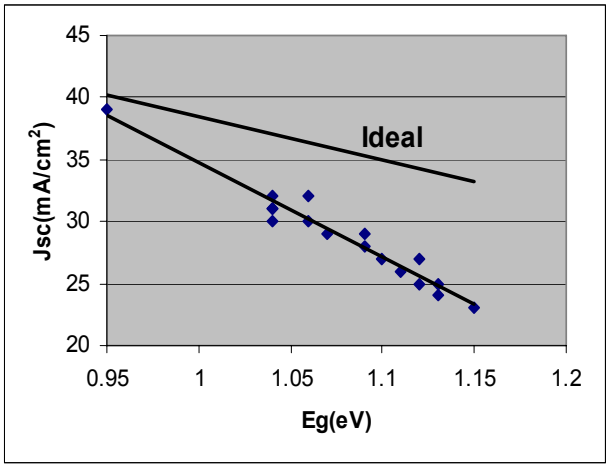


Figure 4. Jsc versus bandgap data ♦ and ideal theoretical curve assuming only bandgap adjustments.

To discuss the additional properties of thinner devices we refer first to Table 1. The simulations indicate a drop in current largely due to absorption losses and a modest increase in voltage and FF. In Fig. 5 we show data for the dependence of bandgap and Voc on thickness. The bandgap is determined from extrapolation of the tails of the QE spectra. While they need further adjustment for absorption losses and thus somewhat overestimate the bandgap, the trend is clear. The observed increase in Voc also supports the bandgap change in that from AMPS we expect a 13 mV increase at 1.0 micron, while the data indicates 20 – 30 mV increase. As can be seen in Fig. 5, Voc drops off dramatically at 0.65 microns. This is due to excessive Ga entering the space charge layer. Accompanying the properly bonded Ga are Ga defects that eventually overcome the effect of increasing bandgap on Voc. The open data points in the figure are initial efforts to modify other process parameters to compensate for the thickness induced changes. As seen, we are having some success, particularly with the thinnest devices.

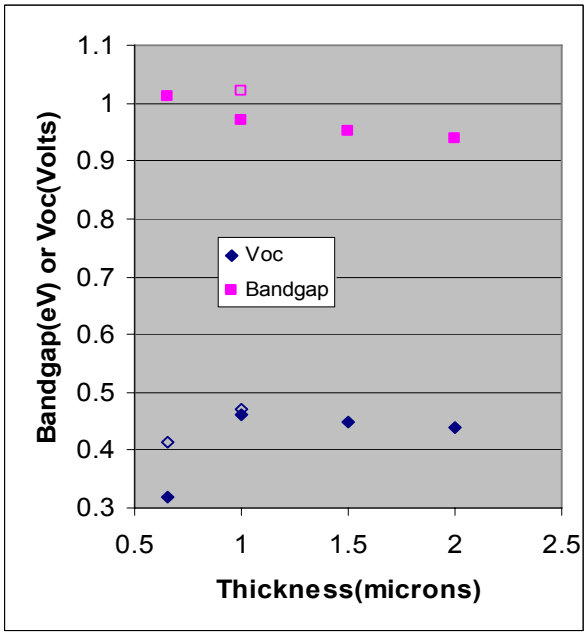


Figure 5. Bandgap and Voc dependence on CIGS thickness. Solid symbols are for our standard process. Open symbols are for a modified process.

In Fig. 6 we show the data for Jsc versus thickness. The dashed line is the AMPS simulated Jsc behavior that is driven predominately by absorption losses. As can be seen, the drop in the device is much stronger than expected from absorption. This is due to two factors: expected losses due to the bandgap shift and losses due to increasing Ga induced defects as the thickness Is decreased. The biggest loss is due to the downshift in the QE spectrum. Our analysis indicates that this is interface induced, and so we have to take corrective measures. The open data point in the plot is the result of adjusting the Se/anneal profile. As seen, we are now at the expected Jsc level, although a bit higher than would be expected because this device has a larger bandgap than the simulation. Referring back to Table 1 AMPS predicts that our performance should be better at smaller CIGS thickness. While our Voc's have increased more than expected due to the bandgap shift, initial Jsc's have been correspondingly lower. However, our most recent data suggests that we can fix the current losses, and thus we expect to achieve comparable, if not better performance than the standard 2 microns from our thinner devices with further work.

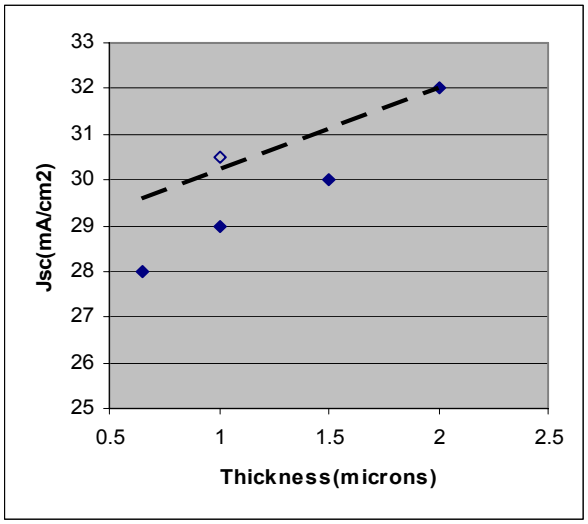


Figure 6. Jsc data versus CIGS thickness. Dashed line is simulated Jsc just assuming absorption losses.

3.0 P-TYPE ZnO

3.1 Background

The performance of CIGS solar cells is strongly dependent upon each layer in the stack, and this is no less the case for the ZnO layers. While the ZnO:Al layer properties are relatively easy to attain and maintain, the undoped ZnO(i-ZnO) layer properties remain sensitive to the nuances of the deposition process. We have over time worked on ZnO to both understand its role and improve its performance and have had reasonable success with ZnO/CIGS structures, particularly with Jsc[9]. These efforts have taught us that the i-ZnO layer plays a strong role in performance and that we don't understand its role very well. As seen in Table 2 we know that thickness is important. In particular we observe the need to tradeoff parameters to optimize efficiency. It is also clear that the defect structure in the i-ZnO layer plays a critical role in its properties and on the influence of those properties on device performance. This is illustrated in Table 3 which shows the parametric dependence on oxygen partial pressure during sputtering of the i-ZnO layer. The tradeoff between Jsc and Voc that occurs has been observed on an ongoing basis throughout this project. We have provided explanations in terms of defect structure at the interfaces [10], an important issue that has implications to bottom-line performance of our devices. This well be discussed further in the next section. What is of interest here is to set the stage for development of p-type ZnO. Since it is clear that the defect structure of i-ZnO is playing a strong role, one might expect that the resulting nature and level of doping in i-ZnO is an important component of the observed effects. Native defects are thus determining the resistivity of the i-ZnO. It might be the case then that adding p-type dopants might lead to improved resistivity and performance. To this end we undertook the development of p-type ZnO. There were already encouraging reports in the literature, though these were met with some skepticism. The reality of p-type ZnO seems to be on sounder footing now, including reports of p,n ZnO homojunctions[11].

Table 2. Dependence of CIGS performance on i-ZnO thickness.

Sample No	Thickness of i-ZnO (Å)	Voc (mV)	Jsc (mA/cm^2)	Fill Factor (%)
C015	300	420	28	52
C016	440	350	35	47
C021	380	440	34	62

Table3. Dependence of CIGS performance on oxygen partial pressure during sputtering of the i-ZnO layer.

Sample No	Oxygen Partial Pressure (mTorr)	Voc (mV)	Jsc (mA/cm^2)	Fill Factor (%)
C013	0.3	450	26	60
C015	0.4	420	28	52
C017	0.5	370	30	57

3.2 Experimental

The Zinc Oxide films discussed in this section were deposited using RF magnetron sputtering. The films were deposited at substrate temperatures ranging from 200C to 400 C with the base pressure values ranging from 2 to 4 µ-Torr. The other deposition conditions such as the partial pressures of oxygen and nitrogen are variables. A Dektak 3030ST auto/surface texture profiler was used to measure the thickness of the samples. The sheet resistance of the ZnO films was determined using a four point probe. The values for carrier concentration and the mobility were obtained using Keithley 900 series Hall equipment. Optical characterization was performed using transmission/absorption spectroscopy. The presence of nitrogen in the films was substantiated by the data obtained from the EDS analysis using a Hitachi S-800T EDAX analysis system.

Undoped zinc oxide films are n-type due to the presence of Zn interstitials and oxygen vacancies. A 99.999 % pure ZnO target used for this purpose was RF sputtered. The substrate temperature was maintained at 491C. The sputtering gas, argon, was maintained at a pressure of 5mT throughout the process. The typical thickness of these films was around 1900Å. Optical measurements show that these films are highly transparent with a transmittance of 90 % in the visible wavelength range. The bandgap of these films was 3.2 eV. Hall measurements confirm the films to be n-type with a resistivity of 1.9 x 10-1 Ω-cm. The values for mobility and carrier concentration were found to be 4.3 x 10-1 cm2/V-s and 7.3 x 1018 /cm3 respectively. This high value of conductivity is due to native defects. The resistivity can be significantly increased by providing an oxygen sputtering ambient. Doping was accomplished by using a ZnO:Al target for n-type films and N for p-type.

3.3 Results and Discussion

3.3.1 Co-doping Using Aluminum

Co-doping is the process of adding acceptor impurities in the presence of donor impurities. The presence of donor impurities decreases the binding energy of the dopant thus improving the incorporation of the acceptor impurity [12]. An aluminum doped ZnO target with 2 wt% AlO was used for this purpose. The substrate temperature was maintained at 411C, and the target was sputtered at an rf power of 60 W. The sputtering pressure was constantly maintained at 5mT throughout the period of deposition. These conditions hold good for all the samples discussed in this section. Table 4 shows the data obtained from the four point probe and hall measurements for ZnO:Al films deposited at various partial pressures of nitrogen. From the table, it can be seen that the resistivity of the ZnO:Al films increased with the introduction of 1mT of nitrogen gas in the ambient. A further increase in the partial pressure of nitrogen gas to 1.7mT produced a highly insulating film. This indicates that nitrogen has compensated the Al and suggests that a further increase in the nitrogen partial pressure might result in a shift in the carrier type. In an effort to obtain this, sample no. 4 was deposited at 2 mT of nitrogen partial pressure. No film was obtained on the substrate deposited under this condition. It is apparent that the presence of excited N is etching the film as it grows. Thus it is not possible to deposit films under these conditions with N partial pressures greater than about 1.7 mT.

Table 4. ZnO:Al:N film properties as a function of N partial pressure.

Sample No.	Partial Pressure of N	Substrate Temp. (ºC)	Thickness (Å)	Resistivity Ω - cm	Carrier Type
1	0	411	1500	4.22×10^{-3}	n
2	1	411	1150	0.97×10^{-1}	n
3	1.7	411	500	Not conductive	-
4	2	411	No film		-

3.3.2 Doping in a Zn-Rich Environment

It is also the case that the solubility and incorporation of dopants can be influenced by the chemical potential of the growth environment. Thus we tried making the growing film Zn-rich while doping with N. This was accomplished as follows. A 99.999_ pure ZnO target was sputtered at an rf power of 70 W. The temperature of the substrateswas varied from 200C to 491C, while the sputtering pressure was maintained at 5mT. The initial experiments used a zinc chunk on the ZnO target to provide the Zn- rich environment during the deposition of the films. In another approach excess Zn was supplied by co-sputtering from an adjacent Zn target. The effect on the film properties by the variation in substrate temperature and partial pressure of nitrogen was studied.

Table 5 summarizes the electrical properties. Sample nos. 1 and 2 are the ZnO films obtained when the Zn chunk was used to provide the Zn-rich environment, while sample nos. 3, 4, 5 and 6 represent the results obtained using the dc sputtering of the Zn target. From the table it is seen that the increase in the nitrogen pressure did not have any effect on the thickness of the film in sample nos. 1 and 2. It can also be observed that the increase in the nitrogen pressure in sample no. 2 as compared to sample no. 1 did not result in measurable conductivity. Though the four-point probe and hall measurements did not show any conductivity of these samples, the EDS analysis indicated the presence of nitrogen. The EDS data showed that the increase in nitrogen partial pressure resulted in a decrease in the atomic % of nitrogen.

Table 5. ZnO:N film properties deposited in a Zn-rich sputtering environment.

Sample No.	Partial Pressure of N	Substrate Temp. (ºC)	Deposition Time (Hrs.)	Thick-ness (Å)	Resistivity Ω - cm	Carrier Type	N Atom %
1	0.5	200	4	3300	-	-	4.54
2	1	200	4	3450	-	-	0.48
3	0.5	200	4	4000	-	-	1.10
4	0.5	466	4	1400	1.6×10^{-1}	n	1.28
5	0.5	466	8	1800	1.8×10^{-1}	n/p	0.72
6	0.5	491	4	4500	3.7×10^{-3}	n	1.28

In order to improve the deposition parameters, the zinc chunk was removed from the target and replaced by sputtering from a second sputter gun. The DC power for the Zn metal gun was maintained at lower values of 3 or 4 W in order to reduce the Zn level to acceptable values. This produced a Zn deposition rate of approximately 0.03 Å/N s. From Table 5 it can be seen for sample no. 3 that the ZnO film still remained non-conductive though deposited at the same substrate temperature of 200 ºC (as sample nos. 1 and 2) and at 0.5 mT of nitrogen partial pressure. The profilometer measurements showed an improvement in the thickness distribution of these films. N was successfully incorporated, but it was not electronically active. To help activate it, the substrate temperature was increased from 200C to 466C. As seen in Table 5, an increase in substrate temperature reduced the thickness of the films. This is in agreement with the results obtained by S.S. Lin et al. [13] and K. B. Sundaram et al. [14]. In their work, it was stated that at low substrate temperatures, the adatom mobility of the atoms is low resulting in a low density and highly porous film with rough surfaces. This indicates the possibility of nitrogen getting incorporated in the defective sites in sample nos. 1, 2 and 3 which resulted in nitrogen being electronically inactive. According to the same research groups, when the substrate temperature was increased, the adatom mobility was increased and re-evaporates the poorly combined structure. Thus an increase in the diffusive ability of atoms or molecules with the increase in substrate temperature resulted in the lowering of the deposition rate. Though the deposition rate is affected, the films obtained in these substrates had better crystallinity. But the deficiency of oxygen in these films lead to a non-stoichiometric film. These effects of high temperature on ZnO explain the n-type conductivity of the films deposited at high temperatures (sample nos. 4, 5 and 6). Sample no. 5 was deposited under the same conditions as sample no. 4 except for the deposition time which was doubled. Although this sample showed an unstable carrier type, it was the first hint of p-type conductivity. The thickness of the film increased by just 400 Å, _ and the nitrogen incorporation decreased. This indicated that maintaining the samples at high temperatures for a longer time could have annealed the samples resulting in a further improvement in the stoichiometry of the film.

3.3.3 Doping in an Oxygen- and Zn- Rich Environment

Since the amount of nitrogen was insufficient in compensating for the oxygen vacancies in the previous set of experiments, instead of increasing the nitrogen partial pressure, oxygen gas was introduced into the ambient. The excess oxygen gas is used to suppress the oxygen vacancies acting as hole killers. The other reason for introducing oxygen and not increasing the nitrogen partial pressure was to avoid etching. In this set of experiments, ZnO films were deposited under different nitrogen and oxygen partial pressures. Argon used as the sputtering gas was varied to maintain the total sputtering pressure at a constant value of 5mT. Table 6 includes the electrical properties obtained from the Hall and four-point probe measurements. The films

Table 6. Dependence of ZnO:N properties on N_2 and O_2 partial pressures(PP).

Samp. No.	PP O_2 (mT)	PP N_2 (mT)	Thick-ness (Å)	Carrier Conc. (/cm^3)	Mobility (cm^2/V-s)	Resist Hall Ω-cm	ivity 4 pt. Ω-cm	Carrier Type
1	0.2	0.5	1700	7.2e17	4.9	2.1	1.8	n/p
2	0.3	0.5	1000	5.6e18	.23	2.2	3.2	n
3	0.5	0.5	700	7.2e18	.46	2.1	3.7	n
4	0.6	0.5	650	1.6e19	.52	0.95	0.79	n
5	0.3	0.8	700	4.0e16	.12	-	3.4e2	p

deposited at an ambience of 0.2 mT of oxygen and 0.5 mT of nitrogen (S.no. 1) showed an n-type resistivity of 2.1 Ω- cm with a mobility of 4.9 cm2/V-s and a carrier concentration of 7.2x1017/cm3. The Hall measurements showed an inconsistent value for the carrier type. This could be due to the fact that the amount of oxygen introduced in the deposition environment was insufficient to compensate for the oxygen vacancies in the films. A rise in the partial pressure of oxygen was expected to increase the amount of compensation in the films. The film thickness and carrier concentration were found to be affected by this variation in the partial pressure of oxygen, although the carrier type still remained the same. It is apparent that excess O supresses film growth as does excess N, though the effect of O is much less dramatic.

Since sample no. 1 in Table 6 indicates some p-type tendencies in the Hall measurements, it was decided to further explore these deposition conditions. A ZnO:N film deposited at 0.3mT of oxygen and 0.8mT of nitrogen produced a film with a thickness of 700 Å. The Hall measurements found the film to be p-type. The best resistivity obtained with these films was 3.4E2 Ω- cm. The carrier concentration of these films was 4.0x1016 /cm3 with a value of 0.12 cm2 /V-s for mobility. The carrier type appeared stable, and thus this film demonstrated p-type behavior for the first time. In addition to having achieved our primary objective, it is clear that we have developed significant understanding of the dependence of doped ZnO on deposition conditions. Were the project to have continued at a sustainable level we would have gone on to apply this understanding to deposition on CIGS as well as to other device structures. Perhaps other opportunities will arise to do so.

4.0 PERFORMANCE LIMITATIONS

In the process of studying the effect of Na on CIGS device performance the oft-observed trade-off between Voc and Jsc was observed once again. The accumulation of experience with this issue over time combined with new insights provided by the Na studies lead to a realization regarding device performance limitations. The Na results were presented at the 31st IEEE PVSC, reference [15]. In this study we were changing the properties of the Mo layer to influence Na access to the growing CIGS layer. In one experiment we varied the Mo deposition rate which is known to affect Mo density which would in turn affect migration of Na through the Mo layer. In Fig. 7 we show the effect of the Mo deposition rate on Jsc and Voc. As the rate increases Mo densifies letting in less Na. This causes an increase in Jsc but a trade-off with a dropping Voc. (The open data points are for a different target voltage than the solid data points and are not relevant to the discussion.)

While continuing to add to our experimental data set through such experiments we have also been attempting simulations of our suggested mechanisms in AMPS. Using the model of Na catalyzed oxidation of VSe donor defects[15] in AMPS we observe good consistency with experimental results. To reiterate the major aspects of our proposed model: VCu ‘s are the primary acceptor states that are shallow enough to be completely ionized under most

conditions. While effects due to (MCu + 2VCu) defect pairs can also be operative[16], we propose that VSe donor defects play a significant role with respect to Na. These are oxidized to acceptor-like states in the presence of Na. The net compensation among these determines the location of the Fermi energy and performance. These compensation effects seem to be most influential in the top surface region of devices. In Fig. 8 we show the AMPS simulated effect on device performance of the presence of donor defects in the surface region. The defect is located at Ec – 0.08 eV to simulate VSe's[15]. As can be seen, lowering of the defect density helps Voc, but at the expense of Jsc, in good agreement with the experimental results presented above. The net effect at the performance level, however, is "pinning" of the efficiency at the 14% level. This is commonly observed in our data, and now we understand that such observations and limitations to performance may be attributable to substrate properties and the influence of those properties on Na migration. We have also seen similar behavior at the junction interface attributable to Ga-based defects. Thus it seems that our devices are predominantly controlled by interface properties. We have demonstrated through numerous experiments that we can attain good bulk properties. However, it is clear that control of the junction interface with our kinetics plus thermodynamics driven growth process has not yet been mastered. The understanding that we have developed over the course of these projects has not led us to a fundamental cause of this problem, so the expectation remains that with further effort it can be solved.

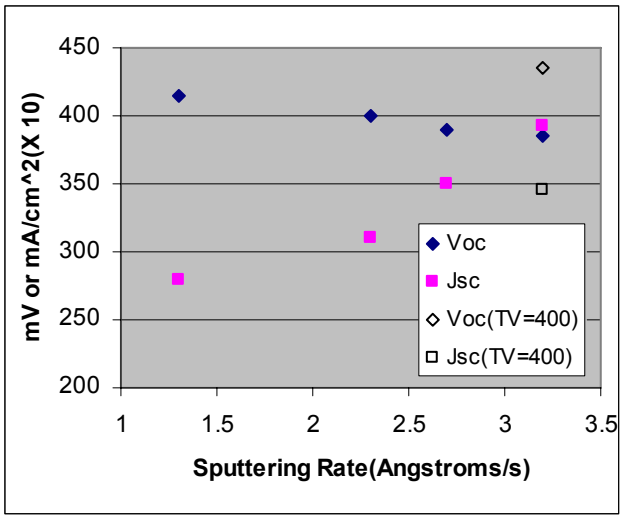


Fig. 7. Effect of Mo sputtering rate on Voc and Jsc.

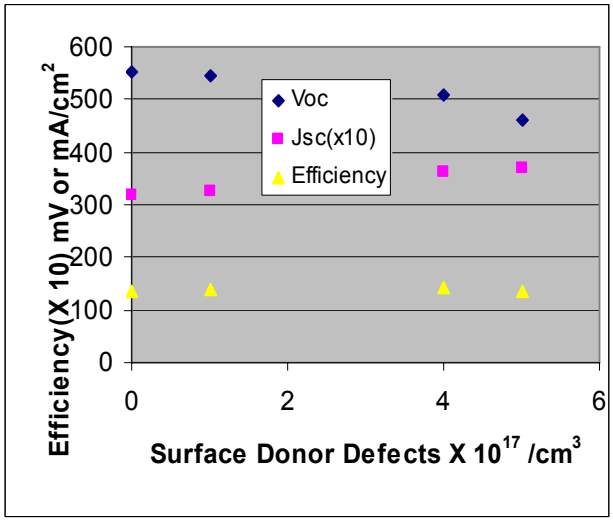


Fig. 8. AMPS simulation of Voc, Jsc and Efficiency as a function of surface layer donor defect density.

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1. "The Structural and Electrical Properties of Zn-Sn-O Buffer Layers and their Effect on CdTe Solar Cell Performance", accepted for presentation at the E-MRS Conference, May, 2006, Nice, France

2. "An Effective Method of Cu Incorporation in CdTe Solar Cells for Improved Stability", accepted for presentation at the E-MRS Conference, May, 2006, Nice, France

3. "Photoluminescence studies of CdTe films and Junctions", accepted for presentation at the E-MRS Conference, May, 2006, Nice, France

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2. *"PL Studies of CdTe Films and Junctions"*, CdTe Team Meeting, March, 2006, Golden, CO

3. *"CdS:Cu and "Buffer" Layers"*, CdTe Team Meeting, May, 2005, Golden, CO

4. *"$CdCl_2$ HT of First Solar's CdTe"*, CdTe Team Meeting, February, 2004, Toledo, OH

5. *"Characterization of First Solar Devices by CSU – IEC – USF"*, CdTe Team Meeting, February, 2004, Toledo, OH

6. *"Defects-Based Simulations in CIGS Including Na"*, CIS Team Meeting, November, 2003

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9. *"$CdCl_2$ Heat Treatment for High Throughput Processing"*, CdTe Team Meeting, July, 2003, Golden, CO

10. *"Defect-Based Simulations in CIGS Devices"*, CIS Team Meeting, January, 2003

11. *"Buffer Layer Mechanisms in CIGS Devices"*, CIS Team Meeting, January, 2003