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CdTe contacts for CdTe/CdS solar cells: effect of Cu thickness, surface preparation and recontacting on device performance and stability

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Abstract

Device performance of thin film CdTe/CdS solar cells having different methods for fabricating the primary back contact are presented. Wet and dry methods for forming the primary contact (Cu_2Te) were evaluated with Cu layers from 0 to 15 nm. Extensive analysis of J–V curves is presented, including effects of temperature, intensity and accelerated stress. A procedure for recontacting stress-degraded cells allowed separation of contact and junction degradation modes. The junction recombination is shown to be a Shockley–Read–Hall mechanism. Stress increases the recombination current density J_0 by 2–3 orders of magnitude, resulting in a loss in V_{oc} of 100–200 mV which is not restored with recontacting. Rollover is eliminated by recontacting the device while fill factor is partially restored with recontacting. For devices with a Cu layer, no significant differences in illuminated solar cell performance between the wet and dry process were observed before or after stress, but there were large differences in the dark J–V related to a blocking contact. To first order, unstressed devices without Cu contact layers behave similar to stressed devices with Cu; lower V_{oc}, higher resistance, and appearance of a blocking contact.

Keywords: Cadmium telluride; Solar cells; Current voltage analysis; Stability; Back contact

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1. Introduction

Thin film CdTe/CdS technology has established itself as a strong candidate for producing large area solar electric modules with high throughput and good efficiency. Small area devices ($\sim$1 cm^2) with over 16% efficiency and large area modules ($\sim$0.86 m^2) with 10.5% efficiency have been reported [1], along with stable outdoor module performance over periods of years [2–4]. However, there are numerous reports in the literature of degradation in performance under conditions of accelerated "stress" testing at elevated temperature (60–100 °C) with cells either under illumination at open circuit voltage (V_{oc}) or in the dark [5–14]. Degradation in device performance is typically due to a decrease in open circuit voltage (V_{oc}) and fill factor (FF) which are, in turn, related to an increase in recombination and series resistance and formation of a blocking back contact. Most of these studies indicate that contact processing and materials, especially Cu, play a critical role in the stability (e.g. Refs. [7,10,11]). There seems to be evidence that Cu moves from the back contact to the front CdS layer and junction region during stress [12,14,15] but Cu concentration in the bulk CdTe does not increase appreciably. There is speculation that the Cu moves along CdTe grain boundaries [10,12]. The electrical bias during stress can have a critical role [5–7,10,11], with stress at forward bias such as V_{oc} or beyond being most severe. Phenomenological models invoking Cu^+ ion motion have been proposed but they fail to fully account for the bias dependence [10,16]. At present, there is no universal explanation of degradation or why it varies significantly with contact processing.

Others have attempted to vary the influence of Cu on initial and stressed performance by changing the concentration of Cu in the graphite ink contact, or the thickness of a ZnTe:Cu contact, but the effect of these changes in Cu on the actual Cu available, at the contact, or in the CdTe, is ambiguous. Therefore, we established a contact fabrication process which allowed us to separate and control various aspects of the contact process, such as removing oxides on the CdTe surface, forming of the Te layer, applying Cu and reacting it to form Cu–Te alloys, and forming a robust current carrying contact. We separate these features into the primary and secondary contacts. The primary contact contains Cu–Te alloys and makes intimate contact to the CdTe. The secondary contact is typically a thick layer of C, Mo, Ni or Al and carries the current to the external connections.

Previously, we reported the accelerated stressing of devices with contacts containing a Cu layer under various temperatures, voltage bias and light conditions, focusing on J–V performance of one type of contact [10]. In this paper, we limit the stressing conditions to bias at V_{oc} under illumination at 100 °C but explore a much wider range of contacts, measurements and analysis. We focus on analysis of the junction and the series resistance, since their properties directly influence V_{oc} and FF.

2. Experimental procedures

2.1. Contacting (wet, dry, primary, secondary, Cu–Te formation)

The contact process is described in greater detail elsewhere [17,18]. It consists of four steps following the $CdCl_2$ treatment in air: (1) chemical removal of deleterious

surface oxide residues; (2) formation of Te excess; (3) deposition of Cu and reaction with Te to form the primary contact; and (4) deposition of the secondary contact to serve as the current carrying conductor. Two approaches, based on wet (chemical) and dry (vapor) chemical reactions, were employed for the surface preparation and Te layer formation. The wet process used a three-step sequential reaction of the CdTe film in bromine–methanol, aqueous dichromate, and hydrazine (BDH). Bromine methanol removes surface residues and a thin layer of CdTe, leaving a terminating layer of Te ~2 nm thick. The dichromate solution produces a considerable Te oxide layer, which is then converted to a 30-nm-thick Te layer by reaction in hydrazine. The dichromate and hydrazine steps are extremely penetrating especially along grain boundaries. Thus, the time in these liquids depends on the CdTe thickness and grain size and is a critical process parameter. The solutions and conditions used for 4–5-μm-thick CdTe are as follows:

bromine-methanol: 0.15 g Br_2 in 100 cc CH_3OH; 25 °C; 5–10 s
dichromate: Fisher-brand Dichrol used at full strength; 25 °C; 1 s
hydrazine: 98% N_2H_4 in H_2O; 40 °C, 60 s

The dry vapor process achieves a similar result by reaction of the CdTe surface in H_2 and Te vapor at a total pressure of 1 atm. The gas phase composition is controlled by flowing 4% H_2 in Ar through a reactor in which the CdTe film is suspended directly over a Te source heated to 380 °C, which establishes a Te partial pressure of ~2 m Torr. The reaction is carried out for 1–2 min, during which the CdTe temperature reaches 180–200 °C. A Te layer ~10 nm thick is formed on the CdTe surface. This process is not considered to be penetrating, is independent of CdTe thickness and grain size, and, thus, the same process has been used on CdTe films with thickness from 1.3 to 7 μm.

For both wet and dry processes, the primary contact is completed by deposition of Cu layers from 2 to 15 nm thick by electron beam evaporation and in situ treatment at 200 °C for 30 min.

A brief summary of measurements with fixed incident beam X-ray diffraction of CdTe films at different stages of primary contact processing showed the predominant surface residue after $CdCl_2$:O_2 treatment is CdO; wet and dry processes leave elemental Te; and, Cu–Te phases obtained depend on Cu to Te ratio, in general accordance with the published phase diagram.

The secondary contact for samples in this work was made by application of Acheson 505SS carbon ink followed by a drying step at ~40 °C for 30 min. An alternative approach to expedite processing was deposition of Cu, application of the secondary contact, then treatment at 200 °C for 30 min. Cells areas defined by the graphite contact were ~0.4 cm^2. One significant difference between our C contact process and those developed by others is that we use an undoped C ink while they use a Cu and Hg doped ink. This allows us to control the formation of primary Cu_2Te contact independent of the C secondary contact. It is commonly found that Cu_2Te is correlated with a low contact barrier and good device performance.

We also have applied alternative secondary contacts such as Mo or Ni, deposited by electron beam evaporation immediately after depositing the Cu layer. Those results will be presented elsewhere.

2.2. Device fabrication

The glass/SnO_2/CdS/CdTe plates for these contacting and stress studies were processed in a commercial-scale system [19]. All devices discussed in this subsection were processed from the same CdS/CdTe module. Devices on other plates yielded similar results. CdS/CdTe solar cells were fabricated using the wet process or the dry process prior to evaporation of Cu layers from 2 to 15 nm thick. Following the Cu evaporation, C ink was applied, and the completed device was heated for 30 min at 200 °C in air to dry the ink and to form the Cu_2Te layer. Contact to the SnO_2 was made with In solder. After receiving contact processing at IEC, typical device J–V parameters were $V_{oc} = 0.80$–0.82 V, $J_{sc} = 18$–20 mA/cm^2, FF = 68–70%, and efficiencies = 10–11%.

2.3. J–V measurements and analysis

J–V characteristics were measured at 28 °C in light and dark using an Oriel brand AM1.5 G solar simulator calibrated to 100 mW/cm^2, and as a function of temperature from −50 to 80 °C at several intensities with GE-ELH-type lamps. The data were analyzed as described below.

Device analysis followed the procedure given elsewhere [20]. The basic diode relation is

$$J = J_D - J_L = J_0 \exp[(qV_J/AkT) - 1] - J_L + GV \quad (1)$$

with

$$J_0 = J_{00} \exp(-\phi/AkT), \quad (2)$$

where J_D is the diode current, J_L is the light generated current ($J_L \sim J_{sc}$ where J_{sc} is the short circuit current), J_{00} is the recombination current density, ϕ is the barrier height and A is the diode factor. ϕ/A is the activation energy for the recombination mechanism. In fact, J_L can be a function of voltage due to field-dependent drift collection $J_L(V)$ as discussed later, but does not seriously impact use of Eqs. (2) or (4). We only analyzed devices where the dark shunt conductance G was negligible, $G < 1$ mS/cm^2, thus we ignore the GV term. For Shockley–Read–Hall (SRH) recombination at midgap states, $\phi = E_G$ which is the bandgap of the absorber region where the recombination is occurring, and $A \sim 2$. More generally, it is found that $\phi = E_G$ and $1.3 < A < 2$ for many other polycrystalline and amorphous heterojunction thin film solar cells [20]. The external voltage V is related to the actual voltage across the internal junction V_J by correcting for the series resistance losses as

$$V_J = V - (JR_S), \quad (3)$$

where R_S is the lumped series resistance.

From Eqs. (1) and (2), the open circuit voltage V_{oc} is when $J = 0$ or

$$V_{oc} = AkT/q[1\log(J_L/J_0] = \phi/q - AkT/q\log(J_{00}/J_L). \quad (4)$$

From Eqs. (1) and (3), the derivative dV/dJ is

$$dV/dJ = R_S + AkT/[q(J + J_L)]. \quad (5)$$

Data were analyzed by plotting V_{oc} vs. T, whose intercept gives ϕ/q; by plotting $\log(J_{sc})$ vs. V_{oc} (in the light) or $\log(J)$ vs. V_J (from the dark) whose intercept gives J_0 and slope gives A, and by plotting dV/dJ vs. $1/(J + J_L)$ whose intercept give R_S and slope gives A.

2.4. Accelerated stress conditions

Unless otherwise noted, the devices were stressed at conditions of 100 °C, in room air, under ~1 sun illumination from 100 W spotlights, at open circuit bias, for 10 days. The effect of stressing similar devices under different bias and dark conditions was reported elsewhere [10,18].

3. Stress of partially completed devices and recontacted devices

Since it is widely reported that fully completed CdS/CdTe/Cu/contact device structures degrade under accelerated stress, it was decided to investigate at what point in the device fabrication that degradation became operable. Was it inherent in the CdS/CdTe semiconductor layers? Did it occur only after the Cu layer was deposited? Could it be eliminated with a second application of a new Cu layer after initial stressing with the first layer? We sought to answer these questions by stressing partially completed devices, then completing their fabrication and testing them. Contacts were removed or otherwise reapplied after stress in some cases.

We stressed CdS/CdTe structures without any contact under the same conditions as used to stress devices. After these incomplete devices were stressed at open circuit at 100 °C for 10 days, they received either wet or dry contact processing, then application of Cu and C layers to complete the devices. When tested, they had J–V characteristics comparable to unstressed (as-deposited) devices; i.e. V_{oc}~0.80 V and FF~70%. CdS/CdTe structures were also stressed having a 6 nm Cu layer but *no C contact* at 100 °C. After stress, some of these devices received a second Cu layer while all received the C contact. The completed devices had V_{oc}~0.65 V and FF~60%, including those with the double Cu layer. Subsequent restressing of these completed devices resulted in no further loss in V_{oc}, but they did exhibit a loss in FF and the appearance of a current limiting blocking contact.

We developed a method to remove the C contact after stress and reapply fresh C in order to separate contact and junction behavior. A CdS/CdTe solar cell with the wet process and 15 nm Cu, having an initial efficiency of 11.8% and V_{oc} of 0.82 V, was stressed at open circuit at 100 °C for 6 weeks in air at 2 suns [21]. This reduced the efficiency to 7.2% and V_{oc} to 0.73 V. J–V results and diode parameters are given in

Table 1
Cell performance measured in initial, stressed and recontacted states of device in Figs. 1 and 2

Condition	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Eff. (%)	R_{oc} (Ω cm^2)	J_0 (mA/cm^2)	A
Initial	0.82	19.6	73	11.8	4.4	3E-8	1.6
Stressed	0.73	18.4	54	7.2	20.2	8E-7	1.6
Recontacted	0.73	19.9	62	9.1	4.7	8E-7	1.6

R_{oc}, J_0 and A determined from analysis of dark J–V curves.

Table 1 for the initial, stressed and recontacted states. Fig. 1 shows light and dark J–V curves in all three states, while Fig. 2 shows log J–V for the three dark curves. After stress, Table 1 and Fig. 2 show that J_0 increased by 30 times with no change in A ($\sim$1.6), suggesting that the magnitude of recombination changes but not the mechanism (bulk recombination). Fig. 1 also shows that curvature develops after stress in both light and dark J–V curves at forward bias, most likely due to a blocking contact. After stressing, the original carbon contact was removed, the CdTe surface was re-etched in weak bromine–methanol, and a new C contact was applied with no additional Cu layer. The efficiency increased to 9.1%, the blocking contact disappeared and the FF increased significantly with no change in V_{oc}, J_0 and A. Together, these experiments suggest that: (1) the CdS/CdTe junction is intrinsically stable; (2) the presence of Cu during stress is correlated with junction (V_{oc}) degradation; (3) reapplying a fresh Cu layer does not immunize the device from further degradation nor does it restore a degraded device; (4) the presence of the secondary contact *during stress* is responsible for contact degradation; and (5) the curvature in forward bias is associated with the back contact.

4. Effect of wet vs. dry process, and Cu thickness (OC stress, 100 °C)

This subsection describes an extensive study of the effect of contact process and Cu thickness. Detailed analysis of J–V curves was performed, including temperature dependence to identify how Cu and stress influence the recombination and diode properties.

4.1. General results of Cu thickness

Figs. 3 and 4 summarize the dependence of V_{oc} and FF on Cu layer thickness before and after stressing for the wet and dry contact processes. Initial performance is very similar for the two processes independent of Cu thickness for Cu $>$ 2 nm. Initial V_{oc} was 0.80 ± 0.02 V and initial FF was 69 ± 2% for all devices except the one without Cu. Note that the device without Cu having the dry contact has the lowest V_{oc} before stressing and the highest V_{oc} after stressing of any device. The two without Cu degraded only 0.04 V compared to $\sim$0.15 V for all the other devices with Cu. Fig. 3 shows that the piece with the wet contact (thicker Te) and thickest Cu layer (15 nm) had the highest V_{oc} after stressing of any device with Cu. Fig. 4 shows

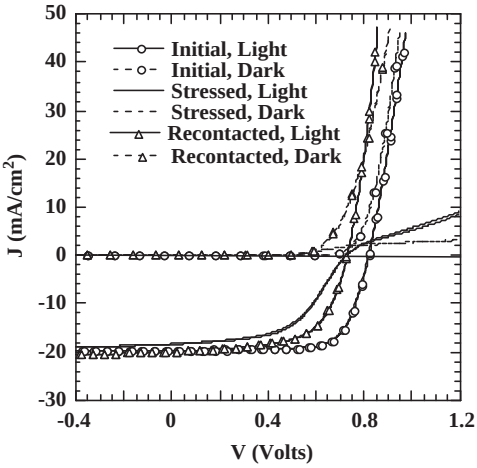

Fig. 1. Light and dark J–V curves for CdS/CdTe device with wet contact and 15 nm Cu: initial, 6-weeks stress at 100 °C and OC; and following recontacting.

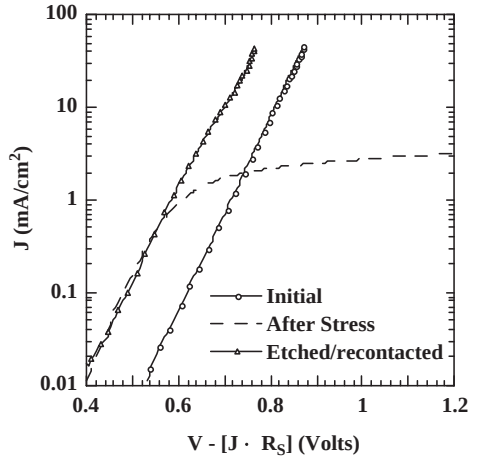

Fig. 2. log J–V of dark curves from Fig. 1 corrected for R_S.

that FF has a 10–20 point decrease with stress. Devices with the wet contact degrade less than those with the dry contact. There is also considerable scatter in the results, especially after stress, from nominally identically processed devices, as shown, e.g. with 15 nm Cu. We believe this is due to the complexity of processing steps and their interaction, and to the multiple degradation mechanisms. Further, we speculate that much of the initial and post-stress results are due to grain boundary activity which would introduce a statistical variation, but these results also demonstrate that, to first order, significant degradation occurs independent of the amount of Cu for both

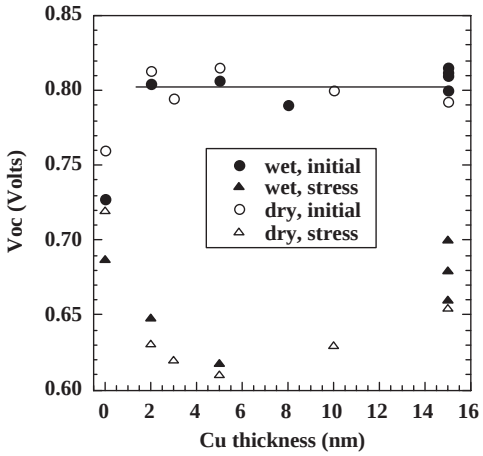

Fig. 3. V_{oc} vs. Cu thickness for devices with wet and dry contact before and after stress at 100 °C in air for 10 days at OC.

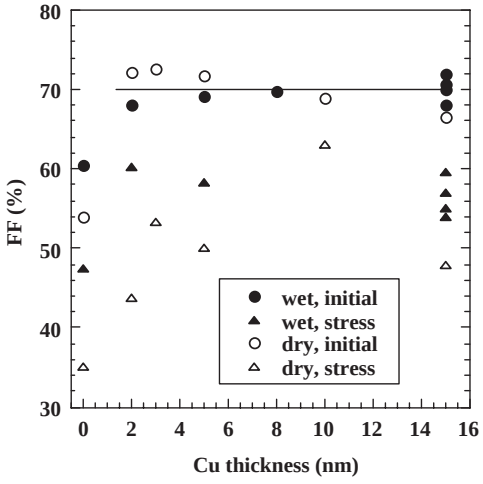

Fig. 4. FF vs. Cu thickness for devices with wet and dry contact before and after stress at 100 °C in air for 10 days at OC.

of the contact processes. Insight into the device behavior which leads to these trends is presented in the following sections based on detailed device analysis.

4.2. Initial J–V performance and analysis

Fig. 5a shows the dark J–V curves of devices having the wet contact process with Cu thicknesses from 0 to 15 nm before any stressing occurred. The dark curves show a clear trend of increasing forward current conduction (i.e. a better diode

characteristic) with increasing Cu. Only the device with Cu = 15 nm has a "normal" highly conducting dark current at forward bias. In contrast, the light J–V curves in Fig. 5b show typical diode behavior for all devices with Cu. Comparing Figs. 5a and b indicates a large light-to-dark crossover (LDXO), where the forward bias diode current in the light is higher than in the dark, for devices with Cu = 0, 2 and 5 nm. The LDXO effect was first reported in Cu_2S/CdS solar cells due to Cu-enhanced photoconductivity of the CdS [22]. Recently, Cu-enhanced photoconductivity was invoked in CdTe/CdS solar cells [12,23]. Figs. 5a and b show the opposite effect, namely the device with the most Cu has essentially no LDXO. More recently, LDXO in CdTe solar cells has been analyzed in terms of minority carrier current flow at the CdTe contact [24,25] which may be a more plausible explanation for this particular dataset.

Fig. 6 shows the light and dark J–V curves for a device having the dry contact with only 2 nm Cu. Also shown are the light and dark J–V curves for the device from Figs. 5a and b with 15 nm Cu and the wet contact. Both have well-formed J–V curves which are essentially identical. Thus, the dry contact process requires much less Cu to achieve an Ohmic contact and high forward current conduction in the dark compared to the wet contact. The present contact process allows exact knowledge of how much Cu is available for contact formation and CdTe doping, in contrast to other methods where the Cu is mixed into a paste which is applied to the CdTe in a thick film and heated. It is important to note that only 2 nm of Cu is sufficient to produce a fully optimized CdTe device. If evenly distributed throughout the 4 μm CdTe layer, this would correspond to a Cu density of 2×10^{16} atoms/cm^3. In reality, much of the Cu is found in the CdS layer and some must remain on the CdTe contact as Cu–Te compounds, indicating the actual amount available for doping the CdTe is much less than the above density.

Fig. 7 plots dV/dJ vs. $1/J$ for the two dark curves in Fig. 6, using Eq. (4) with $J_L = 0$. The data shown spans from $J = 2$ to 50 mA/cm^2. The diode A factors and

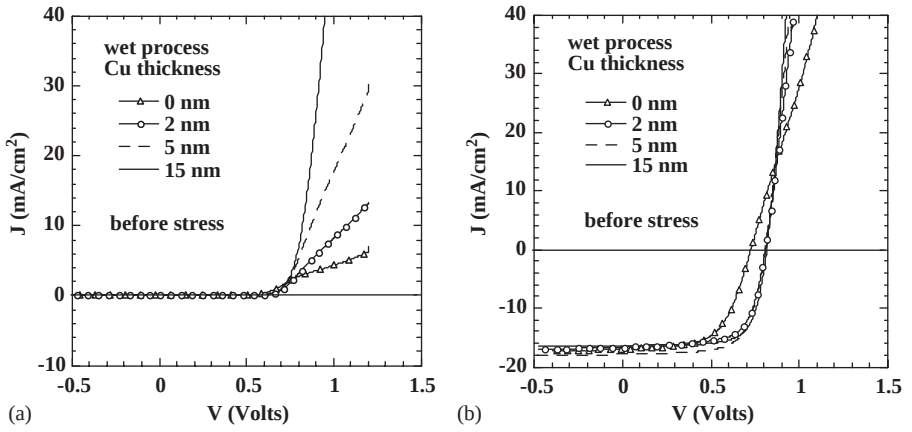

Fig. 5. (a) Dark J–V curves for device with wet contact process before stress. (b) Light J–V curves for device with wet contact process before stress.

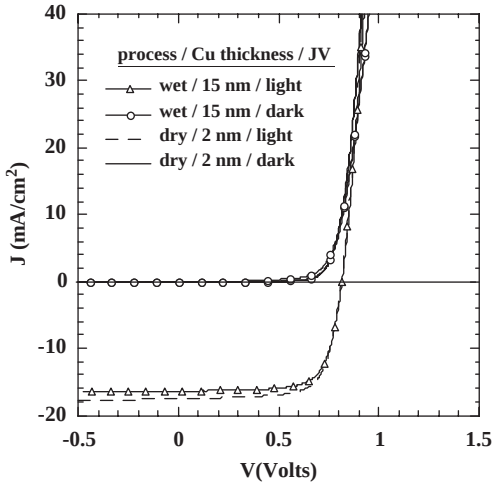

Fig. 6. Light and dark J–V curves for devices with wet (15 nm Cu) and dry (2 nm Cu) contact process.

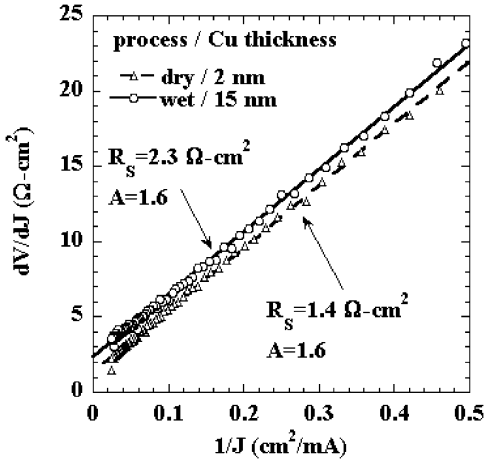

Fig. 7. dV/dJ vs. $1/J$ for dark J–V curves of devices in Fig. 6. Data spans from $J = 2$ to 50 mA/cm^2 in the forward bias region.

series resistances are very similar between the two devices and confirm that, with the appropriate level of Cu at the back contact, equivalent device behavior results with either contact process. Fig. 8 plots $\log J$ vs. $[V-(J \times R_S)]$ for the same two dark curves. The terminal voltage V is corrected for series resistance losses giving the actual voltage across the junction V_J. This "straightens" the data at higher J and allows a better fit to determine A and J_0. Both $\log J$ curves yield nearly the same ideality factor, $A \sim 1.7$, and diode currents, $J_0 \sim 1 \times 10^{-7}$ mA/cm^2. This latter value is 2–6 times larger than that reported for very high efficiency ~14% CdTe devices [26]

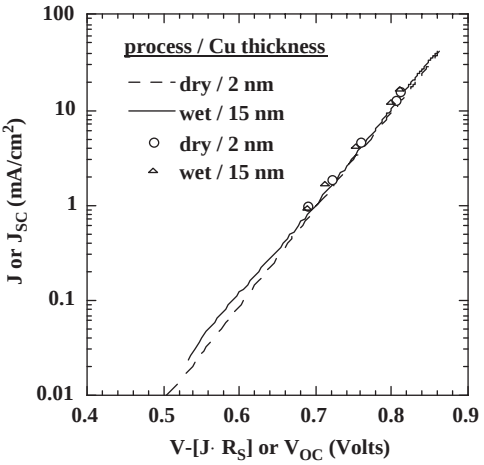

Fig. 8. Lines show $\log(J)$ vs. junction voltage $V-[J \times Rs]$ for dark $J-V$ curves of devices in Fig. 6. Symbols show $\log J_{sc}$ vs. V_{oc} for the same two devices measured at five intensities from 5% to 100%.

but is similar to values reported for devices with comparable efficiency (~10%) [26,27]. The primary conclusion of Figs. 6–8 is that the junction properties and resistance of devices with wet or dry contact processing with Cu are equivalent and similar to those reported in the literature for CdS/CdTe devices of comparable efficiency.

However, some CdTe/CdS devices have very distorted $\log J-V$ curves, even after correction for R_S, especially after stress or without Cu in the contact. It is not possible to analyze $\log J-V$ using the simple series-connected diode-resistor model of Eq. (1). In this case, it is more appropriate to analyze the light $J-V$ characteristic using the intensity dependence of V_{oc} by plotting $\log(J_{sc})$ vs. V_{oc} as from Eq. (3) [28]. Fig. 8 shows $\log J_{sc}$ vs. V_{oc} for the two devices. The A and J_0 values are in Table 2. Note that they are very similar to those from the dark $\log J-V$ analysis. It was not possible to fit the device without Cu using dark $\log J-V$ because of the curvature (Fig. 5a), while $\log J_{sc}$ vs. V_{oc} gave a linear relation allowing determination of A and J_0.

4.3. Temperature dependence of $J-V$ and V_{oc}

To further characterize the device performance, we have measured the $J-V$ curves as a function of temperature. Low-temperature $J-V$ measurements can identify contact-related problems in CdS/CdTe [18,29]. Fig. 9 shows the dark and light $J-V$ before stress for the device with wet contact process and 15 nm Cu at 25 and −30 °C. There is negligible LDXO at 25 °C. At lower temperature, the LDXO becomes very large and even the light $J-V$ curve develops "rollover" beyond V_{oc}. The dark diode failed to conduct even at far forward bias. Similar changes in the $J-V$ curve occurred at lower temperature in all of the devices we studied regardless of their contact

Table 2
Values before and after stress for V_{oc}, ϕ/q, A and J_0 for devices with wet or dry contact, 0, 2 or 15 nm Cu

Contact process	Initial or stress	Cu (nm)	V_{oc} (Volts)	ϕ/q (Volts)	A	J_0 (mA/cm^2)
Wet	Initial	0	0.72	1.23	1.3	5×10^{-9}
	Stress		0.68	1.15	1.3	8×10^{-9}
Wet	Initial	2	0.80	1.45	1.7	1×10^{-7}
	Stress		0.65	1.36	1.9	2×10^{-5}
Dry	Initial	2	0.81	1.52	1.7	1×10^{-7}
	Stress		0.63	1.44	1.8	1×10^{-5}
Dry	Initial	15	0.79	1.47	1.6	7×10^{-8}
	Stress		0.66	1.42	1.9	3×10^{-5}

A and J_0 obtained in the light at 300 K from $\log(J_{sc})$ vs. V_{oc}.

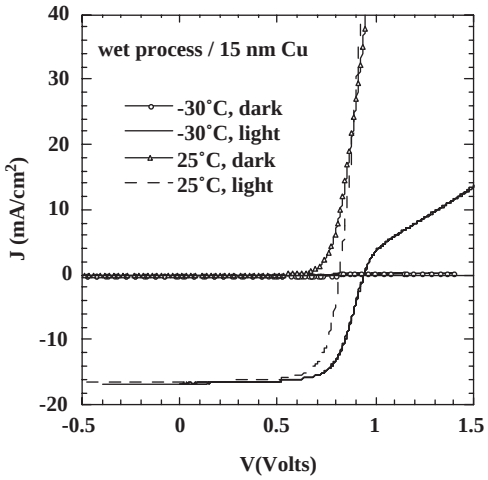

Fig. 9. Light and dark J–V curves at 25 and −30 °C before stress for device with wet contact and 2 nm Cu. Note the dark curve at −30 °C is nearly horizontal even at forward bias >1 V.

process or Cu thickness. In particular, the light J–V characteristic would have a relatively normal shape in the power quadrant but the current is severely restricted beyond V_{oc}. The simplest explanation is that the CdTe contact forms a Schottky barrier in series with the CdS/CdTe junction [18,29], thus become current limiting, or blocking, to holes but other models have been proposed [24,25].

However, blocking contacts will have no effect on V_{oc} at any temperature or intensity because there is no external current flow (providing that the back contact is not photovoltaically active) so we use characterization of V_{oc} to give insight into the device behavior. It is well known that V_{oc} will vary linearly with temperature in an ideal solar cell as given by Eq. (4). Fig. 10 shows V_{oc} vs. T for the two devices with 2 nm Cu along with one having the wet contact with no Cu. All were measured at

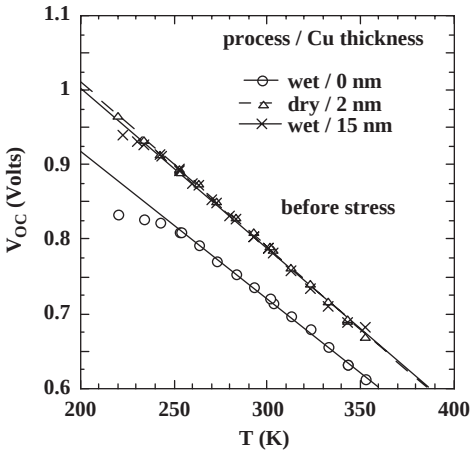

Fig. 10. V_{oc} (1 sun) vs. T before stress for devices with various contact processing.

~1 sun intensity. A linear dependence is seen from 220 to 350 K for the two devices with Cu. Their intercept at $T = 0$ K indicates a barrier height ϕ~1.45–1.50 eV, which is the CdTe bandgap confirming that recombination is governed by space charge recombination in the absorber, but the device without any Cu layer has ϕ~1.2 eV, as listed in Table 2. It also shows that V_{oc} becomes limited at lower T. Fig. 11 shows V_{oc} vs. T for this device without Cu at three intensities. Extrapolation to 0 K has an intercept of ~1.2 eV for all intensities but there is evidence of carrier freeze-out below 250 K, where V_{oc} becomes independent of temperature and light intensity. When there are no longer sufficient free carriers, the quasi-Fermi levels no longer respond to changes in light intensity or temperature. V_{oc} reaches its maximum value of V_{bi} which is determined by the absorber bandgap and the Fermi level of the contacts. V_{oc} then becomes independent of temperature or intensity, violating Eq. (4). Thus, even 2 nm of Cu at the contact is sufficient to establish normal p–n junction behavior. Without Cu, the CdTe behaves as though nearly intrinsic. This suggests the Cu helps to dope the CdTe.

4.4. Post-stress J–V performance and analysis

The devices were exposed to 1 sun illumination at open circuit for 10 days at 100 °C in air to accelerate any degradation mechanisms. Efficiencies decreased from 9–11% to 7–9%. Fig. 12 shows light and dark J–V curves after stress for devices with 2 nm Cu with both wet and dry contact process. For comparison, the initial (pre-stress) light J–V curve for the device with the dry contact is shown. To first order, all devices behave similarly after stress. V_{oc} decreases by 150–200 mV, J_{sc} may decrease slightly due to increased voltage dependence, and FF decreases 5–15%. The LDXO in the first quadrant increases after stress, indicating an increase in photoconductivity of either CdS or CdTe. Weak curvature develops for $V > V_{oc}$

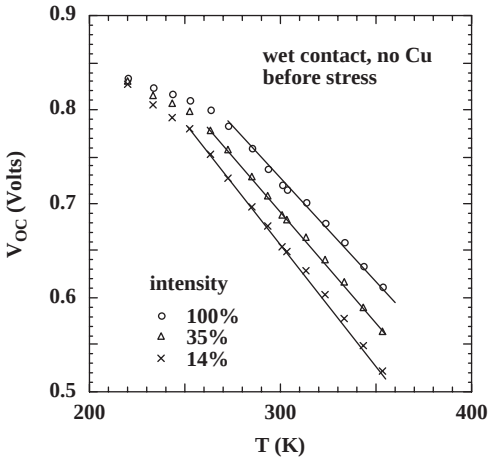

Fig. 11. V_{oc} vs. T for device without any Cu layer at three intensities. The solid lines extrapolate to ~1.2 V at $T = 0$.

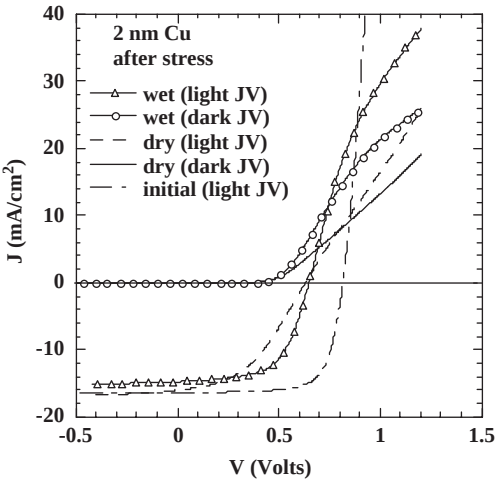

Fig. 12. Light and dark J–V after stress for devices with 2 nm Cu. Typical initial light curve (dry, 2 nm Cu) shown for comparison.

attributed to the back contact as shown in Section 3. These are similar to results reported by others on other CdTe devices with other contacts.

Fig. 13 shows dV/dJ vs. $1/J$ for the dark curves after stress for devices with 2 nm Cu from Fig. 12 and with 15 nm Cu. The data from one of the devices in the unstressed state from Fig. 7 are shown for comparison. This method of examining the J–V data identifies and quantifies changes not immediately obvious in the standard J–V plots. The formation of a blocking contact is clearly indicated in Fig. 13 for the two devices with the wet process contact by the sharp minimum in

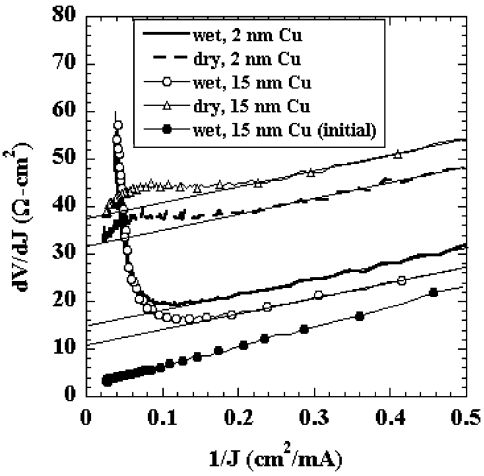

Fig. 13. dV/dJ vs. $1/J$ for the four dark curves after stress for the devices with 2 nm Cu from Fig. 12 and with 15 nm Cu. Data from initial unstressed cell shown for comparison.

dV/dJ for small values of $1/J$ (corresponding to $J > 10\,mA/cm^2$). The intercept of a line fit to the linear portion of the data at higher values of $1/J$ gives R_S, as shown by Eq. (5). This increases from $\sim 2\,\Omega\,cm^2$ for the initial device to 10–15 $\Omega\,cm^2$ for the two devices with the wet contact, to $\sim$30–35 $\Omega\,cm^2$ for the two devices with the dry contact.

Fig. 13 is qualitatively typical of what has been observed for the dark J–V curves of devices made with these contacts on other plates of CdTe. The R_S always increases after stress, and typically increases more for the dry contact. Similar plots for the light J–V tend to show less or no curvature, i.e. less blocking contact, and lower R_S, but they are more difficult to quantitatively analyze due to the complications of voltage dependence [20].

V_{oc} was measured as a function of intensity and temperature after stress, and results from some devices are given in Table 2. Analysis of $\log J_{sc}$ vs. V_{oc}, shown in Fig. 14 before and after stress, indicated that for devices with Cu, the A factor increased slightly, approaching 2, and J_0 increased by about 2 orders of magnitude (Table 2). The device without Cu had the lowest J_0 and A before or after stress, indicating less recombination at deep states and greater resistance to stress.

Fig. 15 shows V_{oc} vs. T after stress for two devices with wet contact process having 0 or 2 nm Cu layer. Also shown are the initial data for the cell with 2 nm Cu. The intercept ϕ/q for the device with Cu decreased from 1.45 to 1.36 V. Comparing Fig. 15 with Fig. 10 shows that the device without Cu has the same shape after stress, just lower values of V_{oc}. Above 280 K, it has higher V_{oc} than the device with Cu, despite having much lower V_{oc} initially (Fig. 10). Fig. 16 shows how ϕ and ϕ/A vary with V_{oc} (298 K) before and after stress for many of the devices in this study from that same CdTe plate. ϕ/A is the effective activation energy for recombination current J_0 (Eq. (4)). The A factor used here was determined from V_{oc} vs. $\log(J_{sc})$ and

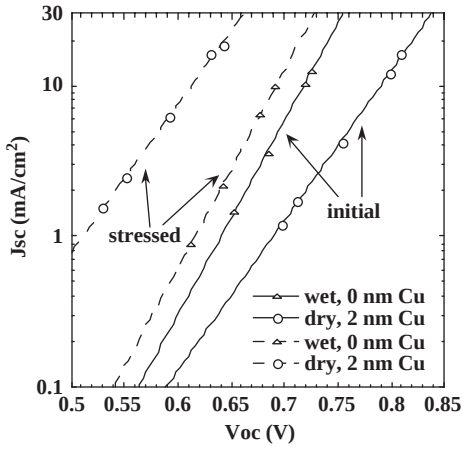

Fig. 14. $\log J_{sc}$ vs. V_{oc} at several intensities before (—) and after (- - -) stress for devices with and without a Cu layer. Slope and intercept were used to determine A and J_0 shown in Table 2.

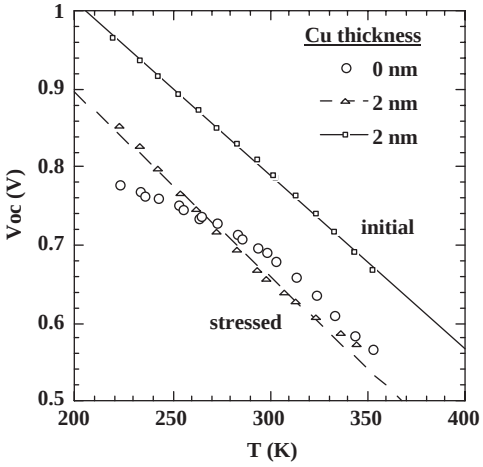

Fig. 15. V_{oc} (1 sun) vs. T for solar cells after stress with wet contact process having 0 or 2 nm Cu layer. Also shown for comparison is initial data for device with 2 nm Cu.

was typically 1.6–1.7 before stress and 1.8–2.0 after stress, as in Table 2. For devices with a Cu layer, ϕ is approximately equal to the CdTe bandgap before and after stress, within the noise of the data. It decreases slightly by 0.05–0.10 eV after stress. Many, but not all, devices that we have examined exhibit this small decrease in ϕ after stress. It is well known that interdiffusion of S and Te in the junction region yields a lower-bandgap CdS_xTe_{1-x} material [30] but this requires temperatures $>400\,^{\circ}C$, greatly exceeding those used in stressing. We do not think that is the reason for the decrease in ϕ. The activation energy decreases from about 0.9–1.0 eV

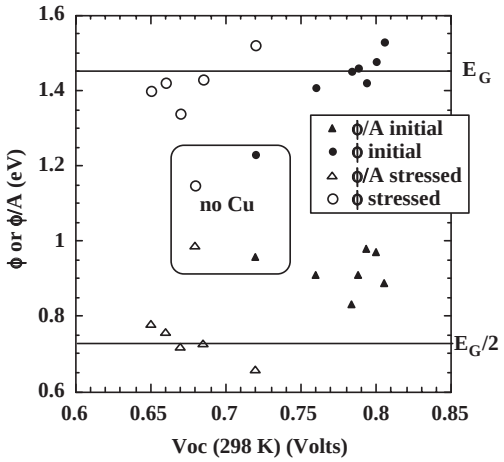

Fig. 16. ϕ and activation energy ϕ/A vs. V_{oc} (298 K) for many devices with Cu layers in this study before and after stress. Data within the box for a device without Cu. Values of E_G and $E_G/2$ are shown for comparison.

before stress to 0.7–0.8 eV after stress, suggesting that the CdTe Fermi level has moved towards midgap after stress for all the devices with Cu. This is due to the A factor approaching 2, also an indication of stronger midgap recombination. However, note that ϕ and ϕ/A for the device without Cu have a different dependence on V_{oc} and on stress. The effective activation energy is deeper after stress than for cells with a Cu layer. The devices without Cu may have different recombination mechanisms.

4.5. Effect of back contact process without Cu layer

Since devices without Cu have lower efficiency and degrade differently, and less, than those with Cu, further studies were performed to characterize the degradation of devices without any Cu layer in the back contact. We hesitate to call them "Cu-free" devices since Cu has been reported, especially in the CdS, of uncontacted devices with no intentional Cu [12,14,15]. Devices were fabricated from the same CdS/CdTe plate as those previously described and were processed without any intentional Cu layer. Some had the wet contact with BDH etch, some had only the Br-methanol step (labeled "wet, no BDH"), and some had the dry contact. Following the surface treatment, the devices received the C ink contact without a Cu layer. Initial J–V performance, shown in Fig. 17, of the devices without Cu with different CdTe surface preparation were comparable with $V_{oc}\sim0.74$ V and FF$\sim$58%. Note that they all had some LDXO despite having no intentional Cu layer, implying the LDXO is not always due to Cu-doped CdS photoconductivity. J–V performance after stressing is shown in Fig. 18. They had comparable $V_{oc}\sim0.68$ V but very different FF (47% with BDH etch and $<$28% without BDH etch). The FF is correlated to the curvature around V_{oc}. After stressing, the slope at open circuit, R_{oc},

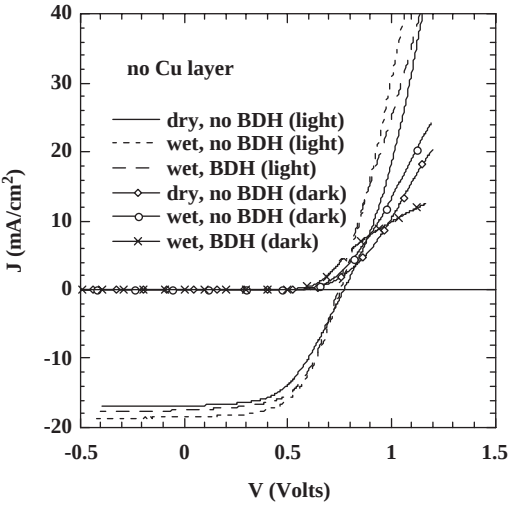

Fig. 17. Initial light J–V curves for devices with no Cu layer in the contact having different CdTe surface treatments prior to C secondary contact.

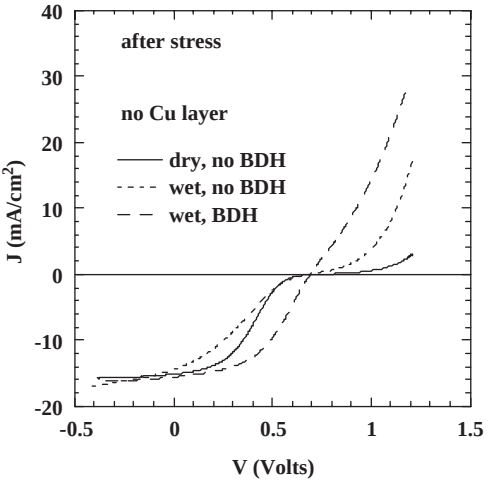

Fig. 18. Light J–V curves after stress for same devices as in Fig. 17.

was $\sim 20\,\Omega\,\mathrm{cm}^2$ for the device with BDH etch but $>200\,\Omega\,\mathrm{cm}^2$ for the devices without BDH etch, independent of whether they had wet or dry contact processing. Clearly, for devices without a Cu layer, the surface preparation method has a much greater effect on the stressed J–V than the initial J–V. This agrees with results [9] where devices with Sb/Au contacts (no Cu layer) having two different surface etches had

very different stability from each other. Thus, for devices without Cu, the surface treatment is critical and the thicker Te layer gives more stable devices.

5. Summary and conclusions

Figs. 3 and 4 summarize the dependence of V_{oc} and FF on Cu layer thickness before and after stressing for the wet and dry contact processes. Varying the Cu thickness varies the Cu_xTe_{1-x} composition and thickness. Initial performance is very similar for the two processes independent of Cu thickness. Initial V_{oc} was 0.80 ± 0.02 V and initial FF was $69 \pm 2\%$ for all devices except those without Cu; thus, as little as 2 nm of Cu is sufficient to produce 11% devices. After stress, cells with Cu contacts had no strong dependence on the contact process. Solar cell performance (V_{oc}, FF, J_{sc}) or device properties (A, J_0, or R_S) were similar for both wet and dry processing. J_0 increased by about 2 orders of magnitude, A increased slightly (approaching 2), R_S increased 5–20 $\Omega\,cm^2$, and activation energy ϕ/A moved to midgap. There was no strong dependence of degradation on Cu thickness (in the range 2–15 nm) for either of the contact processes, with efficiencies decreasing from 9–10% to 5–6%. After stressing, the recombination mechanism does not change but the amount of recombination increases significantly. Devices with the dry contact process tend to have less "roll over" or curvature in forward bias after stressing compared to those with the wet contact. This suggests the wet contact enhanced the formation of the blocking contact. The two key differences between the dry and wet process are that the dry process leaves a thinner Te layer and is less penetrating along grain boundaries. It is not known yet how these differences are responsible for the differences in blocking contact formation.

Analysis of the J–V characteristics as a function of temperature indicates that the junction recombination is an SRH mechanism. Evidence includes A values between 1.5 and 2.0, ϕ approximately equal to the CdTe bandgap, and the activation energy near midgap of CdTe. This suggests that deep centers in the CdTe, whose concentration increases with stress, are responsible for the recombination limiting V_{oc}.

Our recontacting study (Section 3) showed that losses in V_{oc} and FF are partially independent and separable. The loss in V_{oc} is not recoverable, while much of the loss in FF due to the blocking contact is recoverable with a new contact. Losses in V_{oc} and FF occur within the ~1 week stress time used in this study, while stressing for longer times enhances the formation of the blocking contact.

Initial performance of devices without Cu is similar to those with Cu after stress: lower V_{oc}, more LDXO, and higher R_S compared to initial performance of devices with Cu layers, in agreement with Corwine et al. [16]. One critical difference between devices with and without Cu layers is that devices without Cu have much lower J_0 and A factor, suggesting less recombination at midgap defects, but they have lower ϕ leading to a lower V_{oc} despite having less recombination.

Degradation in V_{oc} for "Cu free" devices is less (~0.06 V) than typically found for devices with Cu layer (see Fig. 3). The relatively smaller loss in V_{oc} after stressing is

independent of the contact processing or surface etch. However, severe degradation in FF occurs even without Cu. Devices with the BDH etch do not show the extreme rollover of the J–V curve after stress, suggesting formation of a blocking contact is suppressed with sufficient Te, consistent with maintaining a p^+ surface. Since devices without any Cu layer still show degradation, other degradation mechanisms such as interactions with oxygen, chlorine, and excess Te must be identified and solved. Devices with insufficient Cu dopant will be more susceptible to presence of other doping species and atmospheric reactions which may be less well controlled.

Acknowledgments

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