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Thin-film CdTe cells: Reducing the CdTe

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ABSTRACT

Polycrystalline thin-film CdTe is currently the dominant thin-film technology in world-wide PV manufacturing. With finite Te resources world-wide, it is appropriate to consider the limits to reducing the thickness of the CdTe layer in these devices. In our laboratory we have emphasized the use of magnetron sputtering for both CdS and CdTe achieving AM1.5 efficiency over 13% on 3 mm soda-lime glass with commercial TCO and 14% on 1 mm aluminosilicate glass. This deposition technique is well suited to good control of very thin layers and yields relatively small grain size which also facilitates high performance with ultra-thin layers. This paper describes our magnetron sputtering studies for fabrication of very thin CdTe cells. Our thinnest cells had CdTe thicknesses of 1 μm, 0.5 μm and 0.3 μm and yielded efficiencies of 12%, 9.7% and 6.8% respectively. With thinner cells Voc, FF and Jsc are reduced. Current–voltage (J–V), temperature dependent J–V (J–V–T) and apparent quantum efficiency (AQE) measurements provide valuable information for understanding and optimizing cell performance. We find that the stability under light soak appears not to depend on CdTe thickness from 2.5 to 0.5 μm. The use of semitransparent back contacts allows the study of bifacial response which is particularly useful in understanding carrier collection in the very thin devices.
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1. Introduction

Many advantages accrue from reducing the thickness of the absorber layer in direct bandgap solar cells such as CdTe and CIGS. These include reduced use of materials especially materials such as In and Te with low earth abundance, reduced deposition time, reduced time for post-deposition processing, and lower potential environmental impacts. Direct bandgap semiconductor absorbers seldom need more than one micron to achieve essentially full light absorption beyond a few meV of the band edge. Britt, et al. [1] have discussed thinning CIGS layers and predicted that 0.8 μm should be achievable. In this work we review some of the cell performance data on magnetron sputtered CdS/CdTe solar cells [2] with very thin absorber layers and then discuss some materials issues in ultra-thin CdTe devices [3].

In the case of CdTe, which is normally fabricated in the superstrate structure, back-contact processing may limit the achievable reductions in CdTe thickness due to the chemical etch process, such as nitric–phosphoric acid, that preferentially etches down grain boundaries [4] and can lead to excessive shunting as the CdTe thickness is reduced. In the process used in our group, the back contacting is done without chemical etches and the sputter process at 250 °C deposition temperature yields small grain sizes with compact grain boundaries. These are good conditions for exploring the limits of CdTe thickness.

2. Experimental

Cells were fabricated on 3 mm soda-lime glass substrates with commercial SnO_2:F (Pilkington TEC 15) and an HRT (high resistivity transparent) coating and a 60 nm sputtered CdS layer. The CdTe thicknesses were chosen as: 0.3 μm, 0.5 μm, 0.65 μm, 0.8 μm, 1.1 μm, 1.45 μm, 1.85 μm, 2.2 μm and 2.6 μm as measured by a profilometer. As described previously, the $CdCl_2$ activation treatment and evaporated Cu layer thickness were optimized for each CdTe thickness [3]. After 15 nm of evaporated Au, the cells were completed with a 150 °C diffusion optimized with reduced time as the CdTe layer thickness decreased. A CdS thickness of 60 nm allows for a good blue-green transmission of the window layer but at the same time assures strong electrical properties of the n-side of the junction. Thus the variations in cell performance are mainly due to the properties of the CdTe and the back contact side of the device. For each thickness we prepared at least 35 dot cells of 0.062 cm^2 area providing good statistics for analysis by current–voltage (J–V), J–V vs. temperature (J–V–T) and apparent quantum efficiency (AQE) tests. Furthermore, the ~50% of visible light transmitted through the 15 nm of gold permits AQE under back-contact illumination as well as the standard junction-side illumination.

Above 1.1 μm, the J–V characteristics are nearly independent of CdTe thickness. The J–V characteristics of the five thinnest cell structures are shown in Fig. 1. A gradual drop with CdTe thickness is

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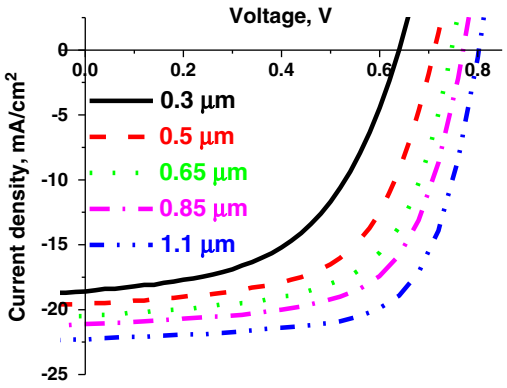

Fig. 1. J–V characteristics of cells with variable CdTe thickness.

observed in all primary cell parameters, V_{OC}, J_{SC}, and FF. (We estimate the error in current density measurements to be ± 0.5 mA/cm^2 mainly from uncertainty in contact area and lamp intensity.) Average of ten and best cell efficiencies are shown in Fig. 2. Note that 12% efficiency is achieved at 1.1 μm and 9.7% at 0.5 μm.

External AQE is shown in Fig. 3 for five different voltage biases (−1 V, −0.5 V, 0 V, 0.3 V and 0.5 V). Although very little voltage-dependent collection is observed at 2.6 μm of CdTe, Fig. 3 shows a moderate (1.1 μm) and strong (0.5 μm) dependence of current collection at forward biases of 0.4 and 0.5 V. This behavior indicates for the thinner cells that when the CdTe is not fully depleted, e.g., at +0.4 or +0.5 V, and the normally strong electric field is reduced, the minority carrier collection is poor. This points to reduced absorber minority carrier lifetime caused by the close proximity of back contact interface and Cu recombination centers near the back contact [5].

In order to obtain a measure of the main junction quality we performed J–V–T measurements of the thin cells using both junction-side and contact-side illumination. For illumination through the Au contacts, the intensity of the incident light was adjusted to match a typical short-circuit current output of the cell under one-sun junction-side illumination. Cell temperature was varied within the range of 255 K to 315 K and open-circuit voltage was extrapolated to 0 K to obtain the main junction barrier height, Φ_b. We find the measure of main junction quality, Φ_b, is essentially independent of CdTe thickness down to 1.1 μm as seen in Fig. 4. All but two data points were obtained from "aged" cells stored in the lab for about 5 months in room air with no encapsulation. The highest Φ_b value of 1.45 eV (2.2 μm CdTe) was obtained for a relatively "fresh" cell, stored about two weeks, in room air. In this case, Φ_b was close to the E_g/q value for CdTe (1.61 eV), [6] indicating Schockly–Read–Hall as the dominant recombination mechanism. The "aged" cell Φ_b values were signifi-

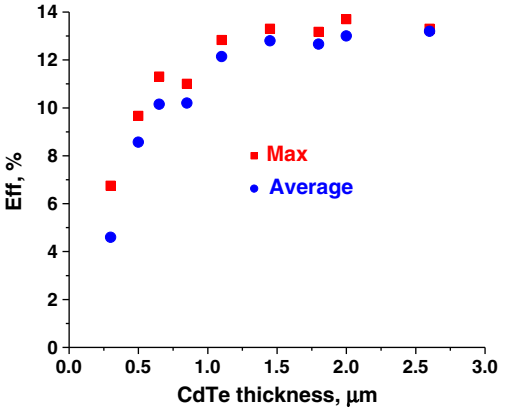

Fig. 2. Average and best cell efficiencies as a function of the CdTe thickness.

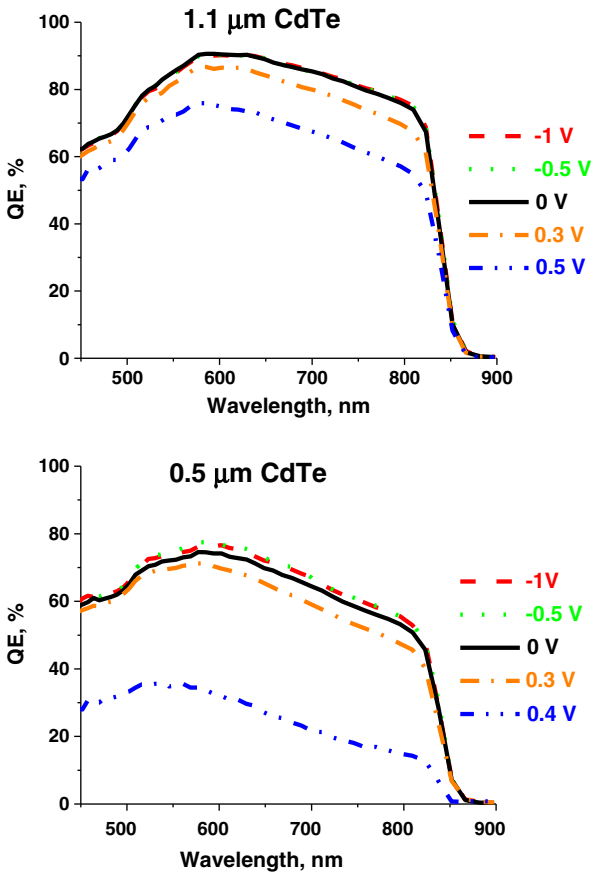

Fig. 3. AQE vs. bias of 1.1 μm and 0.5 μm cells.

cantly lower which suggests that interfacial recombination through the defect states becomes a major factor limiting cell performance after a certain amount of storage time without encapsulation in room air ambient (296 K, about 30% relative humidity). These changes in Φ_b with dark storage are being investigated further.

3. CdTe microstructure

The microstructure of the CdS and CdTe is likely to play an increasingly important role in the cell performance as the thickness

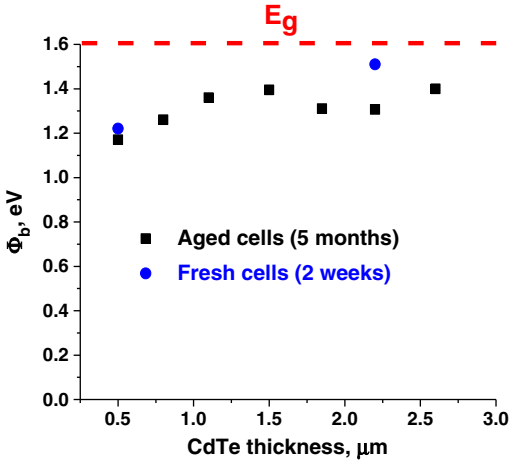

Fig. 4. Φ_b values for several cells with different CdTe thickness. "Aged" cells were measured after 5 months in air; "fresh" cells measured after 2 weeks in air.

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decreases. We have found that the microstructure of sputtered CdTe is affected by the deposition temperature, the sputter gas pressure, the RF power, and the magnetron magnetic field, as well as the $CdCl_2$ activation conditions. Furthermore the grain size and void structures in a polycrystalline thin film typically change with distance from the nucleation interface. Therefore we have studied the profile of our films by using Low-Incidence Surface Milling (LISM) with a gallium Focused Ion Beam (FIB) incident at 3° to the CdTe surface. This allows us to examine the microstructure vs. depth by SEM imaging.

An example of an exposed complete device structure after the FIB milling is shown Fig. 5. This device was fabricated with the sputter sources directed at 45° to the substrate rotation axis at 10 mTorr depositing 0.1 μm CdS and 2.4 μm CdTe layers sequentially, followed with $CdCl_2$ activation at 390 °C for 30 min and Cu/Au metal contact deposition by evaporation. The identification of various layers was done by mapping the energy dispersive X-ray spectroscopy (EDS) on the 3° milled surface from the back contact of the CdTe through the device until reaching glass. This clearly identified the locations of CdTe/CdS and CdS/SnO_2 interfaces. The layer identification was also confirmed by calculating the thicknesses of layers from the observed SEM width multiplied by tan(3°) and comparing to our in-situ optical thickness monitor data. Narrow void structures along some grain boundaries are evident in (a) and (b) in the later stages of the CdTe growth. However, the early stages of CdTe growth are very dense with little evidence of voids. An interesting feature is the appearance of a porous CdTe or perhaps CdSTe layer of ~0.1 μm (observed width of 2.5 μm in Fig. 5) appearing at the CdTe side of the junction, but only in $CdCl_2$ treated films. The effect of such a thin, porous layer on device performance is not so clear, but for 1.1 μm of CdTe and above our device efficiencies are in the 12 to 13% range, even with this thin porous layer. We speculate that such a porous layer may actually benefit light collection in very thin CdTe by enhancing light scattering as it enters the CdTe absorber layer. Possible contributing mechanisms for the generation of such a porous layer are the ~10% lattice mismatch between CdS and CdTe, the S, Te interdiffusion, and the release of strain during the chloride activation process. Further studies of the mechanism(s) driving this localized void formation during chloride treatment are in progress. The porous region appears to be limited to about 100 nm on the CdTe side of the CdS/CdTe junction which would be the region of high stress due to the ~10% smaller lattice constant for CdS.

Quantitative analysis of voids by ImageJ [7] shows the *area* fraction, after activation annealing, to be about 8% for CdTe films. Assuming a void shape is approximately spherical, the void *volume* fraction is estimated at about 2% in the treated CdTe films.

4. Device stability vs. Cdte thickness

It might be expected that thinning the CdTe and bringing the back contact closer to the main junction would lead to increased degradation of the device. In order to identify changes in stability, we performed accelerated life testing (ALT) measurements on devices of different CdTe thickness. These ALT studies were done under one-sun illumination at 85 °C and open-circuit conditions. Earlier ALT studies of CdTe cells have shown that generally open-circuit conditions lead to faster degradation than holding the cells at the

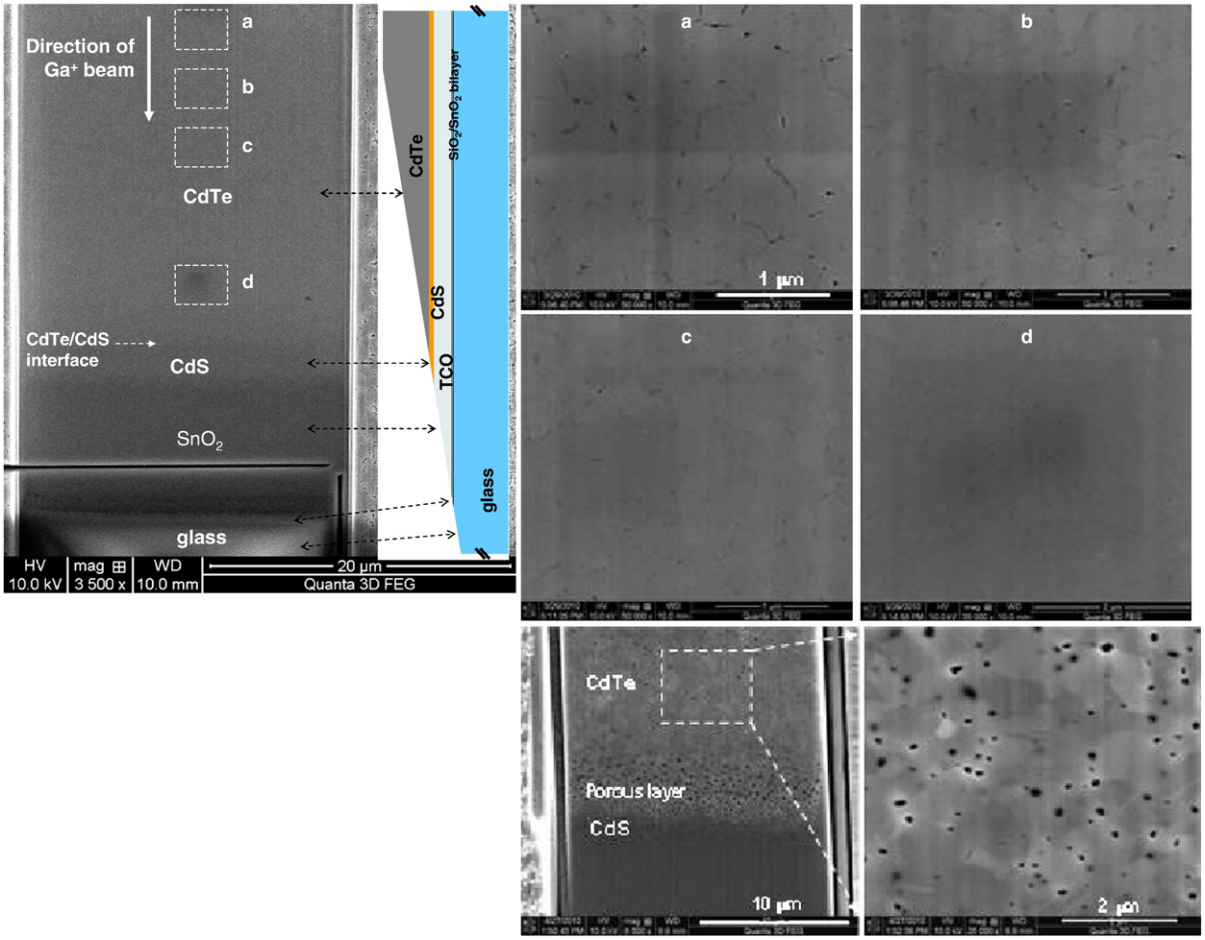

Fig. 5. Sketch of LISM-FIB milling preparation of CdS/CdTe (2.4 μm) cell structure. Low resolution SEM showing beveled area before $CdCl_2$ activation with 3 μm × 3 μm magnified areas a) b) c) d) near CdTe surface to near junction.

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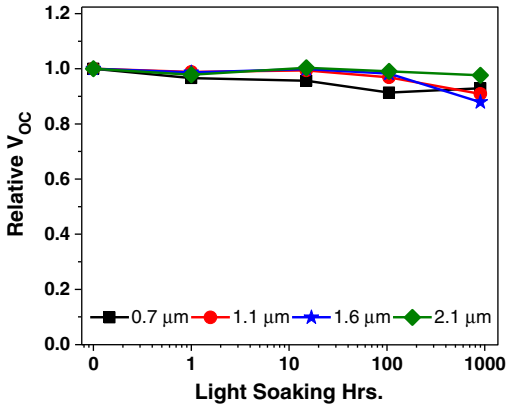

Fig. 6. V_{OC} normalized to initial value vs. time under light soak at 85 °C without encapsulation for cells of four different thicknesses. Note logarithmic time scale.

maximum power point, the normal cell operating condition [8,9]. Our test was done with unencapsulated cells exposed to room air. Some of the results of the study are shown in Fig. 6 where each datum point constitutes an average of 20 cells. We show only V_{OC} which is the cell parameter we found to be most sensitive to this ALT process. To facilitate comparison among the different CdTe thicknesses, we have normalized the data. The small degradation seen in this test does not appear to correlate with CdTe thickness but further work will be needed to achieve greater confidence in this conclusion.

5. Conclusion and impacts on Cdte maximum module production

We investigated the performance of magnetron sputtered cells on CdTe thickness for CdTe layers ranging from 0.3 μm to 2.6 μm. We find that an average efficiency of greater than 12% can be achieved for cells as thin as 1 μm with the appropriate post-deposition treatment and an optimized back-contact scheme. We also found that further reduction of CdTe thickness leads to a gradual decrease in performance although 9.7% efficiency can be obtained with a 0.5 μm CdTe cell. Recombination at the back contact, identified by J–V–T in combination with bifacial illumination, is believed to be one of the major mechanisms limiting performance of the thin cells. Much of the efficiency loss is due to incomplete photoabsorption. In fact modeling the J_{SC} according to single-pass absorption with no optical reflection at the back contact accounted for most of the current loss in the best of the thin cells [3]. More studies are underway to resolve the issues of the V_{OC} and FF losses as well as collection probability less than unity from the space charge region in the thin cells. The use of appropriate optical and electron reflector structures should lead to improved performance of cells with ultra-thin layers of CdTe. With appropriate modifications, we believe that 12% efficient cells will soon be achieved using CdTe layers of only 0.5 μm.

Fthenakis [10] and Zweibel [11] have recently discussed projections of the supply of Te and its impact on CdTe module production. Both authors considered reductions from today's typical module thickness of 3 μm. Fthenakis considered a 1 μm as an optimistic thickness, Zweibel considered both 0.67 and 0.2 μm. Based on the results presented here, we consider 0.2 μm a serious challenge but the other scenarios are very reasonable. Thus, Zweibel's conclusion seems justified that were 10% of world electricity production to be delivered by PV, CdTe-based modules could supply 50–100% of that.

Acknowledgments

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