

Study of Indium Tin Oxide (ITO) for Novel Optoelectronic Devices

by

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“বিসমিল্লাহ আর-রাহমান আর-রাহিম”

To,

My parents

and

in loving memory of my grandparents

“যারা স্বনির্ভরতার পথ খোঁজে,
খোদা তাদেরকে সাহায্য করেন”

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Abstract

Indium Tin Oxide (ITO) films were deposited on a number of semi-conductor materials using reactive r.f. sputtering technique to form both rectifying Schottky and ohmic contacts. These contacts were applied in the fabrication of a number of novel optoelectronic devices: Schottky photo-diodes, transparent gate High Electron Mobility Transistors (HEMTs), heterojunction bipolar transistors (HBTs) being used as heterojunction phototransistors (HPTs), light emitting diodes (LEDs) and vertical cavity surface emitting lasers (VCSELs). A number of these novel devices were studied in comparatively greater detail; these were the Schottky diode and the HPT.

Deposition conditions necessary to produce ITO films with high conductivity and optical transparency over a wide spectral range were studied and optimised. Separate post deposition techniques were developed to produce near ideal rectifying contacts and ohmic contacts with low contact resistance respectively. A thin film of indium (In) was also used to optimise ITO ohmic contacts to n⁺ - GaAs substrates.

Near ideal Schottky diodes were realised on n-GaAs substrates using aluminium (Al) and gold (Au) metal contacts. A simulation model was then developed and implemented to study the behaviour of current transport mechanisms over a wide temperature range. Photodiodes with ITO as the Schottky metal contact were fabricated and a study comprising of both their electrical and optical behaviour was undertaken.

Relatively large geometry HBTs and HPTs were fabricated using AlGaAs/GaAs, InGaP/GaAs and InP/InGaAs systems respectively; the latter devices were first reported as a result of this study. A comparative study between devices fabricated from these systems were then made. This was followed by an appraisal of the electrical properties of each of their optical counterparts which had ITO emitter contacts. The specific photo responsivity and the spectral responses of these HPTs were analysed. In light of HPTs with transparent ITO emitter ohmic contacts, a brief examination of the merits of vertical versus lateral illumination was also made in this work.

Finally a spectral response model was developed to understand and help design optoelectronic detectors comprising of single layer devices (n-GaAs Schottky photo diodes) or multiple semiconductor materials (HPTs using AlGaAs/GaAs or InP/InGaAs systems) to help predict responsivities at a given incident wavelength. As well as material properties of the constituent semiconductors, this model takes into account the specific lateral and vertical geometrical dimensions of the device.

List of Abbreviations, Constants and Symbols

Symbol	Meaning	Units/Notes
A	Area	m^2
α	Absorption co-efficient	cm^{-2}
\AA	Angstrom, unit of length ($1\text{\AA} = 10^{-10} \text{ m}$)	
A^*	Richardson constant	$\text{Am}^{-2}\text{K}^{-2}$
A^{**}	Modified Richardson constant	$\text{Am}^{-2}\text{K}^{-2}$
Al	Aluminium	
Ar	Argon	
As	Arsenic	
Au	Gold	
AuGe	Gold-germanium eutectic alloy	
B	Bandwidth	
β	DC Current Gain of bipolar transistors	
BER	Bit Error Rate	
BJT	Bipolar Junction Transistor	
C	Capacitance	Farad, F
c	velocity of light in vacuum	$3 \times 10^8 \text{ ms}^{-1}$
χ_B	Electron affinity of base	V
χ_E	Electron affinity of emitter	V
C_f	Correction factor	
CH_4	Methane	
CO_2	Carbon dioxide	
χ_s	Electron affinity of a semiconductor	eV
CTO	Cadmium Tin Oxide	
d	Film thickness (or MESA height in TLM analysis)	m
D	Diameter	m
δ	Thickness of oxide layer	m
ΔE_c	Conduction band offset at a heterojunction in eV	eV
ΔE_g	Bandgap difference at a heterojunction in eV	eV
ΔE_v	Valence band offset at a heterojunction in eV	eV
$\Delta\phi$	Image-force induced reduction to barrier height	eV
D_n	Electron diffusion constant	$\text{cm}^2 \text{s}^{-1}$
D_p	Hole diffusion constant	$\text{cm}^2 \text{s}^{-1}$
D_s	Density of surface states	cm^{-2}
ΔV_{CE0}	Offset voltage	V
DVM	Digital Volt Meter	
E_{br}	Breakdown electric field	Vm^{-1}
E_c	Energy at the bottom of the conduction band in eV	eV
EDFA	Erbium Doped Fiber Amplifier	
E_f	Fermi level energy in eV	eV

E_g	Semiconductor bandgap in eV	eV
ϵ_0	Permittivity of free space	$8.8542 \times 10^{-14} \text{ Fcm}^{-1}$
E_o	Tunneling constant	
E_{oo}	Tunneling parameter	
ϵ_r	Relative permittivity	
eV	Electron volts, ($1\text{eV} = 1.602 \times 10^{-19} \text{ J}$)	
E_v	Energy at the top of the valence band	eV
Φ	Photon flux	
Φ_{abs}	Photon flux absorbed in the semiconductor	
ϕ_b	Barrier height	V
ϕ_{bo}	Unbiased barrier height	V
FET	Field Effect Transistor	
ϕ_m	Work function of a metal	V
ϕ_n	Barrier height to electrons in the emitter-base junction	V
ϕ_p	Barrier height to holes in the base-emitter junction	V
Φ_{ref}	Reflected photon flux	
ϕ_s	Work function of a semiconductor	V
G	Optical gain	
Ga	Gallium	
GaAs	Gallium Arsenide	
Ge	Germanium	
g_m	Transconductance of FETs	
h	Planck constant	$6.6262 \times 10^{-34} \text{ Js}$
η	Quantum efficiency	
H_2	Hydrogen	
H_2O	Water	
H_2O_2	Hydrogen Peroxide	
H_2SO_4	Sulphuric acid	
H_3PO_4	Phosphoric acid	
HBT	Heterojunction Bipolar Transistor	
HCl	Hydrochloric acid	
HEMT	High Electron Mobility Transistor	
HF	Hydrofluoric acid	
$h\nu$	Photon energy	J
HPT	Heterojunction Photo Transistor	
I	Current	Amps, A
I_b	Base current (of a bipolar transistor)	A
I_c	Collector current (of a bipolar transistor)	A
I_e	Emitter current (of a bipolar transistor)	A
I_{gr}	Current due to generation-recombination	A
I_{lk}	Leakage current	A
In	Indium	
I_n	Electron current	A
InGaAs	Indium Gallium Arsenide	

InGaP	Indium Gallium Phosphide	
InP	Indium Phosphide	
I _p	Hole current	A
I _{Ph}	Photo current	A
I _{te}	Current due to thermionic emission	A
I _{tn}	Current due to tunneling	A
ITO	Indium Tin Oxide	
J	Joule, unit of energy	
J _n	Electron current density	Acm ⁻²
J _p	Hole current density	Acm ⁻²
k	Boltzmann constant	1.38 x 10 ⁻²³ JK ⁻¹
K	Kelvin, unit of absolute temperature	
k'	Extinction co-efficient	
kg	Kilogram, unit of mass	
KOH	Potassium Hydroxide	
λ	lambda, wavelength	m
l	litre, unit of volume ($1l = 10^3$ cm ³)	
L	Probe or pad spacing	m
LED	Light Emitting Diode	
L _n	Electron diffusion length	m
L _p	Hole diffusion length	m
MBE	Molecular Beam Epitaxy	
m _e	mass of an electron	kg
m _h	mass of a hole	kg
μ _H	Hall mobility	cm ² V ⁻¹ s ⁻¹
μ _n	Electron mobility	cm ² V ⁻¹ s ⁻¹
MOCVD	Metalo-Organic Chemical Vapour Deposition	
μ _p	Hole mobility	cm ² V ⁻¹ s ⁻¹
v	Oscillation frequency of electro-magnetic radiation	Hz
n	Refractive index	
N	Carrier concentration	cm ⁻³
N ₂	Nitrogen	
N _A	Ionised acceptor concentration	cm ⁻³
N _c	Density of states in the conduction band	cm ⁻³
n _c	Critical doping density	cm ⁻³
N _D	Ionised donor concentration	cm ⁻³
NH ₃	Ammonia	
n _i	Intrinsic carrier concentration	cm ⁻³
Ni	Nickel	
n _{no}	Majority carrier concentration in n-type semiconductor	cm ⁻³
n _{po}	Minority carrier concentration in p-type semiconductor	cm ⁻³
N _v	Density of states in the valence band	cm ⁻³
O ₂	Oxygen	
π	pi	3.141592654

P	Phosphorous	
PAr	Partial pressure of argon	
p _{no}	Minority carrier concentration in n-type semiconductor	cm ⁻³
P _o	Optical power	W
PO ₂	Partial pressure of oxygen	
p _{po}	Majority carrier concentration in p-type semiconductor	cm ⁻³
P _T	Total Pressure	torr
q	Charge on a proton	1.6 x 10 ⁻¹⁹ coulombs
r	Resistance	Ohms, Ω
ρ	Resistivity	Ωcm
R	Responsivity	AW ⁻¹
ρ _c	Specific contact resistance	Ωcm ²
R _c	Contact resistance	Ω
R _{cc'}	Collector contact resistance	Ω
R _{Diode}	Responsivity of diode	AW ⁻¹
R _e	End contact resistance	Ω
R _{ee'}	Emitter contact resistance	Ω
R _{HPT}	Responsivity of HPT	AW ⁻¹
R _{lk}	Leakage resistor	Ω
r _p	Rate of photon arrival	s ⁻¹
r _q	Rate of photo-generated electron collection	s ⁻¹
R _s	Series resistance	Ω
R _{sh}	Sheet resistance	Ω/□
R _{sk}	Sheet resistance under an ohmic contact pad	Ω/□
RTA	Rapid Thermal Annealing	
s	Length of a (TLM) contact pad	m
SCR	Space Charge Region	
Si	Silicon	
S _λ	Spectral response	
Sn	Tin	
SPA	Semiconductor Parameter Analyser (HP 4145B)	
T	Absolute temperature	K
TFA	Thermal Furnace Annealing	
Ti	Titanium	
T _{ITO}	Optical transmittance of ITO film	
τ _n	Electron life time	s
τ _p	Hole life time	s
T _r	Optical transmittance	
V	Voltage	Volts
V _{app}	Applied bias	V
V _{bc}	Base-collector voltage	V
V _{be}	Base-emitter voltage	V
V _{bi}	Built-in potential	V
V _{br}	Breakdown voltage	V

V_{ce}	Collector-emitter voltage	V
VCSEL	Vertical Cavity Surface Emitting Laser	V
V_{eff}	Effective bias across an interface	V
V_n	Potential difference between E_c and E_f	V
v_{nB}	Mean electron velocity at the emitter end of the base	ms^{-1}
V_p	Potential difference between E_f and E_v	V
v_{pE}	Mean hole velocity at the base end of the emitter	ms^{-1}
V_r	Reverse bias	V
V_t	Turn-on voltage (for a diode at a set current)	V
W	Watts, unit of power	W or Js^{-1}
w	Width of a (TLM) contact pad	m
ω	Angular frequency	radian s^{-1}
w_b	Base width (of a bipolar transistor)	m
W_c	Energy at the bottom of the conduction band	J
W_f	Fermi Level energy	J
W_g	Bandgap energy	J
W_λ	Spectral radiancy	$\text{Wm}^{-2}\mu\text{m}^{-1}$
W_v	Energy at the top of the valence band	J
x_{dep}	Depletion width	m
x_n	Depletion width of n-type semiconductor	m
x_p	Depletion width of p-type semiconductor	m
Zn	Zinc	
ZrB_2	Zirconium diboride	

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1. Introduction

1.1 Genesis

With the demonstrated advantages of an optical fiber telecommunication system over a conventional copper-wire based system, the efficient conversion of an electrical signal to an optical signal and vice versa, is now of utmost importance. Similarly, rapid progress in semiconductor materials growth technology and the emergence of novel techniques in device fabrication has led to a continual improvement in the performance of opto-electronic integrated circuits (OEICs). In addition, with similar maturity in new technologies such as monolithic microwave integrated circuits (MMICs), the commercial viability of direct integration between optical and microwave circuits is becoming more and more likely.

One of the vital components of any high frequency optical system is a large bandwidth, low noise photo receiver which may be realised using monolithic integration of photo diodes with high speed transistors to act as preamplifiers. A wide range of materials and devices, including semi-transparent metal/semiconductor Schottky photo diodes and integrated p-i-n diodes with HBTs have been used for this purpose.

The use of a Schottky diode is ideal for high speed applications where it has many advantages. One of these is the inherent absence of any slow component associated with minority carrier effects. Its usage enables the absorption layer thickness to be engineered to obtain the optimum compromise between external quantum efficiency and detector bandwidth. The latter of these arises from a combination of carrier transit time and RC effects. An inherent disadvantage, however, is the high series resistance and low optical coupling efficiencies obtained which are associated with the thin semi-transparent metal layer. A solution to this problem is to use a layer of Indium Tin Oxide (ITO), a practically transparent and highly conductive material, as the Schottky contact to fabricate both high speed and highly efficient photo diodes.

Renewed interest in using photo transistors as detectors has been aroused world wide, particularly with the advent of Heterojunction Bipolar Transistors (HBTs). Studies using such HBTs with opaque emitter contacts show excellent suitability of these devices as photo detectors in terms of optical performance where signal to noise ratios in excess of 30dB have been obtained. The optical gain of any photo transistor depends on the coupling efficiency,

the collection efficiency and its internal gain; in the HPT structure, there lies an inherent trade-off between the speed and the collection efficiency. However, by using a transparent emitter contact, the coupling efficiency can be significantly improved thereby raising the overall gain-bandwidth of the device correspondingly.

Similar arguments could be presented in support of using a transparent ITO contact to a number of other devices such as in transparent gate HEMTs, LEDs and VCSELs. Hitherto, ITO had been the subject of extensive study by material scientists and engineers for a wide range of other applications ranging from anti-reflection coatings to transparent contacts in solar cells. Its usage in the fabrication of microelectronic devices for optoelectronic applications is a relatively new field. Hence, this study essentially represents some of the novel work in this area.

1.2 Aims and Objectives

One of the primary objectives of this work was the application of a transparent ITO contact to a number of optoelectronic devices. These required the development of both Schottky and ohmic contacts. In particular, n-GaAs Schottky photo diodes and the heterojunction photo transistors, both as optical detectors, were studied in detail.

With this goal in mind, the ITO film deposition based on a r.f. reactive sputtering technique was first studied and then optimised. Extensive work involving the calibration of the sputtering machine was carried out to understand the particular effects of various deposition conditions on the ITO films. These films were then characterised to study their electrical conductivity and optical transmittance. A number of different post-deposition annealing techniques were also developed for specific application as either Schottky or ohmic contacts. The use of a thin indium metallic layer between the sputtered ITO and the underlying semiconductor was also studied for its influence on sputter damage, ohmic and Schottky contacts. Work was also carried out to ensure that adequate patterning techniques were developed to realise small geometry devices based on ITO contacts. Similarly, contacts to ITO with pad metals was also studied and assessed.

Once it was established that satisfactory ITO films could be produced, the work was extended to the fabrication of the devices. These films were used to realise novel optoelectronic devices which were characterised and compared to their opaque counterparts.

Schottky diodes with near ideal electrical characteristics were realised on n-GaAs substrates using aluminium (Al) and gold (Au) metal contacts. A simulation model was then developed and implemented to study the behaviour of current transport mechanisms over a wide temperature range. Photo diodes with ITO as the Schottky contact were fabricated and a study comprising of both their electrical and optical behaviour was undertaken. This involved further optimisation work to ensure the sputter damage sustained during the ITO deposition could be first minimised and then the remainder removed to an acceptable level without compromising the rectifying behaviour of the junction, reducing the series resistance and dark currents for photo diode operation. All this had to be carried out while retaining the desired high transparency and high conductivity properties of the ITO film itself.

The next stage of the study involved the use of heterojunction transistors as photo detectors. Large geometry HBTs and HPTs were fabricated using AlGaAs/GaAs, InGaP/GaAs and InP/InGaAs systems respectively with both conventional and transparent ITO emitter ohmic contacts. A comparative study between devices fabricated from these systems were then made. This was followed by an appraisal of the electrical properties of each of their optical counterparts which had ITO emitter contacts. The specific photo responsivity and the spectral responses of these HPTs were analysed. In light of HPTs with transparent ITO emitter ohmic contacts, a brief examination of the merits of vertical versus lateral illumination was also made in this work.

A spectral response model was also developed to understand and help design optoelectronic detectors comprising of single layer devices (n-GaAs Schottky photo diodes) or multiple semiconductor materials (HPTs using AlGaAs/GaAs or InP/InGaAs systems) to help predict responsivities at a given incident wavelength. As well as material properties of the constituent semiconductors, this model takes into account the specific lateral and vertical geometric dimensions of the device.

In collaboration with other researchers, two by-products of this study were the first VCSEL and TG-HEMT using ITO as the transparent ohmic and Schottky gate contacts respectively. Some preliminary work was also carried out to produce ITO contacts to visible LEDs which had an emission wavelength of approximately 630nm.

1.3 Summary and Layout of Thesis

In this thesis the background theory and the relevant literature survey are presented in the second chapter. This is followed, in chapter three, by a description of all the processing steps involved in the fabrication of the devices, while chapter four consists the details of the measurement and analysis techniques. Chapter five contains the first set of experimental results of this research; these are the findings concerning the ITO films used in the devices. Finally, chapter six constitutes the second and the larger part of results, namely that of the Schottky diodes and their temperature dependent current transport model, the heterojunction photo transistors, and the spectral response model respectively. The conclusion of the work and a list of suggestions for further work are presented in chapters seven and eight.

A list of publications resulting from this work is given in Appendix A. Appendix B contains the processing steps for liftoff and etch lithography steps. Appendix C has the Hewlett Packard HP4145B Semiconductor Parameter Analyser (SPA) settings for the device parameter extractions while some mathematical derivations are given in Appendix D.

2. Background Theory and Literature Review

2.1 Indium Tin Oxide (ITO)

Interest in transparent conductors can be traced back to 1907 when reports of transparent and conductive cadmium oxide (CdO) films first appeared. Since then there has been a growing technological interest in materials with these unique properties as evidenced by not only their increased numbers but also the large variety of techniques that have been developed for their deposition. It is now known that non-stoichiometric and doped films of oxides of tin, indium, cadmium, zinc and their various alloys exhibit high transmittance and nearly metallic conductivity is achievable [1]. However, tin doped indium oxide (ITO), with reported transmittance and conductivity as high as 95% and $10^4 \Omega^{-1}\text{cm}^{-1}$ respectively, is among the most popular of these thin films which have found a host of electronic, opto-electronic and mechanical applications. Hence, some of the physical and technological aspects behind ITO films will now be reviewed and discussed.

2.1.1 Introduction and Uses of ITO

Although partial transparency, with acceptable reduction in conductivity, can be obtained for very thin metallic films, high transparency and simultaneously high conductivity cannot be attained in intrinsic stoichiometric materials. The only way this can be achieved is by creating electron degeneracy in a wide bandgap ($E_g > 3\text{eV}$ or more for visible radiation) material by controllably introducing non-stoichiometry and/or appropriate dopants. These conditions can be conveniently met for ITO as well as a number of other materials previously mentioned.

Uses of ITO have traditionally ranged from transparent heating elements of aircraft and car windows, antistatic coatings over electronic instrument display panels, heat reflecting mirrors, antireflection coatings and even in high temperature gas sensors. Early electro-optic devices using ITO include CCD arrays, liquid crystal displays and as transparent electrodes for various display devices. More recently, ITO has been used as a transparent contact in advanced optoelectronic devices such as solar cells, light emitting and photo diodes, photo transistors and lasers - some for the first time as a result of this investigation [2]. Thus it is soon becoming an integral part of modern electronic technology wherever there is a potential for improving optical sensitivity of light detecting devices or quantum efficiency of light emitting devices.

However, with increased development in electronic technology has come the need for a greater understanding of the optical and electrical properties of ITO. As a result some of the solid state physics of ITO has also emerged. Although no concise and accurate knowledge is available, the literature survey indicates that many of these properties can be tailored by careful control of the deposition parameters.

2.1.2 Physical Structure and Properties of ITO

Indium Tin Oxide is essentially formed by substitutional doping of In_2O_3 with Sn which replaces the In^{3+} atoms from the cubic bixbyte structure of indium oxide [3]. Sn thus forms an interstitial bond with oxygen and exists either as SnO or SnO_2 - accordingly it has a valency of +2 or +4 respectively. This valency state has a direct bearing on the ultimate conductivity of ITO. The lower valence state results in a net reduction in carrier concentration since a hole is created which acts as a trap and reduces conductivity. On the other hand, predominance of the SnO_2 state means Sn^{4+} acts as a n-type donor releasing electrons to the conduction band. However, in ITO, both substitutional tin and oxygen vacancies contribute to the high conductivity and the material can be represented as $\text{In}_{2-x}\text{Sn}_x\text{O}_{3-2x}$. ITO films have a lattice parameter close to that of In_2O_3 and lie in the range 10.12 to 10.31 Å [4].

A summary of electrical and optical properties of typical ITO films deposited using various techniques is shown in Table 2.1. Variations in film properties can be easily noted; these are attributable to both pre- and post-deposition treatments as well as the techniques themselves.

Deposition Technique	Thickness [Å]	Hall Mobility μ_H [$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$]	Carriers N [cm^{-3}]	Resistivity ρ [Ωcm]	Transmittance T _r [%]	Ref. No.
r.f. Sputtering	7,000	35	6×10^{20}	3×10^{-4}	90	[5]
r.f. Sputtering	5,000	12	12×10^{20}	4×10^{-4}	95	[6]
r.f. Sputtering	4,000	25	3×10^{20}	8×10^{-4}	-	[7]
Magnetron Sputtering	800	26	6×10^{20}	4×10^{-4}	85	[8]
d.c. Sputtering	1,000	35	9×10^{20}	2×10^{-4}	85	[9]
Reactive Evaporation	2,500	30	5×10^{20}	4×10^{-4}	91	[10]
Ion Beam Sputtering	600	26	2×10^{20}	12×10^{-4}	-	[11]
Spray Pyrolysis	3,000	45	5×10^{20}	3×10^{-4}	85	[12]

Table 2.1: Typical electrical and optical properties of ITO deposited by various techniques

The high conductivity, σ , of ITO films is said to be due to high carrier concentration, N , rather than high Hall mobility, μ_H [1] bearing in mind that resistivity, $\rho = 1/\sigma = 1/(qN\mu_H)$ according to Ohm's law. The observed low mobility of ITO, compared to bulk In_2O_3 , and its dependence on carrier concentration and substrate temperature has been explained in terms of scattering mechanisms due to ionized impurities or grain boundaries. Mobility is said to increase due to enhanced crystallinity of films deposited at higher substrate temperatures [10]. TEM and electron diffraction studies of r.f. sputtered ITO films on glass substrates by Sreenivas *et al* suggest that films grown at room temperature have large stacking faults and represent an amorphous structure [6]; increasing this temperature to 200°C leads to a polycrystalline structure and finally annealing results in near single crystallinity with uniform grain size which leads to increased conductivity. The authors further suggest that deposition of ITO on single crystal substrates, rather than amorphous glass, can enhance the grain growth process.

The direct optical bandgap of ITO films is generally greater than 3.75 eV although a range of values from 3.5 to 4.06 eV have also been reported in the literature [3,13]. The high optical transmittance, T_r , of these films is a direct consequence of their being a wide bandgap semiconductor. The fundamental absorption edge generally lies in the ultraviolet of the solar spectrum and shifts to shorter wavelengths with increasing carrier concentration, N . This is because the bandgap exhibits an $N^{2/3}$ dependence due to the Moss-Burstein shift [14]. The band structure of ITO is assumed to be parabolic as shown in Figure 2.1:

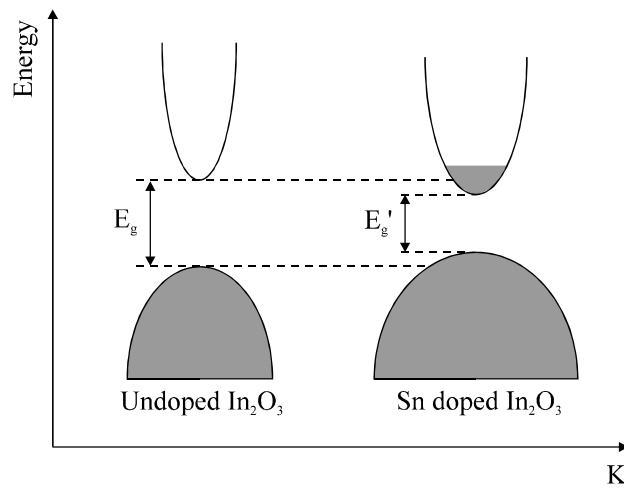


Figure 2.1: Assumed parabolic band structure of undoped In_2O_3 and the effect of tin doping; (After Gupta *et al* [14])

The conduction band is curved upwards, the valence band is curved downwards and the Fermi level is located at mid bandgap for the undoped material; addition of Sn dopants results in the formation of donor states just below the conduction band. As the doping density is increased, these eventually merge with the conduction band at a critical density, n_c , which was calculated to be $2.3 \times 10^{19} \text{ cm}^{-3}$ by Gupta *et al* [14]. Free electron properties are exhibited by the material when the density of electrons from the donor atoms exceeds this value. As Table 2.1 shows, all reported values of carrier concentration are greater than n_c . Hence all ITO films are expected to be degenerate in nature. Once the material becomes degenerate, the mutual exchange and coulombic interactions shift the conduction band downwards and the valence band upwards - effectively narrowing it from E_g to E_g' - as shown in Figure 2.1 earlier. The bandgap increase by the Burstein-Moss shift is partially compensated by this effect.

The reported value for the refractive index of ITO is 1.96 [7]. The transmittance of ITO films is also influenced by a number of minor effects which include surface roughness and optical inhomogeneity in the direction normal to the film surface. Inadvertently grown dark brown (effectively translucent) metallic films of ITO have also been reported. This opaqueness has been attributed to unoxidised Sn metal grains on the ITO surface as a result of instability due to absence of sufficient oxygen during deposition [3,6].

2.1.3 ITO Deposition Techniques

Sputtering, of one form or another, is by far the most extensively used technique for the deposition of ITO. This is closely followed by thermal evaporation - which can also be achieved using several different techniques. ITO has also been prepared by other methods such as Spray Pyrolysis and Screen Printing. The choice of deposition technique is dictated by a number of factors such as quality and reproducibility of the ITO film, homogeneity over a wide cross section, capacity, ease and cost of use as well as detrimental side effects and limitations specific to each technique. In addition, since the properties of ITO depend strongly on the microstructure, stoichiometry and the nature of the impurities present, it is inevitable that each deposition technique with its associated controlling parameters should yield films with different characteristics. Some of these issues will now be discussed briefly.

2.1.3.1 Sputtering

Sputtering involves knocking an atom or molecule out of a target material by accelerated ions from an excited plasma and condensing it on the substrate either in its original or in a

modified form. When this modification is induced by a chemical reaction during the transit from the target to the substrate, the process is referred to as reactive sputtering. In general, most ITO sputter sources consist of hot pressed 90% In_2O_3 : 10% SnO_2 compound targets. The sputtering can be achieved by a number of ways which include accelerating the plasma ions by a d.c. field [9] or a d.c. field combined with a magnet (to direct the high velocity emitted electrons away from the substrate), r. f. (with its self induced bias) as well as by ion beams [11]. Hence names such as magentron [8] and reactive r.f. sputtering [5,6] reflect on the process that has been used for the deposition of the ITO film.

The technique used in the course of this study involves reactive r. f. sputtering in an Ar/O_2 plasma. This method is reputed for its excellent uniformity, high conductivity and high transparency. The r. f. field ensures that sputtering of non-conductive materials can also be achieved at a practical rate. Parameters known to influence ITO quality include sputtering pressure, pre-conditioning, film thickness and r. f. power amongst others. The control of oxygen partial pressure is particularly critical in determining the conductivity and transmittance. However, without the ability to direct unwanted high velocity electrons away from the substrate, damage is associated with this technique; on the other hand magentron sputtering yields high deposition rates and minimises this damage. Detailed description of the system used here is presented in section 3.2 while the detailed optimisation of the deposition parameters is discussed in section 5.1 and elsewhere in the thesis.

2.1.3.2 Thermal Evaporation

Thermal evaporation involves vaporising a solid by heating the material to sufficiently high temperatures and recondensing it on a cooler substrate. The high temperature can be achieved by resistively heating or by firing an electron or ion beam at the boat containing the material to be evaporated. Similarly, reactive thermal evaporation is achieved by introducing oxygen into the chamber during deposition and is one of the most widely and successfully used techniques for good quality ITO depositions [10]. A 95% In - 5% Sn alloy (by weight) is commonly used as the source.

There is no damage associated with resistive thermal evaporation since there are no high velocity particles. Film properties strongly depend on oxygen partial pressure and film thickness [15], deposition rate, substrate temperature and tin concentration [13]. Reports of substrate temperatures being raised from 300°C up to 450°C during evaporation in order to enhance conductivity and transmittance are available in the literature [16].

2.1.3.3 Spray Pyrolysis Technique

Pyrolysis refers to the thermal decomposition of gaseous species at a hot susceptor surface. The spray deposition scheme is particularly attractive because of its relatively fast rate ($> 1000 \text{ \AA/sec}$) and because it does not require a vacuum. The ITO spray is obtained from an alcoholic solution of anhydrous indium chloride (InCl_3) and tin chloride ($\text{SnCl}_4 \cdot 5\text{H}_2\text{O}$) with nitrogen acting as the carrier gas. The spraying is carried out in a furnace, held at 400°C . Critical parameters including positioning of the substrate and the chemical composition of the spray solution. Ashok *et al* [17] have reported resistivities of $1 \times 10^{-3} \Omega\text{cm}$ for a 4200 \AA thick ITO film with transmission greater than 90% at 550 nm while corresponding values obtained by Haitjema *et al* are $3 \times 10^{-4} \Omega\text{cm}$ and 85% respectively [12]. As for most other techniques, this demonstrates an apparent trade-off between the conductivity and the transmittance of ITO films.

2.1.3.4 Screen Printing Technique

This technique is suitable for large scale non-device orientated applications where relatively thick layers of ITO are required such as in liquid crystal displays, blackwall contacts and anti reflection coatings for solar cells [18]. Typically, the deposited thickness varies in the range 10 to $30 \mu\text{m}$ and the post deposition crystallization temperature can be as high as 600°C for a period exceeding an hour. Although the resistivity ($> 4 \times 10^{-4} \Omega\text{cm}$) of the ITO film is said to be comparable to those obtained by other deposition techniques, its transparency is markedly lower ($< 80\%$).

2.2 Schottky Contacts

Although our knowledge of Metal-Semiconductor contacts can be traced as far back as early work by Braun (1874), it was not until 1938 that both Schottky and Mott independently suggested a model for the rectification mechanism. They pointed out that the observed direction of rectification could be explained by supposing that electrons passed over a potential barrier through the normal process of drift and diffusion.

2.2.1 Theory of Rectifying Metal Semiconductor Contacts

The basic theory of these contacts is outlined in the following material. A more comprehensive version was recently reviewed by Rhoderick [19,20]. Figure 2.2 shows a schematic of the band structure of an unbiased metal semiconductor contact.

The Schottky-Mott theory is expressed as follows:

$$\phi_{bo} = \phi_m - \chi_s \quad (\text{eqn. 2.1})$$

where,

ϕ_{bo} = contact barrier height, at zero applied bias

ϕ_m = work function of the metal

χ_s = electron affinity of the semiconductor and is further expressed:

$$\chi_s = \phi_s - (E_c - E_f) \quad (\text{eqn. 2.2})$$

where,

ϕ_s = work function of the semiconductor

E_c = conduction band energy, in eV

E_f = Fermi energy level, in eV

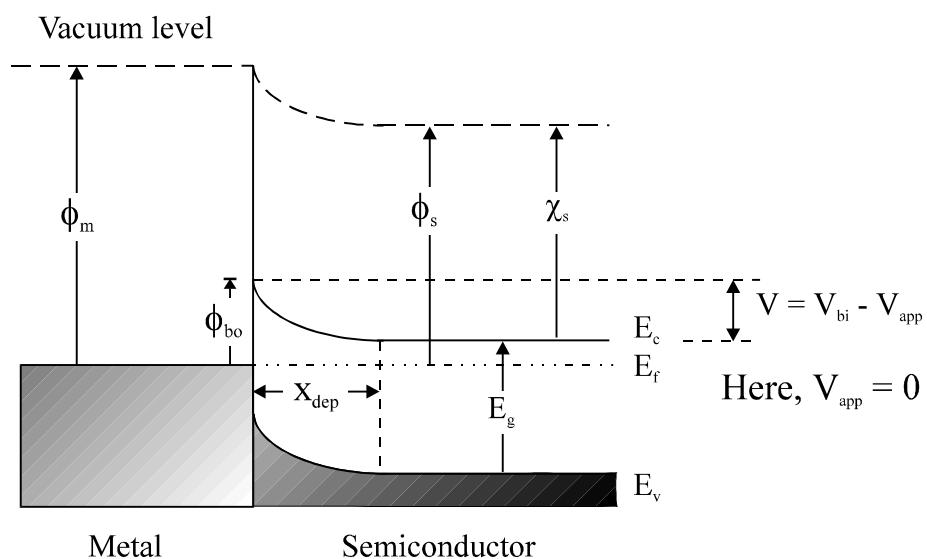


Figure 2.2: Unbiased band structure of a metal/n-type semiconductor contact

ϕ_{bo} is the barrier encountered by electrons in the metal whereas the built-in potential, V_{bi} , encountered by electrons in the semiconductor, is given by:

$$\begin{aligned} V_{bi} &= \phi_m - \phi_s \\ &= \phi_{bo} - (E_c - E_f) \end{aligned} \quad (\text{eqn. 2.3})$$

This theory is rather simplistic in the sense that it assumes ideal conditions where dipole surface contributions to the barrier height and the electron affinity are thought to be unchanged when the metal and the semiconductor are brought into contact. It also assumes that there are no chemical reactions or physical strains created between the two when they are brought into contact.

In practice, however, surface dipole layers do arise. This is because at the surface of a solid the atoms have neighbours on one side only. This causes a distortion of the electron cloud belonging to the surface atoms, so that the centres of the positive and negative charge do not coincide. It was discovered that ϕ_{bo} does not depend on ϕ_m in contradiction to (eqn. 2.1). Thus the assumption of constancy of the surface dipole cannot be justified.

One of the first explanations for the departure of experiment from this theory was given in terms of localised surface states or “dangling bonds”. The surface states are continuously distributed in energy within the forbidden gap and are characterised by a neutral level, ϕ_0 , such that if the surface states are occupied up to ϕ_0 and empty above ϕ_0 , the surface is electrically neutral.

In general, the Fermi level does not coincide with the neutral level. In this case, there will be a net charge in the surface states. If, in addition (and often in practice due to chemical cleaning of the semiconductor prior to processing) there is a thin oxide layer between the metal and the semiconductor the charge in the surface states together with its image charge on the surface of the metal will form a dipole layer. This dipole layer will alter the potential difference between the semiconductor and the metal. Thus the modification to the Schottky-Mott theory is expressed as follows [19]:

$$\phi_{bo} = \gamma(\phi_m - \chi_s) + (1 - \gamma)(E_g - \phi_0) \quad (\text{eqn. 2.4})$$

where,

E_g = bandgap of the semiconductor, in eV

ϕ_0 = position of neutral level (measured from the top of the valence band)

and,

$$\gamma = \frac{\epsilon_i}{\epsilon_i + q\delta D_s} \quad (\text{eqn. 2.5})$$

where,

ϵ_i = permittivity of oxide layer

δ = thickness of oxide layer

D_s = density of surface states

Hence if there are no surface states, $D_s = 0$ and $\gamma = 1$ and (eqn. 2.4) becomes identical to (eqn. 2.1) (the original Schottky-Mott approximation). But if the density of states is very high, γ becomes very small and ϕ_{bo} approaches the value ($E_g - \phi_0$). This is because a very small deviation from the Fermi level from the neutral level can produce a large dipole moment, which stabilises the barrier height by a negative feedback effect [19,20]. When this occurs, the Fermi level is said to be “*pinned*” relative to the band edges by the surface states.

2.2.2 Current transport mechanisms in the Schottky diode

The current transport through the device by emission over the barrier is essentially a two step process: first, the electrons have to be transported through the depletion region, and this is determined by the usual mechanisms of diffusion and drift; secondly, they must undergo emission over the barrier into the metal, and this is controlled by the number of electrons that impinge on unit area of the metal per second. This is expressed in (eqn. 2.6):

$$I = A A^{**} T^2 \cdot \exp\left(\frac{-q\phi_{bo}}{kT}\right) \cdot \left(\exp\left(\frac{V_{eff}}{nkT}\right) - 1\right) \quad (\text{eqn. 2.6})$$

where,

A = cross-sectional area of the metal/semiconductor interface

A^{**} = Modified Richardson constant for metal/semiconductor interface

T = temperature in kelvins

k = Boltzmann constant

q = electronic charge

V_{eff} = effective bias across the interface

n = ideality factor

The ideality factor, n , in (eqn. 2.6) gives a measure of the quality of the junction which is highly process dependent. For an ideal Schottky junction, $n = 1$. In practice, however, larger values are obtained due to the presence of non-ideal effects or components to the current through the junction. This mode of current transport is commonly referred to as the “*thermionic emission*” current [21,22].

where,

I_{gro} = generation-recombination saturation current and is given by:

$$I_{gro} = \frac{qn_i x_{dep} A}{2\tau_o} \quad (\text{eqn. 2.9})$$

where,

n_i = intrinsic carrier concentration of the semiconductor

x_{dep} = depletion width

τ_o = effective carrier lifetime within the depletion width

2.2.2.4 Current due to Quantum Mechanical Tunneling

For a moderately to heavily doped semiconductor or for operation at low temperatures, the current due to quantum mechanical tunneling of carriers through the barrier may become the dominant transport process [21, 24]. For all except very low biases, the tunneling current, I_{tn} , can be represented by:

$$I_{tn} = I_{tno} \left(\exp\left(\frac{qV_{app}}{E_o}\right) - 1 \right) \quad (\text{eqn. 2.10})$$

where,

I_{tno} = tunneling saturation current.

E_o = tunneling constant

The tunneling saturation current is a complicated function of temperature, barrier height and semiconductor parameters. In the notation of Padovani and Stratton [21], E_o is given by :

$$E_o = E_{oo} \coth\left(\frac{E_{oo}}{kT}\right) \quad (\text{eqn. 2.11})$$

where,

E_{oo} = a tunneling parameter inherently related to material properties of the semiconductor and is expressed as:

$$E_{oo} = \frac{qh}{4\pi} \cdot \sqrt{\frac{N_D}{m_n^* \epsilon_o \epsilon_r}} \quad (\text{eqn. 2.12})$$

where,

h = Planck's constant

N_D = impurity doping concentration

m_n^* = effective mass of electron

2.2.2.5 Leakage Current

The leakage current, I_{lk} , is another parallel component of the total current. It is caused by surface leakage and can usually be significantly reduced by various designs and fabrication techniques. In practice, it is the component which appears to by-pass the metal/semiconductor interface altogether and is often thought of as a large leakage resistor, R_{lk} , in parallel to it. Thus the leakage current can be expressed as :

$$I_{lk} = \frac{V_{app}}{R_{lk}} \quad (\text{eqn. 2.13})$$

2.3 Ohmic Contacts

The term "ohmic" refers in principle to a (metal-semiconductor) contact which is non-injecting and has a linear I-V characteristic in both directions. In practice the contact is usually acceptable if it can supply the required current density with a voltage drop that is very small compared to the drop across the active region of the device even though its behaviour may not be strictly linear.

Historically, metal-semiconductor contacts were predominantly used as rectifying contacts until suitable methods of fabricating p-n junctions became available. Then, these contacts began to assume a less significant role as ohmic contacts for transporting current into and out of p-n junctions. With greater understanding and technological advancements, there was a renaissance of the rectifying metal-semiconductor or Schottky contact in the 1960's. At the same time, the need for higher speed devices with their smaller and more complex geometries acted as the driving force behind the search for high performance ohmic contacts.

2.3.1 Theory of Ohmic Contacts

One of the most comprehensive papers that deals with the theory of ohmic contacts to III-V compound semiconductors is that by Rideout [25]. Nearly all practical metal-semiconductor contacts initially result in the formation of depletion layer Schottky barriers as shown in Figure 2.3. As such, they are essentially rectifying to begin with.

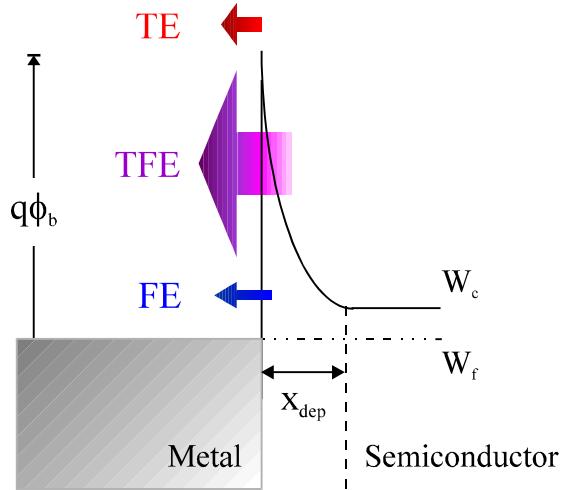


Figure 2.3: Schematic band energy diagram of a metal/n-semiconductor contact showing the three major current transport mechanisms: thermionic emission (TE), thermionic-field emission (TFE) and field-emission (FE).

The conduction properties of these contacts are determined by the actual transport mechanisms, most of which were discussed in section 2.2:

- TE - thermionic emission of carrier, giving rise to rectifying behaviour
- TFE - thermionic field emission or tunneling of hot carriers through the top of the barrier
- FE - field emission or carrier tunneling through the entire barrier (the preferred mode in ohmic contacts)

In addition to these, recombination in the depletion region and the lowering of the barrier due to image force also affect, albeit to a much lesser extent, the behaviour of the ohmic contact. Taking the expressions for the first three dominant mechanisms, the current is determined by [26]:

$$\exp \frac{\phi_b}{kT} \quad \text{for TE} \quad (\text{eqn. 2.14})$$

$$\exp\left[\frac{\phi_b}{E_{00} \coth(E_{00}/kT)}\right] \quad \text{for TFE} \quad (\text{eqn. 2.15})$$

$$\exp\frac{\phi_b}{E_{00}} \quad \text{for FE} \quad (\text{eqn. 2.16})$$

where E_{00} is the tunneling parameter proportional to $\sqrt{N_d}$ (the doping concentration).

Thus, for $kT/E_{00} \gg 1$, TE dominates and the contact is rectifying; for $kT/E_{00} \ll 1$, FE dominates and the contact is ohmic while a mixed mode prevails for the condition $kT/E_{00} \approx 1$. Note that both TE and TFE are temperature dependent while FE is not.

It is seen that there are several possible ways of achieving a good ohmic contact:

- The most common method is to have a layer of very highly doped semiconductor (typically $N_D = 5 \times 10^{18} \text{ cm}^{-3}$ for n-type GaAs) immediately adjacent to the metal giving rise to a very narrow depletion/barrier width ($\approx 100\text{\AA}$). Increased conduction is then dominated by quantum mechanical tunneling.
- Another approach is to have a negligible potential barrier, ϕ_b , to start with. In practice, this is harder to achieve for III-V covalent compounds such as GaAs where ϕ_b is essentially determined by interface states rather than the difference between the work function of the metal and the electron affinity of the semiconductor as theory predicts.
- A third approach is to deliberately increase interface states aimed at reducing contact resistance by causing space-charge recombination to dominate. But, in practice, this has adverse effects on the device stability.

2.3.2 Practical Ohmic contacts

In most practical ohmic contacts the metal layers usually contain a suitable dopant species - donor or acceptor atoms. A heat treatment is used to drive the dopant into the semiconductor to form a n^{++} or p^{++} layer thus creating a tunneling metal-semiconductor junction required for enhanced ohmic behaviour. The quality of an ohmic contact is ultimately assessed by determining its specific contact resistance, ρ_c , as discussed later in section 4.1.

Other desirable properties of ohmic contacts include good adhesion to the semiconductor, smooth surface morphology (particularly where near micron device geometry is concerned), ability to bond gold wires to connect the device to external circuitry and finally contact

reliability. With these in mind, the practical ohmic contact system often consists of a “wetting agent” to promote adhesion, followed by the dopant species and finally a thick layer of Au for bonding purposes. Where indiffusion of the top Au poses potential reliability hazards, often a diffusion barrier is inserted between the gold and the dopant layer.

The most commonly used n-type contacts to GaAs is the Ni/AuGe/Ni/Au system. Thus many studies have been carried out to determine its alloying behaviour [27], effect of varying Ge (the dopant species) content [28] as well as investigation of the semiconductor surface cleanliness prior to metalisation [29]. However, this system has several ill effects such as “balling up” during annealing as a result of liquid phase reactions, non-uniform contact resistivity and vertical and lateral spiking. An alternative which addresses many of these issues is the Pd/Ge/Au system [30,31].

The usual p-type contact for GaAs is the Au/Zn/Au system [32] where Zn atoms act as acceptors. In devices such as HBTs base is very thin ($>1000\text{\AA}$); hence junction shorting due to Au spiking is often more of a concern than the resistivity, especially for high temperature or high current applications. In this case, Pt/Ti/Au is used as an alternative [33] although there are no dopant species. It is argued that since the base doping is already very high ($N_A > 5 \times 10^{19} \text{ cm}^{-3}$) the need for extra acceptor atoms is diminished.

Pd/Ge based systems are known to have been used as both n and p-type contacts to InGaAs layers [34]. As in p-GaAs, Zn atoms also act as acceptors in p-InGaAs [35].

2.4 Heterojunction Bipolar Transistors

The idea behind the heterojunction bipolar transistor (HBT) is as old as the transistor itself. It was proposed by W. Shockley in 1948 and subsequently patented by him in 1951 [36]. However it was H. Kromer [37], who is credited with developing the detailed theory and analysis of HBTs leading up to its present day status in semiconductor electronics and integrated circuit applications.

2.4.1 Heterostructure Concepts

Kromer’s Central Design Principle (CDH) of heterostructure devices uses the energy gap variations in addition to electric fields as forces acting on electrons and holes, to control their distribution and flow [38]. Therefore, by carefully selecting the appropriate bandgap and the

electric fields, it becomes possible (within limits) to control the forces acting on electrons and holes, *separately and independently of each other* - a design freedom not rendered by homostructures. With the evolution of more and more advanced growth technologies such as MBE and MOCVD, a change in semiconductor (and hence in energy gap) is not significantly harder to achieve than a change in doping level.

In a practical HBT, the emitter consists of a wide bandgap material (e.g. AlGaAs, InGaP or InP) while the base is a narrow bandgap material (e.g. GaAs or InGaAs). The band energy diagram for such an emitter-base heterojunction, before and after the two materials are brought into contact, is depicted in Figure 2.4a and b respectively.

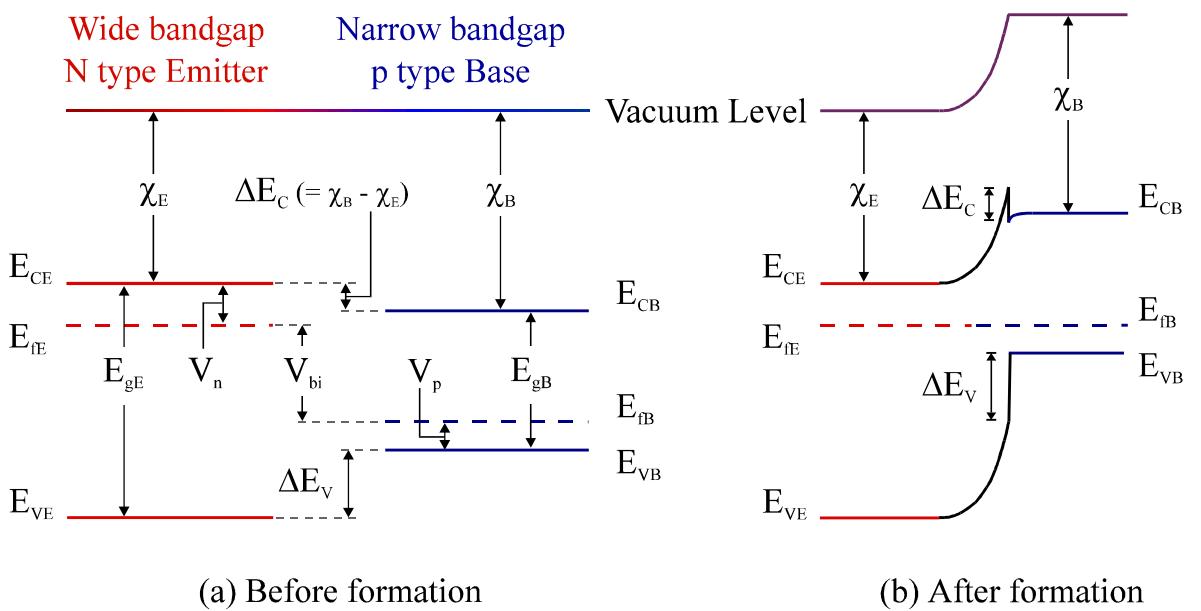


Figure 2.4: Energy band diagram of a wide bandgap N-type emitter and a narrow bandgap p-type base heterojunction at equilibrium (a) before and (b) after formation.

As in homojunctions, once contact is made the conduction and valence bands join in a manner such that the Fermi levels align. However, since the electron affinities of the emitter and the base, χ_E and χ_B respectively, are different in heterojunctions a discontinuity in the conduction band, ΔE_c , appears. Analytically, this is given by:

$$\Delta E_c = \chi_B - \chi_E \quad (\text{eqn. 2.17})$$

Since, the bandgap energies are different, a discontinuity in the valence band, ΔE_v , also appears. The total bandgap discontinuity, ΔE_g , is the sum of the discontinuities in the conduction and valence bands:

$$\Delta E_g = \Delta E_c + \Delta E_v \quad (\text{eqn. 2.18})$$

In the HBT a large ΔE_c is undesirable as it acts as an extra barrier to electron injection from the emitter to the base thereby requiring a high emitter-base forward bias voltage, V_{be} , (typically 1.3V) [39]. This ultimately limits the device current gain far below that expected from an HBT [38]. By the same analogy, a large ΔE_v is ideal as it limits reverse injection of holes from the base into the emitter. Table 2.2 lists some of the band discontinuities of common HBT systems. Thus a large $\Delta E_v / \Delta E_c$ ratio is desirable.

HBT Material Structure	ΔE_c (eV)	ΔE_v (eV)	ΔE_g (eV)	$\Delta E_v / \Delta E_c$	Ref. no.
$\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$	0.24	0.13	0.37	0.54	[40]
$\text{In}_{0.5}\text{Ga}_{0.5}\text{P}/\text{GaAs}$	0.19	0.29	0.48	1.53	[41, 42, 43]
$\text{InP}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	0.25	0.34	0.59	1.36	[44]

Table 2.2: Band discontinuities for common HBT material heterostructures

Heterojunctions, such as InGaP/GaAs which naturally exhibit relatively large ΔE_v compared to their ΔE_c , are more advantageous than AlGaAs/GaAs. However, since AlGaAs is lattice matched to GaAs for all fractions of Al, it is possible to reduce or even remove this conduction band discontinuity by compositionally grading the mole fraction of Al in the emitter material immediately (few hundred angstroms) before the GaAs base [45]. This helps lower the V_{be} by 150mV compared to that in the non-composition graded emitter HBTs. However, it should be noted that the bandgap of AlGaAs becomes indirect once the Al mole fraction is raised above 50%, and thus is not of interest from a device application point of view.

Using Figure 2.4 the built-in potential, V_{bi} , for a heterostructure can be derived as follows:

$$E_{gE} - V_n = \Delta E_v + V_p + V_{bi} \quad (\text{eqn. 2.19})$$

where,

E_{gE} = emitter bandgap in eV

V_n = potential difference between the bottom of conduction band and Fermi level

V_p = potential difference between Fermi level and the top of valence band

Expressing V_n and V_p in terms of emitter and base doping levels, N_{DE} and N_{AB} , and the respective density of states in emitter conduction band and base valence band, N_{cE} and N_{vB} , we obtain:

$$V_n = (E_{cE} - E_{fE}) = - \frac{kT}{q} \ln\left(\frac{N_{DE}}{N_{cE}}\right) \quad (\text{eqn. 2.20})$$

and,

$$V_p = (E_{fB} - E_{vB}) = - \frac{kT}{q} \ln\left(\frac{N_{AB}}{N_{vB}}\right) \quad (\text{eqn. 2.21})$$

Combining (eqn. 2.18) to (eqn. 2.21), we obtain:

$$V_{bi} = E_{gE} + \frac{kT}{q} \ln\left(\frac{N_{DE}}{N_{cE}}\right) - \Delta E_g + \Delta E_c + \frac{kT}{q} \ln\left(\frac{N_{AB}}{N_{vB}}\right) \quad (\text{eqn. 2.22})$$

But,

$$\Delta E_g = E_{gE} - E_{gB} \quad (\text{eqn. 2.23})$$

Hence,

$$V_{bi} = E_{gB} + \Delta E_c + \frac{kT}{q} \ln\left(\frac{N_{DE} N_{AB}}{N_{cE} N_{vB}}\right) \quad (\text{eqn. 2.24})$$

2.4.2 Current Transport in HBTs

The operating principle of a (n-p-n) bipolar transistor consists of electron injection from the emitter into the base and their subsequent collection by the collector. Figure 2.5 shows the energy band structure of an N-p-n HBT with wide-gap emitter, with the various current components, and the hole repelling effect of the additional energy gap in the emitter. The band energies are expressed in joules; thus bandgap is expressed using W_g rather than E_g . In this case it is assumed that the emitter junction has been graded sufficiently to obliterate any band edge discontinuities or even any non-monotonic variations of the conduction band edge.

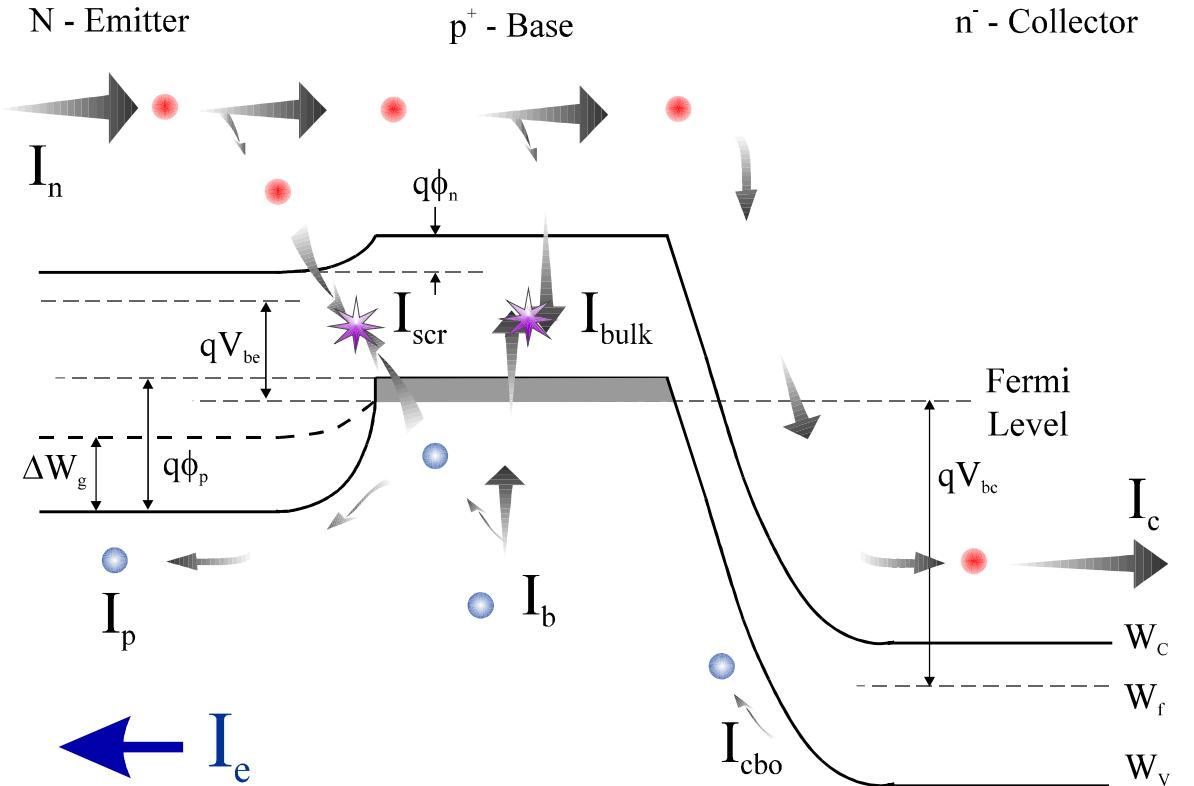


Figure 2.5: Band diagram of an N-p-n HBT biased in emitter ground configuration.

There are the following injection related dc currents flowing in such a transistor:

1. A current I_n of electrons injected from the emitter into the base;
2. A current I_p of holes injected from the base into the emitter;
3. A current I_{scr} due to electron-hole recombination within the forward biased emitter-base space-charge layer.
4. A small part, I_{bulk} , of the electron injection current, I_n , is lost due to bulk recombination in the base.
5. A small thermally generated minority hole current from the n-type collector, I_{cbo} , flows into the base from the reverse biased base-collector junction.

$$\text{Emitter current, } I_e = I_n + I_p + I_{scr} \quad (\text{eqn. 2.25})$$

$$\text{Collector Current, } I_c = I_n - I_{bulk} + I_{cbo} \quad (\text{eqn. 2.26})$$

$$\text{Base Current, } I_b = I_p + I_{bulk} + I_{scr} - I_{cbo} \quad (\text{eqn. 2.27})$$

The device operation mainly depends on current contribution I_n while the other components are strictly nuisance currents, as are capacitive currents (not shown above) that accompany voltage changes. The effect of the space charge recombination current, I_{scr} , on the transistor

performance has been explained elsewhere by Morgan *et al* [46]. Since the base thickness, w_b , is much smaller than the electron diffusion length, L_{nB} , in the base, I_{bulk} is very small. Similarly, any currents due to electron-hole pair generation in the collector depletion layer, I_{cbo} , are also insignificant and can be ignored at this stage. Expressed in terms of the dc current gain, β :

$$\beta = \frac{I_c}{I_b} = \frac{I_n - I_{bulk} + I_{cbo}}{I_p + I_{bulk} + I_{scr} - I_{cbo}} \quad (\text{eqn. 2.28})$$

and,

$$\beta_{\max} = \frac{I_n}{I_p + I_{scr}} \quad (\text{eqn. 2.29})$$

β_{\max} is the highest possible value of β in the limit of various negligible recombination and other minor currents; in fact, it is the improvement in β_{\max} to which the wide-gap emitter idea addresses itself. This can be expressed in terms of the electron and hole injection current densities, J_n and J_p [38]:

$$J_n = N_{DE} v_{nB} \exp\left(\frac{-q\phi_n}{kT}\right) \quad (\text{eqn. 2.30})$$

$$J_p = N_{AB} v_{pE} \exp\left(\frac{-q\phi_p}{kT}\right) \quad (\text{eqn. 2.31})$$

where,

$q\phi_n$ and $q\phi_p$ = potential energy barrier heights for electrons and holes at the B-E junction
 v_{nB} and v_{pE} = mean speeds (due to the combined effects of drift and diffusion) of electrons at the emitter end of the base and holes at the base end of the emitter respectively.

The above equations are often expressed in terms of diffusion current effects only:

$$J_n = \frac{qN_{DE} D_{nB}}{w_b} \exp\left(\frac{-q\phi_n}{kT}\right) \quad (\text{eqn. 2.32})$$

$$J_p = \frac{qN_{AB} D_{pE}}{L_{pE}} \exp\left(\frac{-q\phi_p}{kT}\right) \quad (\text{eqn. 2.33})$$

where,

D_{nB} , D_{pE} = minority carrier diffusion coefficients in the base and emitter respectively
 L_{pE} = hole diffusion length in the emitter region

If the band gap of the emitter is larger than that of the base by ΔW_g , we have :

$$q(\phi_p - \phi_n) = \Delta W_g \quad (\text{eqn. 2.34})$$

Hence,

$$\frac{I_n}{I_p} = \beta_{\max} = \frac{N_{DE} V_{nB}}{N_{AB} V_{pE}} \exp\left(\frac{\Delta W_g}{kT}\right) \quad (\text{eqn. 2.35})$$

or in terms of diffusion currents only,

$$\beta_{\max} = \frac{N_{DE} D_{nB} L_{pE}}{N_{AB} D_{pE} W_b} \exp\left(\frac{\Delta W_g}{kT}\right) \quad (\text{eqn. 2.36})$$

Of the three variables in (eqn. 2.35), V_{nB}/V_{pE} is least subject to manipulation; hence, for a large β_{\max} , we need either $N_{DE} \gg N_{AB}$ or ΔW_g to be several times larger than kT . Since bandgap differences many times greater than kT is readily obtainable, very high values of I_n/I_p can be achieved almost regardless of the doping ratio. Therefore, the hole injection current I_p becomes negligible and $I_b \equiv I_{scr} + I_{bulk}$. For a useful, transistor we must still have $I_{bulk} \ll I_n$. If we approximate I_e by I_n , we obtain:

$$\beta = \frac{I_n}{I_{scr} + I_{bulk}} \quad (\text{eqn. 2.37})$$

In contrast to homojunction transistors, in a properly designed high gain HBT, the interface recombination current component I_{scr} , can be as small as $I_n/10^3$ making I_{bulk} the dominant part of I_b . Hence, I_{scr} is neglected beside I_{bulk} ; the bulk recombination current density may be written as [38]:

$$J_{bulk} = \gamma n_e(0) \frac{W_b}{\tau_n} \quad (\text{eqn. 2.38})$$

where,

$n_e(0)$ = the injected electron concentration at the emitter end of the base

τ_n = average electron life time in the base

γ = a factor between 0.5 and 1 indicating how much electron concentration in the base differs from the electron concentration at the emitter end of the base.

Thus combining (eqn. 2.30), (eqn. 2.37) and (eqn. 2.38) and making the necessary substitutions, we may write the gain as follows :

$$\beta = \frac{1}{\gamma} \frac{V_{nb}\tau_n}{w_b} \quad (\text{eqn. 2.39})$$

This depends on the base doping only through the effect of the base doping on the lifetime; for heavy base doping levels, the life times may be short [47]. Evidently no serious problems from reduced minority carrier lifetimes arise unless the latter drop to the vicinity of 10^{-10} s or lower, at least not for plausible base widths not exceeding 1000Å.

2.4.3 Fundamental Advantages of HBTs

Some of the key benefits of HBTs can be summarised as follows [48]:

- Low base resistance, R_b , as dopings of 10^{19} cm^{-3} can be used without increasing the hole reverse injection into the emitter
- High base doping ensures that when the base-collector reverse bias is increased, there is minimum change in the base width making the device suitable for high power application
- Lower emitter-base capacitance since wide band gap emitters no longer need to be more highly doped than the base; in microwave application, a lower emitter capacitance reduces the noise figure significantly
- In turn these enhance the high speed performance of HBTs as f_{max} , the maximum oscillation frequency, is proportional to $\sqrt{1/R_b}$.
- Since speed determining part of the current path is perpendicular to the surface, and to the first order the speed is determined by the layer thickness which can easily be made much smaller than horizontal dimensions, there is an inherent higher speed potential in bipolar structures than in Field Effect Transistors (FETs).
- For digital switching applications, in HBT based circuits, better threshold voltage control is ensured since in these devices this is dependent on the bandgap of the base and the emitter materials rather than doping dependent as in MESFETs.

2.4.4 Abrupt Emitter-Base HBT

A conduction band discontinuity, ΔE_c , exists in the abrupt emitter-base heterojunction as shown in Figure 2.6. Since in a practical HBT, $N_{AB} \gg N_{DE}$, this discontinuity appears close

to the base leading to a potential barrier ΔE_b . In addition there is also an insignificant conduction band notch on the base side, ΔE_n ; thus, $\Delta E_c \approx \Delta E_b$.

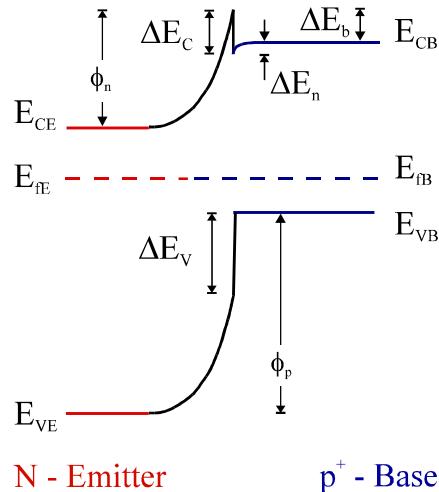


Figure 2.6: Band diagram of an abrupt emitter/base heterojunction

Hence, for an abrupt junction, (eqn. 2.34) is modified to:

$$q(\phi_p - \phi_n) = q(\Delta E_c + \Delta E_v - \Delta E_b) \approx q(\Delta E_v) = \Delta W_v \quad (\text{eqn. 2.40})$$

Hence (eqn. 2.35) is also modified and the β for a HBT with an abrupt emitter-base junction is now given by:

$$\beta_{\text{abrupt}} = \frac{N_{DE} V_{nb}}{N_{AB} V_{pe}} \exp\left(\frac{\Delta W_v}{kT}\right) \quad (\text{eqn. 2.41})$$

or,

$$\beta_{\text{abrupt}} = \frac{N_{DE} D_{nb} L_{pe}}{N_{AB} D_{pe} W_b} \exp\left(\frac{\Delta W_v}{kT}\right) \quad (\text{eqn. 2.42})$$

2.4.5 Common III-V HBT Material Systems

Among all the GaAs-based materials used for HBTs, the most investigated combination has been the AlGaAs/GaAs system which exhibits high current gain, high f_T and f_{\max} . However, the InP-based lattice matched systems, in particular InP/InGa_{0.53}As_{0.47} came into contention primarily because of its bandgap of 0.75eV which is sensitive to 1300nm and 1550nm wavelengths - wavelengths which correspond to the low loss windows of optical fibers and

universally used for long haul optical fiber telecommunications. Apart from the high current driving capacity of HBTs, the material compatibility that the InP/In_{0.53}Ga_{0.47}As system allows, one can monolithically integrate HBTs with other optoelectronic devices. Also its superior transport properties with respect to the AlGaAs/GaAs system makes it one of the strongest competitors.

The material band alignments for various materials for HBTs were shown in Table 2.2. ΔE_v for the InP/InGaAs heterojunction is much larger than its ΔE_c allowing a high injection efficiency without compromising the base doping level. Extremely high doping ($N_{AB} > 10^{20} \text{ cm}^{-3}$) has been achieved in InGaAs by GSMBE using Be as the p-type base dopant [49]. High frequency performance is also expected for InGaAs/InP HBTs due to the high electron mobility of InGaAs. In addition, the large Γ -X and the Γ -L inter-valley separation ($\Delta E^{\Gamma-X} = 1.0 \text{ eV}$, $\Delta E^{\Gamma-L} = 0.55 \text{ eV}$) in InGaAs allows large collector voltage swing with high peak carrier velocity. Furthermore, the surface recombination velocity associated with InGaAs, which is 10^3 lower compared to that of GaAs [50], enables the development of transistors with high current gain but insensitive to collector current density and emitter dimension; thus allowing the latter to be scaled to the sub-micrometer regime.

2.5 Optoelectronic Devices

The performance of an optical link is largely determined by the detector which constitutes one of the dictating elements. Early optical detectors were based on Si which is sensitive to 0.8 to 0.9 μm and compatible with AlGaAs/GaAs lasers and LEDs. As detection at longer wavelengths (1.1 to 1.6 μm) became necessary, devices based on Ge and III-V compounds became available and research is underway to develop III-V detectors for yet longer wavelengths. This section focuses on the factors behind the evolution of modern optoelectronic devices, basic detector and transmitter operation, the key parameters relating a photodetector to a system, photo receiver configurations and a summary of various detector types with their advantages/disadvantages and typical published performance parameters.

2.5.1 The Case for Fiber-Optic Telecommunication

Immense growth in the telecommunication market has forced large consortium of companies to develop advanced networks and systems based on several aspects of this field: digital signal processing, networks, transmission media, systems and finally components - implementation of novel and highly advanced monolithic optoelectronic integration technology [51].

In the early days of distant telecommunication using modulated microwaves in the 1920's, the links were generally limited to 'line of sight' distances ($\approx 30\text{km}$). Thus orbiting satellites were needed to relay information over long distances. Today most of these are in geo-stationary orbits (35,800 km above the earth) with only three satellites necessary for continuous coverage to any point on the globe [52]. However, signals are weakened by several orders after travelling these large distances thus requiring high gain antennas and powerful transmitters. A more pertinent problem is the delay and echo in long distance phone calls using these satellites.

The accommodation large traffic requires the use of higher frequency bands. Commercial satellites have been allocated 6 GHz and 4 GHz frequencies for up-links and down-links. Other frequencies include the 12/14 GHz and 20/30 GHz bands for down-links/up-links. But, some of the fundamental limitations of satellite communication systems at frequencies greater than 10 GHz result from a strong interaction of radio waves with rain and ice in the lower atmosphere forcing its capacity to be halved during a rainy period. Also a substantial number of terrestrial relays are required between the exchange and the satellite ground station.

Real interest in optical communication was aroused with the invention of the laser in early 1960's and proposals for using dielectric waveguides or optical fibers to avoid degradation of the light while propagating, were made almost simultaneously in 1966. Although early systems were lossy (1000 dB/km), today attenuation of less than 0.2 dB/km is easily achieved for a carrier wavelength of $1.55\mu\text{m}$ [53] - a point that lies at the bottom of the lowest fiber transmission loss window as shown in Figure 2.7.

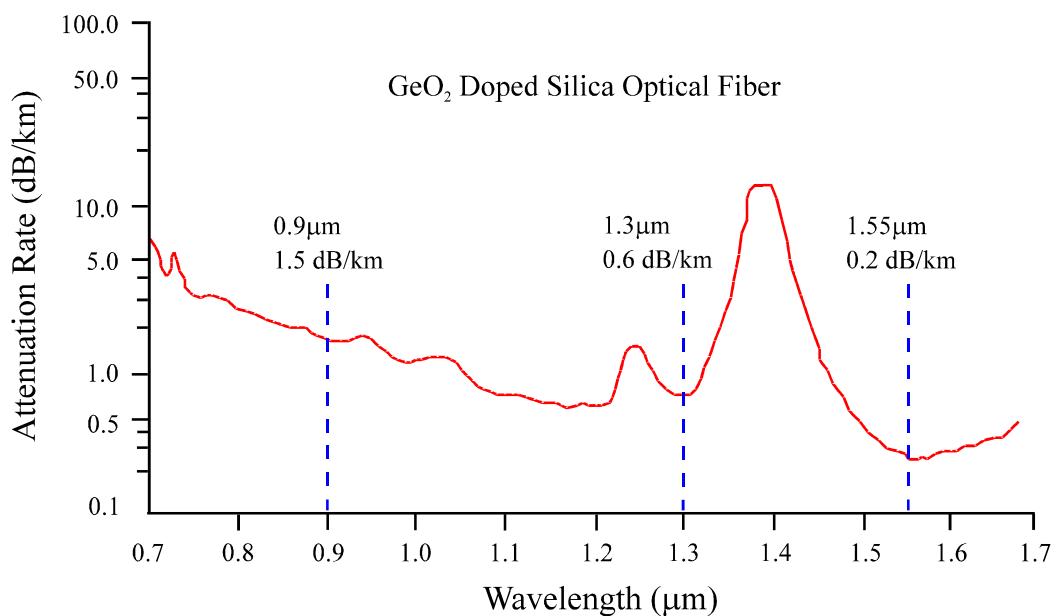


Figure 2.7: Loss Characteristics of a Silica Optical Fiber showing the three wavelengths of interest. (After Miya *et al* [53])

This formed the single most influential factor in determining the course of further developments. Thus majority of today's long haul transmission and receiver systems are geared for operation at the $1.55\text{ }\mu\text{m}$ wavelength. Unlike some of its predecessors, fiber optics technology has many unrivaled advantages [54]:

- *Enormous potential bandwidth*: the optical carrier frequency in the range 10^{13} to 10^{14} Hz offers the potential capacity (bandwidth $\approx 40,000\text{ GHz}$) that is many orders of magnitude greater than the copper cable ($< 1\text{ GHz}$) or microwave radio ($< 300\text{ GHz}$) systems.
- *Low transmission loss*: with losses as low as 0.2 dB/km , this feature has become a major advantage of optical fiber as large repeater spacings (70 to 100 km) may be used in long-haul systems reducing both cost and complexity. Given their bandwidth capability this property provides a totally compelling case for the adoption of optical fiber communication in the majority of long-haul telecommunication applications.
- *Small size and weight* : an optical fiber is often no wider than $50\mu\text{m}$; thus even after applying several protective layers, they are far smaller and much lighter than corresponding copper cables. This is a tremendous boon to alleviating duct congestion in cities.
- *Immunity to interference and cross talk*: they form a dielectric and are free from electromagnetic interference making it easy to reduce optical interference and cross talk.
- *Signal security*: as light from a fiber does not radiate significantly, a transmitted optical signal cannot be obtained non-invasively.
- *System reliability and ease of maintenance*: due to the low loss property, system reliability is generally enhanced in comparison to conventional electrical conductor systems.

By the mid 1990's, up to 60% of the global telecommunication traffic was said to have been carried over optical fibers [55] and expected to rise to 85% by the millennium. Intercity systems based on optical fibers and using digital transmission with pulse rates ranging from a few hundred Mbit/s to about 2Gbit/s have now been widely implemented. Shorter wavelengths, 820 to 890 nm, are used in short distance links where the higher fiber loss is offset by the low-cost LED/lasers and Si photo diodes which are adequately sensitive.

2.5.1.1 Submarine Optical Fiber Systems

In 1858 the first transatlantic cable was laid for telegraphy and transmitted less than a few words per minute. In 1956, the first analog transatlantic telephone cable (TAT-1) became operational and carried 36 voice channels [56]. The analog TAT family grew with further

development and the last such cable, TAT-7, carrying 4200 channels per co-axial cable was fully operational by 1983.

However, an increasing demand by the mid 1980's for reliable intercontinental telecommunication resulted in the introduction of submarine optical fiber based systems [57,58] later that decade. High capacity cables using a carrier wavelength of $1.3\text{ }\mu\text{m}$ were laid under the Atlantic (TAT-8) and the Pacific oceans (TPC-3) respectively. These can transmit data at 280 Mbit/s per fiber pair; they formed part of the first generation digital lightwave systems [59]. The second generation cables (TAT-9 to TAT-11 and TPC-4) using a carrier wavelength of $1.5\text{ }\mu\text{m}$ and with enhanced transmission rate of 560 Mbit/s per fiber pair are now in operation while the third generation cables (TAT-12 and 13 and TPC-6) are just being commissioned. The latter, using dispersion shifted fibers and a carrier wavelength of $1.55\text{ }\mu\text{m}$, will implement the first fully optical system using erbium doped fiber amplifiers (EDFAs). The second and third generation cables have extended digital connectivity to the South Pacific, South East Asia and other points [60]. Two such global optical fiber systems are the "SEA-ME-WE-2", a 560 Mbit/s second generation system, and the FLAG, a third generation system with a maximum expected capacity of 5 Gbit/s.

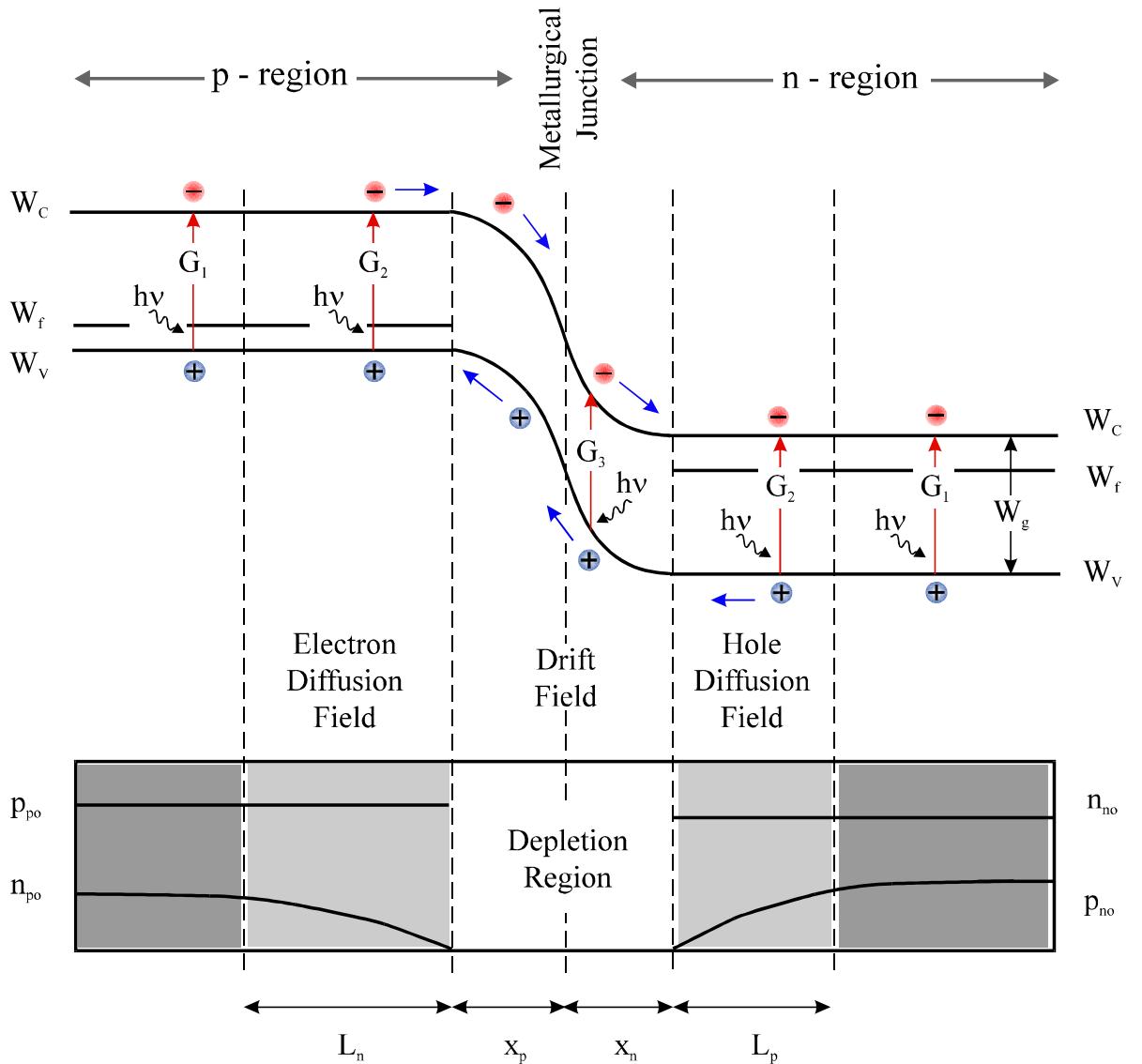
2.5.2 Optical Detection Principles

Photo detection involving electron excitation from the valence band to the conduction band is referred to as intrinsic absorption while those involving impurity centres within the material is known as extrinsic absorption. However, due to its associated efficiency and fast response it is the former process which is of general interest [61].

In reviewing the basic concepts of photo detection in a p-n junction, it will be shown that only the detectable photo generated electron hole pairs are the ones which give rise to a photo current, I_{Ph} , in the external circuit of a detector. In order for I_{Ph} to have maximum effect in a device, it has to cause maximum change in the output. Although a p-n junction can sense a photo current under forward bias it is over shadowed by the bias dependent thermionic emission current component. Therefore, p-n junction photo detectors operate under reverse bias conditions where all other significant current components are very small and bias independent.

The schematic electron energy band diagram and the spatial carrier concentration diagrams for a p-n junction photo detector are shown in Figure 2.8a and b respectively. The diode is under reverse bias and is illuminated by a super bandgap radiative energy.

(a) Electron energy diagram



(b) Carrier concentration diagram

Figure 2.8: Schematic diagrams of a reverse biased p-n junction showing intrinsic photo generation processes

Here energy levels are expressed in joules using the notation W (rather than in eV, using E); other symbols have the following meanings:

x_n = depleted n-region

p_{po} = majority carrier conc. in p-region

x_p = depleted p-region

n_{no} = majority carrier conc. in n-region

L_n = electron diffusion length

n_{po} = minority carrier conc. in p-region

L_p = hole diffusion length

p_{no} = minority carrier conc. in n-region

In order for photo generation to occur, the incident radiation must consist of photons with super bandgap energy, $h\nu$. Also, the radiation must enter the semiconductor material to energetically promote a valence band electron into the conduction band thereby creating an electron-hole pair. The significance of penetration by the incident radiation is discussed in detail in Section 6.3 of this thesis. Assuming the above conditions are met, Figure 2.8 shows that the photo generation can take place in the bulk of either the p or the n regions - depicted by transition G_1 , in the regions between the bulk and the depletion region - depicted by transition G_2 or indeed in the depletion region itself - depicted by transition G_3 . Each of these three transitions will now be discussed.

If the absorption of an incident photon results in transition G_1 the photo generated electron hole pairs in the bulk will randomly scatter within the p or the n-type regions until they recombine as dictated by their respective lifetimes τ_n and τ_p . This is because they do not experience electric field in the neutral bulk region. Therefore, these will not contribute to a current in the external circuit and are of little use - these cannot be detected.

If the photon penetrates deeper into the material and is absorbed giving rise to transition G_2 , it will create an electron-hole pair within a diffusion length from the high field depletion region. In the p-region the electrons will be the minority carriers while in the n-region, the minority carriers will be the holes. The diffusion length may be described as the average distance that a minority carrier diffuses in a medium prior to recombining with a majority carrier; conversely, it is the distance in which an excess (in this case brought about by photo generation) minority concentration is reduced to $1/e$ of its peak value. The respective diffusion lengths can be calculated using (eqn. 2.43) and (eqn. 2.44) as follows :

$$L_n = \sqrt{D_n \tau_n} \quad (\text{eqn. 2.43})$$

$$L_p = \sqrt{D_p \tau_p} \quad (\text{eqn. 2.44})$$

where,

D_n = diffusion constant for electrons ($= \mu_n kT/q$)

τ_n = electron lifetime

D_p = diffusion constant for holes ($= \mu_p kT/q$)

τ_p = hole lifetime

Therefore, if a G_2 transition takes place in the p-region, the minority electrons experiencing the concentration gradient or the diffusion field will “diffuse” into depletion region boundary. Once it reaches the depletion region, it will fall under the influence of the high drift field

which will sweep it across to the n-region. An electron traversing the junction contributes a charge q^- to the current flow in the external circuit. Similarly, a G_2 transition in the n-region will cause a photo generated hole to traverse the junction and give rise to another component of the photo current.

Finally a G_3 transition will cause both the photo generated electron and hole to give rise to a drift current; the electron will traverse to the reverse biased n-region while the hole to travel in the opposite direction. Since each carrier traverses a distance which is less than the full junction width, the contribution of this process to charge flow in the external circuit is q^- .

In practice, the last process is the most desirable since each absorption gives rise to a charge q^- and delayed current response caused by finite diffusion time is avoided.

2.5.2.1 The Key Parameters Relating a Photodetector to an Optical System

Some of the key parameters which relate a photo detector to the ultimate system where it is applied include its sensitivity, dynamic range, quantum efficiency, responsivity, internal gain, bandwidth and noise. The basic goal is to achieve the lowest possible noise at a given bandwidth or data rate.

The sensitivity of a photo detector is defined as the minimum mean optical power needed to achieve a given bit error rate, BER (CCITT standard requires a BER of 10^{-10}). The exact expressions for sensitivity vary according to the particular type of detector. Its dynamic range is the range of input power levels over which the BER is acceptable [62]. The quantum efficiency, η , and the responsivity, R , are interlinked; the η is essentially the efficiency of converting an incident photon (optical power) into useful photo current, I_{Ph} , whereas the R is the amount of I_{Ph} obtained for a unit of incident optical power, P_o . These last two parameters are wavelength dependent as discussed later in section 4.5. The internal gain of a detector refers to the generation of secondary electron-hole pairs created by the primary photo generated pair as in Avalanche Photo Diodes (APDs) or the electrical gain, β , of bipolar transistor based photo detectors. The bandwidth, B , refers to the range of frequencies over which the detector provides useful output at a pre-defined level (e.g. 3dB). Finally, the noise is a term which refers to spurious output in the absence of light; thus thermally generated dark current and surface and other leakage currents all add to this unwanted “signal” and contribute to the noise which essentially limits the sensitivity of the detector [61]. Terms often used to quantify this complex parameter include “signal to noise ratio” (SNR) and “noise equivalent power” (NEP) which is the incident optical power, at a given wavelength, necessary to obtain a I_{Ph} equivalent to the rms noise current within a unit bandwidth B .

There is often a fundamental trade-off between the sensitivity and the bandwidth of a detector. For example, in the case of a p-i-n detector with a FET pre-amplifier, a large resistor may be needed to extract a useful voltage to drive the gate of the FET. In doing so, however, the RC constant becomes large which limits the bandwidth of the receiver.

2.5.3 p-n, p-i-n and Avalanche Photo Diodes (APDs)

Photo diodes can be broadly categorised into two types: those without internal gain such as p-n and p-i-n diodes and those with such as APDs. The penetration depth of light before it is absorbed within a material increases with its wavelength (see section 6.3). Thus a wider depletion region is necessary for long wavelength operation. In the p-n junction, this is achieved by making the n-type material so lightly doped that it can be considered intrinsic; an n^+ layer is added to reduce ohmic contact. This modified device is known as a p-i-n photo diode [61]. The intrinsic layer is wide enough to maximise absorption for a given wavelength and the low doping means it is fully depleted under normal reverse bias resulting in fast collection of photo generated electron hole pairs. Due to the spectral limitations of Si and thermal instabilities and large dark currents associated with Ge, p-i-n diodes have been designed and fabricated using InGaAs which are sensitive over 0.95 to 1.65 μm wavelength range [63] and have dark currents in the pA range at room temperature [64]. Substrate entry heterojunction p-i-n based on InGaAs p^+ and i layers and InP n layers have been used to eliminate absorption in the top p^+ layer. However, this design suffers from charge trapping in the InGaAs/n-InP heterointerface although it is not a severe limitation to its performance [65].

In Avalanche Photo Diodes (APD), the structure of the basic p-n diode is further modified to create an extremely high electric field; the APD consists of a n-p-i- p^+ type layer structure. In addition to the depletion n-p region where majority of absorption takes place, the high field region (i region) accelerates the primary photo generated pairs to acquire sufficient energy to excite new electron-hole pairs by impact ionization [61]. This is known as carrier multiplication; hence these devices have inherent gain. In order to minimise noise, the electric field at avalanche breakdown must be as low as possible. In Si, this has been achieved by using a reach through structure (RAPD) where the multiplication region is much wider than the n-p region. Much of the material problems associated with Si and Ge p-i-n diodes are also relevant to APDs and heterojunction devices have been realised using various compound semiconductor material systems including InGaAs/InP. However, the narrow bandgap of InGaAs gives rise to unacceptably high level of band-to-band defect tunneling currents which precede avalanche field. In common with the Si RAPD, this problem is significantly reduced by using a separate absorption and multiplication region in the SAM-

APDs with the gain occurring at InP p-n junction where tunneling is much less [66]. As in InGaAs/InP p-i-n, the issue of charge trapping at the heterointerface discontinuity is also a limitation in these APDs. However, Campbell *et al* [67] have reported the use of a InGaAsP (with a bandgap located between InGaAs and InP) quaternary grading layer to smooth out the discontinuity and hence improve speed performance in separate absorption, grading and multiplication (SAGM) APDs. Noise arising from multiplication region in APDs has been addressed by Capasso *et al* [68] by incorporating a super lattice structure (SL) in AlGaAs/GaAs and Kagawa *et al* [69] in the InGaAs/InAlAs SL-SAM-APDs.

2.5.4 ITO/n-GaAs Schottky Photo Diodes

The use of a Schottky barrier photo diode has many advantages for very high speed applications. In common with a conventional p-i-n detector, the absorption layer thickness can be engineered to obtain the optimum compromise between external quantum efficiency and detector bandwidth. An advantage however, is that there is no slow component associated with minority carrier effects in the p⁺ region of a p-i-n photo diode [70]. Planar Pt/n-GaAs Schottky diodes with 100 GHz bandwidth have been reported by Wang *et al* [71]; the metal thickness was only 100Å to allow for optocoupling.

An inherent disadvantage of the Schottky photo diode, however, is the high series resistance and low efficiencies arising from the semi-transparent metal layer. This is apparent in the relatively low quantum efficiency of 19% and high series resistance of 190Ω obtained by Emeis *et al* in their p-InGaAs Schottky diodes (for operation at 1.3μm wavelength) with 50Å Ni semi-transparent metal contact [72].

Using a practically transparent and highly conductive layer of Indium Tin Oxide (ITO) to form the metal/semiconductor junction solves both these problems [73]. Figure 2.9 shows the band diagram of such a device.

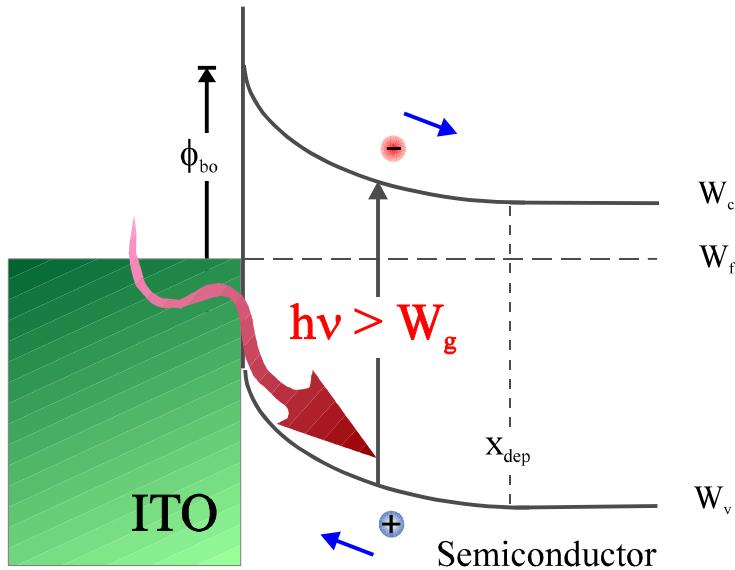


Figure 2.9: Band diagram of an ITO/n-GaAs Schottky photo diode.

The absorption layer is usually lightly doped to maximise depletion and is situated directly underneath the metal contact. Light enters through the transparent ITO contact and creates photo generated electron-hole pairs. These are then swiftly separated by the built-in depletion field giving rise to a photo current. The speed of response of such a device depends on the transit time of photo-generated carriers across the depletion region, the junction capacitance and parasitic circuit element contribution. In a monolithic structure, device isolation, achieved by either proton bombardment or mesa etch or a combination of both, reduces these parasitics. Furthermore, a planar structure is suitable for monolithic integration with other circuit elements such as HBTs or HEMTs.

Further discussion on Schottky diodes and photo detectors are presented in section 6.1

2.5.5 Transparent-Gate High Electron Mobility Transistors (TG-HEMTs)

The use of GaAs Metal Semiconductor Field Effect Transistors (MESFETs) and AlGaAs/GaAs High Electron Mobility Transistors (HEMTs) as optoelectronic detectors have been recently reported [74,75]. These are both essentially field effect devices where current is transported laterally through a channel between two horizontal electrodes, source and drain, that can be modulated by a Schottky electrode placed at an intermediate lateral location [76]. The more advanced heterojunction HEMT device usually consists of epitaxially grown n-type AlGaAs layer on an undoped GaAs layer grown on a semi insulating GaAs layer. The channel is formed by mobile charge accumulation at the heterointerface since electrons from the wider bandgap AlGaAs “supply layer” transfer across into the undoped GaAs in order to

occupy a lower energy state. Extremely high electron mobility results from diminished scattering due to ionised impurity as the coulombic field within the undoped GaAs crystal lattice is greatly reduced [77].

As in the ITO/n-GaAs Schottky photo diodes, radiation with energy greater than the bandgap of AlGaAs gives rise to a photo-generated electron-hole pair in the supply layer directly above the channel. This pair is separated by the built-in Schottky field giving rise to a photo current and corresponding photo voltage across the junction. In turn, this photo voltage effectively reduces the channel width and can be used for the desired optical control [78]. We have recently shown that using a transparent ITO gate enhances this control [79]. On the other hand, a photo conductive effect dominates if the energy of the incident radiation is between the bandgaps of the AlGaAs and GaAs; in this case, electron-hole pairs are generated in the GaAs channel and are separated by the lateral source-drain electric field thus adding to the drain current.

In comparison with the Schottky photo diode, the responsivity of these devices is many times greater as a direct consequence of the in-built gain of the FET structure. An inherent limitation of these devices as optical detectors however arises from the fact that the combined vertical depth of the AlGaAs and GaAs channel layers, typically $0.1\mu\text{m}$, are inadequate to ensure maximised photo absorption.

2.5.6 Heterojunction Photo Transistors (HPTs)

With the problems encountered with APDs in the 1970's for long wavelength use and the advent of high speed HBTs in addition to other fundamental benefits offered by these devices, renewed interest in (heterojunction) photo transistors (HPTs) as optical detectors has been aroused. The HPT offers the dual function of detection and amplification in a single device. In comparison with its rivals such as p-i-n/FET or APD/FET photo receiver combinations, this device is a particularly attractive alternative because of its relatively simple structure, ease of fabrication and integrated nature [80]. From an optical communication point of view, HPTs can be easily integrated monolithically in existing MMIC and OEIC processes resulting in high reliability and low parasitic noise [81].

Studies using HBTs with opaque emitter contacts show excellent suitability of these devices as photo detectors [82] and mixers in coherent photo receivers [83] in terms of optical performance where signal to noise ratios in excess of 30dB have been obtained. Optoelectronic mixing in HPTs has considerable potential for simplification of the

optical/electrical interfaces in some configurations of these systems. Mixing in the HPT is easily realised since the base terminal can be pumped either optically or electrically.

In the photo transistor, radiation incident on the device passes through the wide gap emitter unattenuated and is absorbed in the base, base-collector depletion region and bulk collector. Under normal common emitter operation mode, the base-collector junction is reverse biased. Hence it can be likened to a p-i-n photo diode (the collector doping is relatively very low). The base-collector junction acts as the light gathering element or the absorption layer. Internal gain is achieved through normal transistor action whereby light absorbed affects the base current (effectively adding to the I_{cbo} component) giving multiplication of photo current through the device. The optical gain, G , for a heterojunction photo transistor is given by [84,85]:

$$G \approx \beta\eta \quad (\text{eqn. 2.45})$$

where,

β = electrical gain of transistor

η = quantum efficiency of the base-collector photo diode

In terms of responsivity, this can be re-written as :

$$R_{HPT} \approx \beta R_{Diode} \quad (\text{eqn. 2.46})$$

where,

R_{HPT} = responsivity of the heterojunction photo transistor

R_{Diode} = responsivity of the base-collector photo diode

The quantum efficiency in (eqn. 2.45) is a function of the device parameters only and is independent of the current gain. Other aspects of the HPT are discussed later in Section 6.2.

2.5.7 Light Emitting Diodes (LED) and Vertical Cavity Surface Emitting Lasers (VCSEL)

A detailed theoretical discussion on the operation of LEDs and LASERs is clearly beyond the scope of this thesis. Yet, like detectors these transmitting devices constitute an inseparable part of the optical link. Solid state implementation of these devices essentially involve a p-n junction designed specifically for light emission rather than absorption. In the case of the LED, the p-n junction is formed using degenerate semiconductors to ensure forward current is dominated by the recombination process resulting in spontaneous emission of photons [86].

LEDs have been realised using a host of III-V compounds ranging from GaN for ultraviolet, GaAs for blue through to near infra-red and InGaAsP for emission beyond this spectral range. Unlike LEDs, laser operation is dominated by stimulated emission of light which results in highly monochromatic radiation. Laser modulation is easily achieved by modulating the forward current. Since the photon lifetimes are very short, high speed modulation can be realised. AlGaAs/GaAs lasers are used for 0.8 - 0.9 μm emissions while longer wavelengths of 1.3 - 1.55 μm are catered for by the InGaAsP/InP system.

Internal reflection and substrate absorption losses limit the external quantum efficiencies of LEDs. A significant portion of the drive current crosses the p-n junction directly beneath the contact, generating light that is obscured. Given that at the p-n junction the emitted light intensity is at its peak, this is particularly undesirable. The high resistances associated with a semi-transparent metal electrode lead to rapid decrease in junction current density due to its exponential dependence on the voltage; in turn this significantly reduces the emission from points at a lateral distance from the contact. Therefore, the use of a transparent contact not only allows the entire junction area to emit (which would otherwise be obscured) but it does so with uniformity. Aliyu *et al* have reported very low threshold voltage of 1.7V for 20 mA in their study using ITO contacts on AlGaInP visible LEDs [87].

Vertical Cavity Surface Emitting Lasers have recently aroused interest in a number of fields including fiber optic communication and optical computing. As the name suggests, VCSELs use an orthogonal cavity for light amplification rather than the common lateral Fabry-Perot approach that is associated with an edge emitting laser. High reflection is made possible by epitaxial growth of Bragg reflectors. As in LEDs, the optical path is obscured by the route of the injection current. We have demonstrated that ITO can be used to realise InGaAs/GaAs VCSELs for the first time resulting in very low threshold currents of 20 mA at room temperature [88].

2.5.8 Principal Receiver Configurations

Optical receivers can be classed into three basic categories: direct detection; coherent or heterodyne detection; and optically pre-amplified and tunable direct detection.

In direct detection communication systems, where the photo detector responds merely to the intensity of the incident optical signal, good sensitivity or large signal to noise ratios are very important. Since the noise is dominated by thermal sources in the preamplifier, the sensitivity can be improved either by applying gain or reducing the noise [62]. To this end, the most

popular approach has been in favour of the p-i-n/FET combination [89] rather than single APDs. Other common direct detection based implementations involve using p-i-n/HBT [90] and Schottky/HEMT [91] photo receivers.

Coherent detection, or mixing, involves amplifying the incoming signal by multiplying it with a local oscillator. This has two advantages over direct detection: (a) the receiver sensitivity can approach the Shot noise limit of the signal and (b) much greater wavelength selectivity allows many more channels to be carried at different wavelengths by the same fiber. Heterodyne receivers have also been implemented in a wide range of device combinations: p-i-n/FET [92], p-i-n/HEMT [93]. However, in their comparison of a wide range of heterodyne receivers, Urey *et al* [83] reported that in terms of the available intermediate frequency (IF) signal/noise ratio, the best performance was obtained using HPTs as mixers.

Optical pre-amplification refers to a relatively new technology which has wide ranging implications. Majority of today's developmental work is devoted to the erbium doped fiber amplifier (EDFA) [55]. These utilise a silica fiber with a doped core to provide a medium which affords gain when optically pumped at an appropriate wavelength - presently 980 nm or 1480 nm because of the availability of solid state lasers which couple sufficient power at these wavelengths. The signal is optically amplified en route to the detector end of the link; this reduces component count, increases reliability and opens up full bandwidth of the fiber windows between switching centres. The sensitivity of pre-amplified receivers exceeds that of coherent systems at high bit rates representing a major cost advantage in its favour since it essentially uses a direct detection design; tuning is achieved by selecting a suitable filter.

2.5.9 A Brief Comparison Between Various Types of Detectors

A summary comparison with some of the key performance parameters for various types of optical detector devices is shown in Table 2.3. These represent typical figures quoted in the literature for advanced III-V detectors and not necessarily the best data which is now available. Following the discussion on individual devices in previous sections, the purpose of this table is to present a "at a glance" figures of merit for these devices. For a more careful comparison, one needs to take into account several other factors such as material systems, the layer structures and the wavelength of the optical radiation amongst others; one such performance comparison between HPTs, p-i-n/FETs and APD/FETs has been made by Tabatabaie-Alavi *et al* [80]. In some cases, where no data is reported, an estimate is presented (e.g. bandwidth estimated from quoted impulse response for the device) or left empty where this is not possible.

Device Type	Advantages/Disadvantages	η	Bandwidth	Gain	Ref.
p-i-n	high speed, no internal gain	80%	25 GHz	-	[94]
SL-APD	internal gain, reduced noise	83%	3.6 GHz	25	[69]
Metal Schottky	high speed, no internal gain, low optical coupling	-	100 GHz	-	[71]
Metal Schottky	high speed, no internal gain, low optical coupling	19%	25 GHz (Estimated)	-	[72]
ITO Schottky	high speed, high optical coupling, no internal gain	32%	52 GHz	-	[70]
ITO Schottky	high speed, high optical coupling, no internal gain	25%	110 GHz	-	[73]
Metal HPT	high gain and speed, low quantum efficiency, suitable for mixing	50%	30 GHz	270	[95]
ITO HPT	high gain and speed, improved quantum efficiency suitable for mixing	-	17 GHz (Estimated)	22	[96]

Table 2.3: Summary of detector types and their performance parameters.

It can be noticed from the above comparison that p-i-n devices are designed to provide high speed whereas APDs are essentially high gain devices. Since from a system point of view, the product of the gain and the bandwidth is important, there will be a region of overlap where either device may be equally suitable. Another noticeable feature of this table is the inherent trade-off between the quantum efficiency, η , and the bandwidth of the detector; the two ITO/n-GaAs Schottky detectors [70,73] can be used to illustrate this point at a first order comparison: a slightly (10%) narrower absorption region enhances speed at the cost of lowering the η . HPTs have also come into contention with advancements in device technology and material growth techniques; these devices combine high speed and high gain and can be used as mixers. Finally, it is clearly seen that the use of ITO as both transparent Schottky and emitter ohmic contacts improves the η without fundamentally reducing the bandwidth.

3. Fabrication and Processing

In this chapter, all the major steps involved in the fabrication of a device are described. These start with a description of the wafer growth and carry through to the techniques used in order to realise the finished discreet device in a packaged form. This is followed by a summary, in the form of a schematic block diagram, of the various processing steps used in the fabrication of HBTs with conventional and ITO emitter ohmic contacts.

3.1 The Semiconductor Wafer

Some of the fundamental principles of semiconductor growth mechanisms and the associated practical methods used in the manufacture of wafers for device fabrication are discussed in this section.

3.1.1 Compound Semiconductor Materials

Compound semiconductor materials can be realised by the formation of “solid solutions” of two or more starting materials. These solutions occur when atoms of a different element are able to substitute a given constituent of a material without altering its crystal structure. The ability to do so by the new atom is referred to as its miscibility. In order that atoms can form solid solutions over large ranges of miscibility, they must satisfy the Hume Rothery rules:

- They must belong to the same **group** of the periodic table
- They must have comparable **atomic diameters** allowing substitution without large mechanical distortion
- Their **ionicity** must not be very different so as not to affect the tendency to attract / repel electrons from the site by a large amount
- The **crystal structure** of each constituent must be the same

A two component alloy is known as a *binary* alloy; some common examples include GaAs, AlAs, GaP, InP and InAs all of which have the Zincblende (diamond) crystal structure. Similarly a *ternary* alloy is one with three components and a *quaternary* alloy is one with four.

$\text{Al}_x\text{Ga}_{1-x}\text{As}$ is a ternary compound where both Ga and Al are from group III enabling Al to replace Ga on the alpha sites of the diamond compound lattice. As the compound AlAs has the same structure as GaAs, this makes the formation of solid solutions of Al in GaAs easy and preserves the same crystal structure over the full range of Al substitution. The beta sites with As atoms are not altered in anyway. Thus effectively, AlGaAs is an alloy of AlAs and GaAs.

Simultaneous replacement of atoms from alpha and beta sites of binary compounds allows quaternary alloys to be formed. $\text{In}_x\text{Ga}_{1-x}\text{As}_y\text{P}_{1-y}$ is one such example. This gives a more flexible scheme for tailoring material properties. In this case, the binary compounds GaAs, InP, InAs and GaP are part of the system and together they determine the limits to the range of properties of the resultant compound.

3.1.2 Epitaxy

Epitaxy refers to the ordered growth of one crystal upon another crystal [97]. Because of the large range of possible semiconductor compounds and their alloys, it is rare in device fabrication to grow bulk crystals of all these materials. Instead, it is more attractive to realise the wider range of materials by epitaxial growth. This is partly due to the difficulties involved in developing easy bulk crystal growth techniques for each new material and also because of historical reasons. Two materials for which thorough research and bulk crystal growth and polishing methods have already been developed are GaAs and InP.

There are three main modes of epitaxial growth: (a) monolayer, (b) nucleated and (c) nucleation followed by monolayer. Monolayer growth occurs when the deposited atoms are more strongly bound to the substrate than they are to each other. The atoms aggregate to form monolayer islands of deposit which enlarge and eventually a complete monolayer coverage has taken place. The process is repeated for subsequent layer growth. In case of nucleated growth, the initial deposit atoms aggregate as small three-dimensional (3D) islands which increase in size as further deposition continues until they touch and intergrow to form a continuous film. This mode is favoured where the forces of attraction between the deposited atoms is greater than that between them and the substrate. In the final mode, growth starts with the formation of a single or few monolayers on the substrate followed by subsequent nucleation of 3D islands on top of these monolayers.

3.1.2.1 Epitaxial Lattice Matching

Epitaxy, although a highly successful approach for growing a wide range of materials, none the less suffers from an important constraint. Epitaxial growth requires that the atomic spacing, the lattice constant, of the layer material not differ by more than a few percent and that they have the same crystal structure. While most materials of interest have diamond structure, satisfying the latter requirement, the lattice matching imposes a serious constraint on the range of compositions that can be grown on a given bulk substrate. Although, traditionally, these were provided by GaAs and InP, increasing use is being made of InAs and GaSb as the substrate.

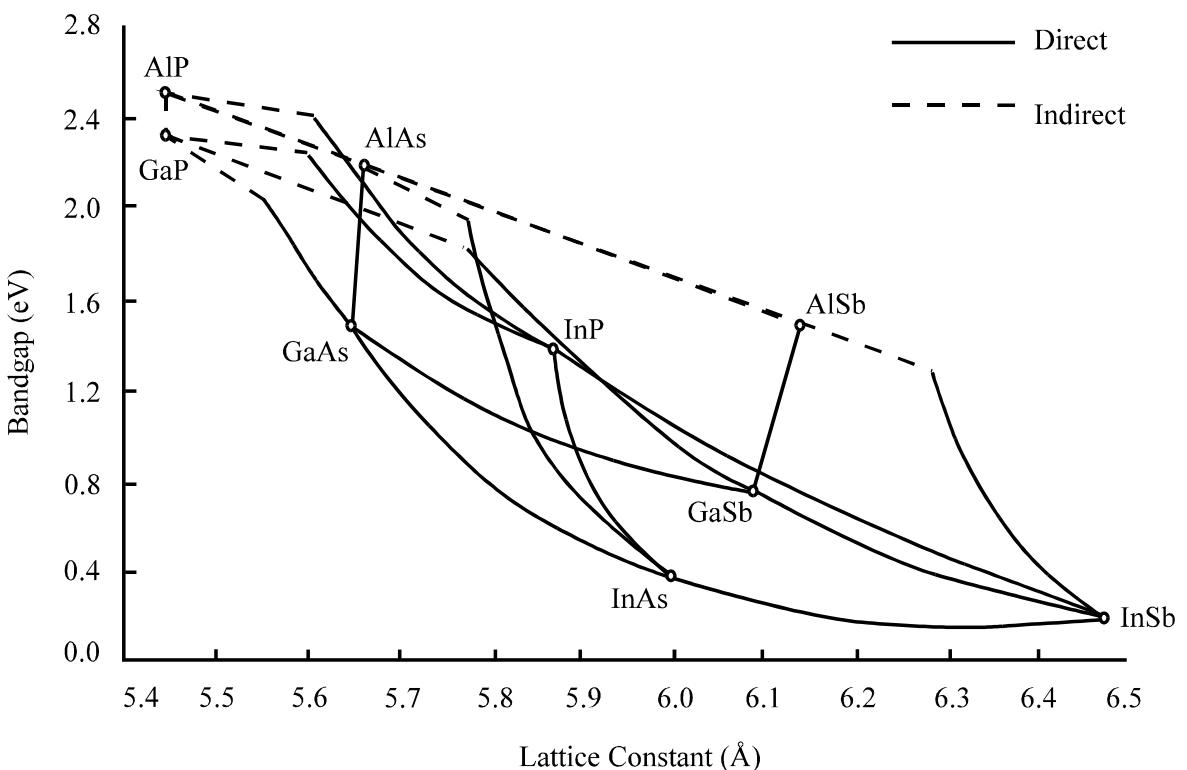


Figure 3.1: A plot of energy bandgap and lattice constant for major III-V compound semiconductors.

This problem is best appreciated by a graph of the energy gap versus lattice constant for major III-V compounds, as shown in Figure 3.1. This is also known as a phase diagram. For a possible range of ternary alloy systems, a solid line is generated between the starting binary materials. In the case of a quaternary compound, the boundary is laid out by four intersecting lines.

The ability to tailor the bandgap of III-V alloys to a desired wavelength makes them particularly attractive for optoelectronic applications. The dark currents are significantly reduced in compound detectors from their Ge and Si predecessors. In addition, heterojunction structures can be easily used to enhance their high speed operations. One such system that is of great interest is the InP/InGaAs heterostructure which is sensitive to $1.55\mu\text{m}$ wavelength. In this case the composition of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ternary compound, with the desired bandgap of 0.75 eV, is dictated by the lattice matching constraint to the InP substrate. Lattice mismatch, on the other hand, manifests itself in the form of dislocation-induced junction leakage and low quantum efficiency in optoelectronic devices.

3.1.3 Growth Techniques : LPE, MOCVD, MBE

The three basic and most commonly used compound semiconductor growth techniques are discussed below. These are Liquid Phase Epitaxy (LPE), Metal Organic Chemical Vapour Epitaxy (MOCVD) and Molecular Beam Epitaxy (MBE). MOCVD is also sometimes referred to as MOVPE (Metal Organic Vapour Phase Epitaxy).

3.1.3.1 Liquid Phase Epitaxy - LPE

LPE refers to the growth of semiconductor crystals from a liquid solution at temperatures well below their melting point [98]. This is made possible by the fact that a mixture of a semiconductor and a second element has a lower melting point than the pure semiconductor alone. Thus, for example, the melting point of a mixture of GaAs and Ga is considerably lowered from $1238\text{ }^{\circ}\text{C}$, the melting point of pure GaAs. The actual melting point of the mixture is determined by the proportion of the constituent Ga and GaAs.

For example, in the growth of GaAs, LPE is commenced by placing a GaAs seed crystal in solution of liquid Ga and GaAs which is molten at a temperature below the melting point of the seed. As the solution is cooled, a single crystal GaAs begins to grow on the seed leaving a Ga rich liquid mixture with an even lower melting point; further cooling causes more GaAs to crystallise on the seed.

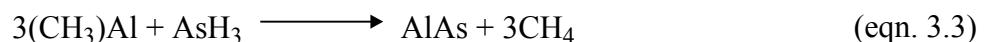
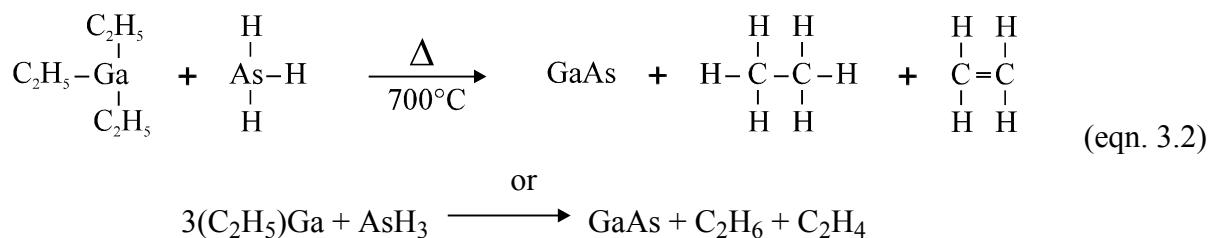
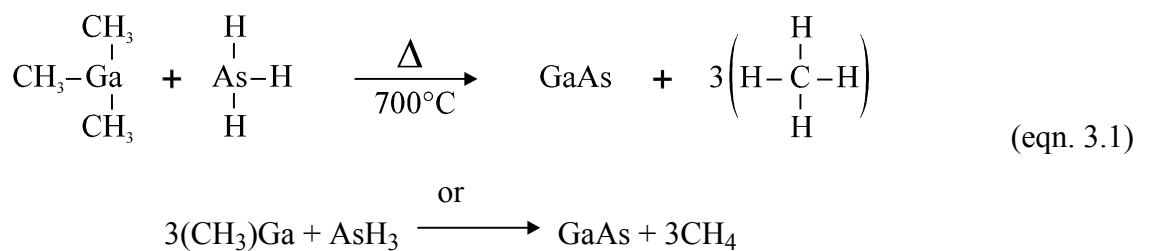
By this technique single crystals can be grown at low enough temperatures to avoid the problems associated with impurity introduction at temperatures near the melting point of the crystal. It is particularly useful for growing III-V compounds based on Ga and In as these metals form solutions at conveniently low temperatures. LPE remains a successful

production technique for structures that do not require thin, uniform and high quality epitaxial layers needed for microwave devices.

3.1.3.2 Metal Organic Chemical Vapour Deposition - MOCVD

This involves the forced convection of the metal organic vapour species over a heated substrate [99]. Those molecules striking the heated crystal release the desired species, resulting in crystal growth. The chemical process involved is quite simple in that an alkyl compound for the group III element and a hydride for group V element decompose in the 500°C to 800°C temperature range to form the III-V compound semiconductor.

Equations (eqn. 3.1) and (eqn. 3.2) represent, to a first approximation, the gas phase reactions that occur during MOCVD growth of GaAs, while the corresponding reactions for the growth of AlAs is given by equations (eqn. 3.3) and (eqn. 3.4). Hence, in order to grow $\text{Al}_x\text{Ga}_{1-x}\text{As}$, a combination of the above reactions is used and the mole fraction ‘x’ is determined by their relative ratios. Similarly, in the growth of InGaAsP/InP heterostructures, the band gap is controlled by the ratio of AsH_3/PH_3 while the ratio between group III elements (i.e. TMGa/TMIn or TEGa/TEIn) determines the lattice matching to the InP substrate. Doping is achieved by introducing the respective n-type (H_2Se or H_2S) and p-type (demethyl zinc DMZn / $\text{Zn}(\text{CH}_3)_2$) gases to the reactor.





These reactions are carried out thermally with the flowing gases and the reactor cell maintained at or near atmospheric pressure. Common sources for group V elements are AsH_3 or PH_3 while for group III these are trimethyl gallium (TMGa / $\text{Ga}(\text{CH}_3)_3$), trimethyl aluminium (TMAI / $\text{Al}(\text{CH}_3)_3$) and trimethyl indium (TMIn / $\text{In}(\text{CH}_3)_3$) or triethyl gallium (TEGa / $\text{Ga}(\text{C}_2\text{H}_5)_3$), triethyl aluminium (TEAI / $\text{Al}(\text{C}_2\text{H}_5)_3$), and triethyl indium (TEIn / $\text{In}(\text{C}_2\text{H}_5)_3$) respectively. A typical horizontal reactor suitable for the growth of GaAs is shown in Figure 3.2.

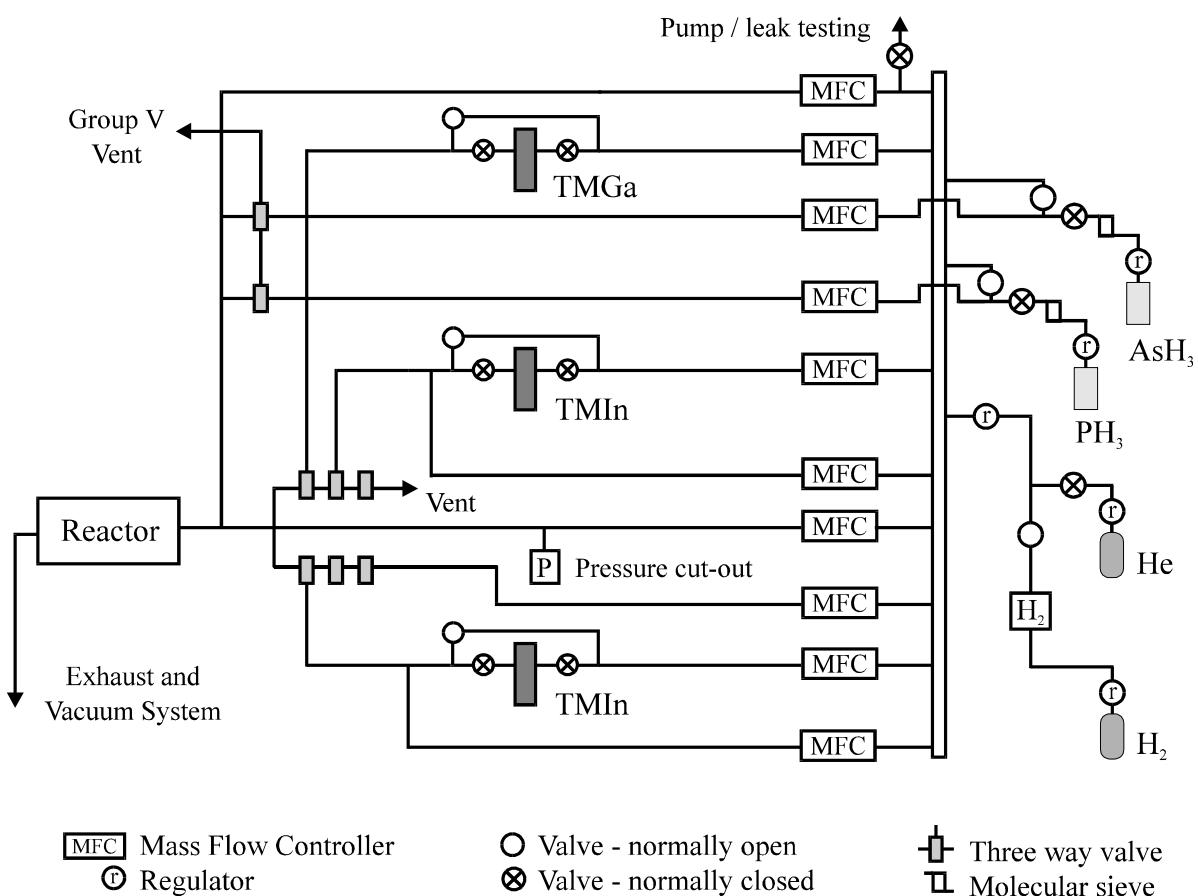


Figure 3.2: Schematic block diagram of a MOCVD reactor

TMGa , TMAI and TMIn are all liquids that have high vapour pressure at room temperature. Hence these are transferred to the reactor by bubbling H_2 as the carrier gas. Similarly, hydrogen is also used as the carrier gas for AsH_3 . In case of PH_3 , which is not easily decomposed, this group V source is transferred to the reactor after thermal decomposition via a special furnace.

Excellent uniformity in layer thickness, composition and carrier concentration are all achieved over a large area wafer using the MOCVD growth technique. This technique also easily lends itself to the growth of abrupt heterointerfaces. From a manufacturing / mass production perspective, MOCVD offers high throughput while retaining the other desirable properties thereby making it a very promising choice [100].

3.1.3.3 Molecular Beam Epitaxy - MBE.

At its simplest, MBE is a refined form of vacuum evaporation [101]. The molecular beams are produced by evaporation or sublimation from heated liquids or solids contained in crucibles. At the pressures used in MBE equipment, collision free beams from various sources interact chemically on the substrate to form an epitaxial film. The ability to start and stop a molecular beam by controlling the shutters attached to the vapour containing crucibles in (typically 0.1 to 0.3 second) less than the time taken to grow a monolayer (typically 1 second) has led to the ability to produce complex multilayer structures.

MBE requires conventional ultra high vacuum (UHV) techniques and, in addition, the pressure in the system has to be low enough (usually 10^{-11} Torr) to ensure that no gas phase collisions occur. Thus homogenous reactions, which can occur in MOCVD, are completely avoided and the process is determined entirely by heterogeneous reactions on the substrate surface. The sample is held at a relatively low temperature (app. 550 °C for GaAs) during epitaxy.

A schematic diagram of an MBE system is shown in Figure 3.3. A critical feature is the extensive cryopanelling surrounding both the substrate station and the evaporation sources. The low temperature (usually 77K) reduces the arrival rate of unwanted species and provides heat dissipation for both the evaporation sources and the substrate heater. The physical and chemical properties of the films can be monitored *in-situ* during MBE growth using reflection high energy electron diffraction (RHEED) and Auger Electron Spectroscopy (AES).

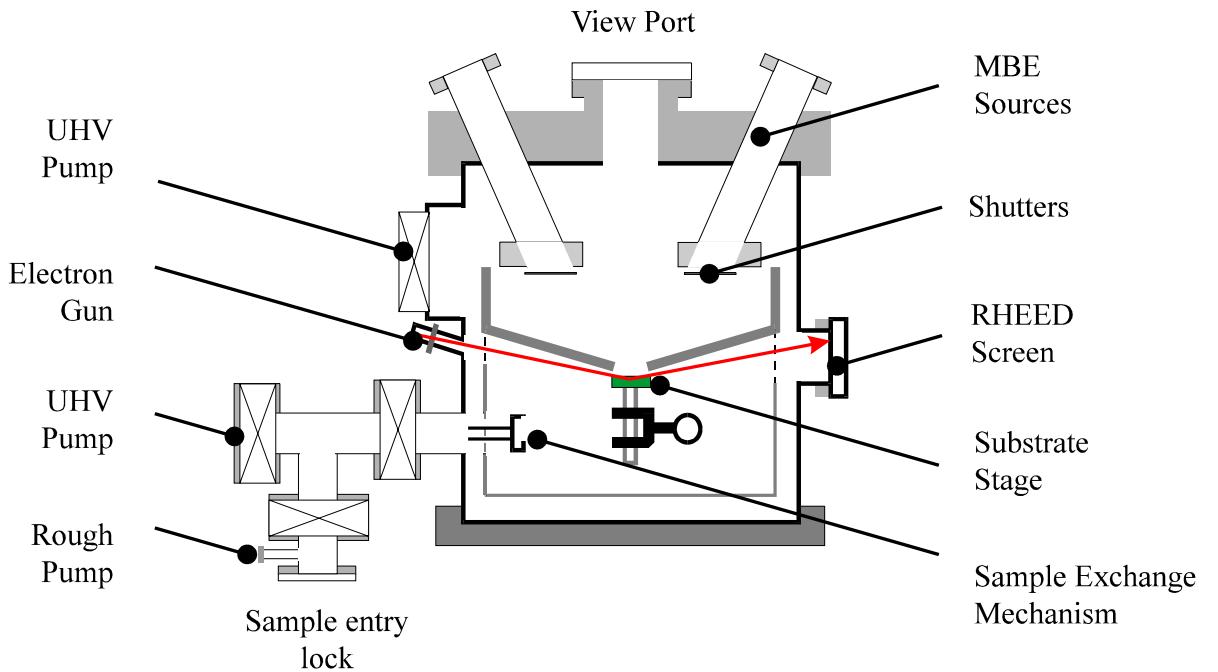


Figure 3.3: Schematic diagram of an MBE system

Despite the need for a sophisticated setup, the versatility offered by the MBE technique renders it attractive for many applications. In addition it offers precise control of film thickness, composition and doping. AlGaAs/GaAs heterojunctions with atomically abrupt interfaces are readily obtained. However, the major disadvantages associated with MBE include high expense because films are usually grown one layer at a time. In addition, so called ‘oval defects’, which can be fatal for base-emitter junction of HBTs, are found at densities of a few hundred per cm^2 ; these defects are a primary factor limiting the yield of HBT circuits. Although extensive use has been made of MBE growth in HBT research, the quest for increased wafer throughput and improved surface morphology continues [100].

3.2 ITO Deposition by Reactive r.f. Sputtering

The basic principles of reactive r.f. sputtering technique are described below. This is followed by a discussion about the calibration of the system used in this work.

3.2.1 Principles

A sputtering system consists of an evacuated chamber, a target (cathode) and a substrate table (anode). The electric field inside a sputtering chamber accelerates electrons which collide with Ar atoms producing Ar^+ ions and more electrons and a characteristic purple/blue plasma. These charge particles are then accelerated by the electric field: the electrons towards the anode and the Ar^+ ions towards the cathode (ITO target). When an ion approaches the target, one of the following may occur:

- i. It may undergo elastic collision and be reflected.
- ii. It may undergo inelastic collision and be buried into the target.
- iii. It may produce structural rearrangement in the target material.
- iv. The impact may set up a series of collisions between atoms of the target leading to the ejection of one of these targets; this process is known as sputtering.

Thus the sputtering process can be likened to a break in a game of “atomic” billiards. The excited ion, representing the cue ball, strikes the atomic array of the target - the neatly arranged pack - scattering them in all directions. Some of these will be ejected in the direction of the original approaching ion i.e. normal the target surface. It is this ejected particle which is useful for deposition on the surface of the wafer. Hence the sputter process essentially involves knocking an atom or molecule out of the surface of a target. Under the right conditions, the sputtered species will travel through space until it strikes and condenses on the surface of the substrate. For further detail see references [102,103]

A r.f sputtering system allows the deposition of non-conductive materials at a practical rate. In such a system, the r.f. power alone is capable of generating the plasma and accelerate ions to the target to cause sputtering.

3.2.2 The Nordiko 1500 r.f. Sputtering System

Figure 3.4 shows the schematic of the sputtering chamber and the associated r.f. power supply of the Nordiko 1500 system. Both the top and the bottom electrodes are shielded by guard rings. The diameter of the top electrode is 20cm while that of the target electrode is 10cm and the distance between them is 7cm. The r.f. generator is operated at 13.56 MHz. Further information is available in the Nordiko r. f. sputtering handbook [104].

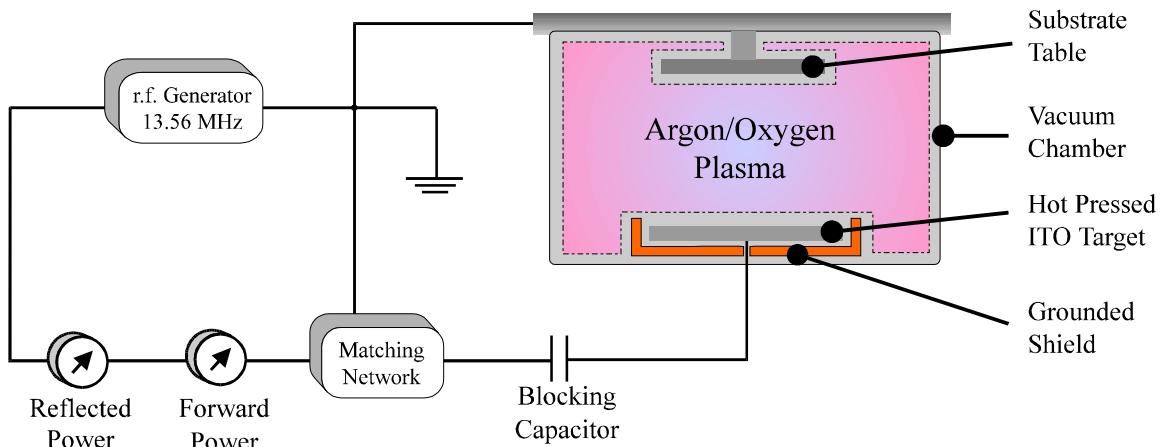


Figure 3.4: Schematic of the r.f. Sputtering Chamber

The material to be sputtered is made into a target and mounted onto a circular copper backing plate using Ablebond 84-1MI heat resilient adhesive [105]. In this case the target consists of a circular disk of hot pressed 99.999% purity ITO ($90\% \text{In}_2\text{O}_3 + 10\% \text{SnO}_2$) which is 4 inch diameter and approximately 0.25 inch thick (available from [106]). During deposition, the sample is inverted and placed into substrate table facing the target. There are two shutters which separate the target and the substrate. These help prevent contamination of the target during sample loading and unloading, protect the sample during pre-conditioning as well as provide means of controlling ITO deposition thickness during sputtering.

The sputtering procedure is commenced by evacuating the chamber to pressures lower than 1×10^{-6} Torr. Ar, being a noble gas which does not react with either the target or the semiconductor wafer, is then introduced into the chamber at a specified pressure. This is followed by allowing O₂ into the chamber at a set rate. The r.f. supply is then switched on and stabilised to the required power and induced d.c. bias levels; this bias is an indication of the sheath potential and is a good sign of the ion bombardment energy. During this time the substrate is shielded by the top shutter. Once pre-conditioning is complete, the top shutter is opened marking the beginning of the deposition process.

3.2.3 Controllability and Calibrations

The specifics of the system and the repeatability of the sputter conditions will be discussed next. The chamber is first “roughed” before being opened to the high vacuum pump. Figure 3.5 shows the chamber pressure dropping as it is pumped by the rotary pump through the “roughing valve”; the pressure was monitored using the thermocouple gauge 1. It is seen that

the pressure drops to below 0.1 torr (the pressure which has to be attained before the high vacuum valve can be opened) in less than 10 minutes.

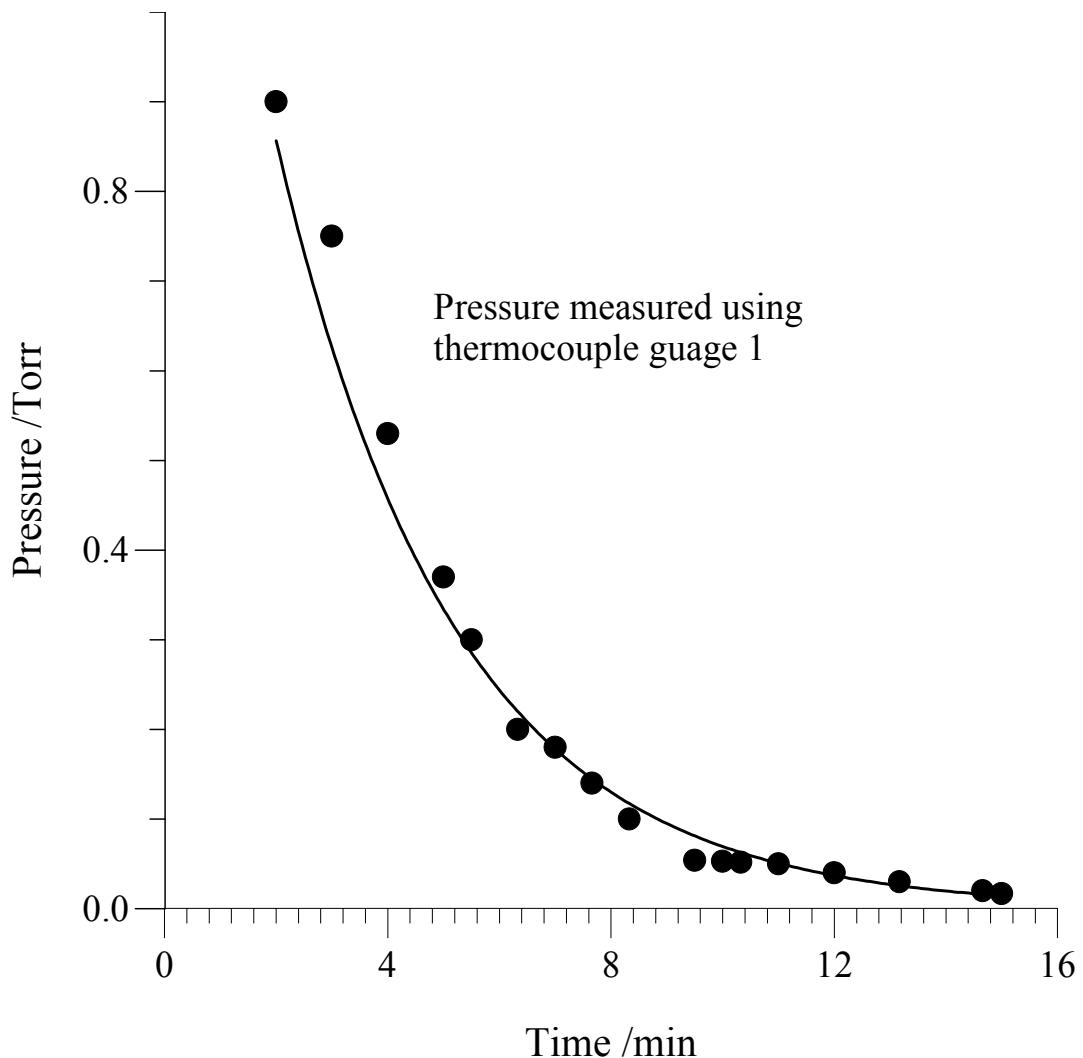


Figure 3.5: Chamber pressure vs. time after opening the roughing valve.

Figure 3.6 shows the schematic diagram of the by-pass pumping system of the Nordiko 1500 sputtering machine along with all the associated vents and pressure gauges. In order to standardise the oxygen content of the plasma during the sputter depositions, it is necessary to measure the partial pressure of the gas rather than the flow rate although the two are proportional for a given system, total pressure and flow rate of the other constituent gases - in this case, Ar.

Thus it was necessary to install a second pressure gauge, Penning 505, into the sputtering chamber in order to monitor actual pressure there and to measure the partial pressures of Ar and O₂ gases respectively prior to exciting the plasma as the existing Hastings gauge did not

cover the necessary range. The alternative is to monitor the respective flow rates of the two gases, but as this relies on the absolute pressure gradients it is not very useful for standardising the deposition conditions. However, once the partial pressures are calibrated against the flow rates, the latter was used to monitor the partial pressures during the deposition because the ion gauges become unstable once the plasma is excited.

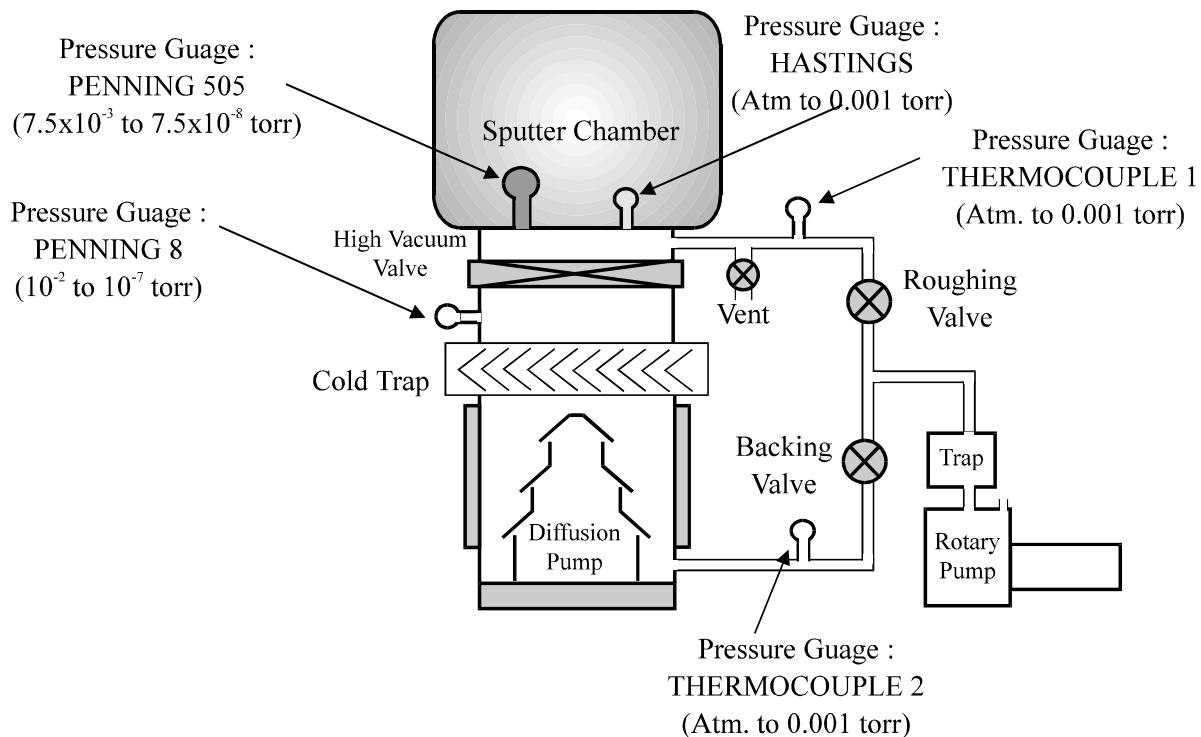


Figure 3.6: Schematic of the by-pass pumping system

Figure 3.7 shows the chamber pressure vs. time once the high vacuum valve is opened and it is pumped by the diffusion pump. It is seen that the actual chamber pressure, as monitored by the newly installed Penning 505 gauge, is always slightly higher than the pressure between the diffusion pump and the chamber. Figure 3.7 also shows that the time taken to reach the “base pressure” (usually 1×10^{-6} torr) is approximately 2.5 hours.

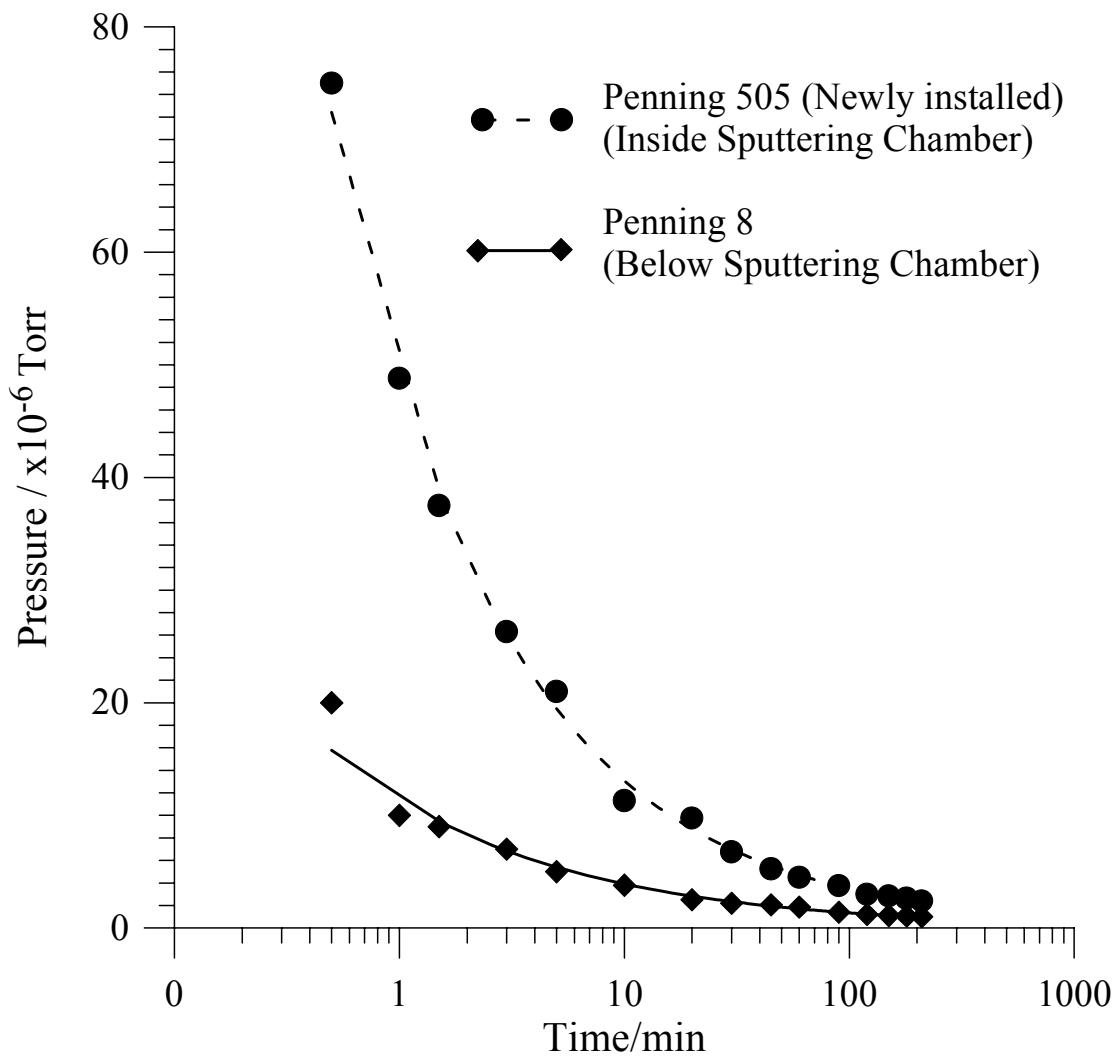


Figure 3.7: Chamber pressure vs. time after opening high vacuum valve

Once the chamber was pumped down to the base pressure, argon gas was flowed in at $150 \text{ mlcm}^{-2}\text{s}^{-1}$ and the high vacuum valve adjusted to maintain a chamber pressure of 5×10^{-3} torr. At this stage, the “throttle pressure”, $P_{(\text{Throttle})}$, was found by switching off the argon flow and was found to be 2×10^{-5} torr. Ar flow was restored and O₂ was then flowed in at the required rate (over the range 15 to 105 $\text{mlcm}^{-2}\text{s}^{-1}$); the high vacuum did not need to be readjusted at any of these stages to maintain the set pressure of 5×10^{-3} torr. The Ar was then switched off again to find the chamber pressure, $P_{(\text{Chamber})}$ due to the O₂ flow alone under these conditions. The partial pressure of O₂, PO₂, was then found using (eqn. 3.5), as follows :

$$\text{PO}_2 = \frac{P_{(\text{Chamber,oxygen})} - P_{(\text{Throttle})}}{P_{(\text{Chamber,oxygen+argon})} - P_{(\text{Throttle})}} \quad (\text{eqn. 3.5})$$

Figure 3.8 shows the PO_2 , the oxygen partial pressure, as a function of the O_2 flow rate. As expected, the partial pressure was found to be a linear function of the flow rate.

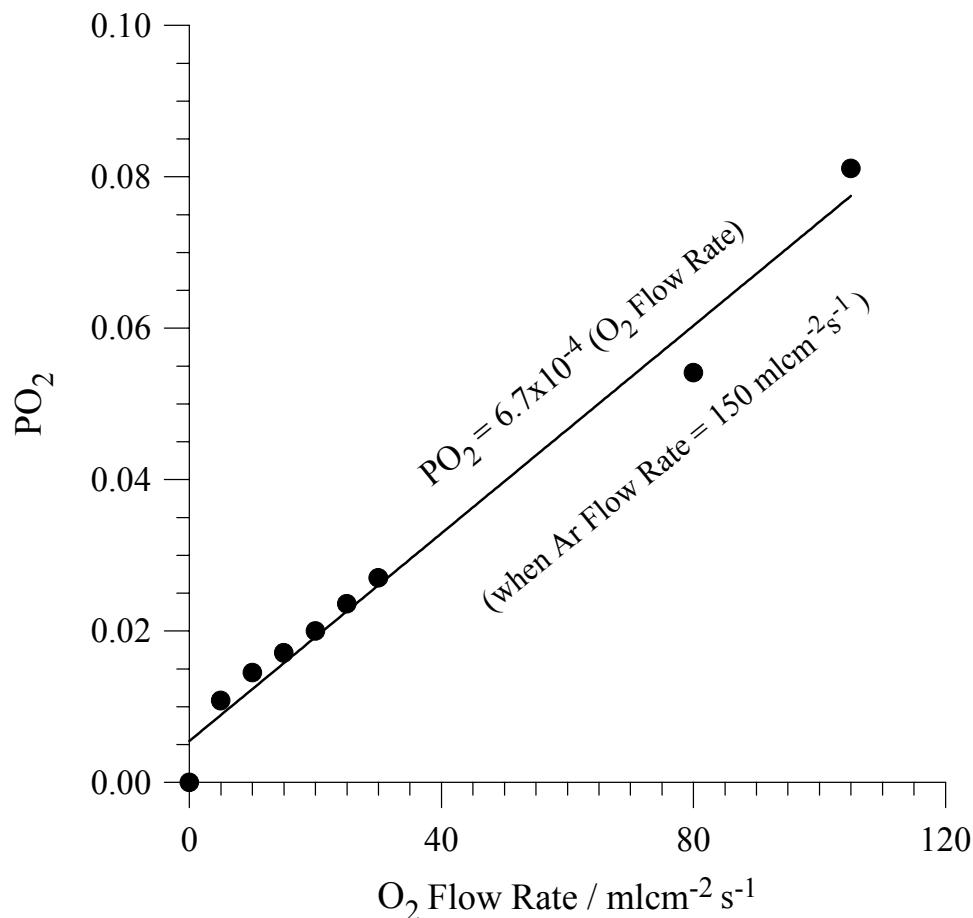


Figure 3.8: O_2 Partial Pressure vs. O_2 Flow Rate; the Ar flow rate was kept constant at 150 $\text{mlcm}^{-2}\text{s}^{-1}$ throughout.

3.2.4 Sample Preparation Prior to ITO Deposition

Following usual cleaning of samples in TCE, acetone, methanol and D.I. water, these were etched in a 1 HCl : 1H₂O solution for up to 1 minute (in case of InGaAs samples, the soaking period was reduced to 20 seconds as InGaAs is etched in this solution). This pre-etching promotes ITO adhesion to semiconductor substrates and is particularly useful for subsequent reliable patterning of ITO by wet chemical etching techniques. A mild solution of HF (10%) for 10 seconds has also known to have been used for this pre-etching prior to ITO deposition.

3.3 Photolithography

Photolithography is used to pattern the wafer surface for defining the exact dimensions of devices and circuits. Although e-beam lithography provides the most advanced technology, this work involved only conventional photolithography using an ultra violet source. This involves spinning on a thin layer of a light sensitive polymer, known as photoresist, on the wafer surface. Ultra-violet light is shone onto this layer through a mask containing the pattern to be transferred. Areas exposed to UV light can then be removed using a developer solution. The remaining pattern on the wafer can now be used for etching the wafer or depositing a metallic layer onto it. Further detail is available in [107].

The thickness of the resist layer is critical. It is usually set by the duration and the speed of the spinner for a given photoresist. In this case Shipley 1400-27 photoresist was used and spun at 4,500 rpm for 35 seconds producing a thickness of approximately 1 μm . Best results were achieved for wafer dimensions of roughly 1cm x 1cm.

3.4 Metallisation by Resistive Thermal Evaporation

Resistive thermal evaporation is one of the most commonly used metal deposition techniques. It consists of vaporising a solid material (pure metal, eutectic or compound) by heating it to sufficiently high temperatures and recondensing it onto a cooler substrate to form a thin film. As the name implies, the heating is carried out by passing a large current through a filament container (usually in the shape of a basket, boat or crucible) which has a finite electrical resistance. The choice of this filament material is dictated by the evaporation temperature and its inertness to alloying/chemical reaction with the evaporant. This technique is also known as “indirect” thermal evaporation since a supporting material is used to hold the evaporant.

Once the metal is evaporated, its vapour undergoes collisions with the surrounding gas molecules inside the evaporation chamber. As a result a fraction is scattered within a given distance during their transfer through the ambient gas. The mean free path for air at 25°C is approximately 45 and 4500 cm at pressures of 10^{-4} and 10^{-6} torr respectively. Therefore, pressures lower than 10^{-5} torr are necessary to ensure a straight line path for most of the evaporated species and for substrate-to-source distance of approximately 10 to 50 cm in a vacuum chamber. Good vacuum is also a prerequisite for producing contamination free deposits [108,109].

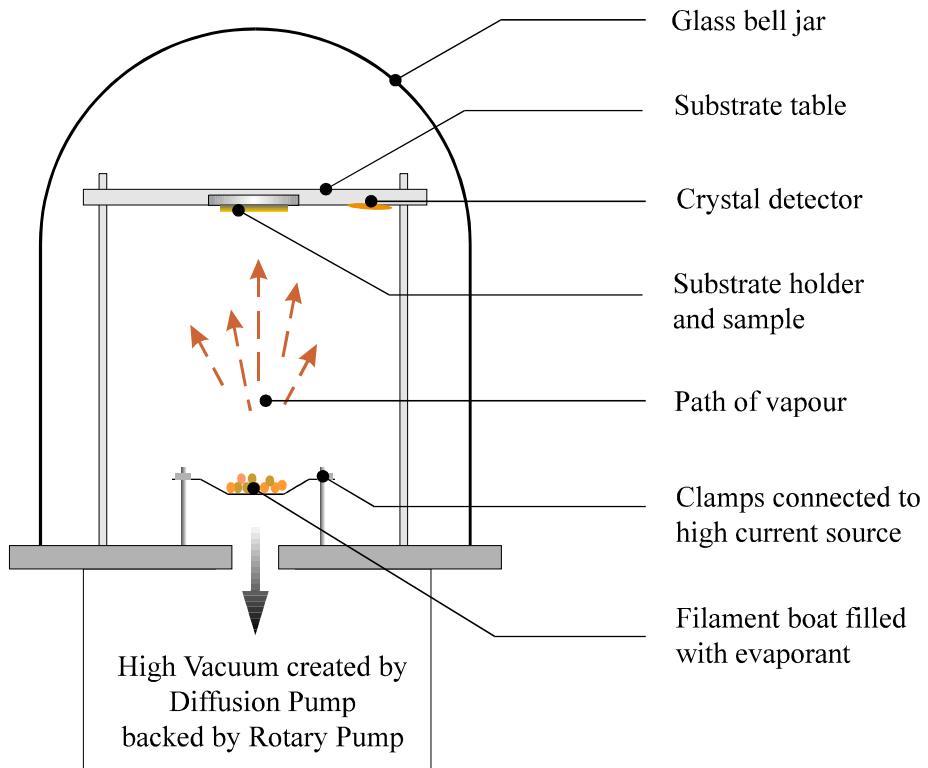


Figure 3.9: Schematic diagram of a resistive thermal evaporation system.

Two separate Edwards E305 thin film coating systems were used for the deposition of all the metals referred to in this work; a schematic diagram of one such system is shown in Figure 3.9. These systems are fitted with an acoustic crystal monitor which is linked to Edwards film thickness monitor (model no. FTM5) for controlling the amount of metal deposit. Because of the exceptionally large scattering tendency of Zn during evaporation, depositions involving Zn (e.g. Au/Zn/Au ohmic contacts) were carried out in only one of the evaporators, hereafter referred to as the “p-type system”. All other metalisations were carried out in the other evaporator, named the “n-type system”, to prevent cross contamination.

Because there is a lateral distance between the crystal detector used for *in-situ* monitoring of the deposited films and the substrate, it is necessary to determine the ratio of respective amounts of deposit between these two surfaces. This ratio is known as the “tooling factor” and is a unique quantity for a particular evaporator which depends on a number of factors including the dimensions of the system and the actual evaporant. Table 3.1 lists the experimentally determined tooling factors for the metals used in this work.

Metal	Density [g/cm ³]	Z (Acoustic Impedance)	Tooling Factor	Current [A]
Al	2.70	8.20	1.71	44.0
Au	19.30	23.17	1.55	54.0
AuGe	20.17	23.18	1.51	52.0
In	7.30	10.49	1.30	34.0
Ni	8.91	26.66	1.26	80.0
Ti	4.50	14.05	1.42	75.0
Zn	7.04	17.17	1.55	25.0

Table 3.1: List of metals used in the fabrication of devices in this study and their properties relevant for resistive thermal evaporation. The ambient pressure is below 2×10^{-6} torr.

All filament boats used consisted of tungsten material and unless otherwise stated, prior to commencing each evaporation, the base pressure was better than 2×10^{-6} torr. Typical values for the minimum current required to evaporate each of these metals is also listed in Table 3.1. It should be noted that Ni evaporation is particularly tricky and requires two boats. Hence a large current is needed to reach its boiling point. Best results were obtained when a Ni wire was placed diagonally across the boat thereby itself providing an added current path.

3.5 Wet Chemical Etching

Etching process, like metalisation, is an integral part of fabricating semiconductor devices on wafers with epitaxially grown active layers. These vertically stacked layers have to be defined by mesa etching in order to make contacts to underlying layers or simply to electrically isolate a working device to restrict undesirable leakage currents. In addition, certain metals and compounds can also be defined by etching after deposition. Chemical etching is one of the more convenient ways of achieving this. Table 3.2 lists a host of chemical solutions which were used in the course of this work for various device fabrications; a more comprehensive list of etching solutions is available in [110].

Material	Etching Solution	Etch Rate [Å/sec]
GaAs	8NH ₃ : 3H ₂ O ₂ : 400H ₂ O (isotropic)	30
	1H ₂ SO ₄ : 1H ₂ O ₂ : 30H ₂ O	60
	1HF : 1H ₂ O ₂ : 10H ₂ O	80
AlGaAs	8NH ₃ : 3H ₂ O ₂ : 400H ₂ O	25
	1H ₂ SO ₄ : 1H ₂ O ₂ : 30H ₂ O	60
	1HF : 1H ₂ O ₂ : 10H ₂ O	80
InGaP	conc. HCl	Fast
InP	1HCl : 1H ₃ PO ₄	Fast
InGaAs	1H ₂ SO ₄ : 1H ₂ O ₂ : 20H ₂ O	30
ITO	1HCl : 1H ₂ O	8
	1HF : 1H ₂ O ₂ : 10H ₂ O	125
Al	conc. KOH (at 30 °C)	10
In	1HCl : 5H ₂ O	Fast

Table 3.2: List of chemical solutions and their approximate etch rates for wet etching various materials used in the course of this study. Unless otherwise stated, all rates correspond to a 20 °C and 60% humidity ambient conditions.

In its simplest mode, chemical etching involves the dissolution of the material without any change in the chemical nature of the dissolved species. Factors affecting etch rates include temperature, humidity, strength of the etching solution as well as the morphology and the cleanliness of the surface being etched. In addition, given the tendency of different crystallographic planes to etch at dissimilar rates, various orientations of single-crystal substrates may etch very differently in a given etchant [111]. An example is GaAs in ammonia solution (8NH₃ : 3H₂O₂ : 400H₂O) which is therefore referred to as an *isotropic* etchant in this case.

In this study, wherever possible all etching was carried out in a controlled environment with known temperature and humidity. The samples were cleaned thoroughly in organic solvents to remove surface contaminants in steps prior to etching.

One of the more difficult steps in the fabrication of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ HBTs is reaching the thin base (usually 1000\AA or less) and leaving enough material for a good ohmic contact; a schematic of the processing steps involved is given in section 3.11. Although selective etching techniques (involving $\text{KI} + \text{I}_2 + \text{H}_2\text{O}$) can be used to minimise the risk, it is inapplicable where the Al mole fraction is less than 40% [112]. Selective etching is a process which refers to difference in etch rates between different materials. Thus to etch these $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ HBTs the ammonia solution was used and the etching had to be carefully monitored. Estimated doping levels monitored from breakdown voltage of the surface layer were used as a guide. These aspects are further discussed in section 3.7.

Etching InGaP/GaAs or InP/InGaAs wafers is relatively simple as a selective etching solution is readily applicable. InGaP only etches in conc. HCl (dilute solution is ineffective) which does not attack GaAs while the ammonia solution does not etch InGaP. Similarly, the respective etchants for InP and InGaAs listed in Table 3.2 do not etch the other material. Although it is difficult to quantify the etch rates of InGaP in conc. HCl or InP in orthophosphorous acid ($1\text{HCl} : 1\text{H}_3\text{PO}_4$), it was found that approximately 1000\AA of both these materials can be removed in 10 sec. in the respective etching solutions.

In the fabrication of GaAs based Schottky diodes, given the large thickness involved (several μm in total), the ammonia solution was used for etching to the highly doped substrate. Both breakdown voltage and Talystep was used for judging the depth of the etch. The HF ($1\text{HF} : 1\text{H}_2\text{O}_2 : 10\text{H}_2\text{O}$) solution was also used in cases where etch depth was not very critical such as in the isolation of TLM mesas consisting of thin conductive layers over thick SI substrates.

3.6 Reactive Ion Etching

The principles of reactive ion etching are the same as those in reactive sputtering. The exception is that the sample to be etched is used as the target from which atoms are removed. For further information see [113].

A previously in-house built RIE system was used for this work; this system was modified from a plasma deposition system (model no. DP80 with load lock option) manufactured by

Plasma Technology (UK) Ltd. [114]. It was used in the dry etching of ITO and the results are discussed in section 5.2. The system will be briefly described here. It is fitted with Ar, O₂ and Freon gas sources and is capable of delivering up to 200W r.f. power. The sample to be etched is placed on a glass slab in the centre of the chamber. It is then evacuated to pressures better than 1×10^{-4} torr using a turbo pump; the etchant gas is then flowed in at a constant rate regulated by flow controllers. The r.f. power is then switched on to start the etching.

3.7 Thickness Monitoring and Calibration

Monitoring metal deposition thickness or wafer etch depth are regular but vital parts of the whole fabrication process. Post deposition thickness measurement is also the only easy means of monitoring the ITO sputtering where no *in-situ* detector is available. In the course of fabrication, the doping on wafers vary according to their depth and etching processes have to be carefully monitored and controlled. This can be done by etching for a predetermined length of time if the etch rate of a particular solution is known. Similarly, the accuracy of film thickness monitors often need to be cross checked in the case of metalisation. However, definite results are obtained if the wafer is tested *after* the deposition or etching is complete. Two methods were widely used for doing so in this work; the first method can be used for measuring actual thickness and is applicable for both etching and depositions while the second is only suitable for judging etch thickness. These are described next.

3.7.1 Talystepping

The Taylor-Hobson Talystep (model no. 5) is a highly sensitive purpose built instrument designed for the micro-electronics industry which can measure vertical features down to 100Å within a few percent accuracy [115]. This method involves physically traversing the surface with a fine stylus suspended from an electro-magnetically sensitive spring. Vertical movement of the stylus is amplified electronically and recorded on paper by a spark pen. After leveling the sample with respect to the traverse plane, the stylus is scanned either across the test feature or over its edge. An accurate surface profile can be built up in this way and to some extent the instrument will also reveal the surface roughness up to a given range. Lateral features wider than a few μm such as edge profile of mesas or metal pads can also be inferred at very low stylus scan speed - this dimension being limited by the physical width of the stylus. The maximum traverse length is 1 mm.

A more advanced version of this principle has been developed and incorporated into what is known as an “Atomic Force Microscope” or AFM [116]. This instrument is linked to a computer and as well as printing out surface profiles, the AFM is capable of producing 3-dimensional graphics of a relatively large surface (1mm by 1mm) which can manipulated to alter the perspective.

3.7.2 Electrical Method

The electrical method relies on the breakdown voltage of a reverse biased Schottky diode to estimate the doping concentration and hence the thickness of an etched sample whose doping profile is known. It is particularly suited to situations when the entire surface needs to be etched or the mesas are too small where either no edges remain or those that do would be unsuitable for Talystping.

Thus the breakdown voltage is measured by placing two gold (tipped) probes firmly on the test surface. These can be treated as two Schottky diodes connected in a manner such that one is reverse biased if the other is forward biased. Thus, the reverse breakdown voltages, V_{br} , of either of the diodes, derived from Poisson's equation for a Schottky diode can be expressed as [117]:

$$V_{br} = \frac{-E_{br}^2 \epsilon_0 \epsilon_r}{2N_D q} \quad (\text{eqn. 3.6})$$

where,

E_{br} = field required to cause breakdown

It is seen that the V_{br} is inversely proportional to the doping concentration. Knowing the doping profile, allows the estimation of the current surface doping from the breakdown voltage (for a given bias, the current will be increased if the doping is greater and vice versa). Hence, the need for further etching can be judged on this basis.

In practice, the probes must be kept clean and sharp with a reasonable separation between them. Figure 3.10 shows the plot of a typical V_{br} as a function of etch time in ammonia solution for an AlGaAs/GaAs HBT layer; typical etch rates for GaAs and $Al_{0.3}Ga_{0.7}As$ are 30 Å/sec and 25 Å/sec respectively. The large change in the V_{br} is used as guide to judge the etch depth and therefore it relies on significant variation in the doping profile of the wafer between successive layers.

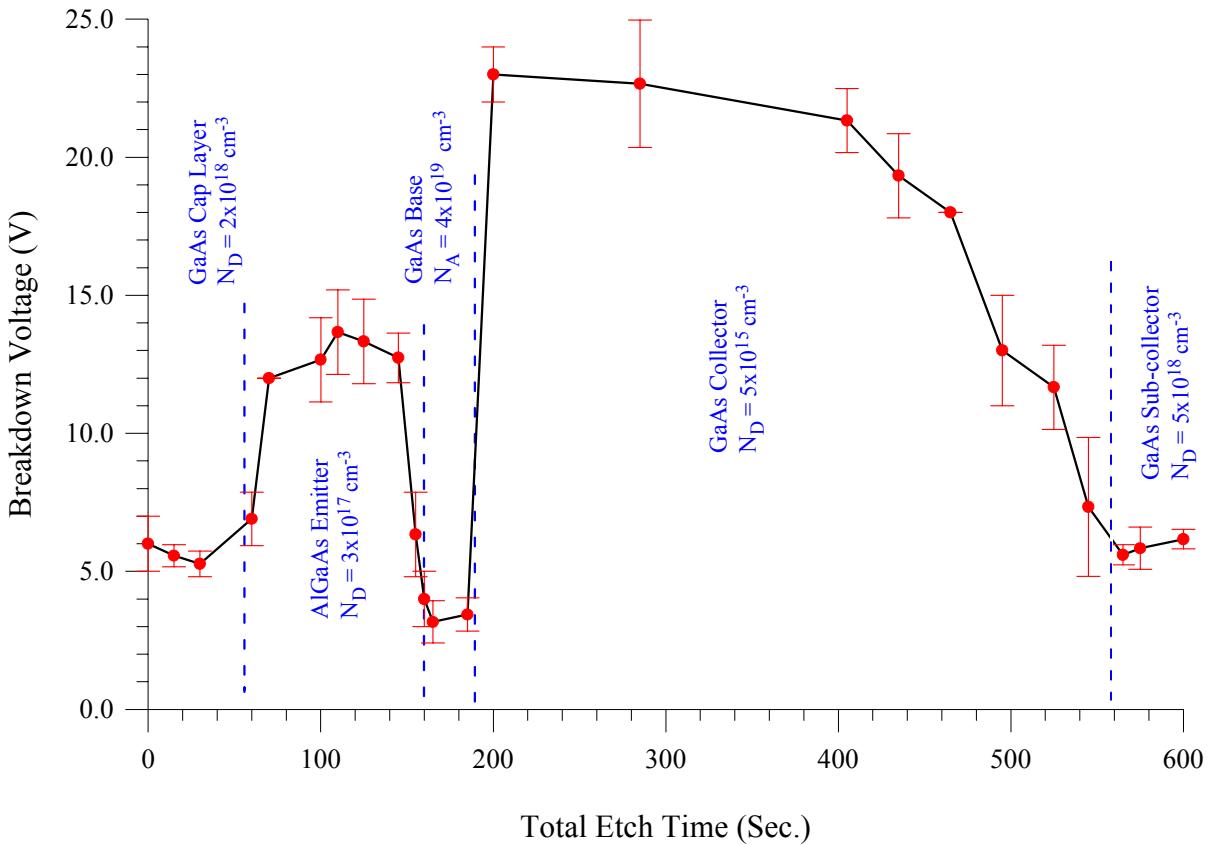


Figure 3.10: Plot of a typical breakdown profile as a function of etch time for an AlGaAs/GaAs HBT wafer (no. 3075-3); an ammonia solution ($8\text{NH}_3 : 3\text{H}_2\text{O}_2 : 400\text{H}_2\text{O}$) was used at room temperature and below 60% humidity.

This technique has been used successfully over the course of this work to fabricate AlGaAs/GaAs HBTs and other devices where selective etching was not a viable option.

3.8 Annealing Methods

There are two distinct techniques which were used for alloying ohmic contacts or annealing sputter induced damages out of substrates where appropriate. These are presented below. This is followed by a brief description of a technique adopted for producing good ITO ohmic contacts.

3.8.1 Thermal Furnace Annealing (TFA)

A schematic of the Gallenkamp thermal furnace oven used in this work is shown in Figure 3.11. It consists of long cylindrical hollow glass tube (app. 60 cm long, 2.5 cm diameter) surrounded by heating coils and thermal cladding material. Removable glass bungs with narrower glass pipes are attached at either end. These pipes are connected to allow the flow of forming gas (a mixture of 10% H₂ + 90% N₂) in and out of the tube during treatment.

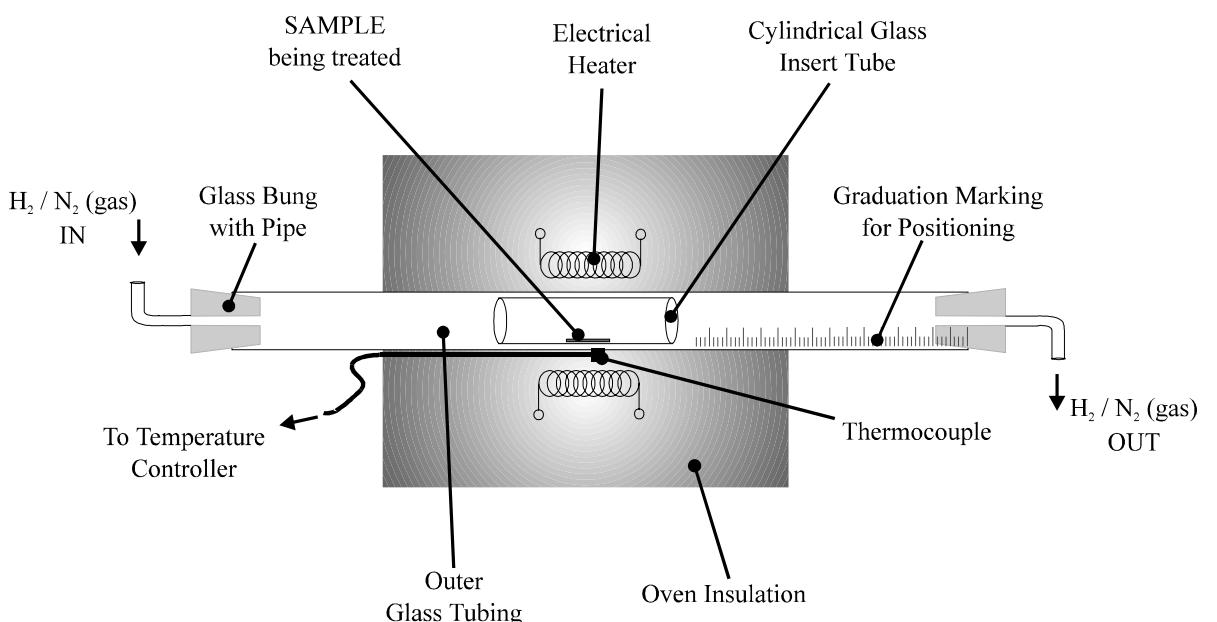


Figure 3.11: Schematic diagram of the Gallenkamp Thermal Furnace Annealing (TFA) system.

A smaller hollow tube (app. 10 cm long and 2 cm diameter), used for carrying the sample to be treated, can be slid in and out of the outer tube using a clean glass rod. There are graduation marks along the outer tube allowing the user to accurately note the position of the inner tube and hence the sample. There is also a thermocouple placed in close proximity to the central part of the outer glass tube, which is the hottest region. The system is capable of operating in the temperature range 100°C up to 800°C. Power to the 1kW heating coils is controlled from a temperature controller to set the desired temperature.

3.8.2 Rapid Thermal Annealing (RTA)

The rapid thermal annealer (RTA) was built in-house previously. As the name suggests, the RTA allows “flash” annealing by swiftly raising the temperature (typically from 25°C to

400°C in 10 sec.). It consists of a small vacuum chamber pumped by an ordinary rotary pump (minimum pressure reached is about 10^{-2} torr) and a N₂ gas inlet to cool and maintain a steady pressure during annealing. Inside the chamber there are two graphite strips (2.5cm x 15cm x 1mm) stacked vertically with app. 2mm separation between them. These strips are clamped between two supportive metal rods through which a large current can be passed to raise the temperature. There is also a thermocouple placed on the centre of the lower graphite strip for controlling purposes.

Annealing is carried out by placing the sample between the two graphite strips. The chamber is then evacuated and then flushed with N₂. This is repeated 3 times to remove any traces of moisture and contaminants. Finally with both the pump outlet and the N₂ inlet opened simultaneously, a steady pressure just below atmospheric is reached. The annealer is set to the desired temperature and switched on for the required period (between 30 to 60 sec. is adequate for most applications). After this period, power is turned off and the sample is allowed to cool in the steady flow of N₂. When the temperature reaches about 45°C (in about 3 min.) the sample is removed.

3.8.3 Annealing ITO Ohmic Contacts

In the fabrication of ITO ohmic contacts, it was necessary to use a “step-wise” annealing approach (see section 6.2.). The TFA was used for this purpose and the temperature controller was set to 800°C with a steady flow of forming gas. The lateral temperature variation along the outer glass tube was calibrated to the distance from the mouth. This was then used to set the required temperature for the ITO ohmic contact annealing scheme and the position was varied when a new temperature was required.

The calibration itself was carried out by using a second thermocouple attached to a glass rod which was placed inside the outer glass tube of the TFA. The temperature and the position of the thermocouple was noted from the graduation marks. Figure 3.12 shows the results of the calibration.

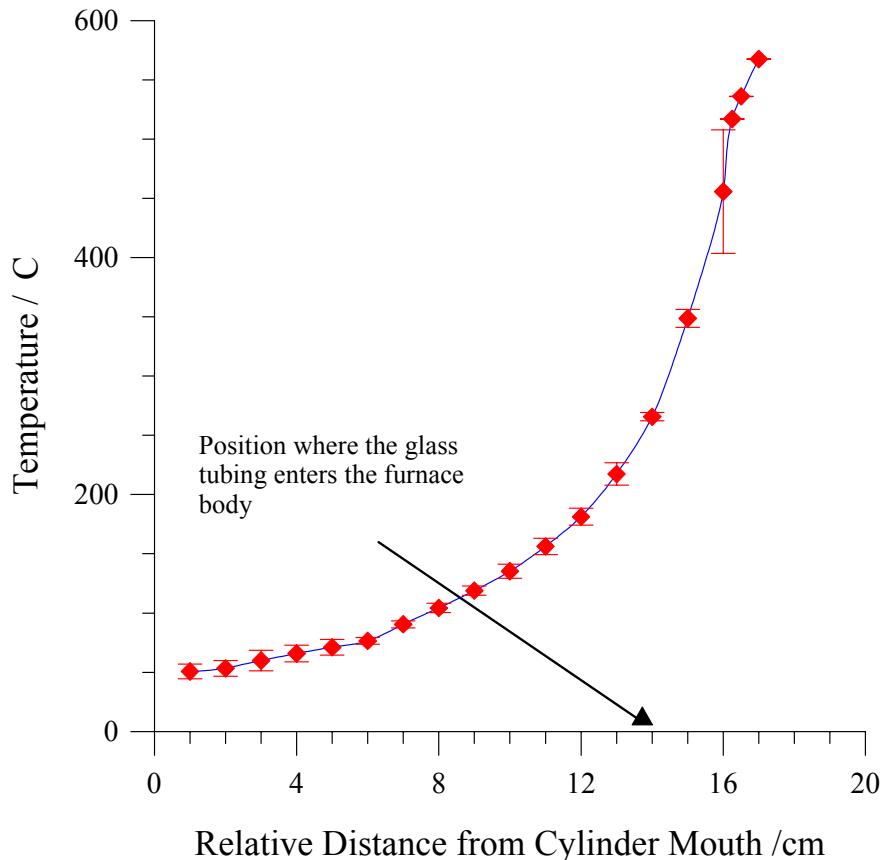


Figure 3.12: Calibration curve for thermal oven set at a temperature of 800°C with forming gas flowing.

3.9 Wafer Thinning Technique

After the major device fabrication steps are complete, the wafer is often thinned from the bottom to ensure maximum heat conduction during device operation. It is also important for scribing very small devices.

The front of the wafer is covered with a thick photoresist (3 μm) and hard baked to protect the devices from any mechanical damage. It is then gently turned upside down and pasted on a cylindrical aluminium chuck (2 cm diameter) with wax. The surface to be lapped faces outward.

The reverse side is then polished using a mechanical polisher covered with fine grained sand paper. Once the required thickness has been removed, the sample is recovered by a soak in TCE to remove the wax. The photoresist from the front surface is removed in the usual way using acetone.

3.10 Scribing, Packaging and Bonding

Before processing can begin, all wafers have to be reduced to a standard size. This is made possible by means of scribing. Scribing is also necessary for precisely separating individual devices (usually in the 100 μm diameter range) for mounting onto transistor headers after all other fabricating stages have been completed.

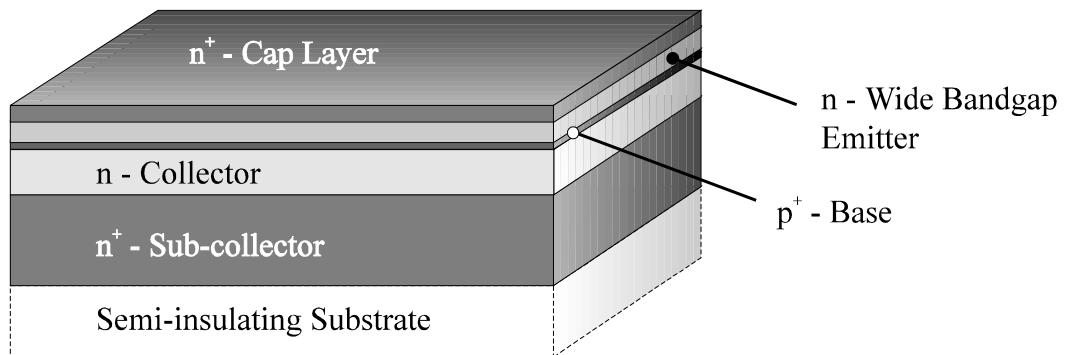
A pneumatic scribe (Tempress Automatic Scribing Machine) was used in this work. The wafer to be cut is firmly held in position on the scribe stage by a vacuum chuck. Scribe marks are made using a diamond tip attached at the end of a mechanised arm which can be accurately positioned and moved across the wafer. Once scribing is complete, the wafer is sandwiched between two thick clean-room wipes. A heavy roller is then firmly run over it. Cracking sound confirms the cleaving action. Individual pieces are then dusted with dry N₂ gas ready for packaging.

T05 transistor headers are used for mounting test samples. At first the T05 is coated with a conductive epoxy resin. A tiny drop of EPO-TEK H21D [118] is sufficient for packaging a sample several millimeters across. Suitably scribed pieces are then gently placed on the glued spot and allowed to cure at 130°C for 2 hours.

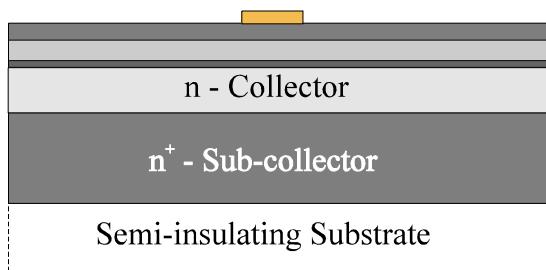
Once the sample has been packaged, the devices are ready to be bonded to individual legs of the T05 header. A wedge bonder (Westbond model no. 7400A) machine and 17 μm diameter gold wire was used for most bondings. Bonding is usually carried out at 125°C. This machine is also equipped with an ultrasound source which may be used for stubborn and difficult bondpads although excessive use can damage the device. A metal cap is then placed on the header to protect the devices within and prevent accidental breakage of the fine bond wires through mechanical stress.

3.11 Processing Steps - the HBT Example

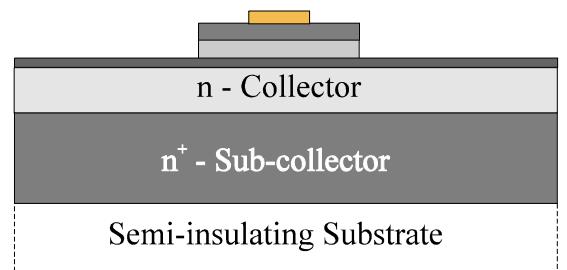
The fabrication starts with thoroughly cleaning the wafer. A liftoff lithography is followed by metalisation of the emitter as shown in step C1 of Figure 3.13. This is followed by step C2 when a mesa etch to the base is carried out after appropriate etch lithography has been done. Steps C3, C4 and C5 involve the base metalisation, mesa etch to sub-collector layer and finally the collector contact metalisation respectively. The relevant chemical etching steps have already been described in section 3.5.



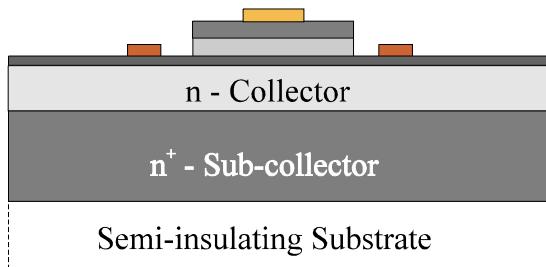
Schematic of a HBT Device Layer Structure Before Fabrication



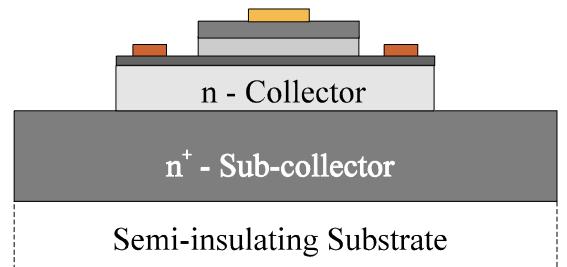
Step C1: Emitter Metal Contact



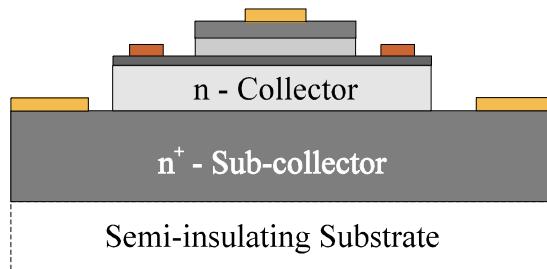
Step C2: Emitter Mesa Etch



Step C3: Base Metal Contact



Step C4: Base Mesa Etch



Step C5: Collector Metal Contact

Figure 3.13: Processing steps for (large geometry) conventional HBT devices

In the case of the ITO emitter contact HPTs, a few of the initial fabrication steps are either different or modified from those of the conventional contact devices. These are shown in Figure 3.14. As before the wafer is thoroughly cleaned followed by ITO deposition as shown in step T1. Step T2 shows that a film of Al is then deposited over the ITO and subsequently patterned with the emitter mesa mask for etch lithography and wet etched using the KOH solution (see section 3.6).

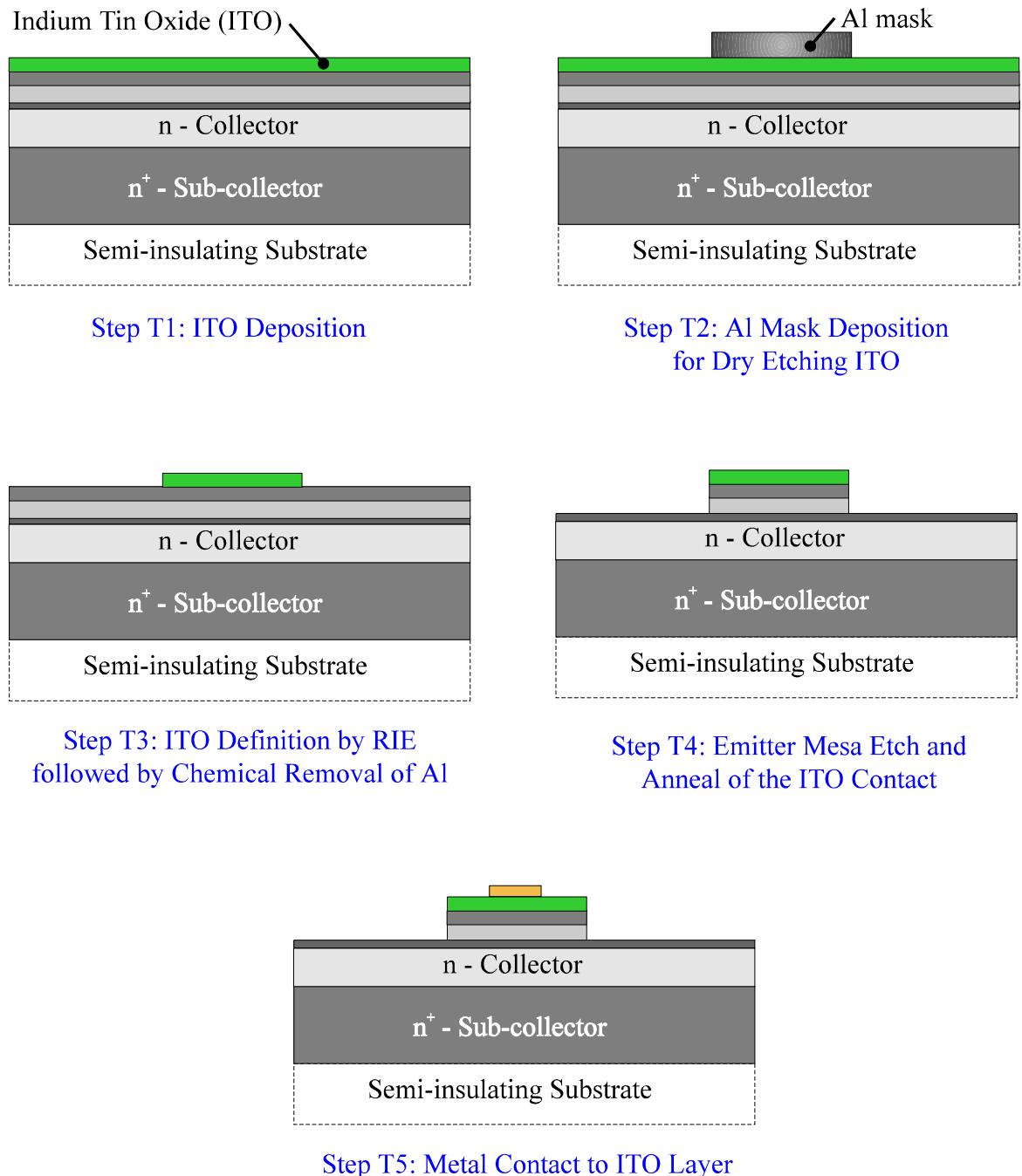


Figure 3.14: Additional processing steps for (large geometry) HPT devices with transparent ITO emitter ohmic contacts

The ITO is then dry etched in Ar followed by Al mask removal by dissolving in KOH as before. This is shown in step T3 of Figure 3.14. The sample is then patterned again with photoresist and etched to the base. At this point the ITO contact is annealed (step T4), followed by further liftoff lithography using the emitter metal mask. A metal is then deposited over a part of the ITO ohmic contact for bonding purposes (step T5). The remainder of the processing is the same as those shown in steps C3, C4 and C5 of Figure 3.13 for conventional HBT fabrication.

4. Measurement and Analysis Techniques

4.1 Transmission Line Model - TLM

Transmission Line Model (TLM) theory was used for assessing the quality of ohmic contacts as well as electrical properties of ITO films used in this study. This technique was proposed by Reeves and Harrison. A detailed analysis is available in their published work [119,120].

4.1.1 Theory

A schematic diagram of a semiconductor material with ohmic contact pads prepared for TLM analysis is shown in Figure 4.1. It can be seen that the sample is first mesa etched usually to a semi-insulating substrate or to a depth where there is a natural depletion layer such as between n^+ and p^+ material. This is done in order to isolate columns of the conductive epitaxial layer thereby restricting current flow within the mesa height, d . Metal pads, of finite width, w , and length, s , are then deposited on the mesa at a linearly increasing pad spacing, L , such that $L_1 < L_2 < L_3$.

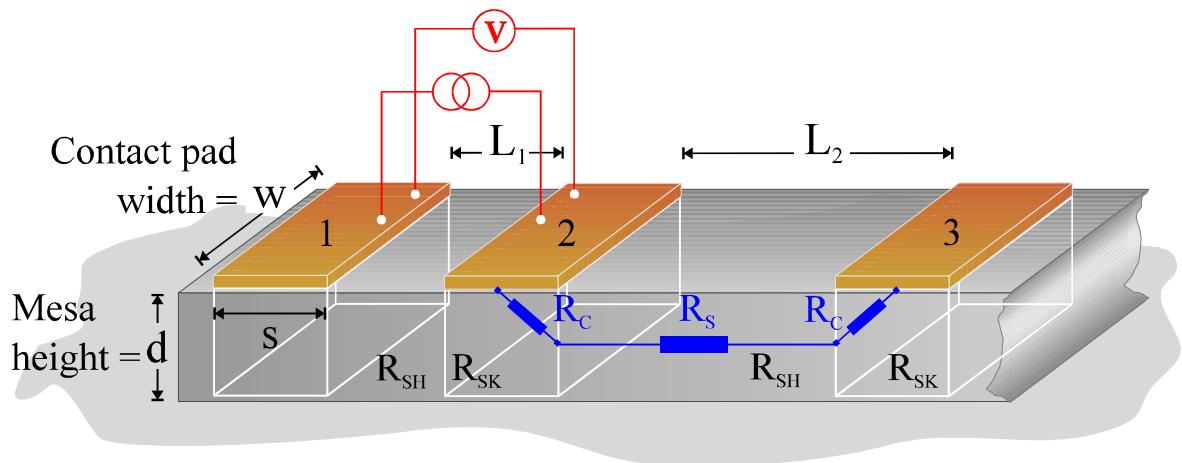


Figure 4.1: Schematic diagram of a semiconductor material with ohmic contact pads prepared for TLM analysis.

A constant current is passed between two adjacent pads through two probes; a second set of probes are then used to measure the voltage drop using a digital volt meter (DVM) enabling the total resistance between the pads to be obtained. Separate current source and DVM are

preferred to a single ohm meter because of the latter's relatively low impedance which may give rise to inaccuracies. The process is repeated and the total resistance is plotted on a linear graph as a function of pad spacing; an example is shown in Figure 4.2.

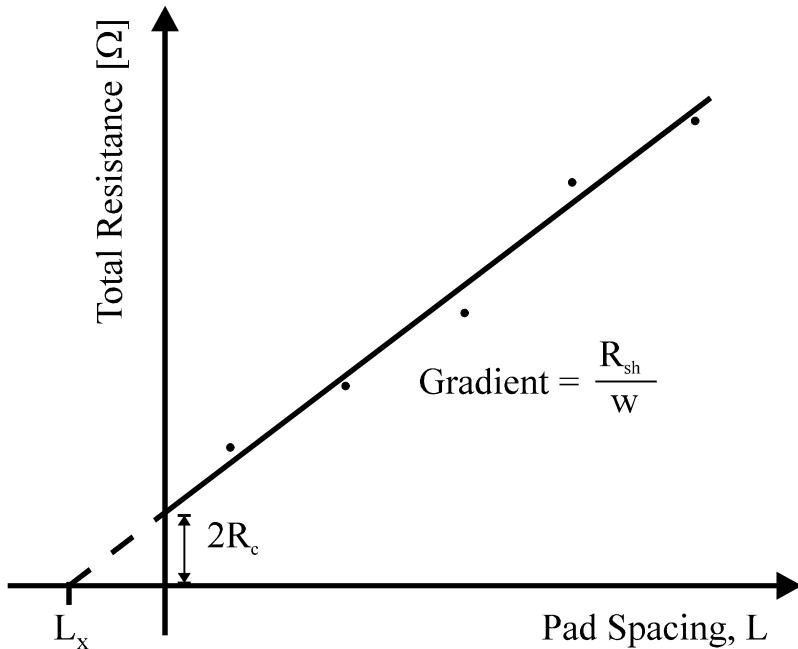


Figure 4.2: An example of a plot of total resistance as a function of TLM pad spacing

From Figure 4.1, it is seen that the resistance, r , between two adjacent pads, is given by:

$$r = 2R_c + R_s \quad (\text{eqn. 4.1})$$

where,

R_c = resistance due to the contact

R_s = resistance due to the semiconductor material

R_s is given by:

$$R_s = \frac{\rho L}{w} \quad (\text{eqn. 4.2})$$

where,

ρ = resistivity of the semiconductor material

But, since the sheet resistance, R_{sh} , of the semiconductor is given by ρ/d , we can re-write (eqn. 4.1) as:

$$r = 2R_c + R_{sh} \frac{L}{w} \quad (\text{eqn. 4.3})$$

Thus, (eqn. 4.3) has a gradient of R_{sh}/w and x and y axis intercepts at L_x and $2R_c$ respectively. Reeves *et al* [119] have shown that R_c can be expressed as:

$$2R_c = \frac{2R_{sk}L_T}{w} \quad (\text{eqn. 4.4})$$

where,

R_{sk} = modified sheet resistance of the material directly underneath the pads

L_T = the transfer length related to the distance required for current to flow into or out of the ohmic contact:

and,

$$L_T = \sqrt{\frac{\rho_c}{R_{sk}}} \quad (\text{eqn. 4.5})$$

where,

ρ_c = specific contact resistance

Using (eqn. 4.3) and (eqn. 4.4), the relationship between L_x and L_T is given by:

$$L_x = \frac{2R_{sk}L_T}{R_{sh}} \quad (\text{eqn. 4.6})$$

Rearranging (eqn. 4.4),

$$L_T = \frac{R_c w}{R_{sk}} \quad (\text{eqn. 4.7})$$

Rearranging (eqn. 4.5),

$$\rho_c = L_T^2 \cdot R_{sk} \quad (\text{eqn. 4.8})$$

Substituting (eqn. 4.7) in (eqn. 4.8),

$$\rho_c = \frac{R_c^2 w^2}{R_{sk}} \quad (\text{eqn. 4.9})$$

In practice, R_{sk} is determined using the “end contact resistance” analysis. Referring back to Figure 4.1, let us consider three resistances between pads 1 and 2, 2 and 3 as well as 1 and 3, denoted by R_{12} , R_{23} and R_{13} respectively. Using, (eqn. 4.3), these can be expressed as:

$$R_{12} = R_{c1} + R_{c2} + R_{sh} \frac{L_1}{w} \quad (\text{eqn. 4.10})$$

$$R_{23} = R_{c2} + R_{c3} + R_{sh} \frac{L_2}{w} \quad (\text{eqn. 4.11})$$

$$R_{13} = R_{c1} + R_{c3} + R_{sh} \frac{L_1 + L_2}{w} + R_{sk} \frac{s}{w} \quad (\text{eqn. 4.12})$$

where,

s = length of the contact pad

Thus, the end contact resistance, R_e is defined as follows:

$$R_e = \frac{R_{12} + R_{23} - R_{13}}{2} \quad (\text{eqn. 4.13})$$

Substituting (eqn. 4.10), (eqn. 4.11), and (eqn. 4.12) in (eqn. 4.13) we obtain:

$$R_e = R_c - \frac{R_{sk}s}{2w} \quad (\text{eqn. 4.14})$$

Hence,

$$R_{sk} = \frac{2w}{s}(R_c - R_e) \quad (\text{eqn. 4.15})$$

Substituting (eqn. 4.15) in (eqn. 4.9), the specific contact resistance, ρ_c , can now be expressed as:

$$\rho_c = \frac{R_c^2 ws}{2(R_c - R_e)} \quad (\text{eqn. 4.16})$$

In addition to these parameters, the transfer resistance, R_t , is often used as a figure of merit in the related literature. R_t is given by:

$$R_t = R_c \cdot w \quad (\text{eqn. 4.17})$$

4.1.2 Experimental Set-up

In this study, the TLM pattern consisted of a rectangular mesa and eight rectangular contact pads. The mesa dimension was $300\mu\text{m} \times 120\mu\text{m}$; the metal pads were $100\mu\text{m} \times 50\mu\text{m}$ (corresponding to w and s respectively); and the pad spacings were $10\mu\text{m}$, $20\mu\text{m}$, ... $60\mu\text{m}$, and $70\mu\text{m}$ (corresponding to L_1 , L_2 , ... L_6 and L_7 respectively). Once the sample to be tested was fully prepared, the “Auto TLM” system was used for taking the measurements [121]; this

consists of a 16 fingered (8 x 2) probe card connected to a current source, DVM, controller card and a PC. Once the probe card is aligned and lowered over the mesa, all resistance values are measured automatically and transferred to the PC; generally, a 10mA source current was used for these measurements. The acquired data was then plotted and analysed to access the ohmic contacts or the ITO films.

From a purely experimental point of view, one has to be very careful about deformation to metal pad shape especially after anneal treatments where AuGe based contacts tend to flow. Deformed pads alter many of the vital dimensions which are pre-set in the analysis program; hence, in such cases, inspection under the microscope is required to obtain more realistic values for these dimensions and they need to be re-entered in order to obtain accurate values.

4.2 Current-Voltage Measurements (I-V)

Current-voltage (I-V) measurements refer to d.c. characterisations of devices for the purposes of performance analysis and parameter extraction. In this section, the importance of various Schottky diode and HBT parameters are briefly discussed. This is followed by a description of the necessary experimental set-up. The actual settings on the measuring equipment are listed in Appendix C.

4.2.1 Schottky Diode Parameter Extractions

The theory behind these parameters has been dealt with in section 2.2. In addition a number of good publications are available in the literature which deal with various general [122,123] and specific extraction techniques where diodes suffer from high series resistance [124]. In practice, most of the diode parameters are extracted by first plotting its I-V characteristics on a $\log_{10}(I)$ vs. V graph as shown in Figure 4.3.

The semi-logarithmic I-V plot can be divided into three distinct regions: region 1 is the non-linear region due to non-exponential behaviour of diodes at low voltages (leakage currents amongst other factors); region 2 is the linear region and region 3 where the current is limited by the series resistance.

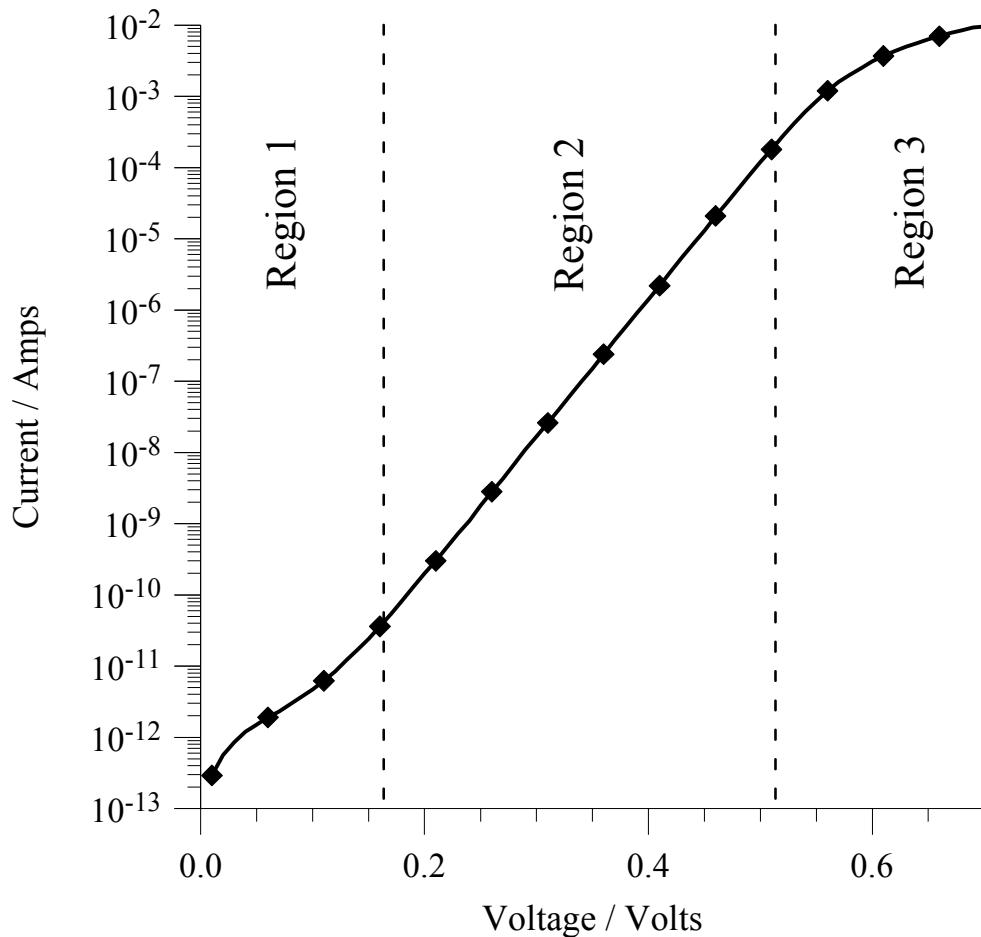


Figure 4.3: Semi-logarithmic I-V plot for a typical Schottky or a p-n junction diode.

4.2.1.1 Barrier Height, ϕ_{bo}

This is defined as the potential barrier to thermionic emission that naturally exists between an intimate metal and semiconductor contact at zero applied bias. Current transport dominated by thermionic emission is assumed and the ϕ_{bo} is extracted by fitting a straight line in region 2 of Figure 4.3. From (eqn. 2.6) it is seen that the y-axis intercept of this fit gives the saturation current I_{teo} :

$$I_{\text{teo}} = AA^{**} T^2 \cdot \exp\left(\frac{-q\phi_{\text{bo}}}{kT}\right) \quad (\text{eqn. 4.18})$$

Thus,

$$\phi_{\text{bo}} = \frac{kT}{q} \ln \frac{AA^{**} T^2}{I_{\text{teo}}} \quad (\text{eqn. 4.19})$$

This approach requires the modified Richardson constant, A^{**} , to be known for the particular metal/semiconductor junction. As discussed later in section 6.1.1, the slope of an Arrhenius plot ($\ln[I_{te}/T^2]$ vs. $1/T$) can be used to extract a more accurate value of the ϕ_{bo} . However, this requires that the diode be first characterised at several temperatures.

4.2.1.2 Ideality Factor, n

The diode junction quality is quantified using its ideality factor, n. Again, using the linear fit to region 2 of Figure 4.3 and (eqn. 2.6), this can be expressed as:

$$\begin{aligned} n &= \frac{q}{kT} \frac{V}{\ln(I/I_{teo})} \\ &= \frac{q}{kT} \cdot \frac{1}{\ln(10)} \cdot \frac{1}{\text{slope}} \end{aligned} \quad (\text{eqn. 4.20})$$

4.2.1.3 Series Resistance, R_s

The series resistance is determined from region 3 of Figure 4.3 where at high current, the plot becomes flat and is assumed to be dominated entirely by the R_s . A plot of V/I is made and R_s is extracted from the point where this curve saturates to a steady minimum value.

4.2.2 Bipolar Transistor / HBT Parameter Extraction

The theory of HBTs was dealt with in section 2.4. Since adequate information is available in the literature [125,126] only an overview of the relevant extraction techniques will be provided here.

4.2.2.1 Output Characteristics

This is a series of plots of the collector currents, I_c , as a function of collector-emitter voltage, V_{ce} , at different base currents, I_b . From this plot, it is possible to ascertain the amount of offset voltages, ΔV_{ceo} , between the emitter-base and the base-collector (hetero and homo) junctions; the linearity of gain with I_b ; and the presence of base-width modulation amongst other phenomena.

4.2.2.2 Gummel Plot

The simultaneous plot of I_c and I_b vs. the base-emitter voltage, V_{be} , on a semi-logarithmic scale is known as a Gummel Plot. This plot is extremely useful in device characterisation because it reflects on the quality of the emitter-base junction while the base-collector bias, V_{bc} , is kept at a constant; in this study, $V_{bc} = 0$. A number of other device parameters can be ascertained either quantitatively or qualitatively directly from the Gummel plot because of its semi-logarithmic nature: the d.c. gain, β ; base and collector ideality factors, n_{Ib} and n_{Ic} ; series resistances and leakage currents.

4.2.2.3 D.C. Current Gain, β

The d.c. current gain, β ($= I_c/I_b$), of a transistor is measured in a common emitter configuration is an important figure of merit for the device. Particularly useful information can be obtained when β is plotted versus the collector current, I_c . Ideally, this should be as flat a curve as possible over a wide range for good devices.

In practice, the gain is limited by leakage currents at low I_c and hence the presence and nature of these leakage currents can be ascertained by a plot of $\log \beta$ vs. $\log I_c$. Similarly, a high collector current densities ($> 10^5 \text{ Acm}^{-2}$), the gain is also reduced primarily due to the onset of high injection effects in the base and the Kirk Effect [127]. High injection effects, occurring at the point where the number of electrons injected from the emitter into the base become comparable to native holes in the base, are unlikely to affect HBTs where base dopings, N_{AB} , of 10^{19} cm^{-3} is common. The Kirk Effect refers to gain reduction due to the electron concentration in the collector depletion region becoming comparable to the native collector donor levels, N_{DC} , which affects the electric field in the base-collector junction resulting in an increase of hole injection from the base into the collector; this is also known as “base pushout”. In HBTs, the latter effect is minimised by the relative (to homojunction transistors) high collector doping density, N_{DC} .

4.2.2.4 Emitter and Collector Series Resistance, $R_{ee'}$ and $R_{cc'}$

The $R_{ee'}$ is measured by connecting the transistor in a common emitter configuration, setting $I_c = 0$ and varying the I_b , as shown in Figure 4.4.

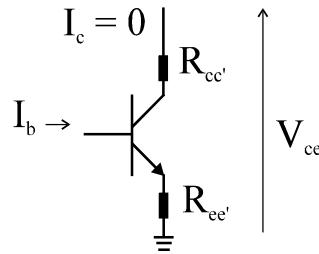


Figure 4.4: Transistor configuration for measuring emitter series resistance, $R_{ee'}$.

Since $I_c = 0$, there is no potential drop across $R_{cc'}$, and hence the entire V_{ce} is dropped across $R_{ee'}$ provided the base-emitter junction is not turned on (i.e. I_b is very low $< 5 \text{ mA}$). $R_{ee'}$ is then given the slope of the plot of I_b vs. V_{ce} . $R_{cc'}$ can be measured by interchanging the emitter and the collector terminals in Figure 4.4.

4.2.3 FET / HEMT Parameter Extraction

4.2.3.1 Transfer Characteristics

This is a series of plots of the drain-source currents, I_{ds} , as a function of drain-source voltage, V_{ds} , at different values of gate bias, V_{gs} . This plot can be divided into three regions: the linear region where V_{ds} is small compared to the sum of the gate built-in potential, V_{bi} and V_{gs} and the channel current responds linearly to an increase in V_{ds} ; the triode region at increased V_{ds} where the gate-drain depleting potential, V_{gd} , is greater than V_{gs} and the channel current begins to be restricted by this expanded depletion region; the saturation region is where the V_{ds} is sufficiently high to fully deplete the channel and current flow saturated at the value, I_{dss} , when this first occurs.

4.2.3.2 Transconductance, g_m

The transconductance is a quantitative measure of an FET device's amplification capability. It is given by differentiating the channel current in the saturated region at a constant V_{ds} . Thus,

$$g_m = \frac{\partial I_{dss}}{\partial V_{gs}} \quad | \quad V_{ds} \text{ constan t} \quad (\text{eqn. 4.21})$$

4.2.4 Experimental Set-up

The d.c. characterisation set-up essentially consists of a probe station, a Hewlett-Packard HP4145B Semiconductor Parameter Analyser (SPA) and an IBM compatible personal computer (PC). The probe station is connected to the SPA via a set of BNC cables enabling the measurement of a number of d.c. parameters. Devices packaged on T05 transistor headers can be characterised using an appropriate box equipped with BNC sockets. The SPA is in turn connected to the PC by an IEEE interface allowing data transfer. A schematic of the set-up is shown in Figure 4.5:

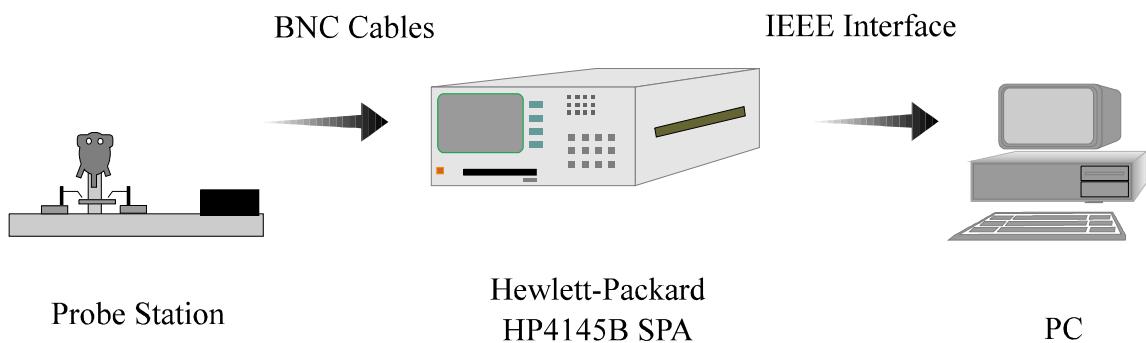


Figure 4.5: Schematic diagram of I-V measurement and data transfer set-up

The SPA is designed to be a fully automatic high performance and versatile test instrument capable of measuring, analysing and graphically displaying d.c. characteristics of a wide range of semiconductor devices. It has four programmable voltage source/monitor ports (SMU), two programmable voltage source ports (V_s) and two voltage monitor ports (V_m). Each SMU can be programmed to operate in one of three modes:

1. voltage source or current monitor (V)
2. current source or voltage monitor (I)
3. common ground (COM)

Thus appropriate programming of the SMUs involving sweeping the voltage/current or holding these at a constant value enables the user to perform a wide range of operations on the device under test. The maximum current which can be sourced from the SPA is 100 mA while the minimum measurable current is 5×10^{-13} A lending itself to good use for most d.c. parameter extractions.

The HP4145B SPA also has a 3.5 inch floppy disk drive which can be used for storing measured data, programs and auto sequences. The data is stored as ASCII text and can be easily transferred into the PC through the IEEE interface at the rear. Programs are usually a

set of instructions entered by the user defining the SMU mode and its limit, the graphical display screen and the axis. An auto sequence, as its name implies, is a series of programs or functions which are automatically carried out by the instrument once it is started by the user. Thus for a HBT, an auto sequence can be written to measure, display and save the output, the gain, the Gummel plot, the individual junction characteristics and the collector and emitter series resistances respectively with the press of a single button. Time delays can also be incorporated into an auto sequence rendering the SPA into a very powerful and indispensable tool.

4.3 Capacitance-Voltage Measurements (C-V)

Capacitance versus (usually reverse) voltage, referred to as C-V, measurements can be used to study the most basic properties of semiconductor rectifying junctions. In addition to obtaining simple capacitance values at a given bias, which may be important for circuit simulation, the data can be manipulated to yield a number of other parameters such as the built-in potential, V_{bi} , the doping profile as a function of depth [128,129] and the barrier height [130]. C-V measurements also form the basis for more advanced analysis techniques such Deep Level Transient Spectroscopy (DLTS) [131]. However, only some of the more basic techniques will now be discussed in greater detail.

4.3.1 Theory

From Poisson's analysis, the depletion width of an abrupt p-n junction is given by:

$$x_{dep} = \sqrt{\frac{2\epsilon_0\epsilon_r}{q} \cdot \frac{(N_A + N_D)}{N_A N_D} \cdot (V_{bi} - V_{app})} \quad (\text{eqn. 4.22})$$

where,

x_{dep} = depletion width of an abrupt p-n junction

ϵ_0 = dielectric constant of free space

ϵ_r = dielectric constant of the semiconductor material

q = electronic charge

N_A = acceptor doping density in the p-region

N_D = donor doping density in the n-region

V_{bi} = built-in potential

V_{app} = applied bias

In case of a n-type Schottky junction, the above equation can be simplified to (eqn. 4.23). This is also appropriate for the analysis of a p-n junction where the p-region is very highly doped in comparison to the n-region, for example in the base-emitter or base-collector junctions of a N-p-n HBT. In these conditions, the application of a reverse bias is assumed to have no significant effect on the base width.

$$x_{\text{dep}} = \sqrt{\frac{2\epsilon_0\epsilon_r}{qN_D} \cdot (V_{\text{bi}} - V_{\text{app}})} \quad (\text{eqn. 4.23})$$

The junction capacitance of the devices is approximated to that of a parallel plate capacitor, which is given by:

$$C = \frac{\epsilon_0\epsilon_r A}{x_{\text{dep}}} \quad (\text{eqn. 4.24})$$

Substituting (eqn. 4.23) into (eqn. 4.24) yields:

$$C = \frac{\epsilon_0\epsilon_r A}{\sqrt{\frac{2\epsilon_0\epsilon_r}{qN_D} (V_{\text{bi}} - V_{\text{app}})}} \quad (\text{eqn. 4.25})$$

The measured C-V data can be manipulated to plot a graph of $1/C^2$ versus V_{app} as follows:

$$\frac{1}{C^2} = \frac{2}{qN_D\epsilon_0\epsilon_r A^2} \cdot (V_{\text{bi}} - V_{\text{app}}) \quad (\text{eqn. 4.26})$$

The x-axis intercept of (eqn. 4.26) yields the built-in potential, V_{bi} .

The doping profile for the semiconductor wafer, i.e. a plot of the doping concentration versus the distance from the junction, can be derived using one of two possible sets of equations. Firstly, the depletion width (corresponding to a measured capacitance value or applied bias) can be calculated from either (eqn. 4.24) or (eqn. 4.23); the use of (eqn. 4.23), however, requires V_{bi} to be determined using the intercept of (eqn. 4.26). Secondly, the doping concentration, N_D , (corresponding to a measured capacitance value) can be determined using either one of the following equations:

$$N_D = \frac{2}{q\epsilon_0\epsilon_r A^2} \cdot \frac{dV_{app}}{d(1/C^2)} \quad (\text{eqn. 4.27})$$

or:

$$N_D = \frac{C^3}{q\epsilon_0\epsilon_r A^2} \left(\frac{dC}{dV_{app}} \right)^{-1} \quad (\text{eqn. 4.28})$$

Whereas the derivation of (eqn. 4.27) is by differentiation of (eqn. 4.26) with respect to V_{app} , and necessary substitutions, (eqn. 4.28) can be derived by differentiating (eqn. 4.25) with respect to V_{app} . These derivations are presented in Appendix D1. The relative practical benefits of choosing between the two possible sets of equations when plotting the doping profile is discussed in section 4.3.3.

4.3.2 Experimental Set-up

The experimental set-up for the C-V measurement system consists of a probe station, a Hewlett-Packard HP4284A precision LCR meter with HP16048A test leads and a PC interfaced with the appropriate GPIB cable and IEEE interface card. The device under test is placed on the probe station and connected to the LCR meter via the test leads.

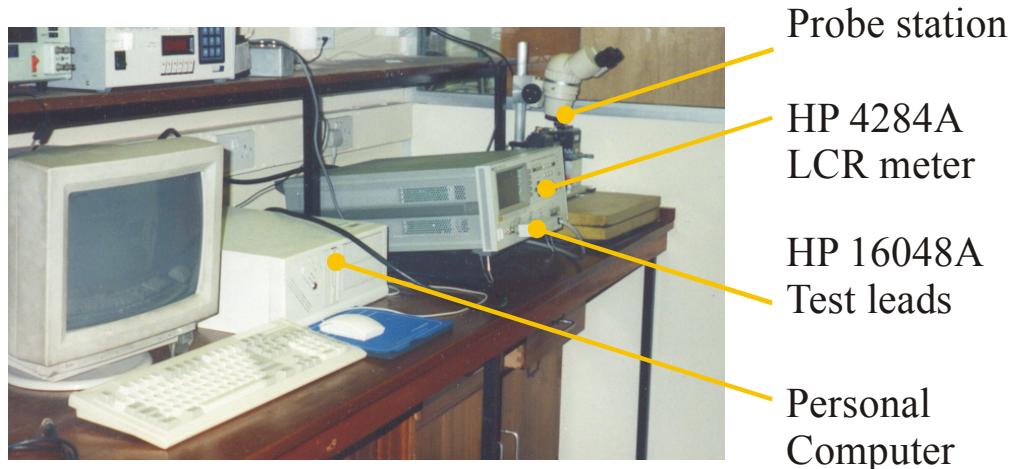


Figure 4.6: Photograph of the C-V measurement system.

A dedicated driver software, developed at King's College, resident in the PC is used to control the various functions of the LCR meter. In addition to C-V measurements over a wide range of bias and test frequencies, the HP4284A LCR meter is also capable of measuring the series resistance and any inductance present in the device being tested. The

frequency range for the test signal is 10kHz to 1MHz and the latter setting is used for all the measurements in this study. The shape of the test signal can also be varied from the usual sine wave to a ramp and triangular wave to study the effects of hysteresis loops. The measured data is saved directly in the PC and later analysed using external software.

4.3.3 Limitations

C-V measurements suffer from a number of fundamental limitations [132]. These include the total depth which can be profiled before the onset of avalanche breakdown on the semiconductor material and the validity of the depletion approximation. In a GaAs sample, where the maximum sustainable field is approximately $4 \times 10^5 \text{ Vm}^{-1}$, this depth varies between $0.02\mu\text{m}$ and $20\mu\text{m}$ for $N_D = 10^{18} \text{ cm}^{-3}$ and 10^{15} cm^{-3} respectively. This limit can be significantly extended at the cost of destroying the sample by using an electrolytic Schottky barrier and etching through it while making CV measurements. However, the two requirements for the depletion approximation, that the depletion region be free from mobile charge and have an abrupt boundary, are harder to fulfill in practice.

As seen from (eqn. 4.24) to (eqn. 4.28), accurate knowledge of the junction area is crucial to CV measurements. In addition, they are also vulnerable to erroneous interpretation particularly due to series resistance and parasitic capacitance [133] as well as those arising from the device geometry [134]. Undetected bias independent parasitic capacitance is particularly misleading when analysing small geometry devices where the perimeter/area ratio may be large; this is because while the peripheral parasitic capacitance proportional to the perimeter, the junction capacitance is proportional to the diode area.

4.4 Cryogenic Measurements

Cryogenic measurements refer to characterisations carried out under low temperature typically ranging from liquid helium (4.2K) or liquid nitrogen (77.3K) to below room temperature (298K). These measurements are used for determining a number of physical parameters & mechanisms in semiconductor materials and devices such as bandgap, barrier heights, defect levels, current transport mechanisms etc. In this study, the lowest temperature was limited to 77.3K, the boiling point of nitrogen.

4.4.1 Experimental Set-up

A Oxford Instruments variable temperature liquid nitrogen cryostat, model DN1704, in conjunction with a temperature controller, model ITC4, also manufactured by Oxford Instruments, constituted the major parts of the experimental set-up. A schematic diagram of the cryostat is shown in Figure 4.7:

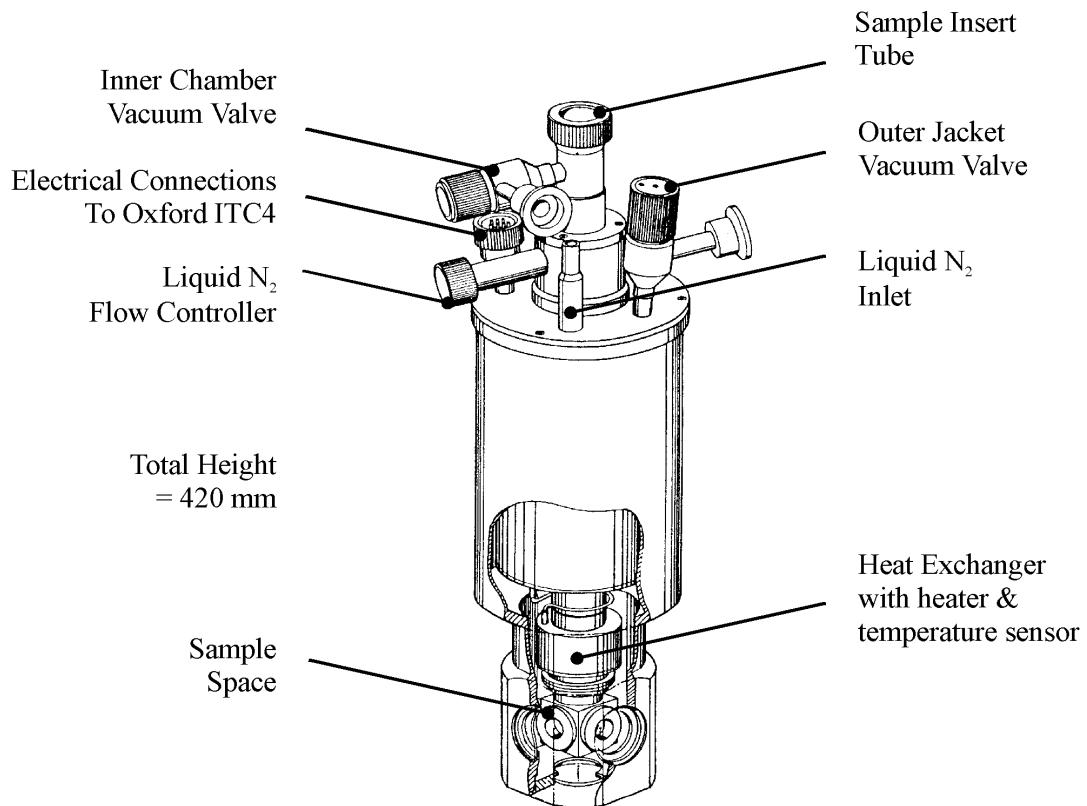


Figure 4.7: Schematic of the Oxford Instruments Cryostat, Model no. DN1704

The cryostat consists of an inner cylindrical sample chamber surrounded by an outer jacket; the outer jacket is pumped to a relative vacuum for thermal isolation during measurements. T05 headers containing the test device are mounted on a metallic rod insert which enters the cryostat from the top, placing the device into the sample space at the bottom. The insert has 11 BNC connectors: 10 for the T05 header and 1 for an additional temperature sensing silicon diode placed in close proximity to the test device a few millimeters above the T05 header.

A heat exchanger with heater and temperature sensor sits slightly above the sample. Following the insertion of the test device, the inner chamber is pumped down and flushed with dry nitrogen; the procedure is repeated several times to remove any water vapour which would otherwise condense at sub-zero temperature and may short out electrical contacts. Temperature control is achieved by setting the target on the ITC4 temperature controller and

adjusting the liquid nitrogen flow rate into the heat exchanger; it is opened progressively for lowering the temperature or closed for raising the temperature.

The temperature sensing diode mounted on the insert rod is first calibrated against the temperature reading of on the ITC4 controller display. This is achieved by passing a $10\mu\text{A}$ forward current from a Keithley source through the diode and measuring the voltage drop across it with a digital volt meter. The current is deliberately kept low to minimise the effects of local heating from the sensing diode. At a constant forward current, the voltage drop across a diode is inversely proportional to the ambient temperature according to the diode equation. This is illustrated by the experimental results as shown in Figure 4.8.

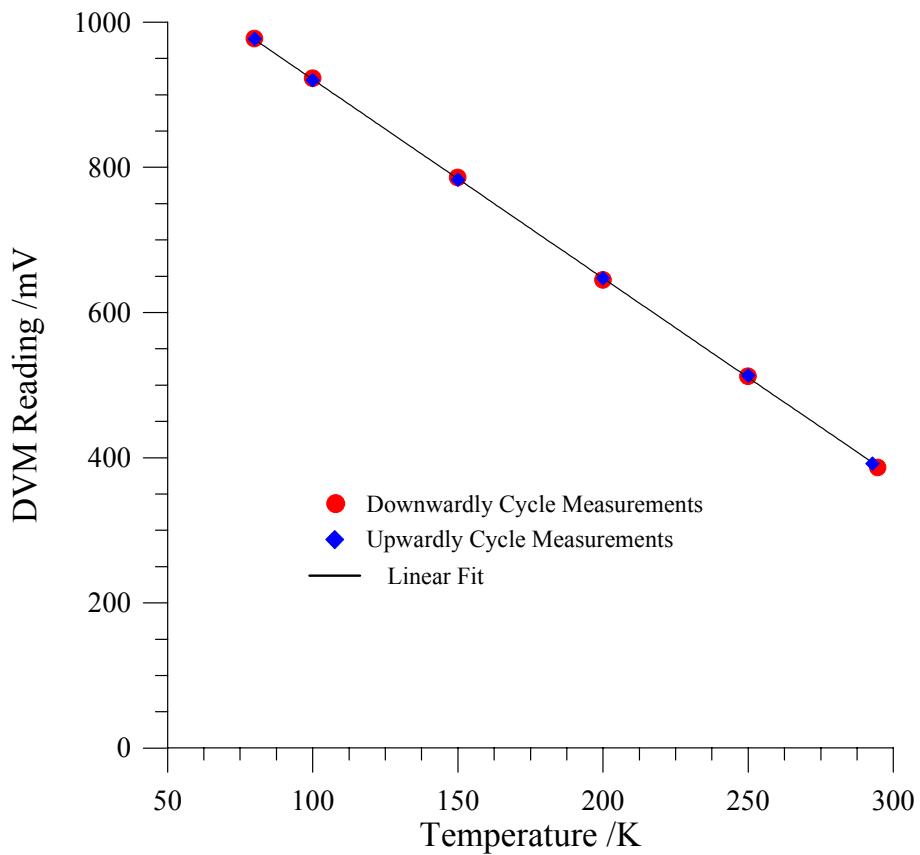


Figure 4.8: Graph of voltage drop across the temperature sensing diode vs. ambient temperature while the forward current was kept at a constant value of $10\mu\text{A}$.

In addition to calibrating the DVM reading versus the temperature for the sensing diode, it is important to establish the time required to reach a target temperature. This is shown by the measured results in Figure 4.9.

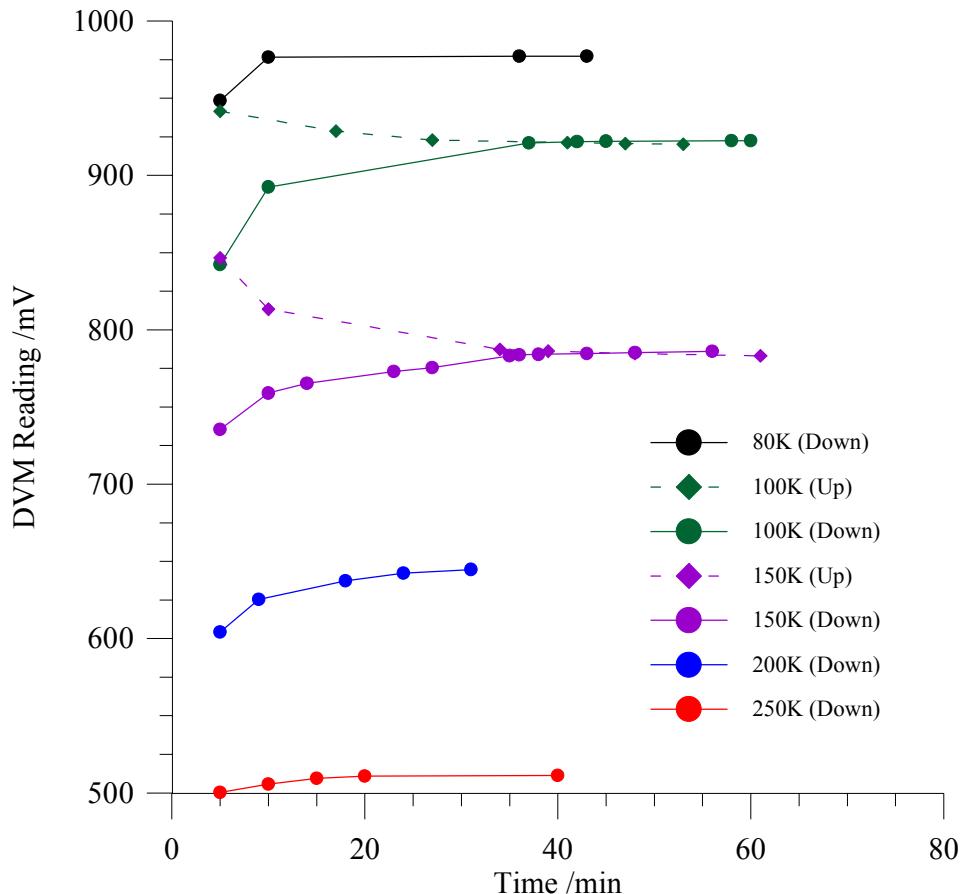


Figure 4.9: Graph showing the time required to reach a target temperature.

It is seen that the approximate time to reach a steady target temperature varies between 25 to 35 minutes. This time is independent of the direction i.e. the time taken to reach a higher temperature takes roughly the same as that for a lower temperature.

4.5 Optical Measurements

This section describes the experimental set-up behind some of the regular optical measurements carried out in the course of this study. These include the optical transmittance measurement of the ITO films and assessment of the absolute responsivities of the optoelectronic devices which were subsequently fabricated.

4.5.1 ITO Film Characterisation

The transmittance of the ITO films were measured using a double beam Perkin Elmer spectrophotometer (Model 330). In this system, the source beam from a filament lamp is first monochromated and then split into two separate coherent beams; a clear glass microscope cover slide is placed in the path of the first beam while an identical cover slide coated with the ITO film to be characterised is placed in the path of the second beam. These monochromatic beams are then converged and converted to a measurable electrical signal. This process is repeated by sweeping the wavelength of the beam over the entire range of the characterisation: 200 - 2000nm in this study. The measured transmittance is then recorded on a X-Y chart recorder or converted to a digital form using a suitable A/D converter.

The benefit of having a double beam spectrophotometer means that there is no need for two separate measurements (one for the uncoated and one for the ITO coated sample) but also the actual transmittance of the ITO films is obtained directly as a result leaving aside any common background artifacts such as interference due to the presence of water vapour or indeed characteristics of the microscope cover slides themselves.

4.5.2 Device Quantum Efficiency and Absolute Responsivity

The quantum efficiency, η , of an optoelectronic device is defined as the fraction of electrons collected over the number of incident photons which are absorbed [61]; this can be expressed as:

$$\eta = \frac{r_q}{r_p} \times 100\% \quad (\text{eqn. 4.29})$$

where,

r_q = rate of electron collection

r_p = rate of photon arrival

As discussed in later chapters, η varies with the wavelength, λ , of the photons and is therefore quoted for a specified λ .

The absolute responsivity, R , of the device at a given wavelength, is defined as the ratio of the output (photo generated) electrical current, I_{Ph} , over the corresponding input optical power, P_0 :

$$R = \frac{I_{Ph}}{P_o} \quad (\text{eqn. 4.30})$$

Since the energy of a photon is given by the product of its associated frequency, ν , and the Planck constant, h , the rate of photon arrival can be expressed as a function of the corresponding optical power:

$$r_p = \frac{P_o}{h\nu} \quad (\text{eqn. 4.31})$$

Substituting (eqn. 4.31) into (eqn. 4.29) yields:

$$r_q = \frac{\eta P_o}{h\nu} \quad (\text{eqn. 4.32})$$

and,

$$I_{Ph} = \frac{q\eta P_o}{h\nu} \quad (\text{eqn. 4.33})$$

where

q = the electronic charge

R , from (eqn. 4.30) can now be expressed as:

$$R = \frac{q\eta}{h\nu} \quad (\text{eqn. 4.34})$$

Since, the speed of light, $c = \nu\lambda$, the responsivity can also be expressed as:

$$R = \frac{q\eta\lambda}{hc} \quad (\text{eqn. 4.35})$$

In order to do absolute responsivity measurements, devices are packaged in T05 transistor headers. These are then plugged on a jig, as shown in Figure 4.10, designed to isolate mechanical vibrations (originating from measuring equipment) disturbing the precision optical alignment of the device under test. The jig can be rigidly mounted on a triple axis micro-manipulator situated on an optical bench.

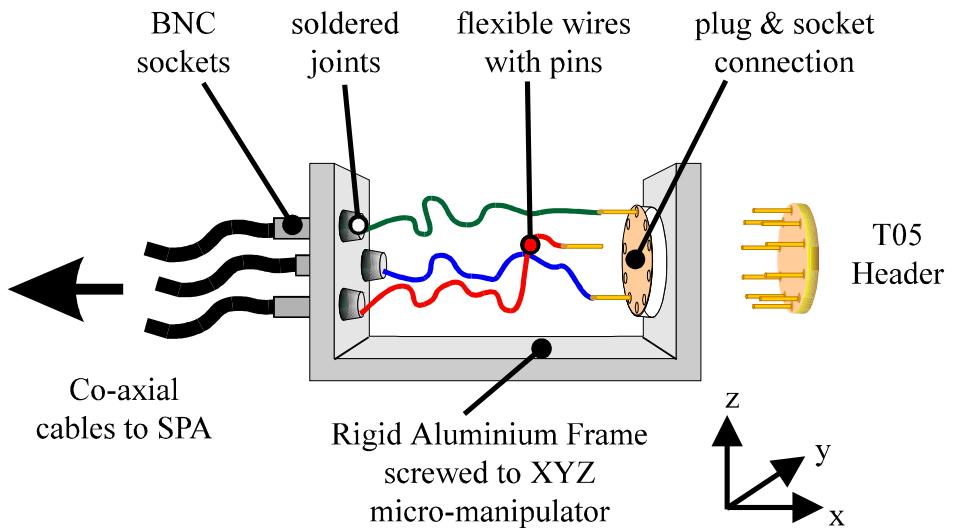


Figure 4.10: Schematic diagram of the jig used for optical characterisation of devices mounted on T05 headers.

A schematic block diagram and a photograph of the actual measurement set-up are shown in Figure 4.11 and Figure 4.12 respectively. The responsivity measurement set-up consists of a solid state Sharp LT022MS0 AlGaAs laser with an emission wavelength of 780 nm and a maximum output power of 5mW. The laser is packaged into a collimator and controlled by a dedicated laser driver circuit (available from Hero Electronics, UK). The emergent beam is then launched onto the surface of the detector using a convergence lens with beam diameter of less than 10 μm . Individual XYZ micro-manipulators, mounted on an optical bench, are used for positioning the laser, the lens and the detector to allow maximum flexibility in obtaining an optimum responsivity.

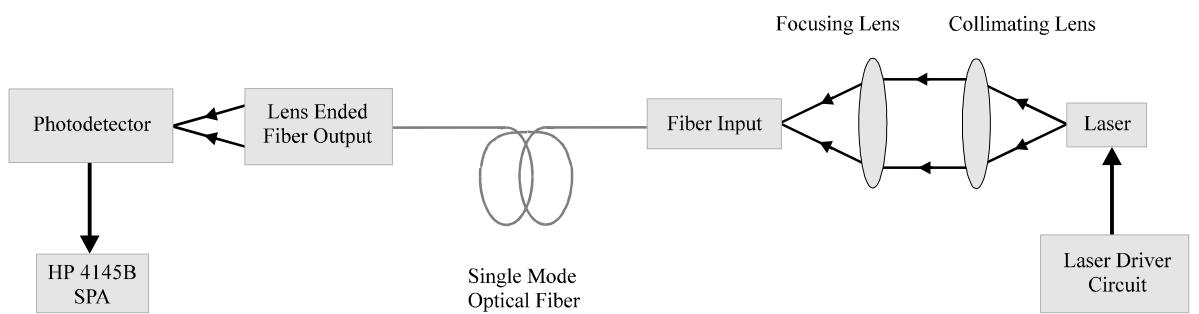


Figure 4.11: Schematic block diagram showing the essential set-up for optical characterisation of a test photodetector.

Figure 4.12: Photograph of optical bench being used for measuring the optical output characteristics of a photo detector under test.

In case of the responsivity measurements at 1310 nm, the Sharp laser was replaced by a Laser Diode Inc.(of Calif. USA) LD 6171 (BN 17444). This laser is packaged on a chip with an on-board fiber interface. Thus a monomode fiber designed to carry light at this wavelength was pig-tailed to the laser. A fiber with LD interface (model no. LOF121A 000411 - available from E-Tek Dynamics Inc., Calif. USA) and a fitted lens was used to focus the beam on the detector. The lens in this case has a nominal focusing capability of 2 μm diameter output beam.

4.6 Spectral Response

Spectral response, S_λ , of a device refers to its responsivity as a function of wavelength. In this section the experimental details and data interpretation methods are described while detailed discussions on the underlying theory is presented in Chapter 6.

4.6.1 Experimental Set-up

Spectral response measurements were carried out using a tungsten filament lamp, chopper and a Bentham monochromator (M300) over the 450 to 1830nm wavelength range. Light from the monochromator was incident on a device biased beyond the turn-on point in series with a suitable resistor. The voltage drop across the resistor was monitored through a lock-in amplifier and the spectral response was recorded on a synchronized plotter.

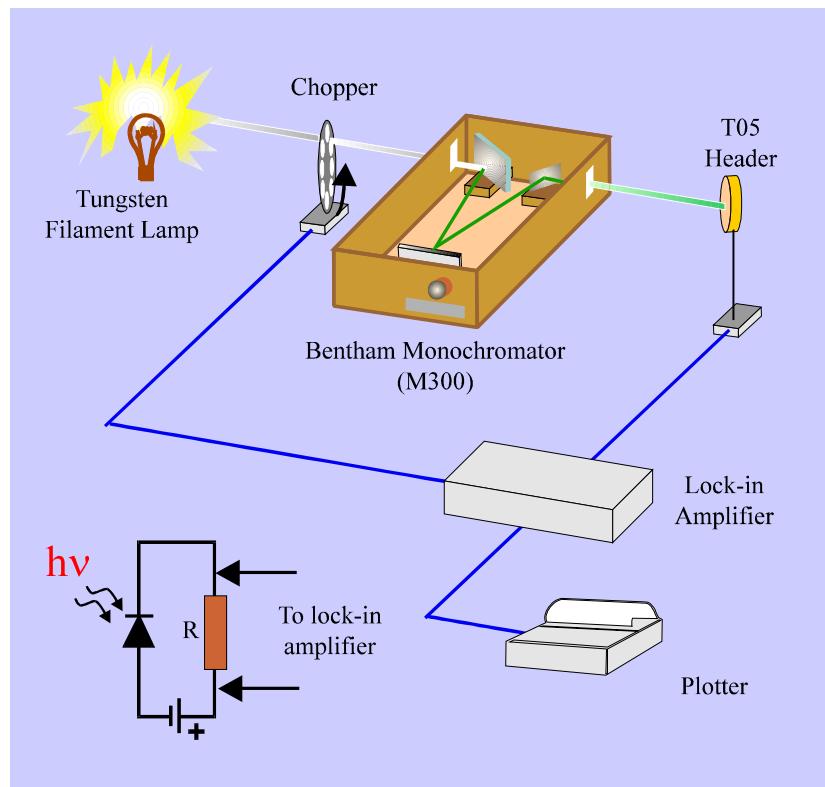


Figure 4.13: Schematic diagram of the experimental set-up for spectral response measurements on detector devices

4.6.2 Deconvoluting Optical Non-linearities

There are sources of non-linearities in a complex optical system such as the one described earlier. Two such sources are the tungsten filament lamp and the grating. These need to be taken into account in order to obtain a true spectral response of the device.

As the white light source is a tungsten filament lamp, the amount of energy radiated through the emission spectrum is not uniform; in practice it behaves like a blackbody source at a temperature of the filament which in this case is 3100K. The spectral radiancy, W_λ , of a blackbody at temperature T is given by Planck's formula [135,136]:

$$W_\lambda = \frac{2\pi hc^2}{\lambda^5} \left(\frac{1}{e^{hc/\lambda kT} - 1} \right) \quad (\text{eqn. 4.36})$$

where all the symbols have their usual meaning and the units for W_λ here is in $\text{Wm}^{-2}\mu\text{m}^{-1}$. The spectral radiancy of the Sun and a tungsten filament lamp are plotted using the above equation in Figure 4.14; the temperature of the Sun and the lamp are assumed to be 4500K and 3100K respectively.

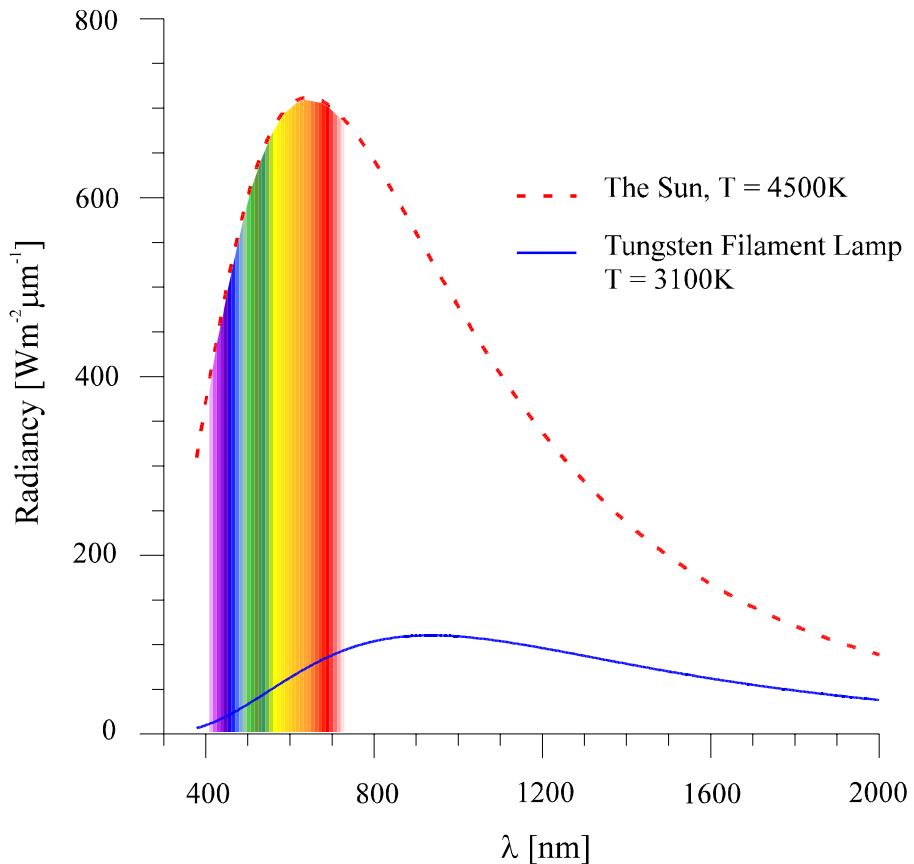


Figure 4.14: Spectral Radiancy of the Sun and a tungsten filament lamp

For accurate interpretation of the data, it is important to remove the effect of this non-linearity present at the light source from the measured spectral response of the device under test. This is known as deconvolution. The measured spectral response is divided by the blackbody radiancy corresponding to each wavelength. The non-linearity due to the grating, on the other hand, was removed by using the actual spectral efficiency of the grating supplied by the manufacturers.

In practice, the absolute responsivities for most of the devices studied were measured at two or more wavelengths using separate lasers where appropriate (630nm, 780nm and 1300nm respectively). The measured spectral response, S_λ , was then normalised to one of these wavelengths while the second absolute responsivity was used to cross-check the validity of the S_λ .

5. Indium Tin Oxide (ITO): Experiment and Results

5.1 ITO Deposition - Results and Discussions

As seen in Chapter 2, a variety of thin film deposition techniques have been employed to obtain ITO films. Of all the techniques, activated reactive evaporation (ARE) and sputtering have yielded the best results [6]. Numerous studies have been carried out on the preparation of highly conducting transparent Indium Tin Oxide (ITO) films. The results reported in these studies vary significantly from one another and suggest that the film properties greatly depend on deposition conditions and demand a careful optimisation of growth parameters as well as post-deposition treatments for reproducible results.

Hence some of the more influential factors determining the optical and electrical properties of the deposited ITO film including the total and partial pressures of the reactive gases, the substrate temperature, target oxidation as well as other growth related effects are discussed here.

5.1.1 Accuracy of Measuring the Electrical Properties of ITO Films

There are several experimental techniques available for measuring the electrical properties of ITO films :

- a. van der Pauw method [137]
- b. four-point-probe method [138]
- c. TLM method [119]

Although the first two are by far the most commonly used techniques in the literature, the TLM method has been used throughout the majority of this investigation for the following reasons:

- (i) While the van der Pauw method is accurate and provides detailed information about the test film, it does however require lengthy post-deposition pattern definition steps similar to those in the TLM method. Because we already had an elaborate and automated set-up for the TLM measurement method, used for appraising conventional metal ohmic contacts to a wide range of compound semiconductor epitaxial layers, allowing swift and accurate measurement (as described earlier in chapter 4), it was more convenient to use

this method. However, minor appropriate modifications in the pre-test sample preparation steps were necessary which are described later in the text.

- (ii) Although the four-point-probe method is an easy and convenient tool for resistivity measurements, it has a number of drawbacks which made it particularly unsuitable for the specific circumstances of this investigation. The accuracy of this method depends on both the sample shape and its dimensions. These are discussed below.

On a slice of finite thickness d , the four-point-probe will introduce voltage gradients perpendicular to the surface. In so far as these gradients are negligible, the slice can be treated in the same way as an infinitely thin slice and the proper sheet resistivity can be obtained. For a four-point-probe on an infinite sheet of finite thickness the following relation holds:

$$R_{sh} = \frac{V}{I} d \frac{\pi}{\ln 2} F\left(\frac{d}{L}\right) \quad (\text{eqn. 5.1})$$

where

R_{sh} = sheet resistance

d = film thickness (typically few thousand Å)

L = probe spacing (= 1.6 mm in our case)

$F(d/L)$ = correction factor approaching unity as d approaches zero.

In our case this correction is not necessary because the ratio (d/L) almost always approached zero.

Figure 5.1 shows a schematic diagram of the four-point-probe measurement set-up; it is shown that the current is applied through probes 1 and 4 and the voltages measured between probes 2 and 3.

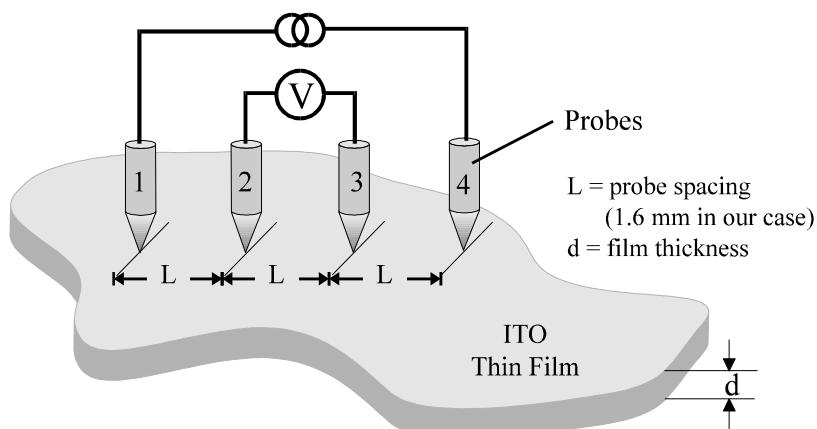


Figure 5.1: Schematic diagram of a four-point-probe measurement set-up for a ITO film of arbitrary shape and dimensions.

In addition to corrections needed for varying film thickness, accurate measurement using the four-point-probe method must take into account the shape of the test sample. This has its own correction factor, C_f , which depends on the relative size and shape of the test sample with respect to the probe spacing and the previous equation is then modified to:

$$R_{sh} = \frac{V}{I} d \frac{\pi}{\ln 2} C_f \quad (\text{eqn. 5.2})$$

where

C_f = correction factor to account for relative size and shape of test sample with respect to probe spacing.

In case of a circular sample of diameter D, for example, as the ratio D/L increases so does the value of C_f . For square or oblong shaped samples, the selection of the appropriate C_f is more complex.

It is these reasons which require that for accurate comparison of electrical properties of successively deposited ITO films, it is necessary to have identical shapes or sizes; each sample had to be at least 1 cm². In practice, this proves rather difficult and at best laborious. A further discouraging factor is that highly resistive ITO films ($R_{sh} > 1 \text{ k}\Omega$) tend to “burn” due to large current concentration at the probe tips rendering the entire sample unusable for further analysis. The results obtained from two samples from the same deposition had a large standard deviation (between ± 10% and ± 20%) and were often not repeatable.

Therefore, the TLM method, although slightly more time consuming in post-deposition sample preparation, was chosen to safeguard the integrity of the results which is vital for any comparative analysis work. The theory and the basic set-up of this technique have already been discussed in Chapter 4 therefore only the modifications needed to apply it for these purposes will now be described.

Following ITO deposition on highly resistive S.I. GaAs substrates, the samples were etched with TLM patterns to form ITO mesas. Further photolithography was used to deposit metal pads on the ITO mesas. The purpose of the ITO mesa is to confine the current between two metal pads when a voltage is applied to them. A schematic diagram of this set-up is shown in Figure 5.2:

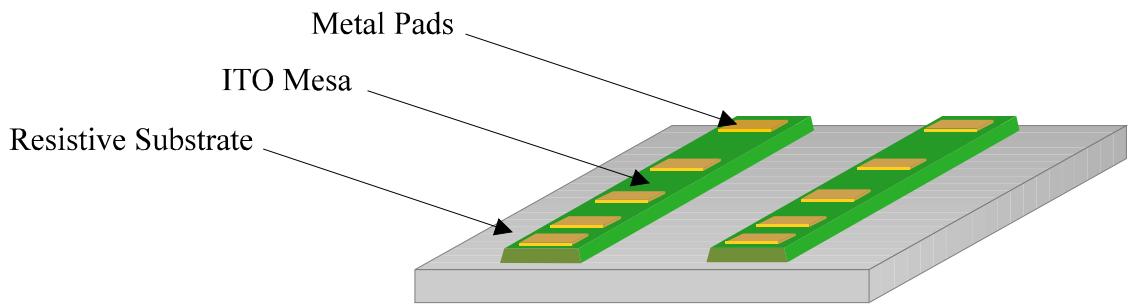


Figure 5.2: Schematic diagram of a typical ITO film sample prepared for electrical measurements using the TLM method.

The TLM method has various advantages over the four-point-probe method :

- sample shapes and sizes are always identical as they are produced using the same TLM mask set hence no correction factors have to be taken into account
- many accurate measurements can be made from a relatively small sample (a 1 cm^2 sample contains 20 TLM mesas allowing as many independent measurements)
- metal pads ensure that the current is uniformly spread out minimising the risk of either heating or burning the ITO underneath, which would increase the resistance or render it unusable
- repeatable results were obtained with acceptable standard deviation (below $\pm 5\%$) for samples from the same deposition run.
- the existing automated TLM measurement system could be used for swiftness and accuracy.

Table 5.1 shows the sheet resistance and the associated standard deviation of the same ITO film measured at four different parts using both the four-point-probe method and the TLM method:

Method	No. of Measurements	$R_{sh} [\Omega/\square]$	σ
4 Point Probe	4	675	16.5%
TLM	4	617	2.5%

Table 5.1: R_{sh} of the same ITO film measured using both the four-point-probe method and the TLM method.

Therefore, all subsequent electrical analysis of ITO films were carried out using the TLM method.

5.1.2 Optical Properties of the Deposited ITO Films

During all ITO depositions, the film transparency was monitored by placing a microscope cover slide on the Nordiko 1500 substrate table. The transmittance measurements were carried out in a double beam spectrometer; details of these measurements are described in Chapter 4.

Figure 5.3 shows the measured transmittance of a typical ITO film over the wavelength range 200 to 2000 nm. It is seen that above 90% transmittance is achieved for the 500 to 2000 nm wavelength range corresponding to 2.48eV to 0.62eV energy range which covers the majority of the III-V compound semiconductors such as AlAs, AlGaAs, GaAs, InP and InGaAs as well as Si and Ge. These results are a marked improvement over those obtained by Zhang *et al* who reported a transmittance of 80% over the 400 to 1300 nm wavelength range for ITO films grown by d.c. magentron sputtering [139].

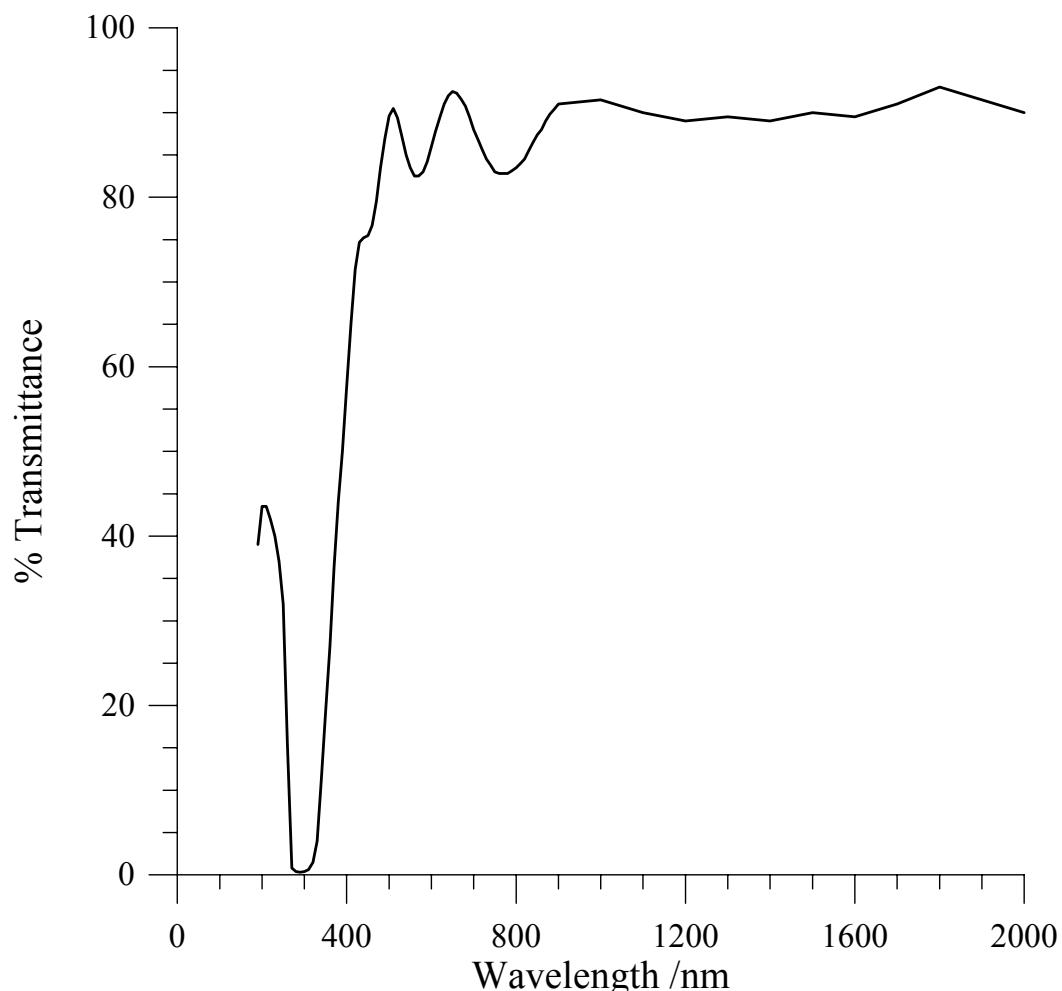


Figure 5.3: Graph of measured transmittance vs. wavelength for a typical ITO film grown by reactive r.f. sputter deposition. Film thickness was approximately 1,500Å.

Figure 5.3 shows that the transmittance sharply decreases below a threshold wavelength; this is due to fundamental absorption of ITO for which the widely reported value of the bandgap is approximately 3.75eV [7,13]. The measured transmittance data can be used to obtain the bandgap of the ITO film - in particular, the dependence of the absorption co-efficient, α , in the absorption edge on the wavelength can be used to calculate this bandgap. The transmittance, T_r , as a function of the wavelength, λ , for a film of thickness d is given by [14]:

$$T_r = A \cdot \exp^{(-4\pi k' d / \lambda)} \quad (\text{eqn. 5.3})$$

where,

k' = extinction co-efficient

and, A is a constant given by:

$$A = \frac{16n_0 n_1 (n_{ITO}^2 + k'^2)}{\{(n_0 + n_{ITO})^2 + k'^2\} \{(n_1 + n_{ITO})^2 + k'^2\}} \quad (\text{eqn. 5.4})$$

where,

n_0 = refractive index of air

n_1 = refractive index of substrate (microscope glass cover slide)

n_{ITO} = refractive index of ITO film

and, α , the absorption co-efficient is given by:

$$\alpha = \frac{4\pi k'}{\lambda} \quad (\text{eqn. 5.5})$$

For $k'^2 \ll n_{ITO}^2$, the transmittance is mainly dependent on the exponential term of (eqn. 5.3) and the constant A can be approximated to 1; hence taking this into account and combining (eqn. 5.3) and (eqn. 5.5), T_r can be simplified to:

$$T_r = \exp^{(-\alpha d)} \quad (\text{eqn. 5.6})$$

rearranging, we obtain α :

$$\alpha = \frac{-\ln(T_r)}{d} \quad (\text{eqn. 5.7})$$

Now, (eqn. 5.7) can be used to plot α^2 as a function of energy, $h\nu$, and extrapolated to $\alpha^2 = 0$ yielding the bandgap of the ITO film as shown in Figure 5.4.

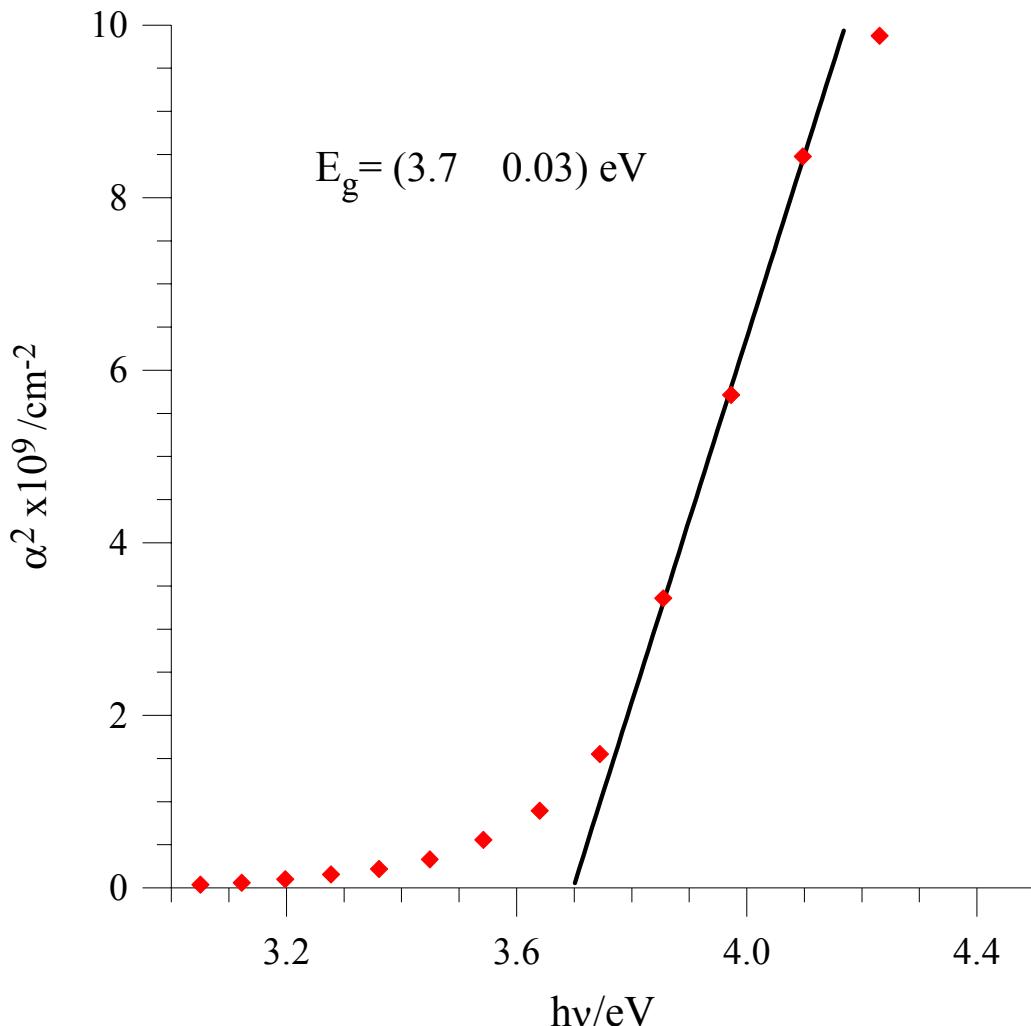


Figure 5.4: Graph of α^2 vs. energy for a typical ITO film grown by reactive r.f. sputter deposition. The extrapolated bandgap for this ITO film is (3.7 ± 0.03) eV.

In this study, the value of the determined bandgap for a typical ITO film deposited by reactive r.f. sputtering is (3.7 ± 0.03) eV. This is in good agreement with the values reported in the literature within the bounds of experimental error. However, it should be noted that most of the data in the literature were measured using ellipsometric measurements - a technique which is more accurate but more cumbersome than the one used here.

5.1.3 Effect of Total Pressure

In a reactive r.f. sputtering environment, a minimum gas pressure, or a threshold pressure - P_T - is required in order to excite the plasma. In our case this was 10^{-3} torr. As most depositions

were carried out below this pressure, it was therefore necessary to raise the chamber pressure momentarily to P_T in order to excite the plasma and then reduce to the required pressure. The plasma was self-sustaining throughout the entire deposition pressure range.

The total pressure effects the deposition process in a number ways :

- greater the pressure, greater the number of particles in the plasma
- increased number of particles increases the probability of sputtering from the target at a given r.f. power and therefore will increase the deposition rate
- however, greater number of particles increases the probability of scattering of sputtered particles during transit from the target to the substrate and will have an adverse effect on the deposition rate beyond a given pressure.
- the total pressure at a given r.f. power also effects the induced bias on the electrodes which in turn influences the deposition rate.

These findings about the dependence of the deposition rate on the chamber pressure are in good agreement with experimental observations of Sreenivas *et al* [6]. Therefore, it is important to take this parameter into account for optimizing ITO deposition. In this investigation, the total chamber pressure was kept at a constant 5 mtorr.

5.1.4 Effect of Oxygen Partial Pressure, PO_2

There is a strong dependence of ITO film properties on the oxygen partial pressure which demands close control for reproducible preparation of such films. For r.f. sputtered ITO films, it is well known that while the transparency of the ITO films is directly proportional to the oxygen content of the plasma in the sputter chamber, the sheet resistance is inversely proportional to it [7,8,140]. Similar findings have also been reported for these films grown by other techniques such as ion-beam sputtering [11] and spray pyrolysis [141].

Figure 5.5 shows the results of ITO films deposited under various oxygen partial pressures at a r.f. power of 150 W. It is evident that the sheet resistance is directly proportional to the exponential of the oxygen partial pressure. Whereas the transmittance of these films were above 90% in the 500 to 2000 nm wavelength range, further reductions in the oxygen content severely degraded the transparency to below 60%. Total absence of O_2 resulted in dark brown deposits with maximum transmittance of 50%, for very thin films of 500Å, which diminished for thicker films.

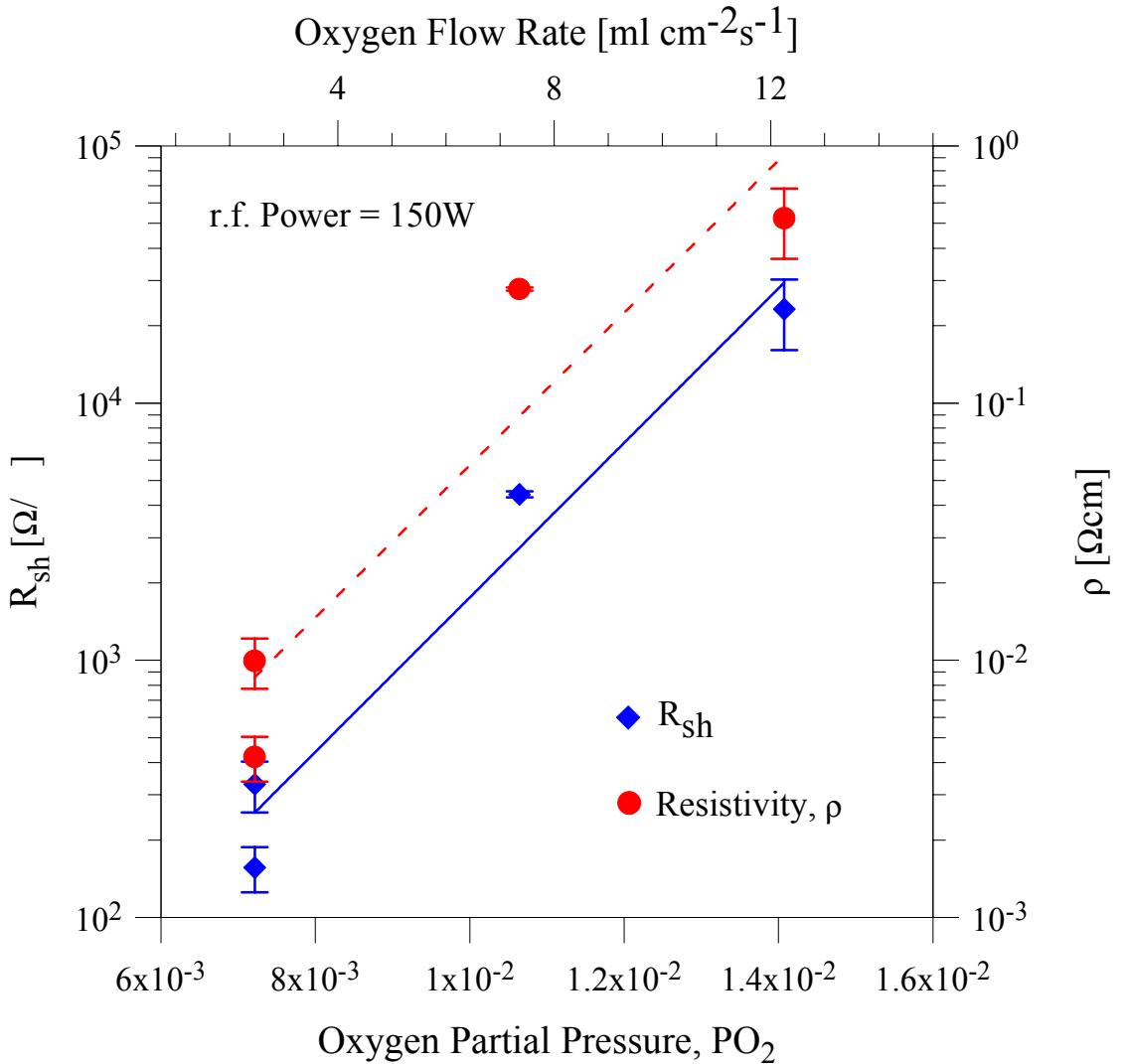


Figure 5.5: The sheet resistance, R_{sh} , and the resistivity, ρ , of ITO vs. the oxygen partial pressure, PO_2 , in the r.f. reactive sputtering plasma; the corresponding O_2 flow is also shown for reference.

The high conductivity of the ITO films has been attributed to both substitutional tin and oxygen vacancies, created either during film growth or post-deposition annealing resulting in a material represented as $\text{In}_{2-x}\text{Sn}_x\text{O}_{3-2x}$ [3]. Increasing the oxygen partial pressure above a value which yields a near stoichiometric film composition would thus result in an accumulation of excess oxygen, mainly at the grain boundaries acting as trapping centres for free carriers [7]. This means that the barrier scattering becomes the dominant process since the barrier height increases strongly. At the same time the density of free carriers is reduced as they are partly localised at the trapping sites [12]. This results in a decrease in the carrier mobility, and therefore a corresponding fall in the film conductivity is observed. Buchanan *et al* [8] have also suggested that the decrease in the conductivity in increased PO_2 is primarily due to a reduction in the carrier concentration caused by the occupation of oxygen vacancies rather than due to tin doping. A rapid increase in the ITO resistivity has been consistently

observed by Kellet *et al* on films grown on both GaAs [142] and Si [143]; they have related this observation to ITO's wide oxygen stoichiometry and its degeneracy (resulting in high conductivity) when the PO_2 (and hence the oxygen content) is reduced.

With regard to the dependency of the transmission of ITO films on the PO_2 , Fan *et al* [5] have reported complimentary findings to those obtained in this study. They observed that the ITO film transmittance increased rapidly with increasing oxygen partial pressure exceeding 80% at a PO_2 of 3×10^{-3} then saturating around 90% for further increase. In addition to increasing the transmission of the films, there is also a shift of the intrinsic absorption edge to longer wavelengths (i.e. lower photon energies) due to an increase in PO_2 . Simple calculations show that this shift can be as much as 10%. Study of r.f. sputtered ITO films by Ohhata *et al* relate this phenomena to a change in the carrier concentration [144].

5.1.5 Effect of r.f. Power

The r.f. power has a direct influence on the deposition rate and the induced voltage as well as generating heat due to the electron bombardment intrinsic to this technique. After experimenting with various r.f. power for ITO deposition we have seen its marked influence on the electrical properties of the deposited films.

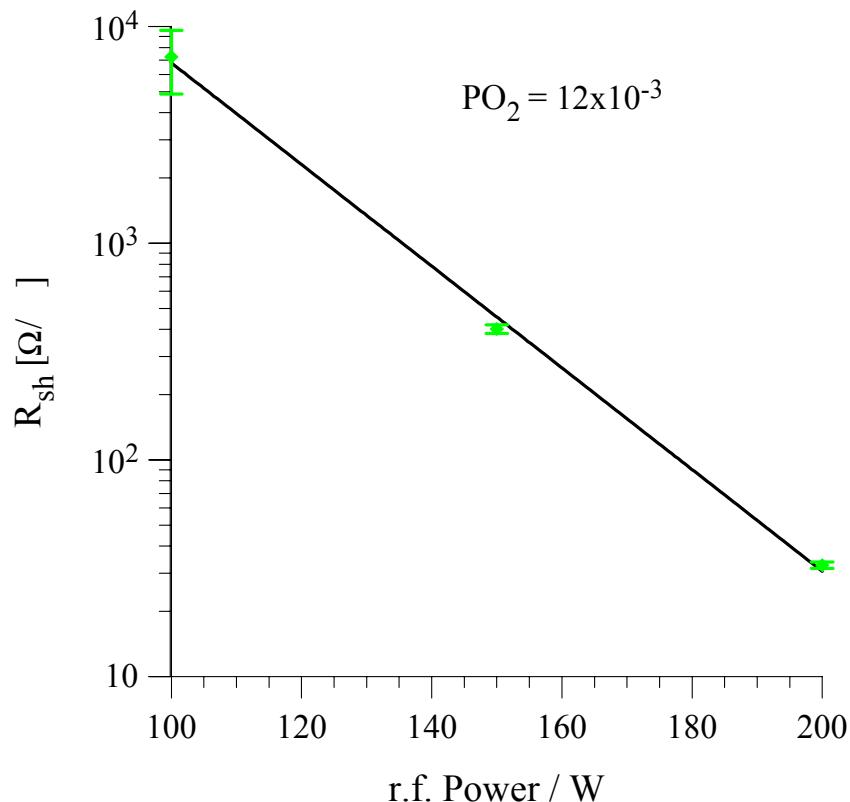


Figure 5.6: Sheet Resistance, R_{sh} , of ITO vs. r.f. sputtering power.

During each deposition, at various powers, the plasma was ‘tuned’ to maximise the forward power and reduce the reflected power to zero. Our results from depositions using a oxygen partial pressure of 12×10^{-3} show that the sheet resistances of the ITO films are inversely proportional to the exponential of the r.f. power used as shown in Figure 5.6. Films grown at 100W showed typical R_{sh} of about $70 \text{ k}\Omega/\square$, at 150W this was $4\text{k}\Omega/\square$ while at 200W the R_{sh} was $40\Omega/\square$. These results are in close agreement with those reported by Sreenivas *et al* [6] and Mansingh *et al* [140], who used very similar deposition techniques and conditions to those in this study.

It should be noted that these values were obtained without any post-deposition annealing; after annealing in forming gas, $R_{sh} < 10 \Omega/\square$ was achieved. On the other hand, very high r.f. powers of 500 W during deposition have been reported to generate sufficient intrinsic heating thus eliminating the need for further treatment usually carried out to obtain good quality ITO films [145]. In this study, however, films deposited at 200 W were difficult to etch; hence the r.f. power of 150 W was used for all subsequent work. Also, from a device application point of view, the use of excessive r.f. power is not suitable.

5.1.6 Effect of Induced Voltage

Figure 5.7 shows that the induced d.c. voltage on the substrate electrode is directly proportional to the r.f. power at a given pressure. The d.c. bias was independent of the oxygen partial pressure.

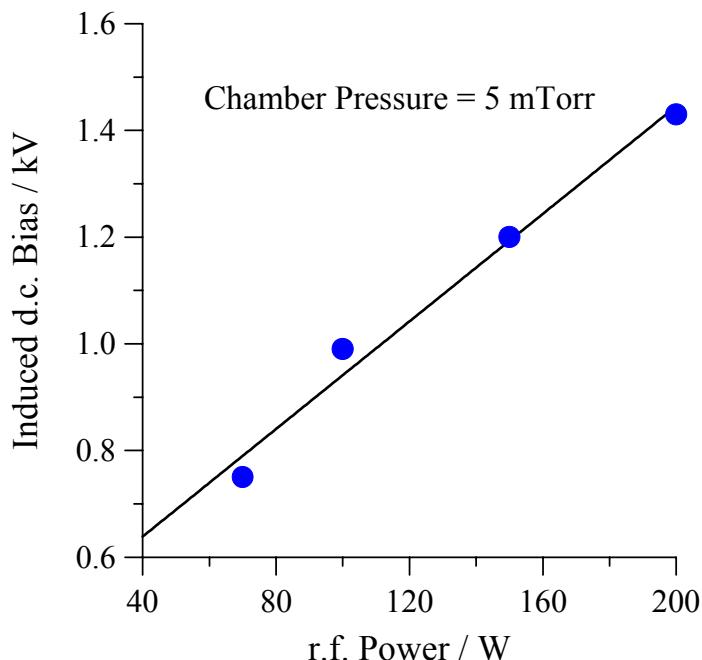


Figure 5.7: Induced d.c. bias on substrate electrode vs. r.f. Sputtering Power at a total chamber pressure of 5 mtorr.

It was also observed that the induced d.c. bias changed if the plasma was de-tuned i.e. if the reflected power was non-zero. As all depositions were carried out in a tuned plasma, any dependence of ITO electrical properties on the induced d.c. bias would be the same as those seen for their dependence on the r.f. power.

5.1.7 Effect of Deposition Rate

Figure 5.8 shows that the deposition rate itself is directly proportional to the r.f. sputtering power at a given chamber pressure and partial pressure of oxygen. Reduction in the oxygen flow rate or the oxygen partial pressure, PO_2 , in the reactive plasma caused a proportional decrease in the deposition rate at a given r.f. power.

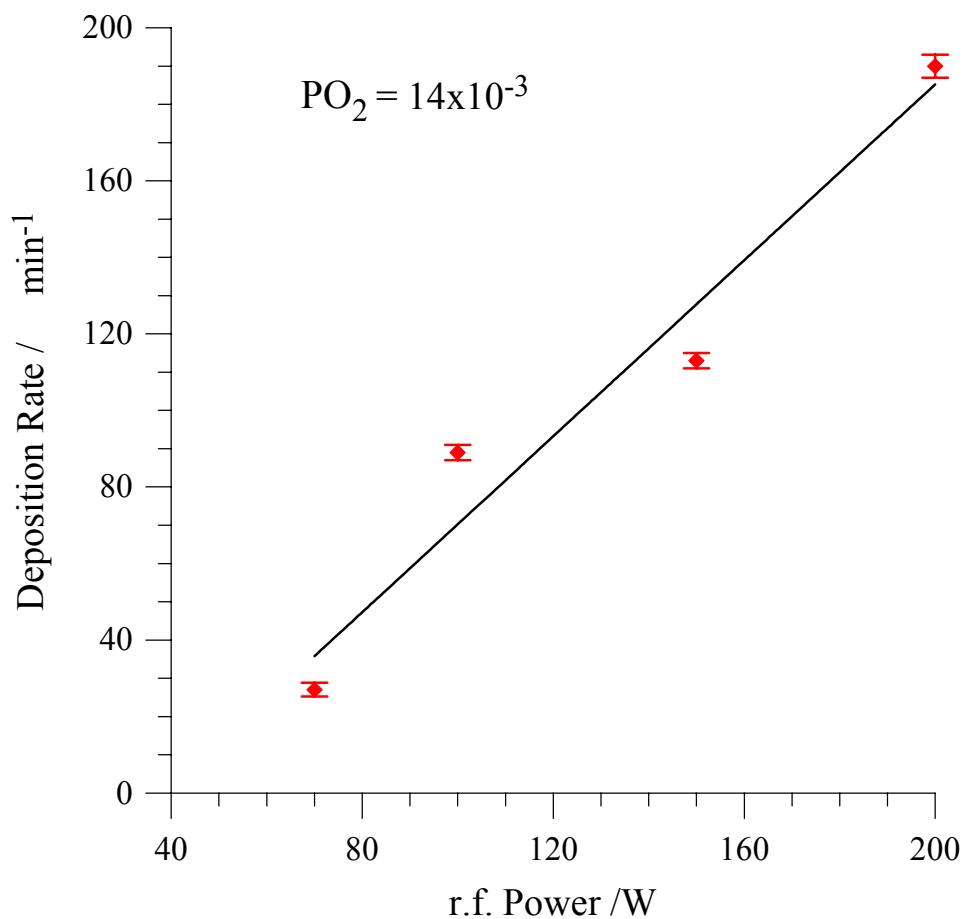


Figure 5.8: ITO deposition rate vs. r.f. sputtering power at a PO_2 of 14×10^{-3} .

Since the ITO deposition rate is directly proportional to the r.f. power for a given set of conditions, any dependence of the film properties on the rate will be the same as those observed for their dependence on the r.f. power for this system.

5.1.8 Effect of Target Pre-conditioning

Pre-conditioning is a term used for attaining stability in the sputter chamber prior to ITO deposition on the substrate. This includes stabilising the chamber pressure, the plasma, the r.f. forward and reflected power. Pre-conditioning has two distinct effects:

1. It cleans the target surface of any debris and deposits a fine layer of ITO on the chamber walls thus preventing further contamination due to natural degassing from the surface.
2. It stabilises the release or sputtering rates of species from the target and particularly so if the target is a composite as in the case of ITO targets.

Without pre-conditioning, results were very difficult to reproduce between consecutive sputter depositions with nominally identical conditions. Both Ar on its own as well as Ar and O₂ mixtures were used as the plasma gas in turn without any pre-conditioning, but neither of these conditions produced satisfactory repeatability.

We have studied the effect of pre-conditioning under varied or similar conditions to those used during the actual deposition; these include using different r.f. power and gas composition to those used in the respective depositions. In general, best results were obtained when the pre-conditioning parameters were the same as the deposition parameters. In all the cases the pre-conditioning period was 30 minutes whereas the deposition time was dictated by the specific needs of any particular experiment.

5.1.9 Effect of Film Thickness

Our initial experiment with Ar as the only plasma gas during ITO deposition showed that the optical transmission was inversely proportional to the thickness and remained below 50%. However, for addition of O₂ in the plasma gas above partial pressures of 7×10^{-3} , consistent transmissions above 90% were obtained in the 500 to 2000nm wavelength range regardless of the film thickness.

Two sets of experiments showed a noticeable trend on the effect of thickness on the R_{sh} and ρ. In each set, ITO was deposited on two otherwise identical samples of S.I. GaAs; all preparation and deposition conditions were identical for each of the two samples except the deposition time, which was varied, resulting in two different thicknesses. The results and conditions are summarised in Table 5.2.

Sample	$\text{PO}_2 (\text{x}10^{-3})$	Power [W]	Thickness [\AA]	$R_{\text{sh}} [\Omega/\square]$	$\rho (\text{x}10^{-3})[\Omega\text{cm}]$
A1	7	70	820 ± 20	6344 ± 100	52.0 ± 0.8
A2	7	70	1633 ± 110	1499 ± 60	24.5 ± 1.0
B1	14	200	3829 ± 45	664 ± 48	25.0 ± 1.8
B2	14	200	5556 ± 169	341 ± 15	19.0 ± 0.8

Table 5.2: Effect of thickness on electrical properties of ITO films deposited under otherwise identical conditions; the films were not annealed prior to these measurements.

These results show that for a given set of deposition conditions, the thicker film has better electrical properties. These results are consistent with the findings of Sreenivas *et al* [6]. Studies involving very thick ITO layers ($> 10,000\text{\AA}$) deposited on metal alloys by Just *et al* suggest that since the stress within the film is independent of its thickness. Hence a shear stress is developed between this film and the substrate ultimately resulting in the loss of adhesion between thick films and substrates. They also observe a decrease in this stress due to annealing and that the ITO film thickness does not have any effect on its refractive index [146].

5.1.10 Effect of Target to Substrate Distance

For a given set of deposition parameters for the sputtering technique, the energy distribution of sputtered neutrals reaching the substrate depends on the distance between the target and the substrate due to molecular collisions in the plasma. Depending on their initial energy, which is proportional to the r.f. power and hence the self-induced bias, these particles travel a ‘thermalization distance’ until its energy reduces to the thermal energy kT . Transport beyond this ‘virtual source’ point towards the substrate is by diffusion under the material concentration gradient.

Experimental work carried out on a very similar system to that used here by Kumar *et al* show that the deposition rate is inversely proportional to the exponential of the distance between the virtual source and the substrate [147]. Thus the substrate position can be located either above or below this virtual source point by increasing or decreasing the distance between the target and the substrate. However, during the course of this investigation, this separation was fixed at a distance of 7.5 cm, slightly above the virtual source which varies between 3 and 6.5 cm for r.f. power of 50 to 200 W respectively. Kumar *et al* reported that ITO films with improved transmittance and more uniform properties were obtained for substrates located below this virtual source.

5.1.11 Effect of Substrate Temperature During Deposition

In the Nordiko 1500 sputtering system used in this work, it is not possible to measure the *in-situ* chamber temperature. However, reports in the literature from groups using an identical system suggests substrate temperatures rise to approximately between 60° C to 70° C during deposition due to intrinsic electron bombardment.

5.2 Patterning ITO

Patterning ITO is necessary not only for appraising the quality of the film (using TLM method for example) but also for fabricating useful micro-contacts to devices. As for metals and semiconductors, there are two potential methods of patterning ITO:

- lift-off lithography
- etch lithography

5.2.1 ITO Patterning by Lift-off Lithography

Due to the high velocity particles involved in a reactive r.f. sputtering system, the liftoff technique was not satisfactory. Both thin ($< 1 \mu\text{m}$) and thick ($> 3 \mu\text{m}$) photoresists (PR) were used in the experiments for ITO deposition by liftoff technique; whereas the thin PR was not removable in acetone, by flood exposure under UV lamp or in heated KOH solution, the thicker PR was less difficult to remove. However, the walls of the thick PR were rigidly stuck to the substrate. Microscopic examination of the thin PR showed numerous cracks on its surface most probably caused by PR hardening and baking as a result of penetration of incident particles through its entire depth. In case of the thick PR, the side walls are most probably damaged by bombardment of high velocity plasma particles reflected from the deposited ITO as shown in Figure 5.9:

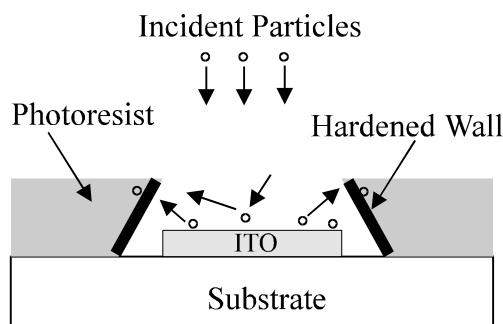


Figure 5.9: Photoresist wall hardening by reflected plasma particles.

In another experiment, the substrate was patterned with PR as usual and placed on the Nordiko substrate table at a 45° degree angle to reduce damage to the PR. However, the PR was still difficult to remove while the ITO deposition rate dropped below satisfactory levels ($< 1 \text{ \AA/sec}$).

Therefore, ITO patterning was carried out by etching methods only. These include wet chemical etching and ion milling or dry etching as presented in the following sub-sections.

5.2.2 Wet Chemical Etching

It was found that ITO readily etches in HF solution ($\text{HF:H}_2\text{O}_2:10\text{H}_2\text{O}$) and HCl solutions of various strengths. However, ITO cannot be etched in ammonia solutions ($8\text{NH}_3:3\text{H}_2\text{O}_2:400\text{H}_2\text{O}$). The etch rates in HF were very high (between 100\AA/sec to 150\AA/sec) and often uncontrollable. Subsequently HCl solution was used for wet etching ITO in majority of the cases.

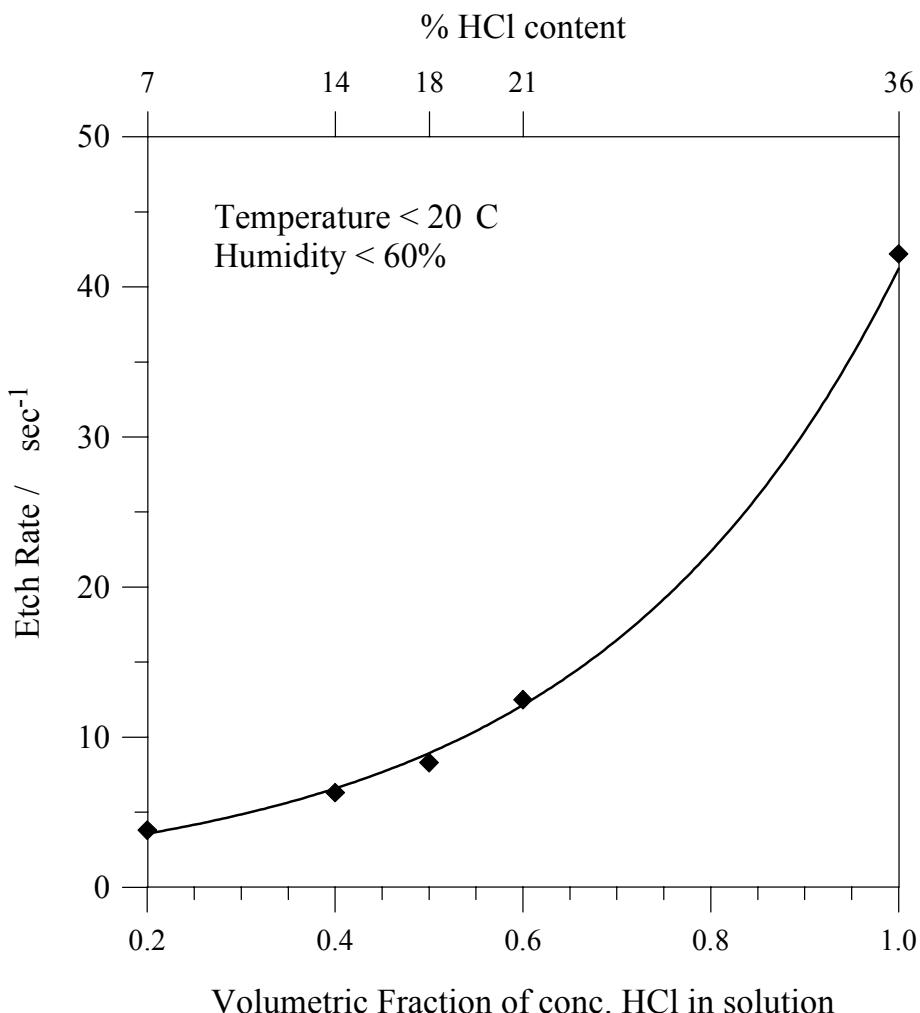


Figure 5.10: Wet Chemical Etch Rate of ITO as a function of HCl concentration at room temperature and controlled humidity.

The undiluted etch solution contained 36% HCl corresponding to a molar solution. Figure 5.10 shows the etch rate of ITO deposited on S.I. GaAs substrates as a function of HCl concentration in the etchant. These reactions were carried out in the cleanroom under controlled conditions where the temperature was kept below 20°C and the humidity below 60%. Although not documented here, excess temperature and humidity resulted in increased etch rates. Therefore, to avoid undesirable results, the above ambient conditions were maintained for subsequent ITO etching.

As mentioned earlier, the wet chemical etch process is highly dependent on a number of ambient conditions. In addition, we noticed that a certain amount of ITO - varying from $0.5\mu\text{m}$ to $1.5\mu\text{m}$ was often etched away from underneath the photoresist. In severe cases, thin traces of the photoresist remained on the substrate.

Figure 5.11 is a photo-micrograph of a TLM pattern chemically etched using HCl to produce ITO mesas on S.I. GaAs substrate. The mesas are $110\mu\text{m}$ wide; the amount of ITO removed completely due to under etching was $1.5\mu\text{m}$. This is an extreme example of lack of control of wet chemical etching technique.

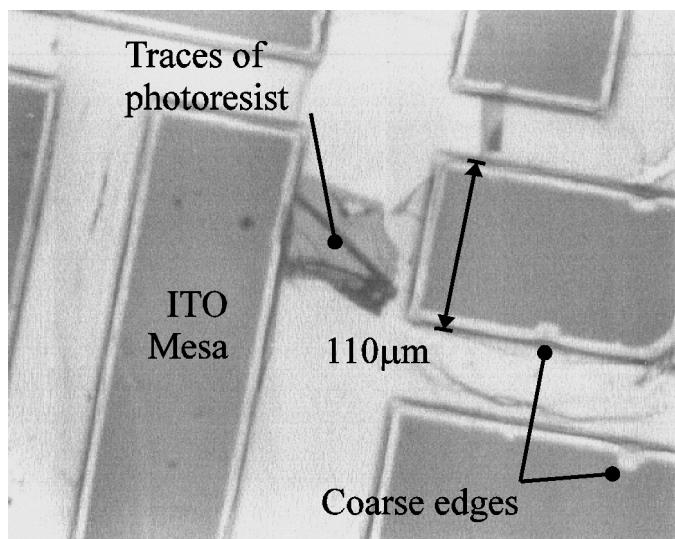


Figure 5.11: Photo Micrograph of an ITO mesa, etched using HCl solution. The figure shows characteristic coarse edges due to solvents creeping under the resist; blemishes and traces of thin photoresist can also be seen.

For relatively large dimensions ($> 100 \mu\text{m}$), wet chemical etching using the above solution was both adequate, repeatable and relatively easy to accomplish. During the course of this investigation, the most frequently used chemical for wet etching ITO, where deemed suitable, was a $1\text{HCl} : 1\text{H}_2\text{O}$ solution corresponding to 18% HCl by content. The corresponding etch rate was 8 \AA/sec .

5.2.3 Effect of Adding Zn Dust to HCl Solution

The addition of zinc dust to the ITO surface is said to enhance wet chemical etching in HCl solutions. A GaAs sample with ITO was first left in a mixture of water and Zn powder. It was then dried by leaving it on a “blotting” surface (i.e. cleanroom wipe) which left fine granules of Zn powder on the sample surface. The sample was then immersed in the HCl solution.

The ITO removal did not seem to be affected by the immersion in the Zn:H₂O suspension; also the etch on the surface was non-uniform. The residue Zn was removed from the sample by placing it in a 3H₂O:1HNO₃ bath. But this latter solution seemed to etch the GaAs substrate. Therefore, this method of ITO patterning was deemed to be unsuitable for controlled and uniform micro patterning of ITO as required in this project.

5.2.4 Selective RIE of ITO in Argon Plasma

The commonly used solution of HCl for ITO definition by wet chemical etching results in removals of approximately 0.5 μm of ITO underneath the photoresist mask. Thus where near micron structures need to be reproduced, wet chemical etching techniques are often unsuitable. Although CH₄/H₂ mixtures can be used for reactive ion etching of ITO [148], this is a potentially explosive gas mixture which is unsuitable for use in environments without relatively expensive exhaust set-ups operating round the clock to remove any build-ups. Dry etching of ITO using a gas mixture of acetone, argon and oxygen - essentially a hydrocarbon etch with acetone being the source of reactive organic radicals in the plasma discharge - has also been reported [149]. However, this technique needs cumbersome optimisation of the various constituent gas partial pressures to ensure that no carbon debris is left on the surface.

Therefore we investigated the suitability of a number of gases for dry etching ITO: freon, oxygen and argon. Dry etching using Ar was found to be the most suitable in terms of speed and selectivity. Figure 5.12 and Figure 5.13 show the results of this investigation.

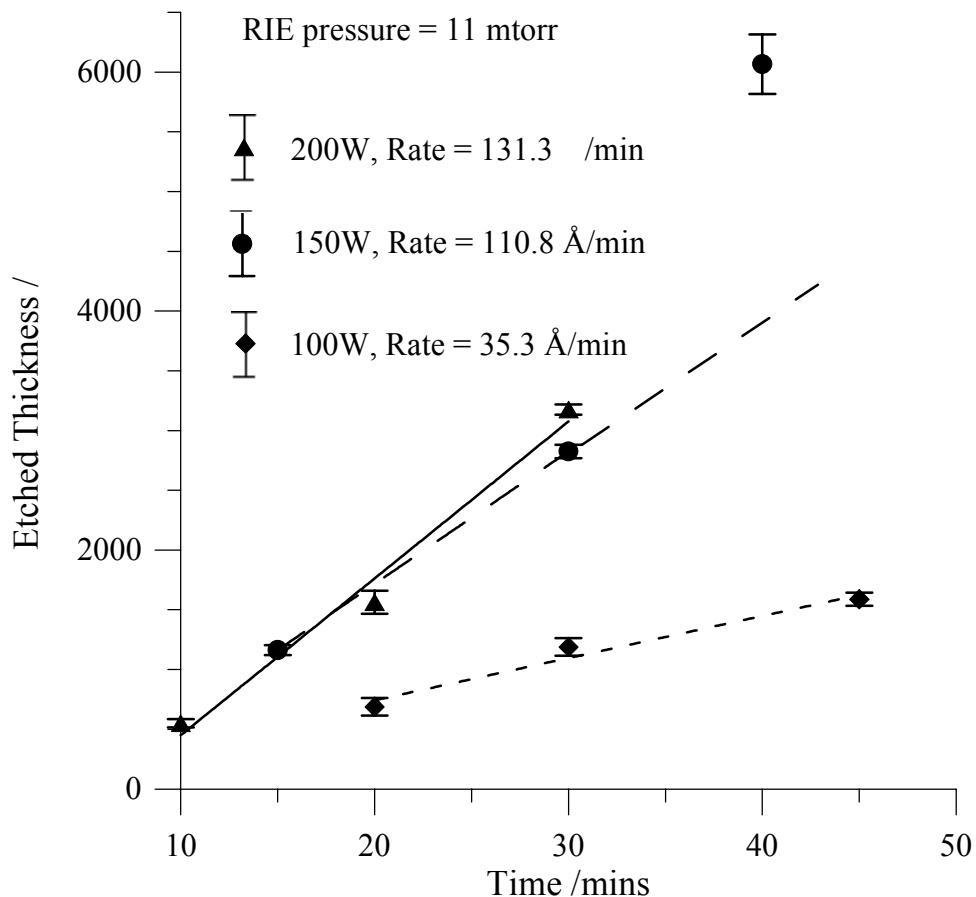


Figure 5.12: ITO Etched Thickness in argon ambient versus time under various r.f. powers

A 4300Å ITO layer was deposited on a Si substrate by reactive r.f. sputtering, the sample was then patterned using standard photolithography process to enable thickness measurements to be carried out following dry etching. Thick photoresist ($> 3 \mu\text{m}$) was used as the mask for these experiments which were performed at three suitable r.f. powers of 100W, 150W, and 200W. The dry etching chamber was pumped to pressures better than 1×10^{-4} torr; Ar was then flowed in at a constant rate to maintain a chamber pressure of 11 mtorr prior to exciting the plasma.

The last point on the 150W power line in Figure 5.12 (corresponding to 40 minutes and 6300Å) was not used for the least square fit as the Si substrate was found to have been etched also. Etch rates of 35 Å/min, 111 Å/min and 131 Å/min were obtained for 100W, 150W and 200W respectively.

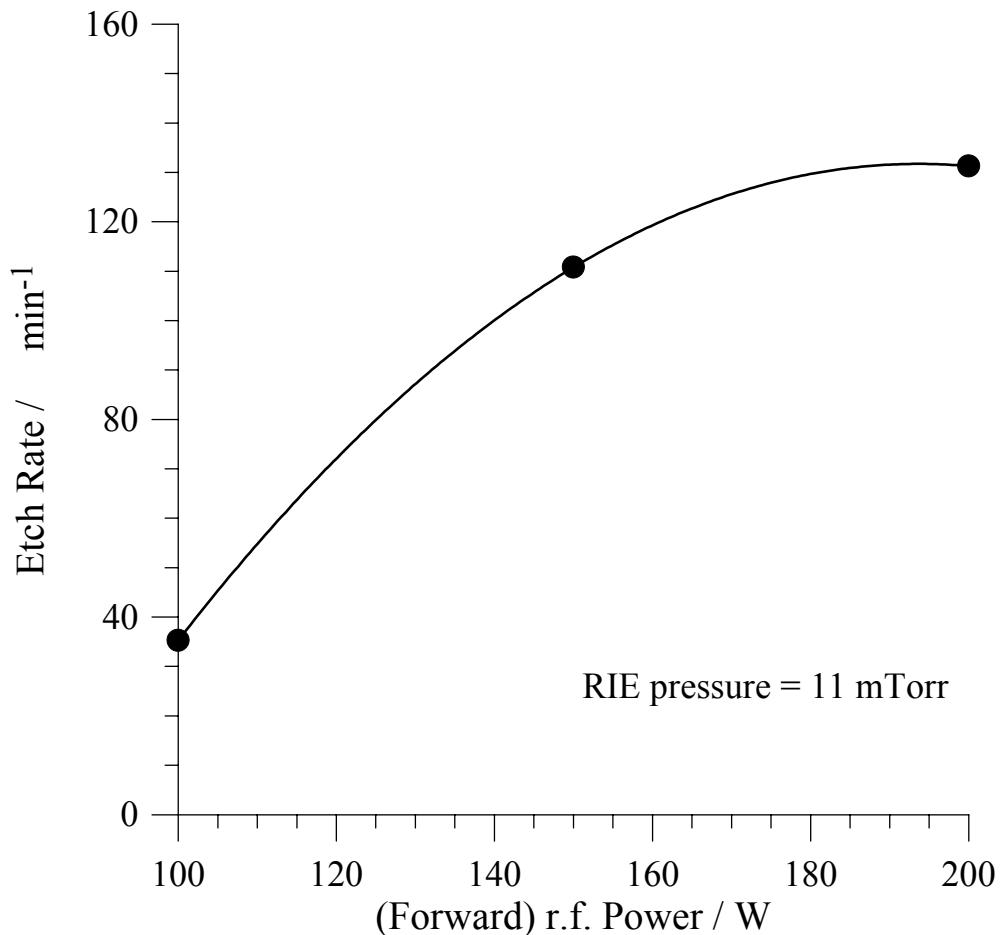


Figure 5.13: ITO Etch Rate in Argon ambient vs. r.f. power of RIE

Figure 5.13 shows that the etch rate is non-linearly dependent on the r.f. power. Also pin-holes were visible on substrates etched at higher powers. Both these effects suggest that the process produces substrate heating and that the process of ITO removal in an Argon plasma is that of a physical knocking of the ITO species rather than by a chemical reaction [150]. Based on these findings, the r.f. power of 100W was decided to be the most controllable and suitable for further dry etching work.

As even the thick photoresist was damaged during the RIE process and was therefore difficult to remove, an alternative material for the mask was necessary. A metal which has a sufficiently lower etch rate than ITO in the Ar plasma but nevertheless can be subsequently removed chemically in preference to ITO would be the ideal substitute. Aluminium was the preferred candidate on both counts.

A resistively evaporated layer of Al was therefore used as a mask. ITO is selectively dry etched over Al in argon plasma. Figure 5.14 shows that while the ITO etch rate at 100W r.f.

power and 11 mtorr pressure, is 35Å/min, the corresponding figure for Al is only 8Å/min making Al a more than adequate candidate to be used as a mask for dry etching ITO.

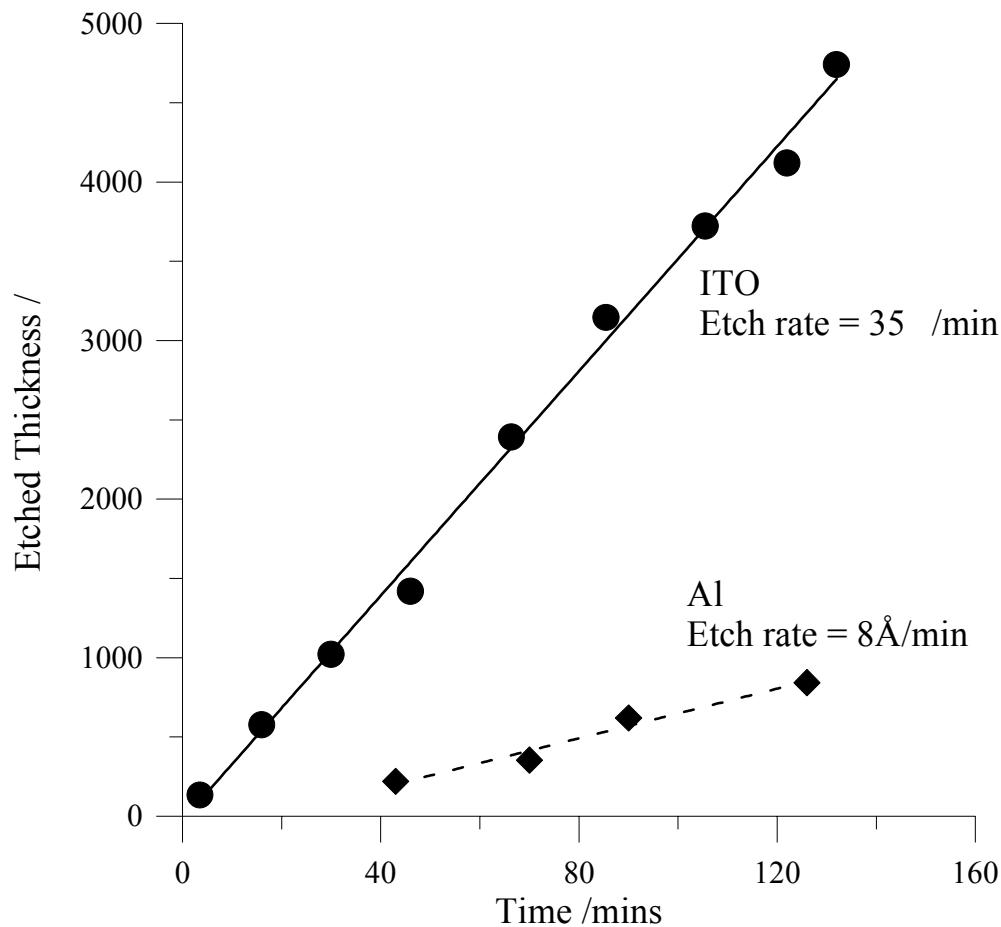


Figure 5.14: Selective RIE of ITO over Al in argon plasma at a r.f. power of 100W

Following dry etching, the Al is selectively removed by placing the sample in a super saturated luke warm solution ($\approx 30^\circ\text{C}$) of KOH for app. 2 minutes. A 1000Å layer of Al was found to be adequate. Thicker layers of Al were difficult to remove chemically; although further heating the KOH solution accelerated Al removal, this also caused partial etching of the ITO. Hence, all subsequent dry etching of delicate ITO patterns were masked using 1000Å of thermally evaporated Al.

In comparison to the ITO dry etching techniques of Adesida *et al* [148] using CH₄/H₂ mixtures, these etch rates are an order lower. This difference most likely arises from a variation in the etch mechanisms involved in the two cases: whereas the carbon in the methane/hydrogen mixture is said to react with the oxygen in ITO, there are no similar reactive species in the Ar plasma. Therefore, it is postulated that the etching of ITO in Ar plasma is essentially an ion milling process.

The etch rates obtained in this investigation for the RIE of ITO is, however, comparable to those reported by Saia *et al* [149]: 22Å/min in C₃H₆O/Ar/O₂ or 60Å/min in hydrogen chloride gas.

Figure 5.15 shows a photo micrograph of a TLM mesa pattern etched on a test ITO sample using the dry etching technique discussed thus far. In comparison with the results obtained for a similar test sample etched using HCl solution, these results show near perfect edges replicated from the mask. There is no apparent lateral etching or residue of debris on the substrate.

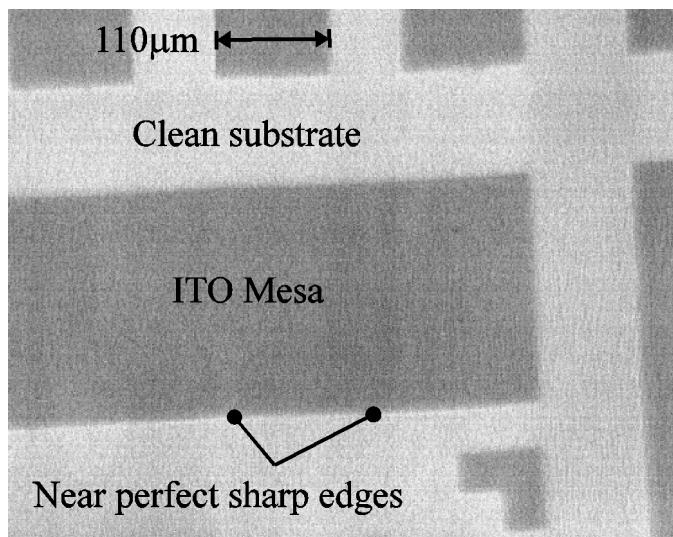


Figure 5.15: Photo micrograph of an ITO mesa pattern, etched using RIE. The figure shows near perfect edges while the substrate appears remarkably clean.

As discussed in Chapter 6, using this dry etching technique with Al as the mask, a 2µm FET gate structure was successfully produced in the fabrication of the first transparent gate HEMT. Therefore, this technique was used in all subsequent fabrication ITO structures below 50µm and proved to be a reliable and very convenient method for patterning delicate ITO structures.

5.3 Post Deposition Treatments

The dependence of ITO film properties on a number of growth parameters for each deposition method has previously been discussed in the earlier section and Chapter 2. Film properties can also be modified by annealing in either oxidising or reducing atmospheres as well as vacuum or nitrogen ambients [151,152,139].

Hence, it is necessary to exploit and develop the understanding of the effects of film structure and stoichiometry on electrical conductivity and optical transmission. Hence, the effects of annealing on the electrical and optical properties of ITO films were investigated.

5.3.1 Effects of Heat Treatment on the Electrical Properties of ITO

The two major types of ITO contacts used in this investigation are Schottky and ohmic. These contacts themselves have very different annealing conditions dictated by material and device processing factors and are thus discussed separately. As in section 5.1, electrical measurements on the films were done using the TLM method. A schematic diagram of this set-up can be seen in Figure 5.2. ITO was the mesa in the TLM pattern and for metal contacts to the ITO, in the following cases the Ni/AuGe/Ni/Au metalisation system was used.

5.3.1.1 Schottky Annealing Scheme

Because Schottky junctions diffuse at high temperatures resulting in lowered barrier heights and degraded performance, it is necessary to employ low but prolonged annealing schemes. In addition, sputter induced damage has to be recovered by the overall annealing procedures. Thus this scheme is dictated by the following factors :

- integrity of the Schottky junction
- adequate removal of sputter damage
- adequate annealing of the ITO to improve electrical properties of the film

Keeping the above in mind, the following temperature and times were used consecutively: (a) 5 hours at 240°C followed by (b) another 5 hours at 340°C. Similar schemes have also been used by other investigators [9]. The results are summarised in Table 5.3.

Sample	r.f. power [W]	PO_2 ($\times 10^{-3}$)	Before Annealing		After Annealing	
			$R_{\text{sh}} [\Omega/\square]$	$\rho [\Omega\text{cm}]$ ($\times 10^{-3}$)	$R_{\text{sh}} [\Omega/\square]$	$\rho [\Omega\text{cm}]$ ($\times 10^{-4}$)
SAB-GH	100	14	671.4 ± 98	17.9 ± 3	85.7 ± 1.4	22.8 ± 0.4
SAB-5	150	11	978.2 ± 31	29.0 ± 1	50.6 ± 1.7	15.3 ± 0.5
SAB-9	200	14	341.7 ± 15	19.0 ± 1	27.5 ± 1.0	15.3 ± 0.6

Table 5.3: Effect of the Schottky annealing scheme on ITO films deposited under various conditions.

The results shown in the above table are similar to those reported by Sreenivas *et al* [6] who have used a cracked ammonia and N_2 annealing ambient for ITO films deposited using a very similar set-up to ourselves. They report that following the anneal, the carrier concentration increased from 10^{18} cm^{-3} to 10^{20} cm^{-3} while the mobility increased from $2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ to $4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ in N_2 and to $12 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ in cracked ammonia resulting in R_{sh} decreasing from $10^4 \Omega/\square$ to $40 \Omega/\square$ and $11 \Omega/\square$ respectively. They attribute this significant reduction in the R_{sh} to the large increase in the mobility and further suggest that this may be associated with the increase in grain size of the film.

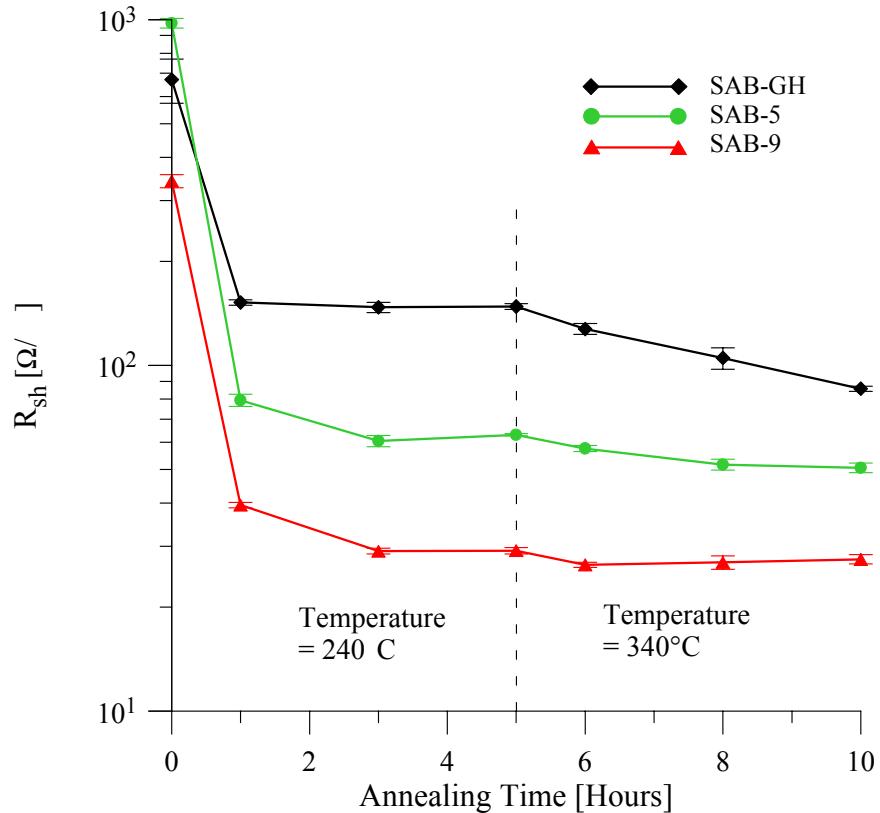


Figure 5.16: Effect of the Schottky annealing scheme on the sheet resistance, R_{sh} , of various ITO films.

The R_{sh} and ρ from Table 5.3 have been plotted in Figure 5.16 and Figure 5.17 as a function of annealing time. It is noticed that the maximum change in R_{sh} and ρ occur within the first hour of annealing at 240°C and the curve becomes near linear indicating minimal change after subsequent annealing for a given temperature. There is little but noticeable further change following an increase in the anneal temperature to 340°C; the electrical properties of the film following additional anneal at this temperature also level off as before.

All three films grown at different r.f. powers - thus having varying initial R_{sh} - show similar decreasing resistivity and sheet resistance as the annealing scheme progresses. The final value of sheet resistance, however, is very much dependent on the film growth parameters rather than the annealing conditions.

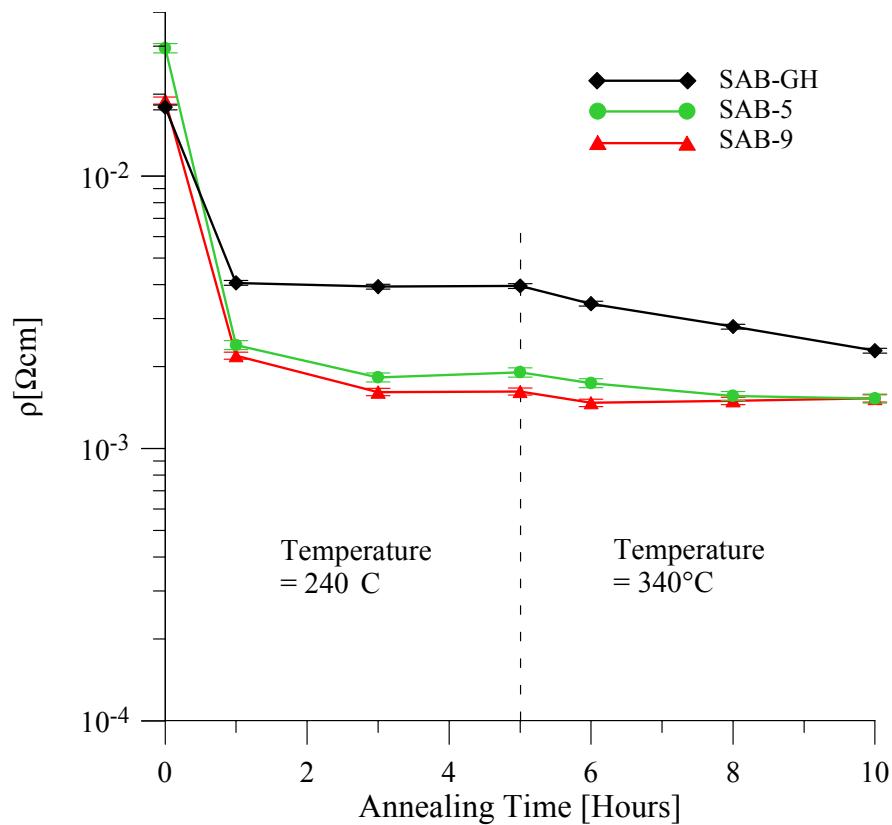


Figure 5.17: Effect of the Schottky annealing scheme on the resistivity, ρ , of various ITO films.

The change in the resistivity, ρ , of each of the three films with annealing as shown in Figure 5.17, is very similar to the corresponding change in their sheet resistances. The final value for the ρ of $(15.3 \pm 0.5) \times 10^{-4} \Omega\text{cm}$ for sample SAB-5 (grown at 150W) is in good agreement with those reported in the literature. Table 5.4 compares the annealed results from this work with those in the literature.

Ref.	Deposition Method	Annealing Method	R_{sh} [Ω/\square]	ρ [$\times 10^{-4} \Omega\text{cm}$]
This work	reactive r.f. sputtering	H ₂ /N ₂ ambient, furnace oven	27.5 ± 1.0	15.3 ± 0.6
6	reactive r.f. sputtering	cracked ammonia (and N ₂)	10.0	4.3
8	r.f. magnetron sputtering	<i>in-situ</i> heating	5.5	4.0
152	r.f. sputtering	RTA in H ₂ at 400°C, 30 sec.	415.0	8.3
153	d.c. magnetron sputtering	RTA in N ₂ at 950°C, 30 sec.	-	2.5

Table 5.4: A comparison of resistive properties of ITO film obtained using different deposition and annealing techniques by various investigators.

5.3.1.2 Ohmic Annealing Scheme

This scheme is less restrictive in terms of the temperatures that can be used because the aim is to form a diffused junction between the underlying highly doped semiconductor and the ITO film. A test ITO sample deposited at 150W (with film thickness = 2,683 ± 118Å) was put through the same annealing scheme as those for producing ITO/semiconductor contacts; this scheme is described in section 6.2.1 in greater detail. A forming gas ambient (5% H₂ + 95% N₂) with a flow rate of 10 sccm was used during the alloying experiment. Table 5.5 shows the results.

Stage	R_{sh} [Ω/\square]	ρ [Ωcm] ($\times 10^{-4}$)
As deposited	791±83	210.0 ± 20.0
After annealing	54.5±1.7	14.6 ± 0.4

Table 5.5: Effects of the ohmic annealing scheme on ITO films.

The above table suggests that the electrical properties improve by an order of magnitude following alloying in forming gas ambient under the afore mentioned conditions.

5.3.2 Effects of Heat Treatment on the Optical Properties of ITO

Figure 5.18 shows the effect of the ohmic annealing scheme on the transmittance of a typical ITO film.

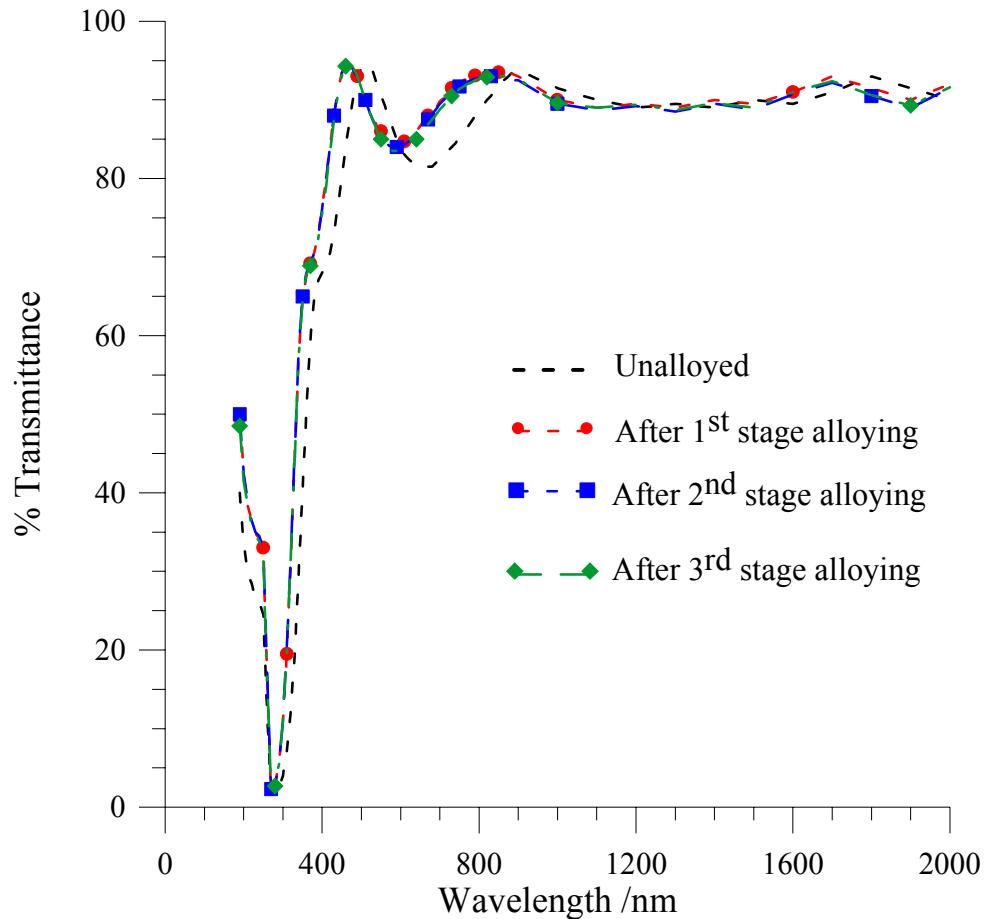


Figure 5.18: Effect of the ohmic annealing scheme on the transmittance of a typical ITO film.

It is seen from Figure 5.18 that there is a minimal change in transparency following the first annealing stage and no noticeable change thereafter. This change is a shift of the transmittance curve to the left of the x-axis, i.e. towards shorter wavelength/higher energy. This shift is most likely due to the increased carrier concentration, N , (also giving rise to better electrical properties) which is known to cause an increase in the absorption edge of ITO [144].

5.3.3 Conclusion

Both the Schottky and the ohmic annealing experiment results show resistivity as low as $14 \times 10^{-4} \Omega\text{cm}$ - similar to those reported in the literature. This suggests that there is minimal structural change to the ITO films following annealing used in this work. Other investigators have reported conflicting effects of heating on the transmittance of ITO: while Haines *et al* [152] suggest a decrease in transmission due to heating, Higuchi *et al* [9] and Sreenivas *et al* [6] observe an increase. These conflicts are most likely due to their differing methods of ITO growth and post deposition treatments.

5.4 Ohmic Contacts to ITO

The application of Indium Tin Oxide in a solid state device, for example, requires a low resistance ohmic contact to the ITO which may itself be an ohmic contact or a Schottky contact. Ohmic contacts are defined as a metal-semiconductor contact with a linear or near linear current voltage characteristic; these have been discussed in greater detail in the following chapter. Direct gold wire bonding to thin ITO films giving a low resistance contact is not easily achieved without undue damage to either or both the underlying ITO and/or the device. Therefore, following the ITO deposition and appropriate pattern definition, the contact metal or the pad is usually thermally evaporated by means of liftoff lithography. Bonds can then be made to the ITO device with as much ease as for devices with conventional contacts.

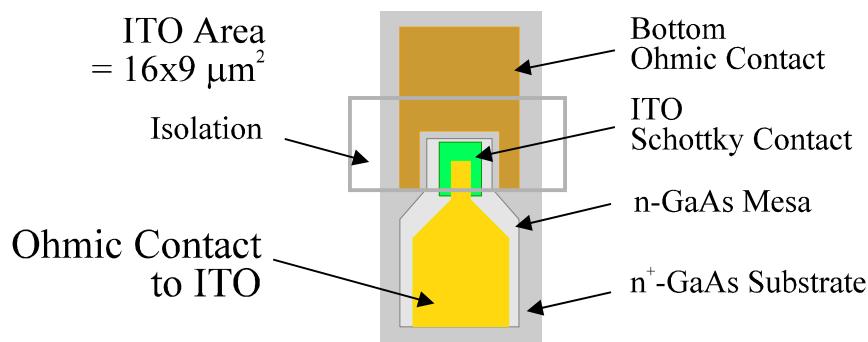


Figure 5.19: Schematic scale diagram of the plan view of a high speed ITO/n-GaAs Schottky photo diode showing the importance of a good ohmic contact to the ITO active area (Diagram after Wang *et al* [71]). Any region outside the “isolation” rectangle was proton bombarded prior to device fabrication.

Where typical contact areas in micro-electronic devices are less than a few $100\mu\text{m}^2$, it is very important for the contact resistance to be less than a few tens of ohms corresponding to specific contact resistance, ρ_c , of approximately $10^{-5}\Omega\text{cm}^2$. A schematic scale diagram of the plan view of a high speed ITO/n-GaAs Schottky photo diode is shown in Figure 5.19; it shows the importance of a good ohmic contact in order to access the active region of the device which is formed by an ITO/n-GaAs Schottky contact.

Weijtens *et al* [154] have used TiW as barrier layers to obtain low resistive, ohmic contacts between ITO and Al or Al/Si. They reported a value of $1.5 \times 10^{-6}\Omega\text{cm}^2$ for the ρ_c after annealing in $4\text{N}_2:1\text{H}_2$ gas mixtures at 450°C or 500°C .

5.4.1 Metalisation Schemes Used

Initial tests with Au deposited on bare ITO produced electrically good contacts but lacked mechanical strength and were unable to sustain the stress during gold wire bonding. Hence the suitability of three convenient metalisation systems for metal/ITO ohmic contacts were investigated. These are shown in Table 5.6. Their choice was dictated by a need to keep the metal/ITO contacts as close in composition to conventional metal/n⁺ - or metal/p⁺ - semiconductor for overall processing compatibility and the ease of device fabrication.

Layer	Set A	Set B	Set C
5	-	-	Au (1000Å)
4	Au (1000Å)	-	Ti (500Å)
3	Ni (100Å)	-	Ni (100Å)
2	AuGe (300Å)	Al (1500Å)	AuGe (300Å)
1	Ni (50 Å)	Ni (50Å)	Ni (50 Å)

Table 5.6: Details the ohmic contact schemes applied to ITO.

The Ni/AuGe/Ni/Au metalisation scheme is the most widely used scheme in our laboratories for making conventional n-type ohmic contacts to a wide ranging substrate materials and devices. Therefore, ITO contacts can be made conveniently by placing the sample into the evaporation chamber in tandem with a wide variety of other devices requiring an n-type ohmic contact. The Ni/Al system provides a cheap and easy way of making ohmic contacts to ITO layers. It is particularly useful when metals are deposited exclusively for making ohmic contacts to ITO devices as opposed to the usual case when a number of other devices are fabricated in tandem. Finally, the Ni/AuGe/Ni/Ti/Au metalisation scheme was used in the fabrication of n-type ohmic contacts to transparent gate HEMT devices. This was chosen because unlike Set A, this scheme retains a smooth surface morphology following rapid thermal annealing (RTA).

5.4.2 Results and Conclusion

Each of the contacts were annealed using the following conditions: 5 hours at 240°C followed by another 5 hours at 340°C in H₂/N₂ ambient. The TLM method was once again used to appraise these contacts. Recall that R_{sh} is the sheet resistance of the mesa (ITO in this case) while R_{sk} is the modified sheet resistance directly under the metal pads deposited on the ITO. The results are shown in Table 5.7.

Metalisation		R _{sh} (ITO) [Ω/□]	R _{sk} [Ω/□]	ρ_c [x10 ⁻⁴ Ωcm ²]
Set A	Unannealed	978.2 ± 31.1	41.7 ± 1.6	2.6 ± 0.3
	Annealed	50.6 ± 1.7	0.98 ± 0.06	0.28 ± 0.04
Set B	Unannealed	664.6 ± 48.0	7.4 ± 0.5	5.4 ± 0.4
	Annealed	24.1 ± 2.6	1.4 ± 0.1	0.8 ± 0.1
Set C	Unannealed	1273.2 ± 68.6	93.3 ± 12.1	3.4 ± 0.4
	Annealed	76.0 ± 3.4	1.8 ± 0.2	0.4 ± 0.02

Table 5.7: Effect of annealing on the electrical properties of various ohmic contacts to ITO films (typically 2000Å thick).

Comparing the electrical properties of the three metalisation systems investigated, it is seen that all the unannealed characteristics of the contacts are very similar - R_{sk} and ρ_c in the region of 50Ω/□ and 3x10⁻⁴ Ωcm² respectively. This is in spite of the sheet resistances, R_{sh}, of the corresponding ITO material varying over a much greater range: 1273.2 Ω/□ to 664.6 Ω/□. The R_{sk} after annealing for all three metalisations reduces by an order and lies approximately in the range 1 to 2 Ω/□ while ρ_c drops to the range 3 to 8 x10⁻⁵ Ωcm².

Hence it may be concluded that while the various metalisation schemes used here ultimately make no significant difference to electrical properties of the metal/ITO contacts, they all are all equally suitable for the purpose of further work in this investigation since excellent ohmic contacts to ITO have been realised.

6. Application of Transparent ITO Contacts

6.1 Devices Based on the Schottky Contact

6.1.1 Results on Metal/n-GaAs Schottky Diodes

Given that the metal-semiconductor contact is one of the most widely used rectifying contacts in industry [23] and the technological importance of GaAs, a full understanding of the nature of the electrical characteristics of Schottky diodes in this system is of great interest. Therefore, prior to studying transparent Schottky contacts, a knowledge of conventional opaque contacts is necessary. In this section, a detailed study of near ideal Au and Al/n-GaAs Schottky diodes is carried out both experimentally and theoretically by empirical modeling. The fabrication process was optimised to produce near ideal diodes with low leakage current and low series resistance. Following d.c. I-V characterisation, cryogenic measurements were done down to 140K and 80K for the Au and the Al/n-GaAs devices respectively in order to study the current transport mechanisms.

6.1.1.1 Diode Fabrication

The epitaxial layers were grown by Molecular Beam Epitaxy (MBE) on Si doped conductive n⁺-GaAs wafer (no. GB445). The layer structure was as follows: 400μm n⁺-GaAs substrate doped to $3.7 \times 10^{18} \text{ cm}^{-3}$, 1.25μm n⁺-GaAs doped to $1.3 \times 10^{18} \text{ cm}^{-3}$ and a 1.75μm n-GaAs layer doped to $1.4 \times 10^{16} \text{ cm}^{-3}$.

A schematic diagram of the metal/n-GaAs Schottky diodes are shown in Figure 6.1. The deposition and alloying of the ohmic contacts was carried out prior to the deposition of the Schottky metal in order to preserve the “abruptness” of these contacts which tend to diffuse at high temperatures and lose their rectifying capability.

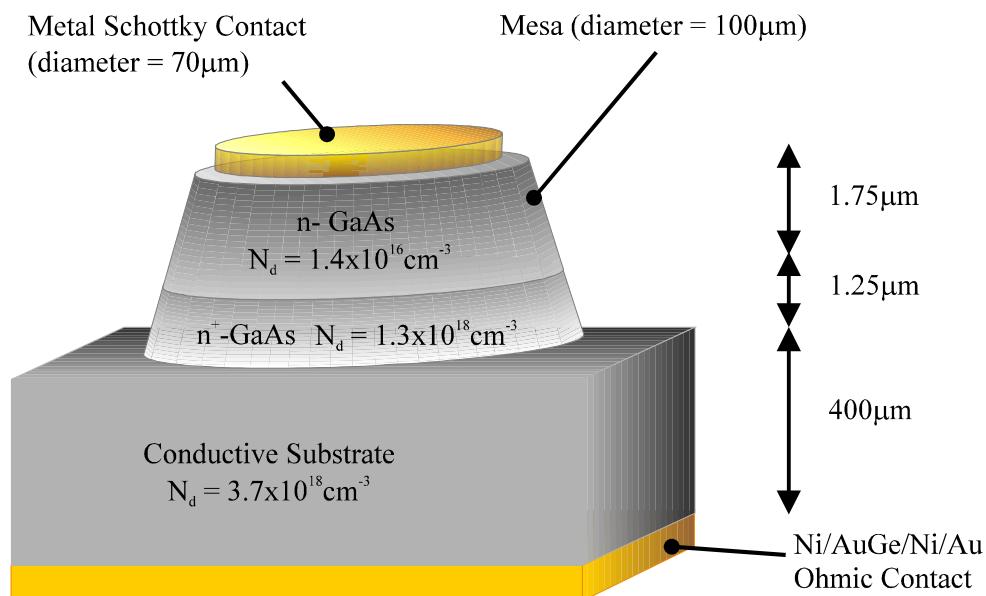


Figure 6.1: A schematic diagram of metal/n-GaAs Schottky diodes.

Different sets of Schottky diodes were fabricated with both top and bottom n-type ohmic contacts. In case of the top contact devices, the wafer was first mesa etched to the substrate layer with circular photoresist mask for the subsequent deposition of the Schottky metal at a later stage. The diameter of the mesa was 100μm. For the devices with bottom ohmic contacts, the mesa etching step could be carried out either before or after the ohmic metalisation was complete. The ohmic contacts were made to the n⁺-GaAs substrate layer by thermal evaporation of Ni(50Å)/AuGe(300Å)/Ni(100Å)/Au(1000Å) metalisation scheme and alloyed by RTA technique at 400°C for one minute.

The samples were then thoroughly cleaned in acetone, methanol and D.I. water at 60°C for 10 minutes in each solution. Following this step, 70μm diameter windows were defined using 1μm photoresist on the circular mesas to carry out metal deposition by the lift-off process. Immediately prior to loading the samples into the evaporation chamber, they were cleaned in 10% HCl solution for 20 seconds to remove any native oxides. The chamber pressure was better than 1×10^{-6} torr before the respective metals (Al or Au) were evaporated. It should be noted that during this Schottky metalisation, no “degassing” was carried out. The thickness of the Schottky metals were typically 1500Å.

Following fabrication, devices were scribed, packaged and bonded onto T05 transistor headers for characterisation and analysis. The T05 headers were placed in an Oxford Instruments Cryostat and the temperature was scanned from 140K to 360K; I-V characteristics were plotted using a HP4145B Semiconductor Parameter Analyser (SPA).

6.1.1.2 I-V Results

I-V measurements were carried out to extract the barrier height, the modified Richardson constant and to analyse the current transport mechanisms. Figure 6.2 shows typical semi-logarithmic plots of forward I-V characteristics for Au/n-GaAs Schottky diodes. It is apparent that the linear parts of the characteristics are almost ideal within the measured temperature range. The temperature dependence of the series resistance, R_s , due to poor ohmic contact is also apparent. Indeed, other experimental data obtained with samples with improved ohmic contact showed that the temperature dependence of the ohmic contact can be removed completely. The ideality factor, deduced from the linear part of the curves, which exceeds 8 decades in current at 260K, was approximately 1.06.

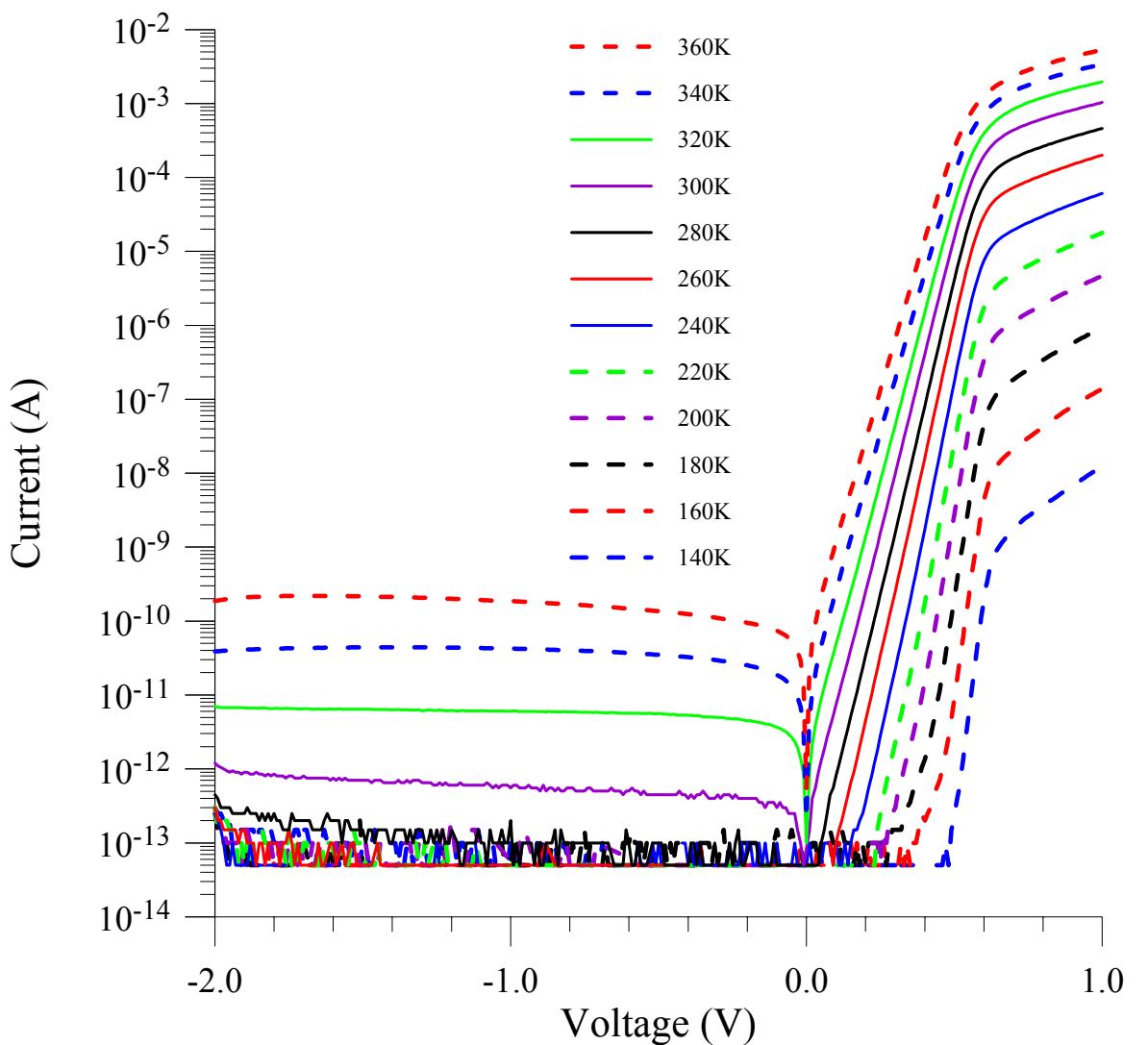


Figure 6.2 : Measured I-V Characteristics of Au/n-GaAs as a function of temperature.

Figure 6.2 also shows that the reverse current is independent of bias over the temperature range 300K to 360K. Their increase in magnitude with temperature can be attributed to the increase in the saturation values of the various temperature dependent current transport mechanisms. The linearity of the reverse currents versus bias suggests absence of parasitic effects such as high surface leakage currents. However, at temperatures below 300K (only 280K and 260K are identifiable in Figure 6.2), the reverse current becomes increasingly non-linear as a function of bias. This can be explained by an increase in the overall series resistance which continues to rise with falling temperature as confirmed by the high forward bias regions of the low temperature I-V plots; the reverse currents at these temperatures were below the 5×10^{-14} A threshold of the SPA.

Important information on the transport mechanism can also be obtained from the Arrhenius plot of $\ln(I_{te}/T^2)$ versus $1/T$. A typical Arrhenius plot for the Au/n-GaAs Schottky diodes, as shown in Figure 6.3, was obtained by extrapolating the linear portions of the forward I-V curves in Figure 6.2 to zero bias and plotting these values as a function of $1/T$.

From Figure 6.3 it is seen that at high temperature, where the thermionic emission process is the dominating current transport mechanism, a linear fit can be achieved. The ideality factor in this range never deteriorates beyond 1.06. However, at lower temperature the experimental data is seen to be deviating from the linear region due to the presence of other parallel current transport routes.

From the y-axis intercept of the Arrhenius plot the modified Richardson constant, A^{**} , for Au/n-GaAs interface can be obtained. Similarly, the slope of the linear fit can be used to obtain the barrier height ϕ_{bo} . In this case, the values for ϕ_{bo} and A^{**} were 0.84eV and $12.5 \times 10^6 \text{ Am}^{-2}\text{K}^{-2}$ respectively.

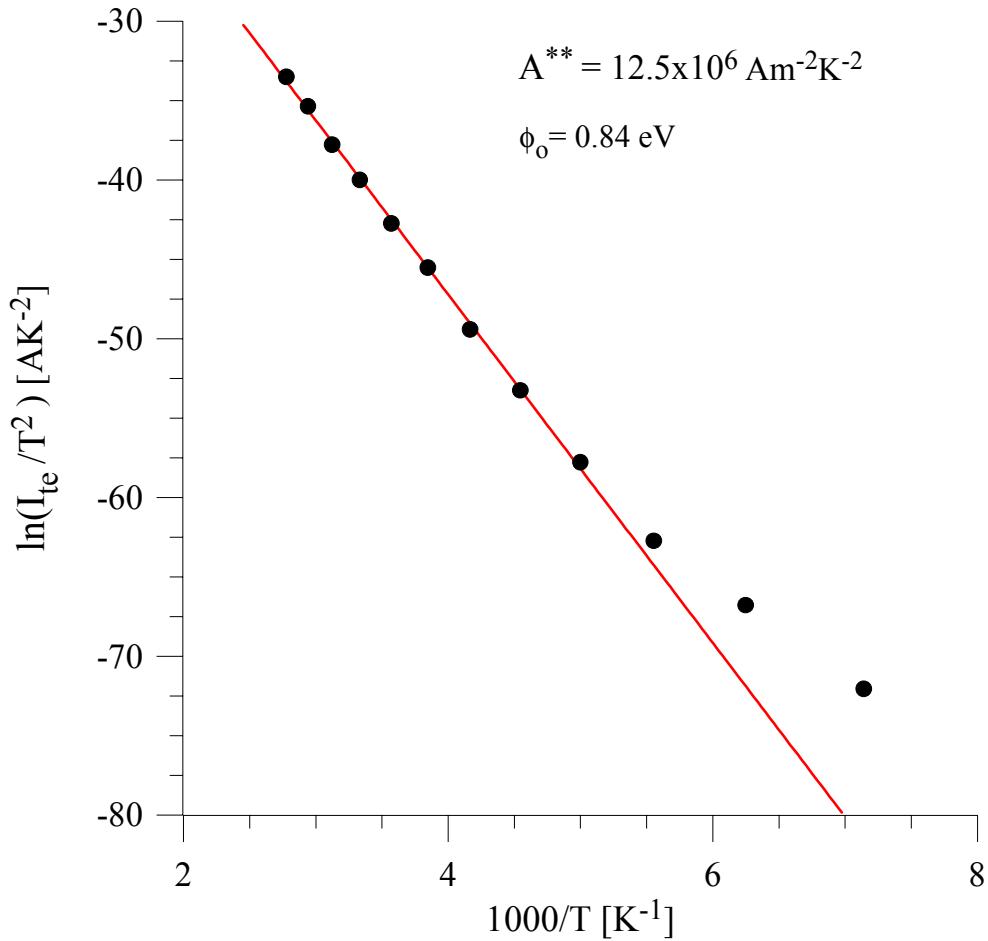


Figure 6.3: Arrhenius plot of $\ln(I_{te}/T^2)$ versus $10^3/T$ showing the temperature dependence of thermionic emission current in the Au/n-GaAs Schottky diode.

Table 6.1 compares the results of this work with those reported by Srivastava *et al* [155] and Missous *et al* [156] respectively.

Material	Metal Deposition Technique	n	ϕ_{bo} [eV]	A^{**} [Am ⁻² K ⁻²]	Ref.
MBE (Si) grown, n-GaAs, $1.4 \times 10^{16} \text{ cm}^{-3}$ $1.75\mu\text{m}$ active layer	surface etched chemically	1.04	0.84	12.5×10^6	This work
LPE grown n-GaAs, $1 \times 10^{15} \text{ cm}^{-3}$ $2\mu\text{m}$ active layer	surface etched chemically	1.02	0.92	$(83 \pm 24) \times 10^6$	[155]
MBE (Si) grown, n-GaAs, $3 \times 10^{15} \text{ cm}^{-3}$ $2\mu\text{m}$ active layer	in-situ	1.03	0.85	16.0×10^6	[156]

Table 6.1 : Electrical parameter comparisons of Au/n-GaAs Schottky diodes deduced from I-V measurements

It is interesting to note that the results obtained in this work are close to those reported by Missous whose diodes were fabricated by in-situ deposition of the metal contact, i.e. without breaking the vacuum in the MBE chamber. This is inspite of the doping in this work being several times greater than that of Missous *et al.*

6.1.1.3 Analysis and Modeling

The most common approach in analysing Schottky behaviour in semiconductor diodes assumes pure thermionic emission of carriers over the barrier. In such cases the effect of the series resistance and all the other current transport mechanisms are accounted for by the ideality factor, n. The thermionic current, I_{te} , is then modified and can be expressed by:

$$I_{te} = I_{teo} \left[\exp\left(\frac{q(V - IR_s)}{nkT}\right) - 1 \right] \quad (\text{eqn.6.1})$$

where,

IR_s = the potential drop outside the Schottky junction due to series resistance R_s

I_{teo} = the saturation current given by:

$$I_{teo} = AA^{**} T^2 \exp\left(\frac{-q\phi_{bo}}{kT}\right) \quad (\text{eqn. 6.2})$$

where,

A = the diode cross-sectional area

A^{**} = the modified Richardson constant

ϕ_{bo} = the barrier height at zero applied bias.

In using (eqn.6.1) and (eqn. 6.2) to determine the barrier height and the ideality factor erroneous results can be obtained when thermionic emission is no longer the dominant current transport mechanism. Several correction methods have been suggested [157,158,159] to improve data extraction. However, these have their own limitations and cannot be used to explain the experimental results fully, especially when the I-V plots cover a wide temperature range.

In this work, an empirical method has been used to fit computer simulation to the experimental data. The influence of the various fitting parameters have thus been used to explain the dominance of the a particular mechanism within a given temperature and/or field

range. As well as the thermionic emission process, the influence of other parallel mechanisms have been accounted for individually thus eliminating the need for the “ideality factor” n . This approach has been used successfully to analyse the temperature dependence of PtSi-Si Schottky diodes over a wide range by Donoval *et al* [22,160].

Most of the other current transport mechanisms were introduced in section 2.2 and include the generation-recombination current, I_{gr} . For moderate to highly doped semiconductors, ($N_D \geq 10^{16} \text{ cm}^{-3}$) thermionic field emission becomes significant - particularly in GaAs where the effective mass of electrons is small [161,162]. Hence it is important to include the effect of electron tunneling through the potential barrier at energies above the bottom of the conduction band. This constitutes the tunneling current, I_{tn} , and is valid for all except very low biases [21,24]. The relative importance of I_{tn} with respect to I_{te} , is determined by the value of (E_{oo}/kT) as expressed in (eqn. 2.11). E_{oo} is known as the tunneling constant and is dictated by the inherent properties of the semiconductor material such as its permitivity, doping concentration and effect mass of electrons as shown by (eqn. 2.12). There is also current contribution through leakage or parallel current paths which bypass the Schottky junction altogether. In the simulation, this is represented by a large resistance value, R_{lk} .

All these mechanisms transport current in a parallel configuration where the effective resistance is dominated by the least resistive path. Hence, for example when the resistance offered by the various mechanisms mentioned earlier become comparable to R_{lk} , the current through the latter becomes significant. All these current transport mechanisms as well as the limits imposed upon them particularly at high currents by the series resistance, R_s , are accounted for in the model. The simulation assumes simultaneous contribution by all these components to the total diode current, I_{tot} :

$$I_{tot} = I_{te} + I_{gr} + I_{tn} + I_{lk} \quad (\text{eqn. 6.3})$$

Thus it is not necessary to divide I_{te} by the “ideality factor - n ”. Equations for these mechanisms account for both their bias and temperature dependence thereby displaying their dominance under particular combinations of these two parameters as discussed later.

Keeping this in mind, the extracted Richardson constant, A^{**} , and the barrier height, ϕ_{bo} , from (eqn. 6.2) are used to calculate the thermionic emission component of the total current. Similarly, for the generation-recombination current, an equation is fitted to represent its temperature dependence from a plot of $\ln(I_{gr}/T^{3/2})$ vs. $1/T$ as shown in Figure 6.4. The temperature dependence of the leakage, tunneling and resistive currents are extracted in a similar manner.

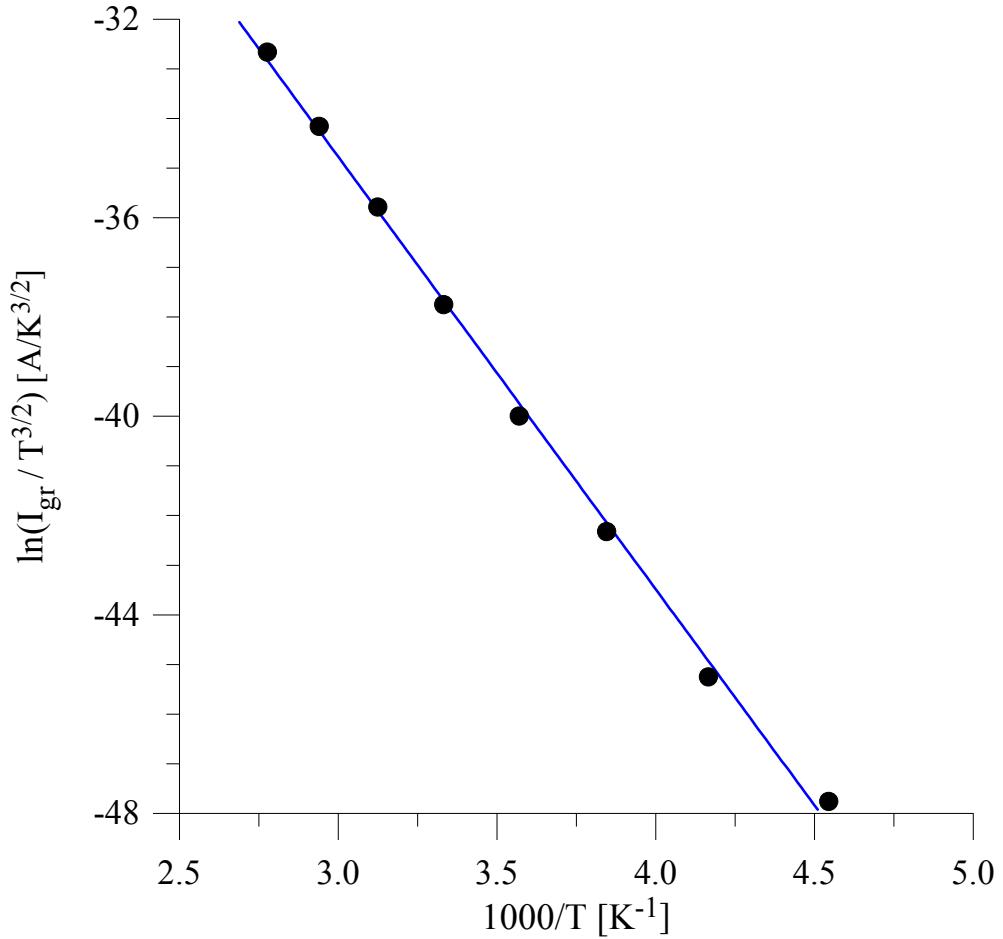


Figure 6.4 : Temperature dependence of generation-recombination current, I_{gr} , for an Au/n-GaAs Schottky diode.

The values of R_s and R_{lk} increase abruptly at low temperatures. Donoval *et al* [22] have also reported similar observations and related this effect to the lack of free charge carriers as a result of imperfectly ionized impurities at low temperatures.

Selecting appropriate values of I_{teo} , I_{gro} , I_{tno} , E_o and the resistances R_s and R_{lk} is necessary for fitting the experimental I-V plots. The total current at any given bias is therefore obtained by summing the individual components of (eqn. 6.3). In its expanded form, this can be expressed as:

$$\begin{aligned}
 I_{tot} = \sum_{i=1}^4 I_i &= I_{teo} \left[\exp\left(\frac{q(V - I_{tot}R_s)}{kT}\right) - 1 \right] + I_{gro} \left[\exp\left(\frac{q(V - I_{tot}R_s)}{2kT}\right) - 1 \right] \\
 &\quad + I_{tno} \left[\exp\left(\frac{q(V - I_{tot}R_s)}{E_o}\right) - 1 \right] + \left(\frac{V - I_{tot}R_s}{R_{lk}} \right)
 \end{aligned} \tag{eqn. 6.4}$$

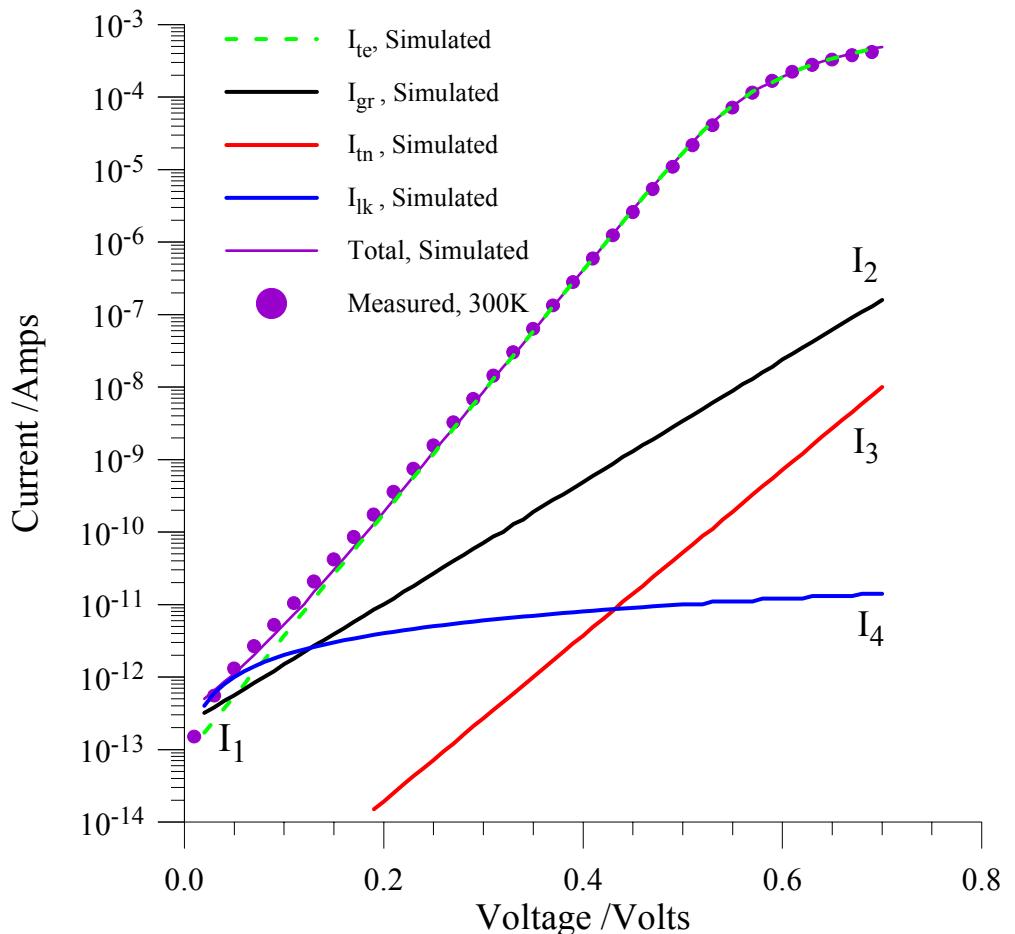


Figure 6.5 : A typical fit of experimental data for a given temperature (300K) by the simulated results with contribution from each of the components; I_1 = thermionic emission current, I_2 = generation recombination current, I_3 = tunneling current and I_4 = leakage current.

Using the summation of (eqn. 6.4), a typical fit of experimental data for a given temperature (300K) by the simulated results with contribution from each of the components is shown in Figure 6.5. At this temperature, the dominant mechanism is thermionic emission as indicated by curve I_1 which overlaps most of the experimental results except a small part in the low bias region; at low biases, the leakage current, indicated by curve I_4 , plays a dominant role and is augmented by a very partial influence from the generation-recombination current, I_2 . The tunneling current, I_3 , has little or no influence on the total current at this temperature. At high biases, the overall current is limited by the series resistance; although each of the components increase with bias, they have diminishing effect in comparison to the thermionic emission component and finally the series resistance.

Figure 6.5 demonstrates suitability of this empirical curve fitting method in analysing the complex behaviour of a Schottky junction over a wide bias range. This principle is extended by taking into account the temperature dependence of the saturation values of each of these

currents in order to simulate the results over a wide temperature range. The experimentally deduced temperature dependence of I_{teo} and I_{gro} are easily obtained from the respective slopes of the $1/T$ plots in Figure 6.3 and Figure 6.4. The tunneling parameter E_0 is determined from theory while I_{tn} , R_s and R_{lk} are fitted to the experimental data.

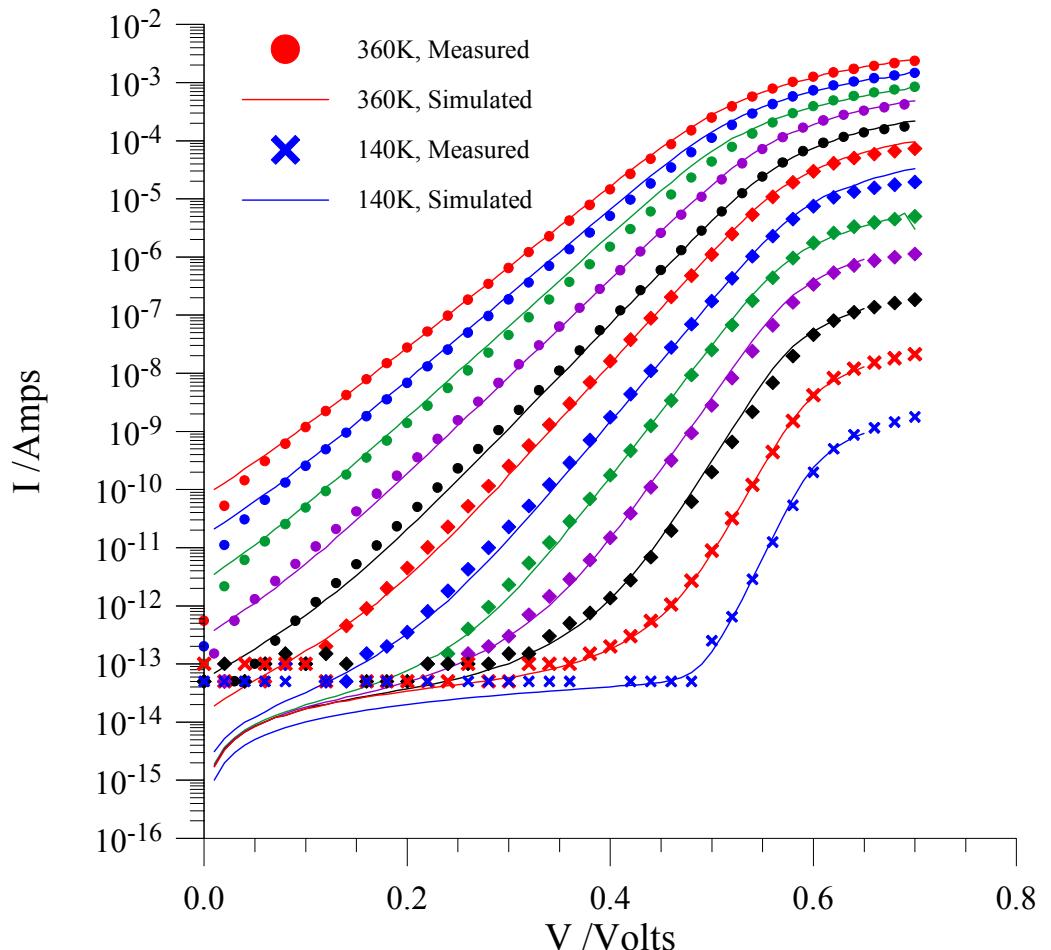


Figure 6.6 : Experimental and simulated plots of forward current versus applied bias over a wide range of temperatures for a Au/n-GaAs Schottky diode; temperature difference between successive lines or set of points = 20K.

The experimental and the simulated results are plotted together in Figure 6.6 for comparison. It is evident that good agreement is found over several decades of current at all temperatures. However, the simulated results are better matched to the experimental data at higher current. This is because I_{te} and R_s are the most exactly determined parameters. The leakage current represented by R_{lk} is largely influential at lower biases while the thermionic emission current dominates in the resulting relationships at higher biases. However, in the regions where neither of the above mechanisms are highly influential, finding acceptable values of I_{gr} and I_{tn} can pose limitations on the model.

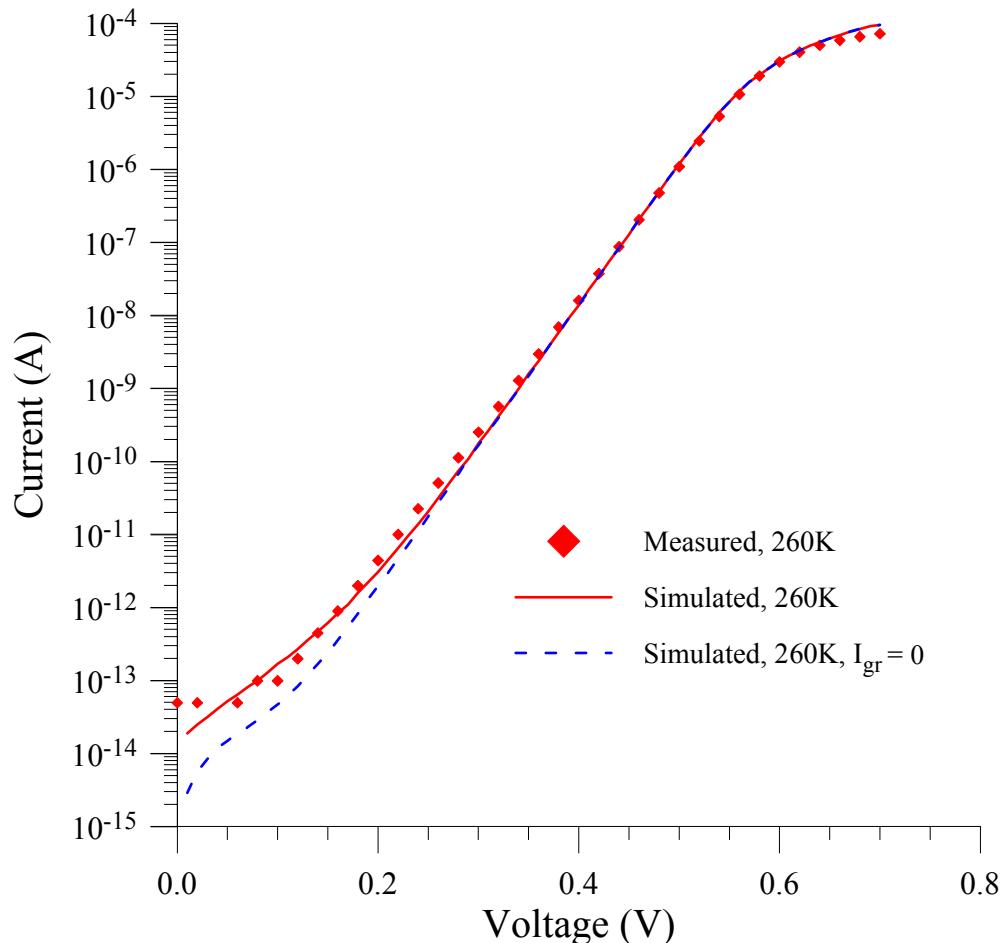


Figure 6.7 : Contribution of generation-recombination current component at higher temperatures high-lighted by simulated results with I_{gr} set to zero.

It was shown earlier that using (eqn. 6.4) it is easy to separate the influence of individual current transport mechanisms. In order to illustrate the effect of generation-recombination current at moderately low temperatures and low biases, the measured data at 260K was simulated with and without the contribution of this component. The three sets of data are plotted on the same graph in Figure 6.7. The dotted curve, representing simulation with $I_{gr} = 0$, is consistently below that of the solid curve, the total simulated current, up to a bias of 0.3V; above this bias, the thermionic emission current overshadows other components. At this temperature, the effect of tunneling was still significantly low to have any influence on the total current. Thus, it is seen that with decreasing temperature, the influence of the other parallel mechanisms begin to take effect rather than a modification to either the junction barrier height or the ideality factor as sometimes cited in the literature [163,164]; in this model, the barrier height used throughout was 0.84eV which was extracted from the slope of the Arrhenius plot in Figure 6.3.

The influence of the generation-recombination current was noticeable under low bias regions over the temperature range 280K to 200K. Below this temperature, it is overshadowed by the leakage current at low bias, tunneling component at mid-range current values and by thermionic emission component at high bias region. Further analysis at lower temperature was used to isolate the effect of the tunneling current as shown in Figure 6.8. Again it is noticed that setting the tunneling current component, $I_{tn} = 0$, results in significant discrepancies between the measured and the modeled results.

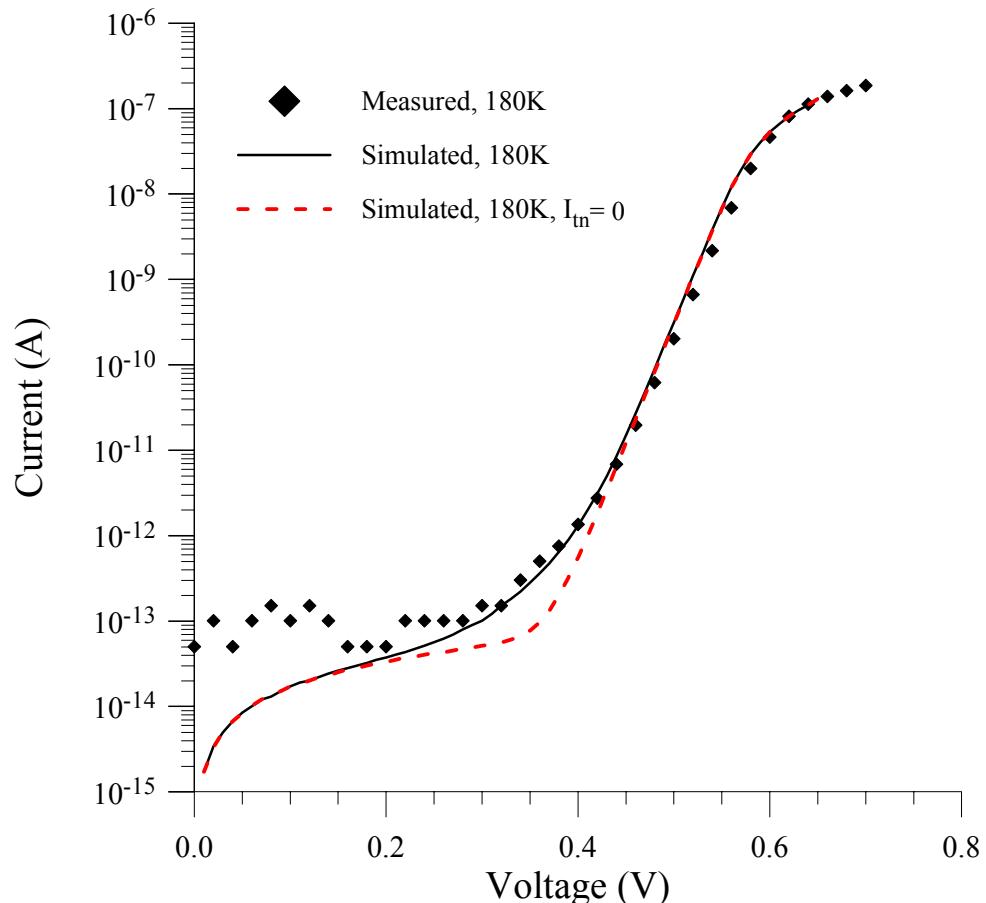


Figure 6.8: Contribution of tunneling current component at low temperatures and high bias highlighted by simulated results with I_{tn} set to zero.

It should be noted that accurate extraction of generation-recombination current becomes acutely more difficult as the measured data begins to approach the limit of the SPA; this is seen in the low bias regions of the low temperature I-V plots, including Figure 6.8. Therefore, it is important to keep these limitations in mind in the modeling and interpretation of the results.

6.1.1.4 Al/n-GaAs Schottky Diodes

The fabrication and the temperature measurement of these devices have already been described in earlier sections. Figure 6.9 shows the measured I-V plots of these devices over the 360K to 80K temperature range.

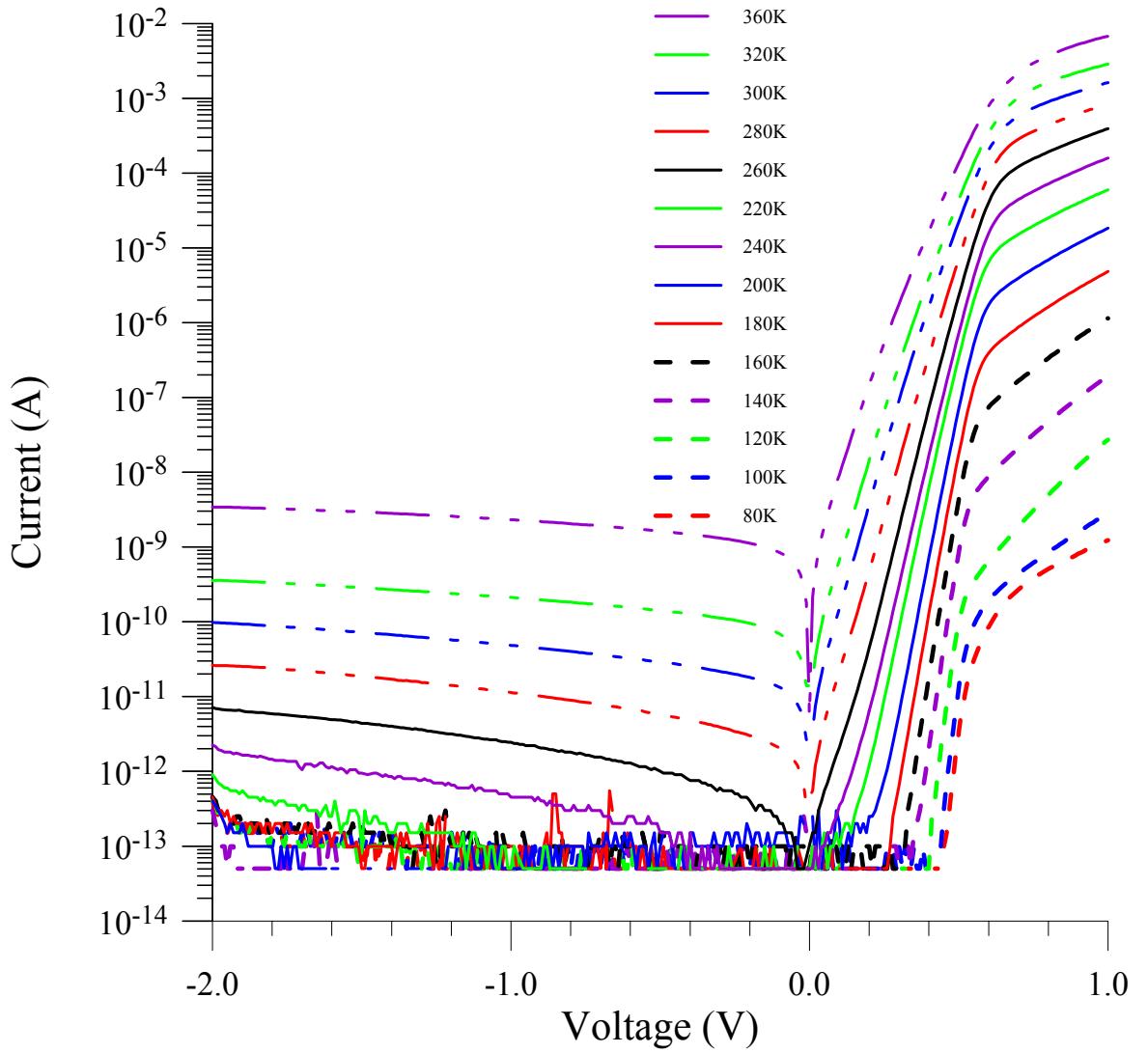


Figure 6.9: Measured I-V Characteristics of Al/n-GaAs as a function of temperature.

The linear parts of the characteristics of these Al/n-GaAs diodes are almost ideal within the measured temperature range as in the case of the Au/n-GaAs diodes. The ideality factor, deduced from the linear part of the curves, which exceeds 8 decades in current at 260K, was approximately 1.08.

Similar analysis to the Au/n-GaAs was done to these devices using the empirical curve fitting model to study the I-V plots over a wide bias and temperature range. The values of ϕ_{bo} and A^{**} were extracted and are compared to those reported in the literature in Table 6.2:

Material	Metal Deposition Technique	n	ϕ_{bo} [eV]	A^{**} [$\text{Am}^{-2}\text{K}^{-2}$]	Ref.
MBE (Si) grown, n-GaAs, $1.4 \times 10^{16} \text{ cm}^{-3}$ 1.75μm active layer	surface etched chemically	1.08	0.77	16×10^4	This work
n-GaAs, $1.2 \times 10^{16} \text{ cm}^{-3}$	surface etched chemically	1.03	0.76	19×10^4	[155]

Table 6.2: Electrical parameter comparisons of Al/n-GaAs Schottky diodes deduced from I-V measurements

6.1.1.5 Conclusion

The electrical behaviour of near ideal Au/n-GaAs Schottky diodes has been simulated over a wide range of currents and temperatures using a empirical curve fitting model in order to understand the behaviour and the influence of the various current components of these devices. The experimental data on the thermionic emission current yields a barrier height, ϕ_{bo} , of 0.84eV and a Richardson constant, A^{**} , of $12.5 \times 10^6 \text{ Am}^{-2}\text{K}^{-2}$.

Similarly, study of the Al/n-GaAs Schottky diodes, in particular the data on the thermionic emission current yields a barrier height, ϕ_{bo} , of 0.77eV and a Richardson constant, A^{**} , of $16 \times 10^4 \text{ Am}^{-2}\text{K}^{-2}$. Both these sets of values are in good agreement with those reported in the literature for Au/ and Al/n-GaAs Schottky diodes respectively.

6.1.2 Fabrication and Process Optimisation for ITO/n-GaAs Schottky Diodes

The general photo detection mechanisms in a Schottky diode were discussed in section 2.5. It is known that this structure is suited for high speed applications [71]. An inherent disadvantage of these devices, however, is their high series resistance and low optical sensitivities arising from the semi-transparent metal layer. Using a practically transparent and

highly conductive layer of Indium Tin Oxide (ITO) to form the metal/semiconductor junction solves both these problems [73]. Figure 6.10 shows a structural diagram for a photo diode with transparent ITO Schottky contact.

In this section the optimisation of the fabrication technique to produce high quality ITO/n-GaAs Schottky diodes is described. It is necessary to modify a number of processing steps used in the fabrication of conventional Schottky diodes. In the following sections, the influence of the critical fabrication steps and their evolution resulting in ideal ITO photo diodes with low reverse dark and leakage currents, low resistance, low ideality factor (close to unity) and high barrier height is discussed.

6.1.2.1 The Effect of Mesa Etch and Post Deposition Annealing

Initially, majority of the ITO diodes were fabricated on a MBE grown conductive GaAs wafer (no. GB85), which had a very similar layer structure to the wafer (no. GB445) used for the metal/n-GaAs Schottky diodes. The layer structure was as follows: $400\mu\text{m}$ n⁺-GaAs substrate doped to $2\times 10^{18} \text{ cm}^{-3}$, $1.25\mu\text{m}$ n⁺-GaAs doped to $1.3\times 10^{18} \text{ cm}^{-3}$ followed by a $1.75\mu\text{m}$ n-GaAs layer doped to $5\times 10^{16} \text{ cm}^{-3}$.

A Ni/AuGe/Ni/Au ohmic metalisation system was used to make a back contact to the substrate; this contact was then alloyed at 400°C using RTA. This was followed by the usual cleaning steps in organic chemicals and D.I. water. Prior to depositing the Schottky layer, the samples were pre-etched in 10% HCl solution for 35 seconds. ITO was then deposited on the top surface of the wafer by r.f. sputtering. The sputtering conditions were as follows:

- Forward r.f. power = 100W
- Duration = 30 minutes
- Ambient = 90%Ar + 10%O₂ by gas flow rate.

The ITO thickness measured was = $(2267 \pm 47)\text{\AA}$ corresponding to a deposition rate of $(75 \pm 1.6) \text{ \AA/sec}$. During these initial experiments, the target was not preconditioned. Following ITO deposition, the layer was patterned with a $180\mu\text{m}$ diameter circular mesa mask for device definition; unwanted ITO was removed by chemical etching in 10% HCl solution for 20 minutes until there was no visible trace. Circular metal pads consisting of Ni/AuGe/Ni/Au and $70\mu\text{m}$ in diameter, were then deposited on the ITO diodes to minimise contact resistance during probing. No mesa etching of the underlying semiconductor was carried out at this stage. These devices were non-ideal, leaky and resistive as shown in Table 6.3. Furthermore, it was also noticed that if one characterised the diode by probing the ITO directly, the series resistance appeared to be $1.5 \text{ k}\Omega$.

Parameter	Value
Ideality factor, n	2.8
Barrier height, ϕ_{bo}	0.51eV
Dark current, I_{dark} (at -3V)	11μA
Series resistance, R_s	300Ω

Table 6.3: Results of early ITO/n-GaAs Schottky photo diodes (on wafer no. GB85)

These devices were then etched using the same mask in a 1HF:1H₂O₂:10H₂O solution for 2 minutes ($\approx 0.6\mu\text{m}$) followed by annealing in a forming gas ambient (10% H₂ + 90% N₂) at 320°C for half an hour. The dark current following the etch and annealing reduced to 0.6μA and 20.7 nA respectively. At each stage, the photo current, I_{Ph} , of the devices were also measured. The total reverse current, I_r , is given by:

$$I_r = I_{dark} + I_{Ph} \quad (\text{eqn. 6.5})$$

As a result of these processing steps progressively flatter reverse I-V characteristics were produced as summarised in Table 6.4:

Stage :	I_{dark} (at -3V)	I_{Ph}
As fabricated	11 μA	50 μA
After mesa etching to remove $\approx 0.6\mu\text{m}$	0.6 μA	3 μA
After annealing in forming gas at 320°C for 30 mins	20.7 nA	0.5 μA

Table 6.4 : Comparison of dark and photo current for ITO/n-GaAs diodes (on wafer GB85) as a function of post fabrication etching and annealing in forming gas ambient.

From these results, it is apparent that the dark current reduces due to mesa etching. This is because any residual ITO outside the device area is removed and it is also more difficult for carriers to flow down the edges of the mesa. The removal of residual ITO from the surface by the mesa etching process means that the effective diode area is no longer as big as the wafer size but is now limited by the mask dimension i.e. 180 μm diameter; therefore, the photo current, I_{Ph} is reduced accordingly.

Since annealing does not produce any significant changes in the transparency of the ITO film (see section 5.2.), the further reduction in I_{Ph} has to be attributed to the reduction in other factors which include sputter induced defect leakage current. Mullins *et al* reported that sputtering causes surface damage and creates traps, the density of which decays exponentially with distance from the semiconductor surface, leading to a lowered Schottky barrier height [165]; the same effect is evident in case of these results. Annealing has the effect of removing a lot of these defects [166,167] and thus the dark current is further reduced.

6.1.2.2 Effect of r.f. Power and ITO Film Thickness

Following on from the previous set of ITO/n-GaAs diodes, subsequent fabrications involved mesa etching to the n^+ GaAs layer. In addition, the effect of pre-conditioning the ITO target and varying the r.f. power during sputtering on the Schottky junction was studied. For this part of the work, the same wafer (no. GB445) as those used for the metal/n-GaAs diodes was used. Figure 6.10 shows a schematic diagram of such an optimised ITO/n-GaAs Schottky photo diode:

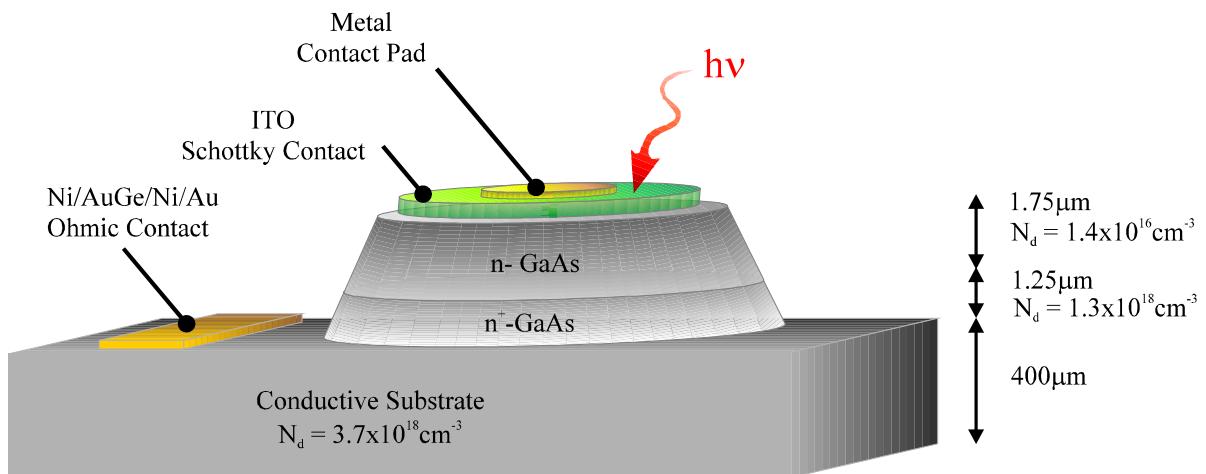


Figure 6.10: Schematic diagram of an optimised ITO/n-GaAs Schottky photo diode (on wafer GB445)

After usual chemical cleaning, pre-etching in 10% HCl for 25 minutes and ITO target pre-conditioning in Ar + 10% O₂ plasma at 100W for 20 minutes, ITO was sputter deposited on the top surface of the wafer at a r. f. power of 70W for 30 minutes. The ITO thickness measured was $= (810 \pm 10)\text{\AA}$ corresponding to a deposition rate of $(27 \pm 0.3)\text{\AA/sec}$. A circular mask of 100 μm diameter was used to etch $\approx 2.35 \mu\text{m}$ (in 1HF:1H₂O₂:10H₂O for 7 minutes) and reach to the n^+ -GaAs layer and define individual Schottky diodes; this solution etches both ITO and GaAs. A 70 μm and 180 μm liftoff mask was used to simultaneously

deposit n-type ohmic contact (Ni/AuGe/Ni/Au) to the ITO and the n^+ -GaAs layers. The ohmic contacts were not alloyed at any stage.

The devices formed were near ideal ($n = 1.08$), with high barrier heights (0.85 eV) and low dark currents (< 5 nA) but these devices showed very high series resistance (≈ 1.5 k Ω). These diodes were subsequently divided into two groups: G1 and G2; G1 was annealed in forming gas, N_2/H_2 , at 325°C a total half an hour in 10 minute steps while G2 was annealed using RTA at 200°C for 30 seconds followed by another 30 seconds at 300°C. The results of these treatments are summarised in Table 6.5 and Table 6.6 respectively:

Parameter	As fabricated	Total annealing time in N_2/H_2 at 325°C		
		10 mins	20 mins	30 mins
n	1.08 ± 0.01	1.09 ± 0.09	1.59 ± 0.41	2.3 ± 0.2
ϕ_{bo} (eV)	0.85 ± 0.01	0.81 ± 0.04	0.65 ± 0.11	0.46 ± 0.05
I_{dark} at -1.5V (A)	4.8×10^{-9}	54.6×10^{-9}	0.7×10^{-6}	9.2×10^{-6}
R_s (Ω)	1.5×10^3	895	538	426

Table 6.5: Effect of annealing ITO/n-GaAs photo diodes in forming gas (G1)

Parameter	As fabricated	30 seconds of RTA in N_2 at	
		200°C	followed by 300°C
n	1.08 ± 0.01	1.24 ± 0.2	1.5 ± 0.08
ϕ_{bo} (eV)	0.85 ± 0.01	0.83 ± 0.08	0.71 ± 0.1
I_{dark} at -1.5V (A)	4.8×10^{-9}	37.4×10^{-9}	0.8×10^{-6}
R_s (Ω)	1.5×10^3	773	648

Table 6.6: Effect of annealing ITO/n-GaAs photo diodes in N_2 using RTA (G2)

These results suggest that careful removal of unwanted ITO and mesa etching helps minimise leakage and dark currents. The high series resistance can be attributed to the combination of high resistivity of the ITO and the unalloyed ohmic contacts. However, the main contributor to this problem is the former factor. This can be justified not only by the data on ITO conductivity dependence on deposition power but also by the fact that a few devices which only had a top ohmic contact (ITO was removed during processing and prior to top metal deposition) showed a series resistance of only a few ohms. As expected, these devices

without ITO showed minimal response to light. Since all devices have metal on the ITO, the cause of the high series resistance cannot be attributed to any spreading resistance from the probes. Further discussion is presented later in section 6.1.2.4.

These diodes were used for photo response measurements using a solid state laser of 630nm beam. The responsivity was found to be 0.4A/W corresponding to an external quantum efficiency of 70%.

In order to investigate the effect of r.f. power, another set of devices (G3) were fabricated on the same wafer as previous set except the r.f. power was increased to 100W. Also, the back of the wafer was first coated with the ohmic contact (Ni/AuGe/Ni/Au) which was alloyed using RTA at 400°C for 45 seconds. Following usual preparation steps, ITO was sputter deposited on the top surface of the wafer at a r. f. power of 100W for 20 minutes; the thickness of the ITO layer was 1600Å. A circular mask of 220 µm diameter was used to mesa etch to the n⁺-GaAs layer and define individual Schottky diodes; the actual diameter of the ITO pattern was found to be 180µm - this was probably caused by under etching by the 1HF:1H₂O₂:10H₂O solution. A 70µm liftoff mask was then used to deposit a metal contact (Ni/AuGe/Ni/Au) to the ITO layer. No further annealing was carried out.

The ideality factor of these G3 devices was 1.09, the barrier height and dark current was 0.65eV and 50nA respectively. However, in comparison to G1 and G2, the (as fabricated) series resistance had dropped considerably to 200Ω. From these results it can be concluded that the R_s has been improved by a number of factors: annealing the ohmic contact prior to ITO deposition, by sputtering at a higher power and depositing a thicker layer of ITO. The last two factors were found to improve the sheet resistance of ITO as discussed in Chapter 5. The comparatively larger dark current is due to the relatively larger area of the G3 devices.

6.1.2.3 Diodes Fabricated at 150W r.f. Power Followed by Gradual Annealing

Given the knowledge of lowered ITO resistivity for a r. f. sputtering power of 150W and benefit of hindsight, a final set of ITO/n-GaAs diodes were fabricated on wafer no. GB445. In addition a very thin layer of indium metal was deposited on the GaAs mesa prior to ITO deposition to study its influence on the ohmic contact, on some of the diodes. The processing sequence was as follows:

1. Mesa etching using 100 µm diameter circular mask to the conductive layer in order to define the diodes and deposit ohmic contact.

2. Ni/AuGe/Ni/Au ohmic contacts were deposited and annealed using RTA at 400°C for 45 seconds.
3. Prior to ITO deposition this wafer was divided into two parts: Sample A was deposited with a 70μm diameter circular dot of 100Å thick thermally evaporated layer of indium on the mesa; Sample B was not altered.
4. Following pre-conditioning under identical conditions, ITO was sputtered at a r. f. power of 150W in a Ar + 10%O₂ plasma for 30 minutes; both samples was left in chamber overnight to allow the system to settle before removing the samples. The measured thickness of the ITO was 1500Å.
5. 100μm diameter circular dots of ITO, aligned with the mesa, were etched using 1HCl:1H₂O; finally Ni/AuGe/Ni/Au (70μm diameter) was deposited on this ITO layer for probing and bonding.

Individual devices were scribed and mounted on T05 transistor headers in order to carry out accurate optical measurements that required precision alignment. Three devices from each set were characterised in detail. I-V and C-V measurements were carried out in the dark using the SPA and a HP4284A LCR meter. The optical measurements were carried out using a 780nm variable power solid state laser diode using the jig described in section 4.5. The voltage ranges for each of these measurements were -2 to 2V for I-V; 0 to -4V for C-V; and -4 to 0.5V for the optical measurements. The results obtained are summarised in Table 6.7:

Parameter	Sample A (ITO/In/n-GaAs)	Sample B (ITO/n-GaAs)
Ideality factor, n	1.14 ± 0.03	1.9 ± 0.01
Barrier height, ϕ_{bo} (eV)	0.59 ± 0.01	0.58 ± 0.01
I_{dark} at -2.0V (nA)	50.6 ± 22.2	98.5 ± 2.24
Series resistance, R_s (Ω)	25.8 ± 3.4	1273.3 ± 219.4
Responsivity, R, at $\lambda = 780\text{nm}$, -2V; (A/W)	0.57 ± 0.04	0.29 ± 0.01
External quantum efficiency, η (%)	91.5 ± 8.5	46.4 ± 1.1

Table 6.7: Summary of some diode performance characteristics prior to any post fabrication annealing; measured ITO thickness was 1500Å.

From Table 6.7 it is seen that the most remarkable difference between the I-V parameters of two sets of devices as a result of the thin film of In between the ITO and the n-GaAs layer are their series resistances. This reduction in R_s could be due to two possible reasons:

- a direct result of forming a highly doped n-GaAs region immediately below the indium surface
- or an indirect effect of selective surface damage whereby the n-GaAs layer is relatively shielded from electron bombardment during sputter deposition of ITO

These samples were then annealed in a forming gas ambient at 240°C for five hours followed by another five hours at 340°C to study the effect of gradual annealing. These results will now be explained by correlating the I-V, C-V and the optical measurements on the two sets of devices.

6.1.2.3.1 ITO/In/n-GaAs Schottky Photodiodes - Sample A

Figure 6.11 shows a semi-logarithmic I-V plot of the devices on Sample A before annealing and at subsequent stages of this post fabrication treatment. It is seen that under forward bias, the linearity of the I-V curves extend over several decades for each of the device annealing treatments. Following the first set of annealing at 240°C for 5 hours, the overall forward current increases significantly and after annealing for a further 5 hours at a higher temperature of 340°C, it falls below its original value. The effect of the annealing on the corresponding reverse currents, however, is a steady decrease in magnitude; the reverse current drops by approximately a decade at each of these annealing steps. This drop is very similar to those noticed in the earlier experiments and can be attributed to annealing which removes a great deal of the defects induced by r. f. sputtering. Similar improvements were also reported by Devlin *et al* for Au-Mo/n-GaAs Schottky contacts although the annealing was carried out in a H₂ atmosphere at 500°C [168].

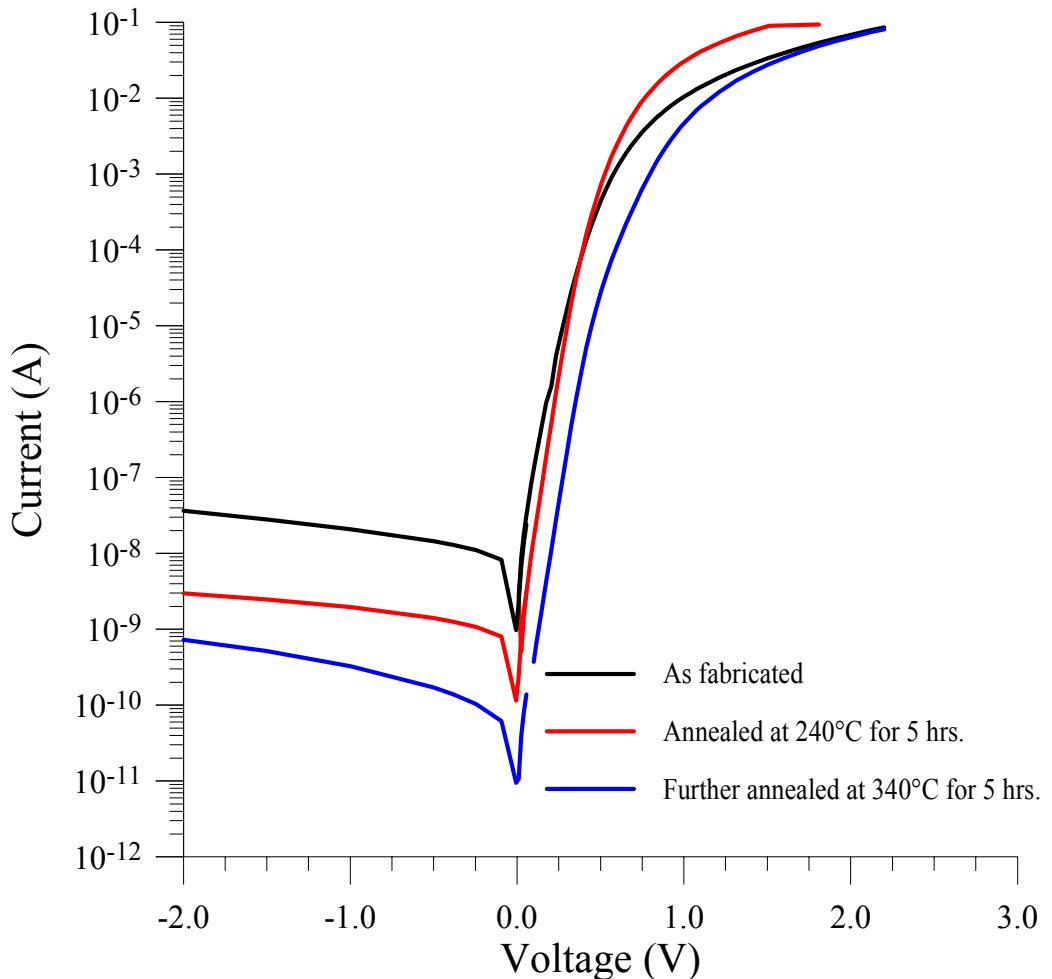


Figure 6.11 : Semi-logarithmic I-V characteristics for (Sample A) ITO/In/n-GaAs Schottky diodes measured in the as fabricated and at subsequent annealing stages

The various I-V parameters for these sets of devices are summarised in Table 6.8 for further discussion:

Parameter	As Fabricated	Annealed at 240°C for 5 hrs	Annealed at 340°C for further 5 hrs
n	1.14 ± 0.03	1.22 ± 0.02	1.16 ± 0.03
ϕ_{bo} (eV)	0.59 ± 0.01	0.65 ± 0.06	0.76 ± 0.01
R_s (Ω)	25.8 ± 3.4	15.8 ± 0.4	24.1 ± 1.3
I_{dark} at -2V (nA)	50.6 ± 22.2	3.53 ± 0.31	0.72 ± 0.1

Table 6.8: Effect of annealing on I-V parameters for ITO/In/n-GaAs Schottky photo diodes (Sample A).

After the first stage of annealing, the maximum forward current increases despite a decrease in the leakage current while the observed barrier height remains unchanged. There are two distinct regions in the forward current:

- Under low bias, where surface leakage current dominates, there is in fact a decrease in the current as a result of annealing and this can be attributed to the corresponding reduction observed in the reverse surface leakage.
- In the high bias R_s dominated region, there is an increase in forward current, I_f , which can be attributed to the reduction in the series resistance by approximately 10Ω as shown in Table 6.8. Simple calculation (similar to that in section 6.2.2) using the measured sheet resistance of the ITO film as a function of annealing (see section 5.3) shows that R_s due to the resistivity of the ITO film alone is initially below 1Ω and drops to a fraction of a $m\Omega$ following annealing. Hence, changes alone in the ITO film cannot be responsible for a 10Ω drop in resistance. This decrease in R_s is most likely due to the formation of a highly conductive InGaAs layer resulting from an inter-mixing of In and GaAs at the ITO/In/n-GaAs interface; indium alloyed to n-GaAs forms a graded InGaAs heterojunction giving rise to ohmic behaviour [169].
- The sputter damaged n-GaAs layer possibly enhances the inter-mixing of In and GaAs. Shannon *et al* reported that sputtering induced damage manifests itself in a donor like behaviour resulting in an increased surface doping in Ni/Si contacts [170] while Luo *et al* have reported complementary findings for ITO/p-InP junctions [171]. This would also account for the observed increase in the ideality factor and lowered ϕ_{bo} .

The observed increase in the ideality factor also tends to suggest an increase in other current transport mechanisms. At room temperature, the only other mechanism competing with thermionic emission is generation-recombination current, I_{gr} , which is n_i^2 dependent, as shown in section 6.1.1. The formation of an InGaAs interface would also be expected to be accompanied with an increase in I_{gr} as it has a lower bandgap than GaAs. Hence, most of our observations tend to suggest the formation of an intermediate ITO/InGaAs/n-GaAs interface.

Following the second annealing stage, at a higher temperature, in addition to a reduction in the reverse (surface) leakage current, there is an increase in R_s and ϕ_{bo} while the ideality factor and I_f decrease. The further reduction in surface leakage causes the low bias I_f to be further reduced; the increase in R_s , approximately back to its original value, results in an corresponding reduction in maximum I_f . The restoration of the R_s suggests the degradation of the highly conductive InGaAs layer from the interface; it is possible that a significant portion

of the original indium atoms have migrated deeper into the GaAs layer as a result of further annealing at the higher temperature. As will be shown by the C-V and optical results, the effect of sputter damage is significantly restored by the second annealing. Therefore, the barrier height increases to 0.76eV, a typical value for undamaged metal/n-GaAs Schottky junctions [155]. Thus the significant reduction in I_f and its shift to the right on the voltage axis of Figure 6.11 (between the original and the final plots) after the second annealing can be explained in terms of an increase in ϕ_{bo} from 0.6eV to 0.76eV; in addition, the surface leakage current drops by approximately two decades

Figure 6.12 shows the corresponding C-V measurements for these ITO/In/n-GaAs Schottky diodes at various stages. It is seen that there is an unexpected decrease in the capacitance profile following the first annealing stage and a recovery past the original value after the final annealing.

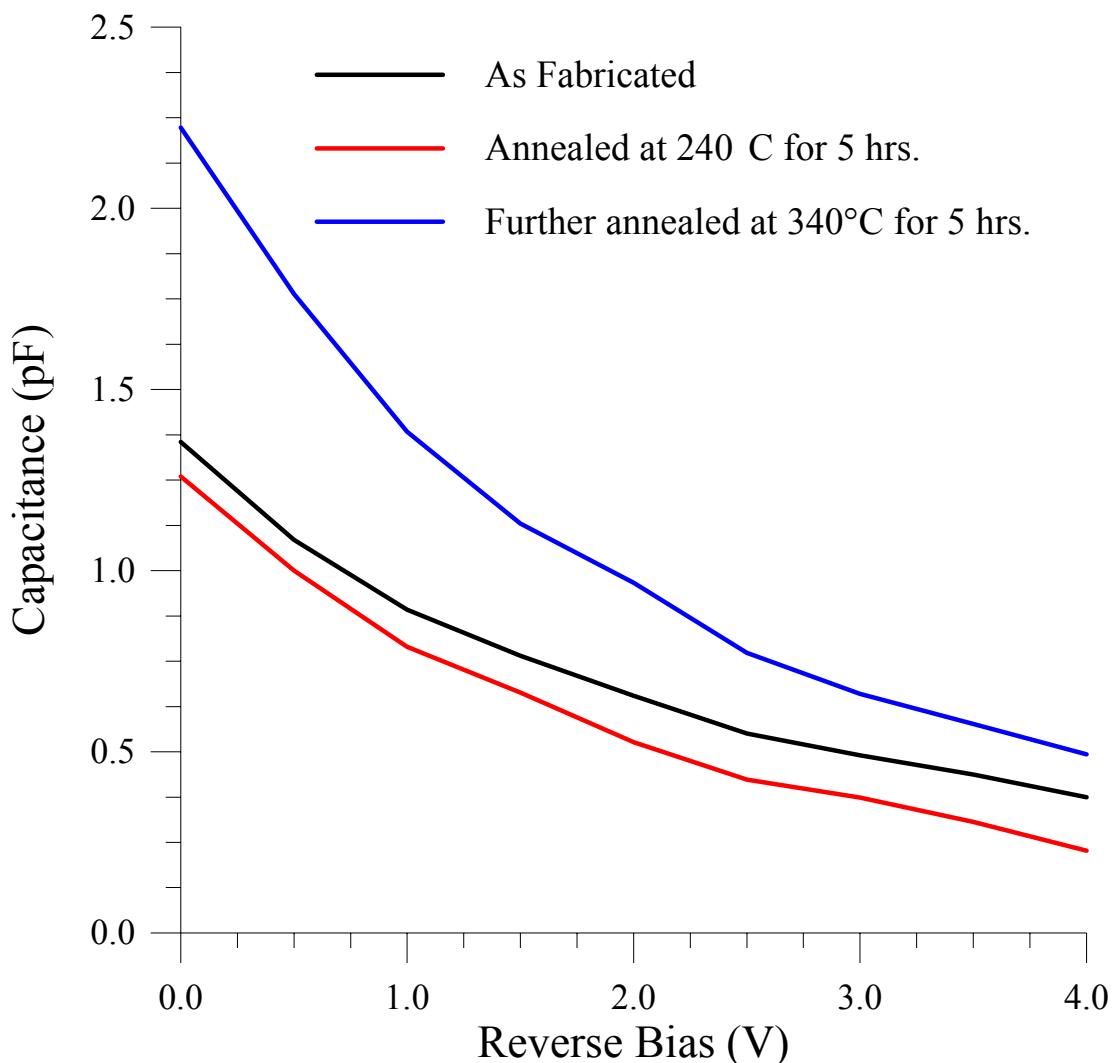


Figure 6.12: Capacitance-Voltage Characteristics for (Sample A) ITO/In/n-GaAs Schottky Diodes as fabricated and at various stages of annealing

In order to interpret this data usefully, the capacitance profile was simulated for an ideal diode with the same dimension and epitaxial doping profile. The effects of R_s and reduction in doping density, N_D , as a result of sputter damage were considered in the model. These are plotted in Figure 6.13 and Figure 6.14 respectively:

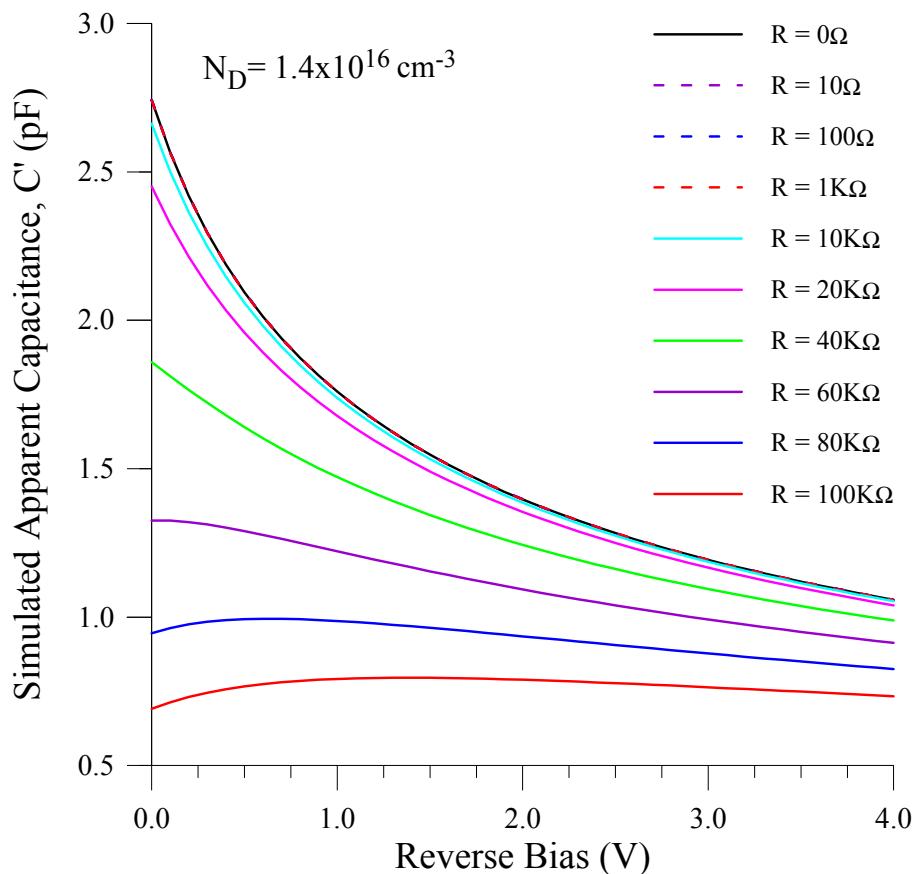


Figure 6.13: Simulation showing the effect of R_s on apparent capacitance, C'

An apparent reduction in the capacitance due to the presence of a high series resistance is a well known phenomenon in C-V profiling [172,173,174]. In the simulation, the apparent capacitance, C' , is given by:

$$C' = \frac{C}{1 + \omega^2 R_s^2 C^2} \quad (\text{eqn. 6.6})$$

where,

C = actual capacitance

ω = angular frequency in radians/second

R_s = series resistance

In the experimental and theoretical treatment of this investigation, the frequency of the a.c. test signal was 1MHz. The actual capacitance was calculated from the measured diode area and the specified doping concentration. The series resistance value was varied over the range 0 to 100K Ω .

It is seen from Figure 6.13 that a series resistance below 10K Ω has no significant effect on a diode of this specification. The I-V measurements do not show the presence of such high series resistance. Therefore, the effect of R_s alone cannot be used to explain our results.

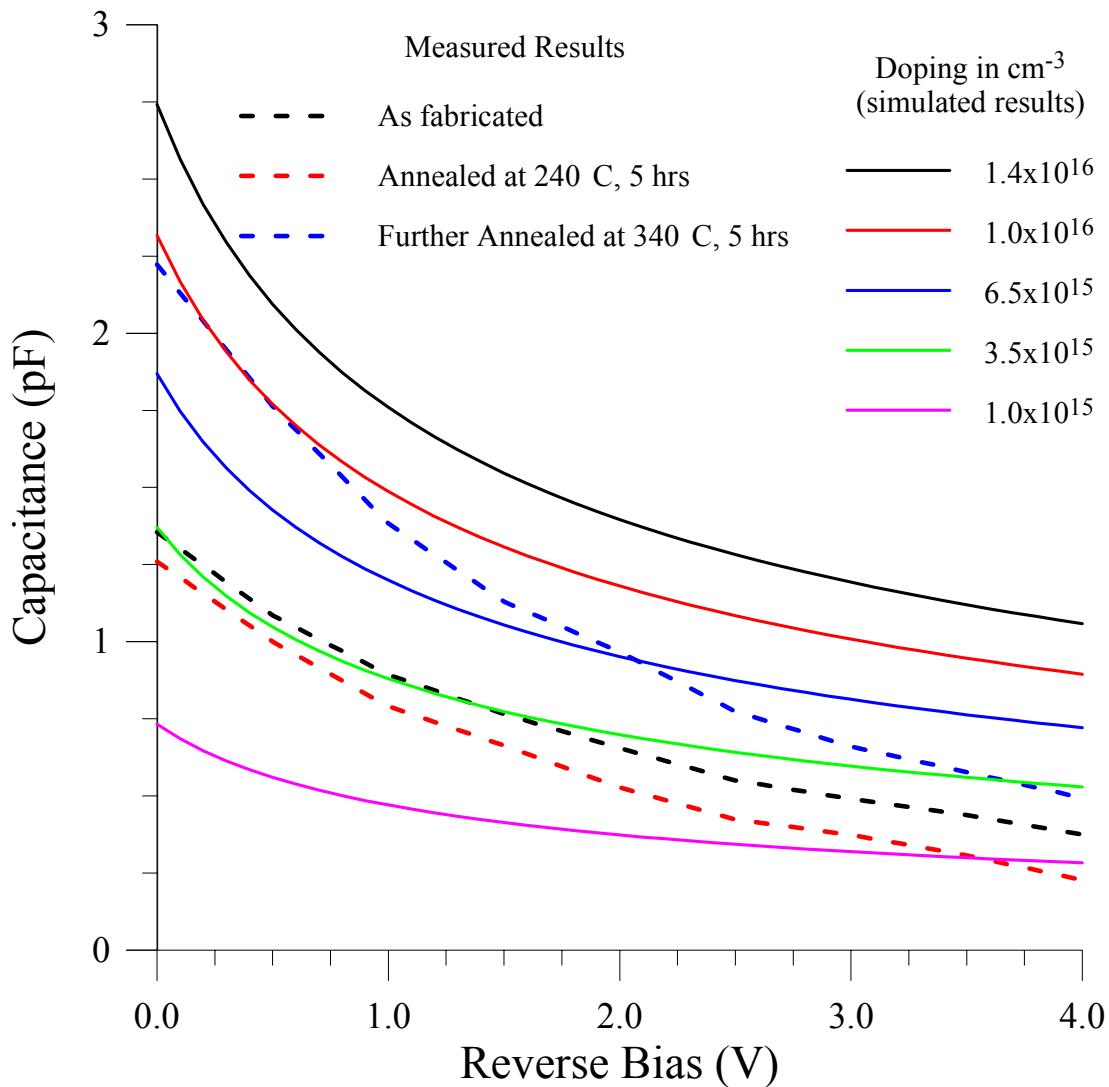


Figure 6.14: Simulation showing the effect of doping on capacitance; the measured results are superimposed for comparison

Figure 6.14 shows the simultaneous plots of measured and simulated C-V profiles for the diodes under test. From the experimental C-V data it is seen that as the reverse bias is

increased, thus “probing” further into the semiconductor layer, the doping density decreases. This is possibly due to the high velocity sputtered electrons slowing down through collision as they penetrate deeper into the GaAs layer; the impact of slower electrons deeper into the surface causes greater lattice damage and creates traps which remove free carriers. These observations are reflected in the doping profile of the diodes in Figure 6.15. The doping profile of a conventional Al/n-GaAs Schottky diode, fabricated on the same wafer by thermal evaporation of Al, is also shown for comparison.

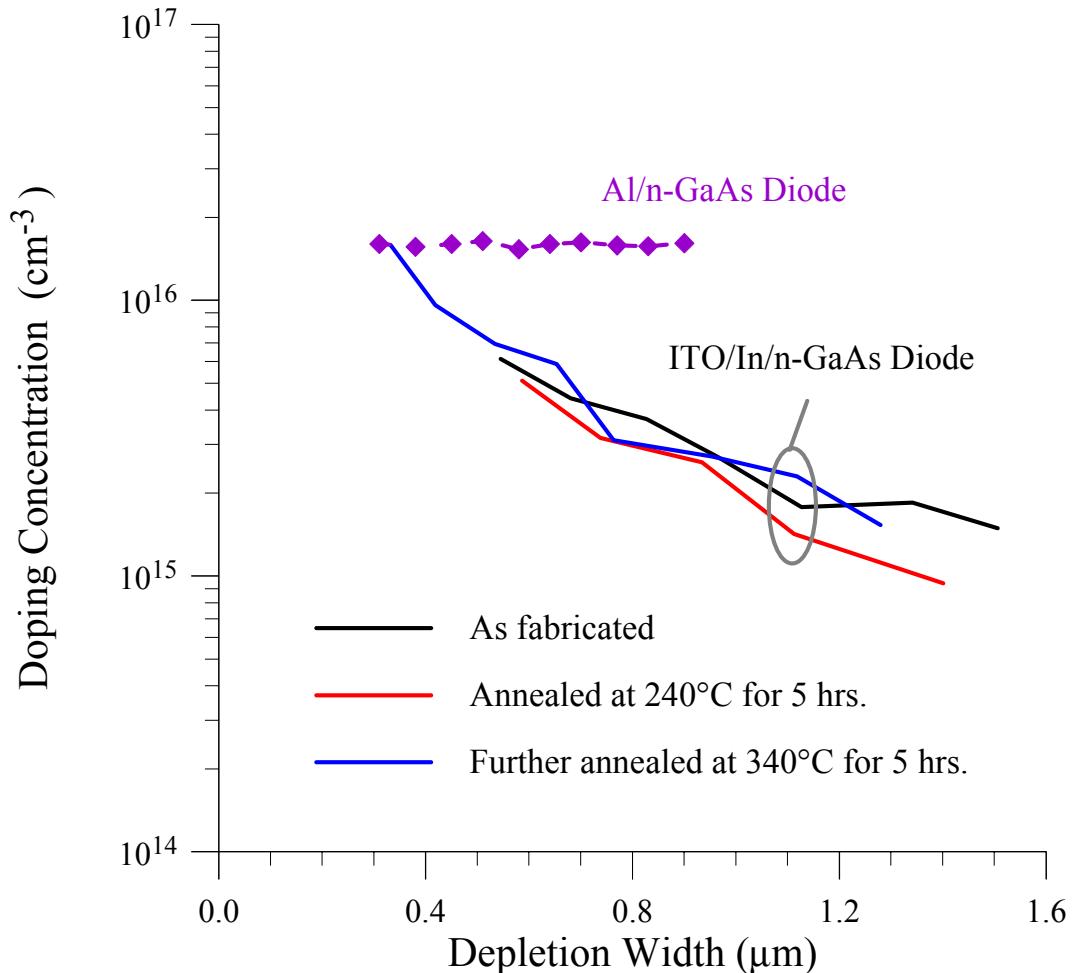


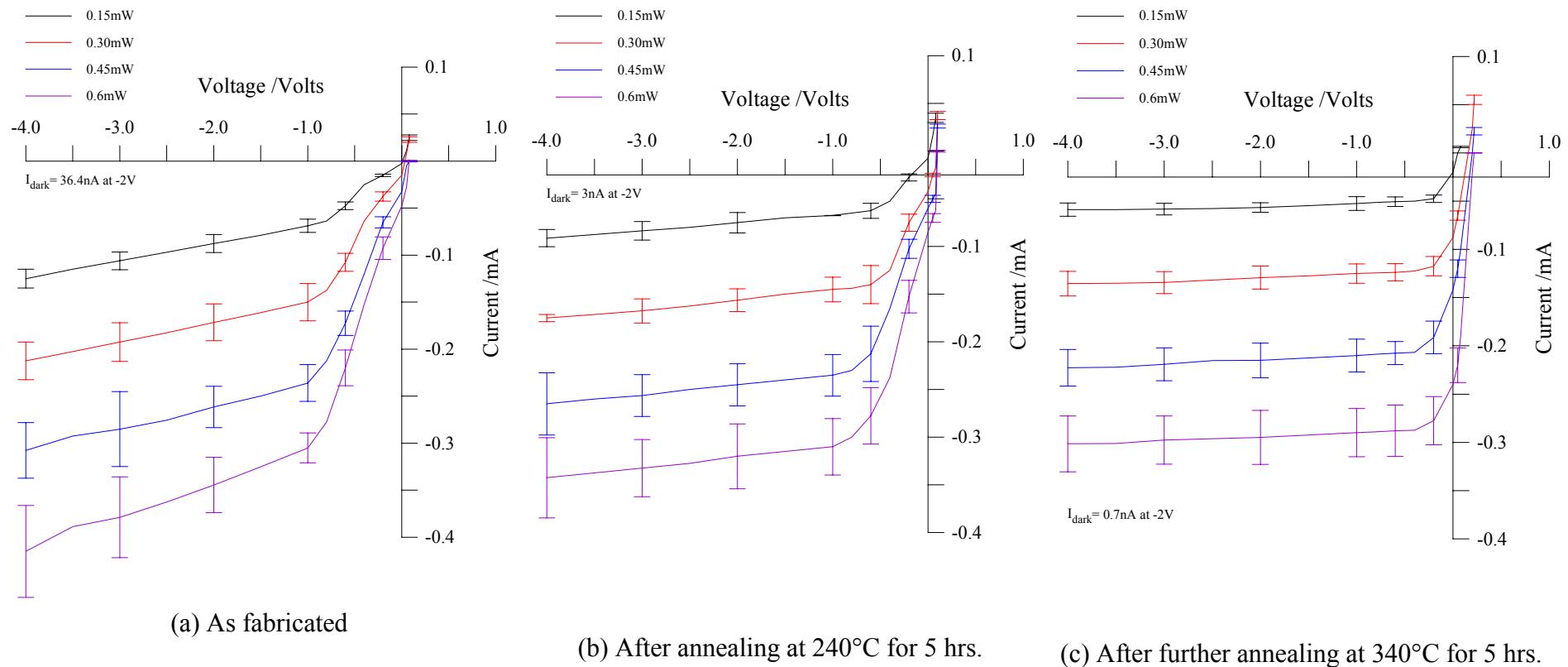
Figure 6.15: Doping profile extracted from C-V measurements for (Sample A) ITO/In/n-GaAs Schottky Diodes as fabricated and at various stages of annealing. The profile of a conventional Al/n-GaAs diode fabricated on the same wafer is shown for comparison.

From the shape of the above semi-logarithmic plot, it is seen that the sputter induced traps cause the doping profile to significantly deviate from the expected straight line (as seen for the Al/n-GaAs diode). Figure 6.15 shows that annealing at 240°C for 5 hours results in a small reduction in the overall doping profile and a corresponding increase in the depletion width. It is possible that heating at this temperature causes the sputter induced defects, which are complex to begin with, to dissociate thereby producing more active point defects. These

point defects are responsible for carrier removal from the bulk giving rise to the observed reduction in the doping profile. The final anneal at 340°C for another 5 hours gradually restores the N_D at the vicinity of the surface nearly back to nominal value of $1.4 \times 10^{16} \text{ cm}^{-3}$ for this wafer; this assumption is supported by the increase in the barrier height observed in the I-V measurements following this annealing stage.

Figure 6.16 shows the plot of photo current, I_{Ph} , as a function of reverse voltage for the ITO/In/n-GaAs Schottky diodes at various stages. It is seen that as the optical power is increased in steps of 0.15mW, there is a corresponding increase in the photo current for all three plots; these correspond to a responsivity, R , of 0.61 A/W. Following the first and second annealing stages the responsivity drops to 0.56A/W and 0.51A/W ($\eta = 80\%$) respectively. This is most likely due to the suppression of the photo-generated surface leakage current as a result of annealing as observed in the I-V plots; although it is unlikely that the actual photo-generation at the surface decreases, the amount which is able to “leak” to a terminal, and therefore contribute to the total I_{Ph} , is reduced. A related effect is that after each annealing stage the I_{Ph} curves become successively bias independent and approaches the ideal case.

In addition, the photo current plots show relatively low responsivity above a certain bias point. This region diminishes and as a result of the first annealing and completely disappears following the annealing step at 340°C. This observation further strengthens the earlier assumption of a “damaged” interface layer between the ITO film and the bulk of the GaAs epitaxial layer. At low bias, the edge of the depletion region falls within this damaged interface. Shannon *et al* have suggested the formation of a shallow highly doped surface layer as a result of sputtering [170] which can be used for explaining this observation. The highly doped layer near the ITO/In/n-GaAs interface is hard to deplete for low biases resulting in a proportional decrease in the collection of carriers which have to travel through this region either by drift or by diffusion. The induced traps may also act as recombination centres and reduce the responsivity. However, once the depletion region extends beyond this highly doped layer, it expands significantly (since doping is reduced) resulting a large increase in the absorption volume. This is reflected in the sudden increase in responsivity beyond a given bias as seen in Figure 6.16. As the sputter induced damage effect is gradually removed by annealing, an observation corroborated by the C-V profiles, there is no abrupt change in responsivity with bias and an “ideal” photo current is obtained.

Figure 6.16: Photo current vs. reverse voltage for ITO/In/n-GaAs Schottky Diodes (Sample A), $\lambda = 780\text{nm}$

6.1.2.3.2 ITO/n-GaAs Schottky Photodiodes - Sample B

Figure 6.17 shows a semi-logarithmic I-V plot of the devices on Sample B (i.e. ITO/n-GaAs diodes without the thin layer of In) at various stages. In marked contrast to the devices in sample A, the linearity of the I-V curves for this set of devices is severely clamped to a few mA by the large R_s . Following the first set of annealing at 240°C for 5 hours, the I_f decreases slightly possibly due to the corresponding reduction in the surface leakage as shown by the reverse current; there is no significant change in R_s . Further annealing for 5 hours at 340°C results in a significant reduction in R_s to 31Ω a corresponding rise in I_f , reaching nearly 100mA as shown in Table 6.9. These values are very similar to the devices in sample A.

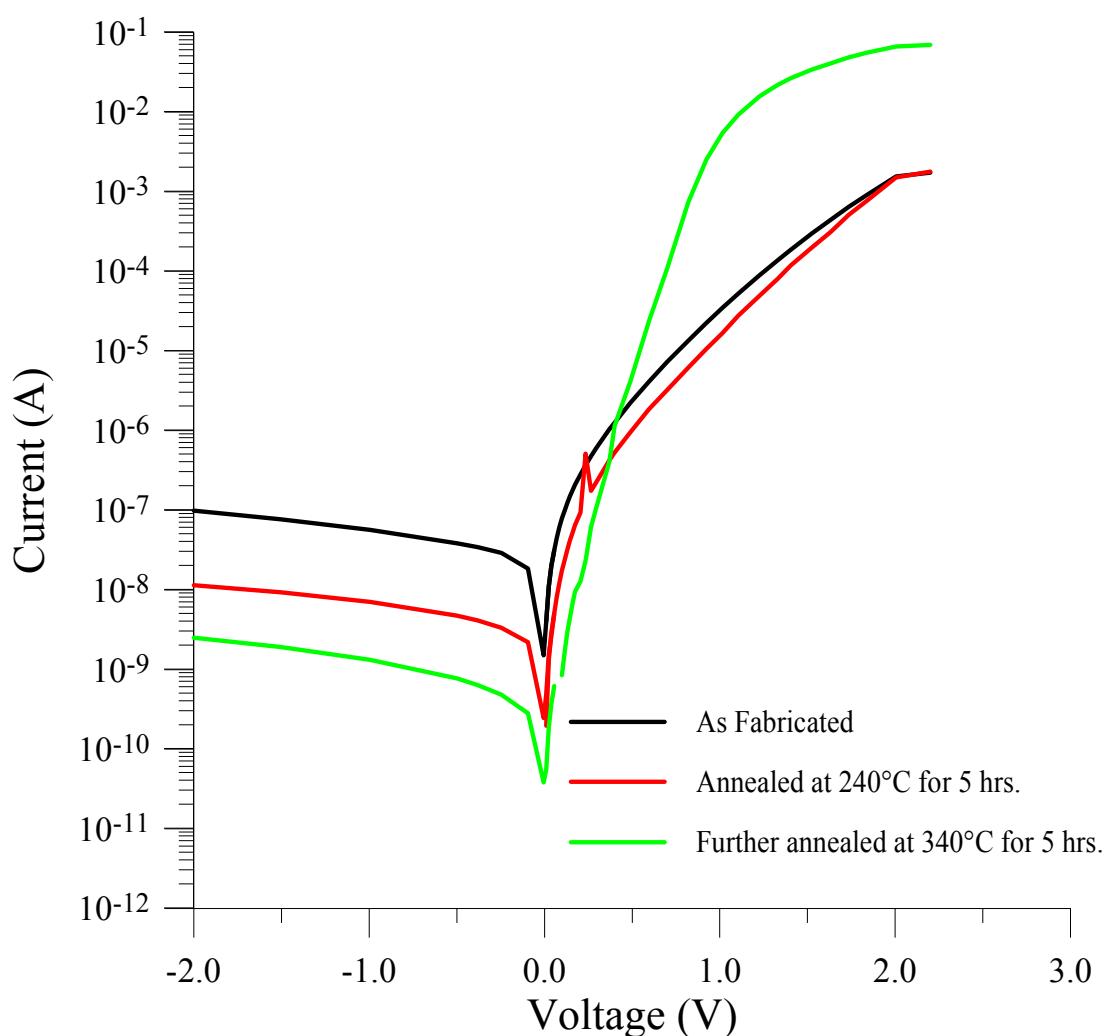


Figure 6.17 : Semi-logarithmic I-V characteristics for (Sample B) ITO/n-GaAs Schottky diodes as fabricated and at various stages of annealing

Parameter	As Fabricated	Annealed at 240°C for 5 hrs.	Annealed at 340°C for further 5 hrs.
n	1.9 ± 0.01	1.70 ± 0.02	1.51 ± 0.02
ϕ_{bo} (eV)	0.58 ± 0.01	0.63 ± 0.02	0.72 ± 0.02
R_s (Ω)	1273.3 ± 219.4	$1,205 \pm 81$	31 ± 8
I_{dark} at -2V (nA)	98.5 ± 2.24	11.41 ± 0.24	2.52 ± 0.07

Table 6.9: Effect of annealing on I-V parameters for (Sample B) ITO/n-GaAs Schottky photo diodes.

After the first annealing stage, there is a slight decrease in the ideality factor and an increase in ϕ_{bo} . The leakage current drops by nearly a decade; R_s is considerably higher than those for Sample A. This is most likely due to greater sputter induced damage on Sample B in the absence of the thin In layer which acts both as a protective and a doping layer. Following the final annealing stage, there is again a reduction in the reverse (surface) leakage current. As in the case of Sample A, the effect of sputter damage is significantly removed by the final annealing and reflected in reduced R_s as well as in the C-V and the optical measurements. The ϕ_{bo} increases to the more typical value of 0.72eV for n-GaAs Schottky diodes.

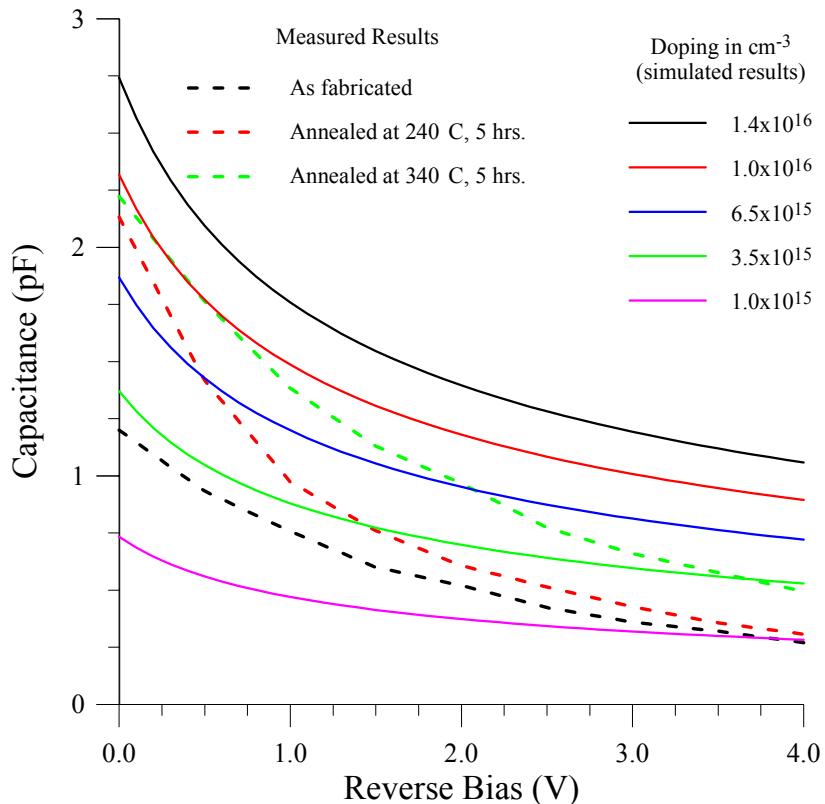


Figure 6.18: Capacitance-Voltage Characteristics for (Sample B) ITO/n-GaAs Schottky Diodes as fabricated and at various stages of annealing. Simulation showing the effect of doping on Capacitance are superimposed for comparison

Figure 6.18 shows the measured and simulated C-V profiles for Sample B. Although these are similar to those for Sample A, there are some notable exceptions: there is a marked increase in the capacitance and there is no intermediate decrease after the first annealing stage. The capacitance shows a gradual increase as a function of annealing. As before, the effect of R_s is not significant on the measured capacitance as it is well below $10\text{K}\Omega$.

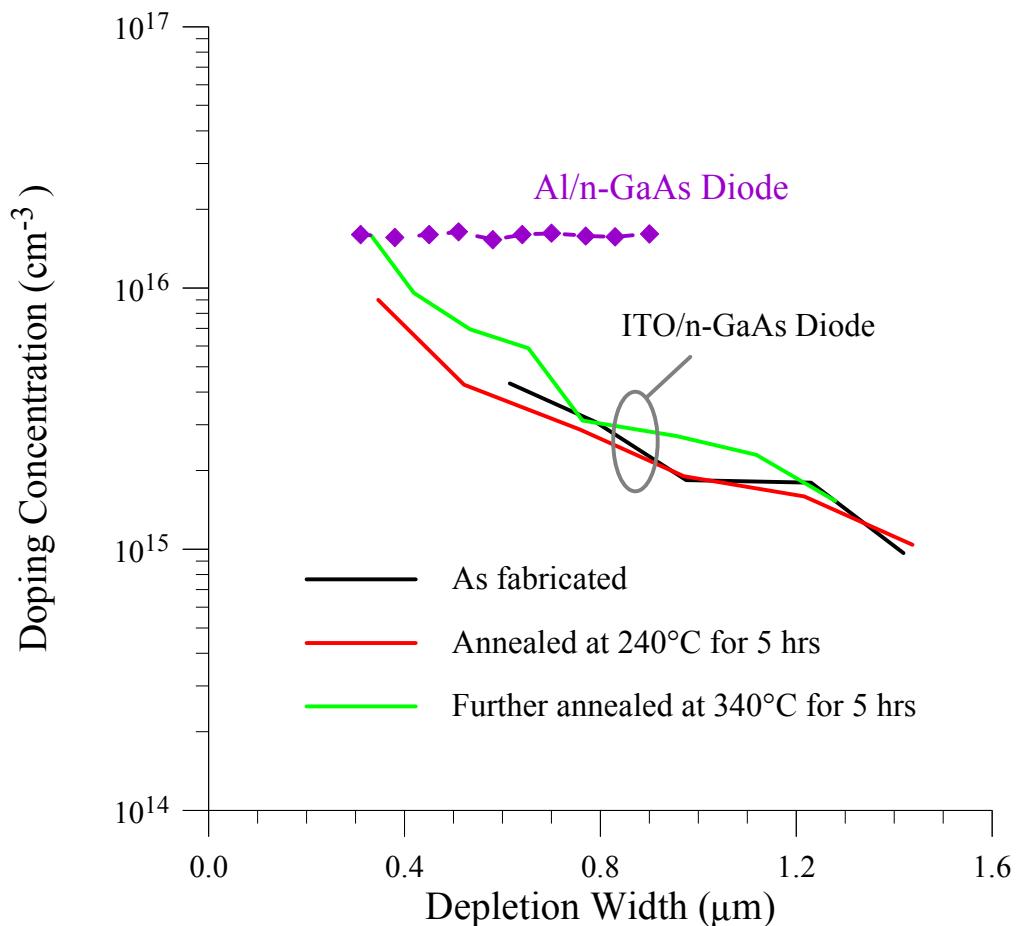


Figure 6.19: Doping profile extracted from C-V measurements for (Sample B) ITO/n-GaAs Schottky Diodes as fabricated and at various stages of annealing. The profile of a conventional Al/n-GaAs diode fabricated on the same wafer is shown for comparison.

The characteristic distortion to the shape of the doping profile due to sputtering is once again noticed. In contrast with Sample A, Annealing at 240°C has a greater effect on the doping profile of the Sample B devices as shown in Figure 6.19; recovery occurs at the surface much more readily than in Sample A. This may be due to the absence of complex defects created as a result of sputter deposition over the thin layer of indium. The final anneal at 340°C for 5 hours gradually restores the doping level near to its as grown nominal value at the surface. These observations correspond to those made by Vandenbroucke *et al* in the study of sputter deposited Al/n-GaAs Schottky diodes resulting in similar damage [167]. Similar findings have also been reported for a number of sputter-like processes by other investigators [175,176].

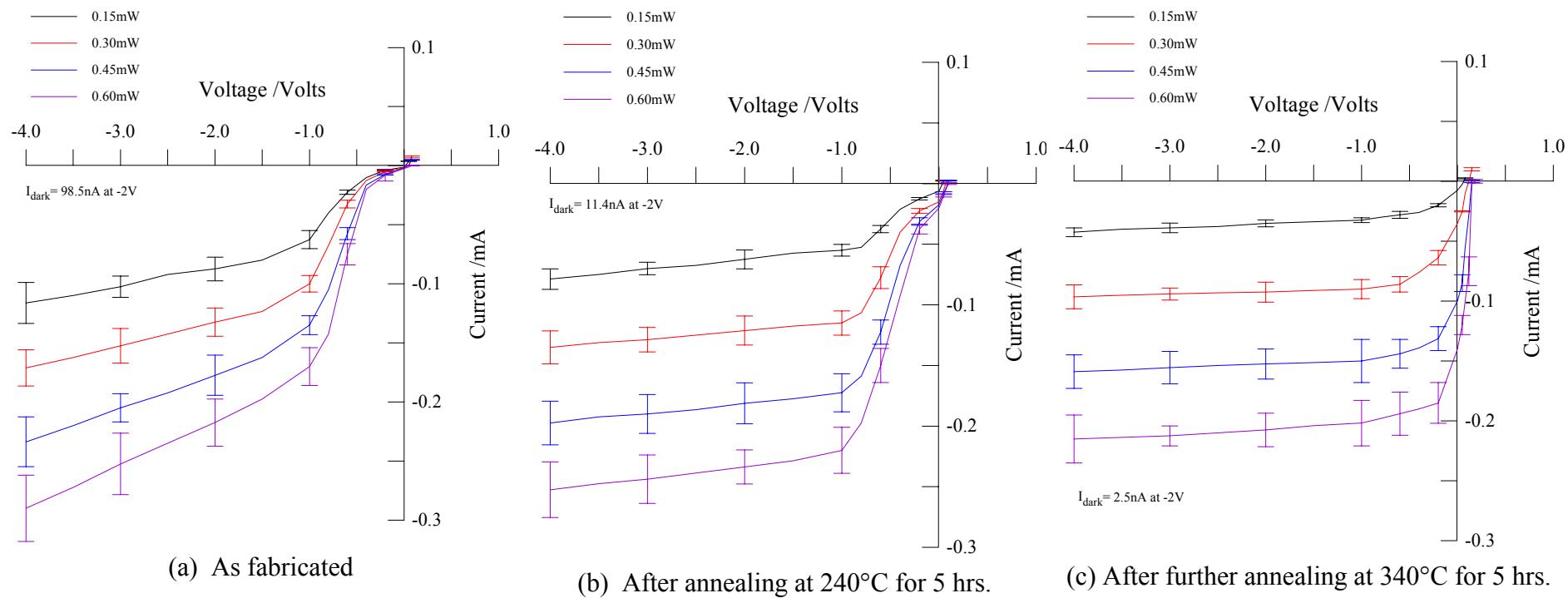


Figure 6.20 : Photo current vs. reverse voltage for (Sample B) ITO/n-GaAs Schottky Diodes, $\lambda = 780\text{nm}$,

A plot of photo current as a function of reverse voltage for the Sample B ITO/n-GaAs Schottky diodes at various stages is shown in Figure 6.20. It is seen that as the optical power is increased in steps of 0.15mW, there is a linear increase in I_{Ph} for all three plots - corresponding to a responsivity, R , of 0.4 A/W ($\eta = 64\%$). Unlike for sample A, this value of responsivity remains constant as a function of annealing. However, like the devices in sample A, the I_{Ph} becomes progressively less bias dependent as a result of the annealing. The effect of the sputter induced highly doped surface layer is more accentuated on the photo-current suggesting that the intermediate In has a protective role to play. Following the first annealing stage, there is little or no change in this damaged region; however, annealing at 340°C for 5 hours results in recovery albeit to a lesser extent than the devices in Sample A.

6.1.2.4 Discussions and Conclusion

Annealing is used to reduce the film resistivity as well as recover the damage inherent to the r.f. sputtering process. Experimental results show that higher power during sputtering helps reduce the film resistivity but results in increased damage; similar reports are also available in the literature [165]. Thus an optimum power was chosen to achieve a satisfactory value for the resistivity of the as deposited ITO film. Annealing at 240°C for 30 minutes was sufficient to reduce this to an acceptable value of $15 \times 10^{-4} \Omega\text{cm}$ from $350 \times 10^{-4} \Omega\text{cm}$. However, annealing at a higher temperature of at least 340°C for several hours was necessary to restore the effect of sputter damage on the semiconductor substrate.

Tables 6.5 and 6.6 showing the effect of annealing on ITO/n-GaAs Schottky Diodes are in apparent contradiction with the later set of devices i.e. Tables 6.8 and 6.9 respectively. The earlier set (G1 and G2) of devices were fabricated using a lower r.f. power of 70W as opposed to 150W for the latter set (A and B). Hence due to annealing there is a significant reduction in the series resistance of G1 and G2, which were very high initially. However, the other electrical parameters, such as ϕ_{bo} , dark current and the n , of these devices degrade due to annealing whereas they improve for the samples A and B. This is an anomaly in the experimental results of the former set (G1 and G2) of devices which cannot be easily explained. However, a number of possible reasons may be offered:

1. the Ni/AuGe/Ni/Au ohmic metals have a eutectic temperature of around 325°C beyond which this system undergoes a series of liquid phase reactions and forms bubbles. It is likely that some of this metal may gradually flow over the edge of the ITO and into the n-GaAs layer giving rise to pseudo ohmic behaviour resulting in lowered ϕ_{bo} , increased dark

current and n . Table 6.6 shows that no significant degradation to the ϕ_{bo} occurs due to annealing at the lower temperature of 200°C.

2. penetration of the ohmic metals through the thin layer of ITO (800Å) into the damaged n-GaAs surface. However, this is less likely to happen in practice since ITO acts as diffusion barrier.

Near ideal, ITO/n-GaAs Schottky diodes with low leakage current, low series resistance and high responsivity have been fabricated on n-GaAs epitaxial layers. The effect of mesa etching, r.f. power, use of a thin layer of indium and gradual annealing have been studied and optimised to produce near ideal photo diodes. Mesa etching significantly reduces the surface leakage current thus suppressing the dark current. Increasing the r.f. power reduces the sheet resistance of the ITO film but causes greater damage to the substrate. This damage can be minimised by depositing a thin layer of indium on the GaAs substrate prior to sputtering and it can also be removed partially by gradual annealing.

Sputtering results in a donor like effect which produces a thin but highly doped surface layer. In contrast to the work by Vandenbroucke *et al* [167] on Al/n-GaAs Schottky diodes, annealing at below 250°C was not sufficient for removing the observed effect of sputtering. Thus the higher temperature of 340°C was used.

The apparently anomalous influence of sputter damage can be reconciled if it is assumed that it consists of two separate effects:

- (a) shallow damage caused by large Argon ions
- (b) deep damage caused by high velocity electrons/smaller particles

The Argon ions in the plasma have sufficient energy to knock out Arsenic atoms from the regions close to the surface of GaAs [167]; this has the effect of releasing an extra electron which is free to transport charge. Hence the resulting Arsenic vacancies give rise to the so called “donor like effect”. However, since the Argon ions are quite large, they are unlikely to penetrate deep into the semiconductor.

The shallow damage thus introduces a thin but highly doped surface layer. The combined effect of the image force and the (increased) built-in potential, V_{bi} , causes the barrier height, ϕ_{bo} , to reduce [170]. As the damage is restored and density of free carriers at this shallow region returns to the original value, both the image force and the V_{bi} are reduced and the ϕ_{bo} assumes a value comparable to an un-damaged metal/n-GaAs Schottky diode.

The effect of the highly doped surface layer is also seen in the photo-current of the Schottky diodes. At low biases, the photo generated pairs at the edge of the (lower field) depletion region do not have a velocity sufficient to ensure that they do not recombine at the highly doped and damaged surface region. As the bias is increased, the field experienced by the photo generated pairs as they arrive at the edge of the depletion region becomes sufficiently high to ensure that no such recombination (resulting in acutely lowered photo current) takes place. Annealing restores the sputter damage and a corresponding improvement in the photo current is noticed at both low and high reverse bias.

On the other hand, electrons and possibly other smaller particles present in the plasma (such as Hydrogen, since the sputtering system is water cooled), which have high kinetic energy, penetrate deeper into the semiconductor surface. Because of their high velocity, they do not undergo inelastic collision and therefore to not cause any significant crystal damage. However, as they penetrate deeper, they lose their kinetic energy and slow down. At this stage they are able to transfer a large portion of the remaining energy through inelastic collision causing greater crystal damage. The damage manifests itself by effectively introducing more and more trapping centres deeper into the semiconductor which give rise to progressive reduction in the density of free carriers as evidenced in the observed CV profiles for Samples A and B. At a certain depth, the majority of the high energy incident particles, having transferred all their energy, will not penetrate further. Therefore, it is expected that the free carrier density profile would then recover to the original value for the undamaged wafer at a point (several microns) deeper still into the substrate [177]. This phenomenon requires further detailed study and is not within the scope of this research.

The barrier heights obtained for the ITO/n-GaAs Schottky diodes in this study lie in the range 0.76 (for high r. f. power of 150W) to 0.85eV (for low r. f. power of 70W); in addition to being comparable to thermally evaporated metal/n-GaAs diodes, these match closely with the values obtained by Aliyu *et al* [178] who fabricated ITO/n-GaAs diodes by sputtering (0.76eV) and Balasubramanian *et al* [179] who fabricated ITO/n-GaAs devices by thermal evaporation (0.83eV). This illustrates that the effect of sputtering induced donor like properties is reduced at lower powers.

In comparison with opaque or ITO/n-GaAs Schottky diodes in the literature [72,73] which have R_s values up to 190Ω and η in the range 19% - 32%, devices with very low R_s of 25Ω and high η of 80% were realised in this study. By shrinking the active region, high speed devices can be achieved; parasitic capacitances and leakage currents can be reduced by a combination of proton bombardment and mesa etch isolation techniques. These comparisons are summarised in Table 6.10:

Photo Diode	Fabrication Method	$R_s [\Omega]$	$\phi_{bo} [\text{eV}]$	$\eta [\%]$	Ref.
ITO/n-GaAs	r.f. sputtering	25	0.80	80	This work
ITO/n-GaAs	r.f. sputtering	-	0.76	-	[178]
ITO/n-GaAs	r.f. sputtering	110	0.85	32 (70 [*])	[70]
Ni/p-InGaAs	Thermal evaporation	190	-	19	[72]

Table 6.10: Comparison of ITO/n-GaAs Schottky photo diodes from this study with similar devices reported in the literature.

* The value of η in brackets for ITO/n-GaAs diodes in reference [70] is the estimated quantum efficiency for these devices adjusted to reflect a structure with a total absorption width of $1.75\mu\text{m}$ (i.e. identical to those fabricated in this study) instead of being $0.5\mu\text{m}$. As mentioned earlier, a shorter absorption width enhances device speed but reduces the absorption. This adjustment provides a better comparison as far as the quantum efficiencies are concerned. Recall that the inherent trade-off between the η and the speed of a photo detector was discussed in section 2.5 and demonstrated in Table 2.3 in section 2.5.9.

6.1.3 Richardson Constant for the ITO/n-GaAs Contact

Detailed reports on ITO growth techniques and its electrical and optical properties are currently available in the literature, mainly so on Si [180] and p-type InP [171] semiconductors and some on n-GaAs. However, in order to model such a junction for predicting device characteristics, it is necessary to understand the properties of the ITO/semiconductor Schottky junction and to determine the modified Richardson constant, A^{**} . In this section the A^{**} for sputter deposited ITO/n-GaAs Schottky barrier is determined from I-V measurements carried out over a wide temperature range.

6.1.3.1 Results and Discussion

The fabrication detail was presented in the section 6.1.2. The devices with ITO deposited on n-GaAs (wafer no. GB445) at a relatively low power of 70W was used because the extent of sputter induced damage is likely to be low. Recall that these ITO diodes had near ideal Schottky barriers ($n < 1.08$) and low dark currents (at -2V, 300K $I_{dark} = 8.7\text{nA}$). The optical sensitivity, using a 630nm incident beam, was found to be 0.4A/W ($\eta = 80\%$). However, the series resistance for these devices were rather high as discussed earlier. This is clearly evident in the forward biased I-V plots for these devices over the entire temperature range as shown in Figure 6.21:

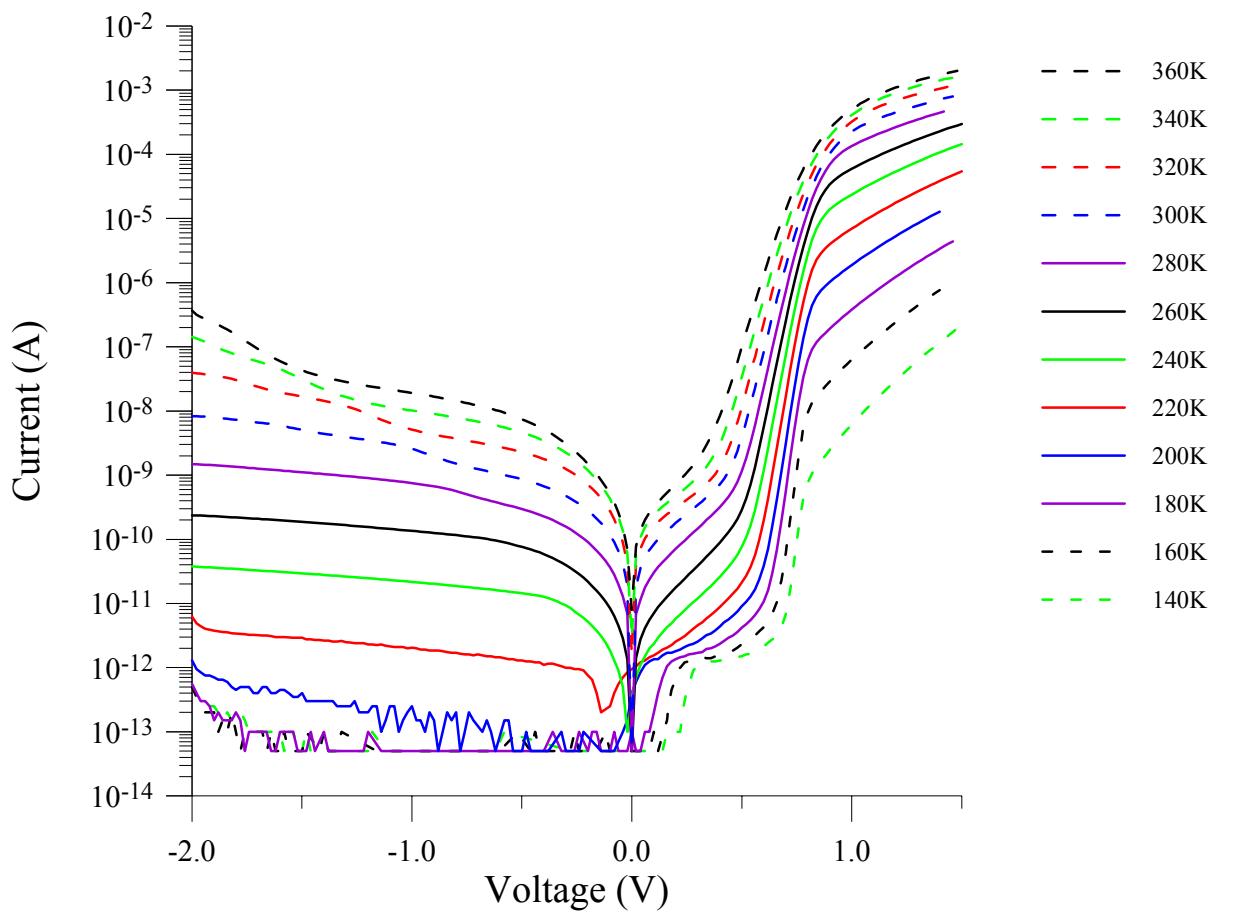


Figure 6.21: Measured I-V characteristics of ITO/n-GaAs diodes over a wide temperature range

In comparison with the Au/n-GaAs diodes fabricated on the same wafer (as shown in section 6.1.1), the reverse current increases rather more rapidly at high temperatures for the ITO/n-GaAs diodes. Furthermore, this current is bias dependent suggesting the increase is mainly due to surface leakage effects.

The Arrhenius plot extracted from the I-V measurements over the 360K-140K temperature range is shown in Figure 6.22. Over this range, the fit to the experimental data shows a good linear fit suggesting the dominance of thermionic emission current transport mechanism. However, below this range, the transport mechanism is believed to be dominated by a combination of tunneling and generation-recombination mechanisms as a linear fit is no longer possible.

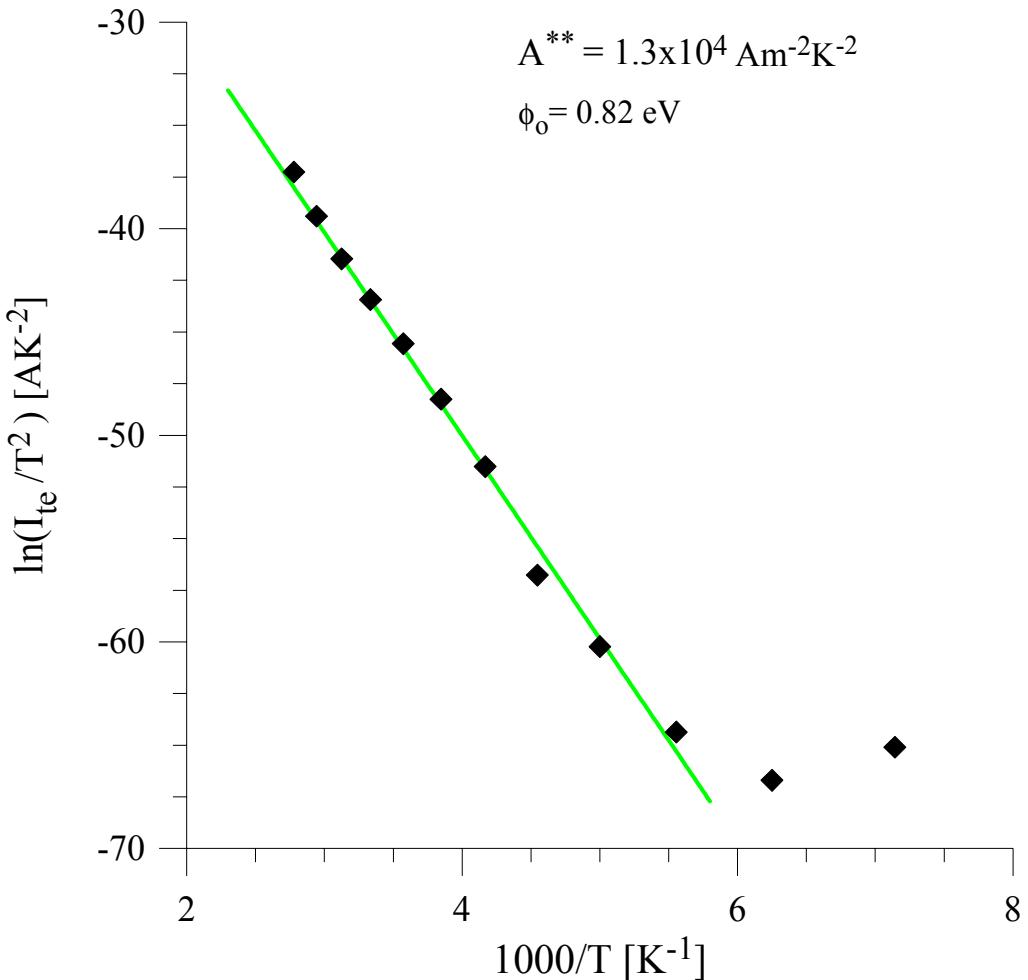


Figure 6.22: Arrhenius plot of $\ln(I_{te}/T^2)$ versus $10^3/T$ showing the temperature dependence of thermionic emission current in the ITO/n-GaAs Schottky diode.

The barrier height extrapolated from the slope of this linear fit indicates a ϕ_{bo} of 0.82eV. These results are similar to those obtained for the $\text{In}_2\text{O}_3/\text{n-GaAs}$ [181] and ITO/p-InP [171] Schottky junctions as well as those reported for ITO/n-GaAs diodes [178,179]. From the y-axis intercept, the modified Richardson constant, A^{**} for ITO/n-GaAs is calculated to be $1.3 \times 10^4 \text{ Am}^{-2}\text{K}^{-2}$. As shown in Table 6.11, this value is closer to the Al/n-GaAs Schottky diodes rather than the Au/n-GaAs devices fabricated in the course of this investigation.

Diode	Ideality factor, n	ϕ_{bo} [eV]	A^{**} [$\text{Am}^{-2}\text{K}^{-2}$]
ITO/n-GaAs	1.08	0.82	1.3×10^4
Al/n-GaAs	1.08	0.77	16.0×10^4
Au/n-GaAs	1.04	0.84	12.5×10^6

Table 6.11: Summary of the various properties of the Schottky diodes fabricated in this study.

The Richardson constant for GaAs in free space, A^* , is quoted as $1.2 \times 10^6 \text{ Am}^{-2}\text{K}^{-2}$ [23]. These results suggest that electron transport for the Au/n-GaAs diodes is much more efficient than in Al/n-GaAs and sputter deposited ITO/n-GaAs Schottky diodes. The low value for the latter Schottky contact may be due to the sputter induced damage.

6.1.4 Realization of Transparent Gate HEMT Using ITO

The basic theory behind optically controlled FET devices [74,75] was introduced in section 2.5. In this study, novel pseudomorphic HEMTs (pHEMT) with a transparent gate (TG-HEMT) were fabricated using transparent indium tin oxide for the first time. The gate of such a device is essentially a Schottky contact. The bulk of this particular work carried out in collaboration with a fellow researcher, A. Khalid and a detailed discussion will be available in his Ph.D. thesis. The objective of this section is thus to demonstrate that novel working devices were realised as a result of extending the work on ITO/n-GaAs Schottky diodes [79,182].

6.1.4.1 Fabrication

The epitaxial layers for these pHEMT devices were grown by MBE on a semi insulating GaAs substrate. Figure 6.23 shows a schematic diagram of transparent-gate HEMTs with ITO Schottky contact fabricated on this wafer:

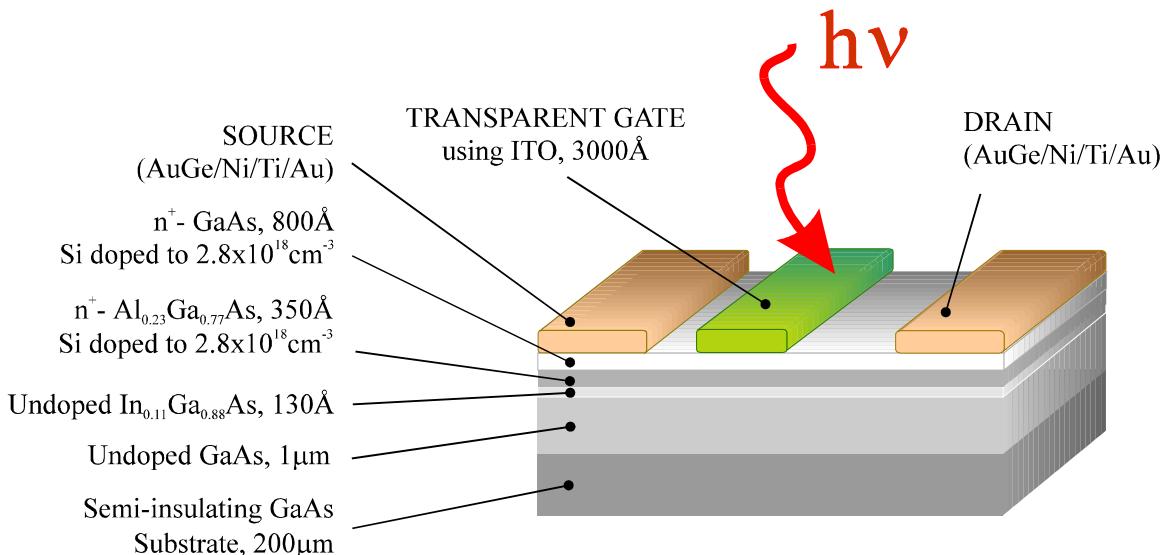


Figure 6.23: A schematic diagram of transparent-gate HEMT with ITO Schottky contact.

The fabrication procedure was carried out using standard photolithography steps. Initially, the wafer was mesa etched to the S.I. GaAs substrate for device definition. Ni/AuGe/Ni/Au metalisation were thermally deposited on the n^+ -GaAs cap layers and annealed to form good contacts to the source and the drain terminals. The wafer was then divided into two parts: the first part used for fabricating opaque gate contact devices with a Ti/Al (200Å/3000Å) metalisation; the other part was used for TG-HEMT fabrication. The entire surface of the second part of the wafer was coated with 3000Å of ITO by reactive r. f. sputtering. Because of the difficulties associated with defining near micron patterns on ITO by wet etching, the dry etching technique involving RIE with an Al mask was used. Hence, Al metal mask for gate definition was then evaporated. This was followed by RIE patterning of ITO to form the transparent gate. In both opaque and transparent devices, the gate dimension was $5 \times 100 \mu\text{m}^2$ and the source-to-drain separation was $7\mu\text{m}$. Appropriate annealing was carried out to remove any sputter induced damage.

6.1.4.2 Results and Discussion

A comparison of the optical responsivity of the opaque and transparent gate HEMTs in Figure 6.24 clearly demonstrates the greater coupling efficiency due to the ITO gate contact in the latter devices.

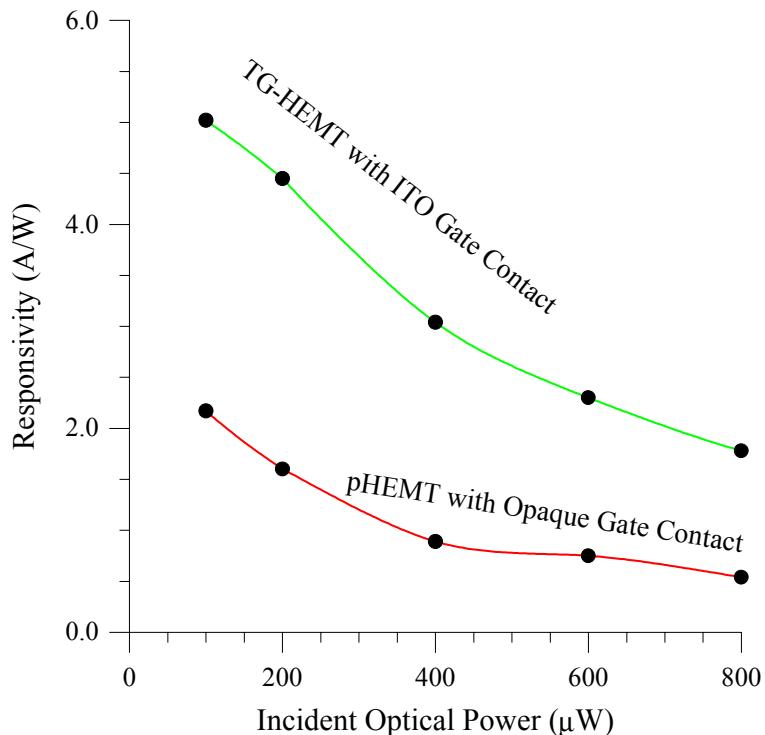


Figure 6.24: Comparison of the optical responsivity of a TG-HEMT and pHEMT measured at $\lambda = 780 \text{ nm}$; $V_{gs} = -0.15 \text{ V}$ and $V_{ds} = 3 \text{ V}$. (After A. H. Khalid, S. A. Bashar and A. A. Rezazadeh [79])

The measured optical responsivity of the TG-HEMT devices was in excess of 5A/W corresponding to an external quantum efficiency, $\eta > 800\%$ for 780 nm incident radiation. It is also seen that the responsivity in both sets of devices tends to saturate at high optical powers. This is most likely due to the very thin absorption volume afforded to the vertically incident optical waves.

As discussed in section 2.5, optical control in these advanced heterojunction devices is achieved by means of either a photo-voltaic or a photo-conductive effect [78] depending on where the majority of the photo-generation takes place; photo current under the gate giving rise to a photo voltage effectively reduces the channel width and can be used for the desired optical control. Using a transparent ITO gate enhances this control. On the other hand, photo generated pairs in the channel will effectively increase its conductivity and add to the drain current.

6.2 Devices Based on ITO Ohmic Contacts

6.2.1 ITO Ohmic Contacts to n⁺ and p⁺ Epitaxial Layers

The advantages associated with using a practically transparent and highly conductive layer of Indium Tin Oxide (ITO) to form the metal/semiconductor junction were discussed in one of the earlier sections. Similarly, transparent conducting electrodes with ohmic properties promise to enhance the performance of surface light emitting or detecting compound semiconductor devices [183,184]. These include heterojunction photo-transistors (HPTs), light emitting diodes (LEDs) and vertical cavity surface emitting lasers (VCSELs).

In this section the optimisation of the fabrication process necessary to produce such transparent contacts with good ohmic properties is discussed. In contrast with ITO/n-GaAs rectifying junctions, the substrates used for ohmic contact formation have doping densities which are several orders of magnitude higher. In addition, there are distinct differences in the post deposition annealing conditions for the ITO ohmic contacts. This dual property of ITO forming either a rectifying or an ohmic contact has also been reported by Kellet *et al* [142]. The transmission line model (TLM) theory is used to evaluate and compare the properties of the ITO/semiconductor ohmic contacts.

6.2.1.1 Contacts to Highly Doped GaAs Epitaxial Layers

ITO was deposited on highly doped GaAs epitaxial layers to study the ohmic properties of the ITO/(n⁺ or p⁺) GaAs interface. In addition, the effect of a thin layer of Indium between the ITO film and the n⁺-GaAs substrate was also examined. Thin layers of metal have been used by previous researchers to achieve superior ohmic contacts between transparent films and semiconductors: Lawrence *et al* used this scheme in the fabrication of cadmium tin oxide (CTO) and ITO contacts to GaAsP surface emitting LEDs [183]; an intermediate layer of thin silver (50 to 100Å) was used by Tu *et al* in the fabrication of VCSELs with CTO contacts [184] and more recently, Li *et al* [96] have used a thin intermediate metallic layer in the fabrication of AlGaAs/GaAs HBTs with transparent ohmic contacts. However, there is no formal study of its effect on the contact using the TLM method.

6.2.1.1.1 Fabrication and Post Deposition Annealing

The GaAs samples used in these experiments consisted of a S. I. GaAs substrate with MOCVD grown n⁺ or p⁺ epitaxial layers; the n⁺-GaAs layers were generally obtained from N-p-n AlGaAs/GaAs HBT wafers by removing all layers except the highly conductive n⁺ sub-collector using appropriate chemical etchants. The fabrication procedure for the n⁺ and p⁺ ITO/GaAs ohmic contacts are identical. However, there are some modifications to the usual fabrication procedure for the ITO/In/n⁺-GaAs ohmic contacts which are described later. Typical values for doping and thickness of the highly doped layers are summarised in Table 6.12:

Sample	Doping [cm ⁻³]	Thickness [nm]	Substrate
n ⁺ GaAs	5x10 ¹⁸	1000	400μm S.I. GaAs(undoped)
p ⁺ GaAs	5x10 ¹⁹	1000	400μm S.I. GaAs(undoped)

Table 6.12: Typical values for doping and thickness of the GaAs samples used for appraising ITO ohmic contacts.

TLM patterns were defined using photolithography and a lift-off process. At first, wet chemical etching was used to define the required mesas on n⁺ or p⁺ on the respective S. I. GaAs substrates in order to confine the current. Indium metal pads were deposited by thermal evaporation and lift-off process on the samples for studying the effect of a thin layer of Indium between ITO and the n⁺-GaAs layers; the thickness of the indium metal pads was approximately 100Å.

Prior to loading the samples into the sputtering chamber, these were cleaned in a 1HCl : 1H₂O solution for one minute; this treatment was found to improve adhesion of ITO films to the substrate. The samples with Indium metal pads were not treated in this manner because Indium is easily removed by the HCl solution. Balasubramanian *et al* [179] have reported the use of a layer of apiezon wax to protect indium back contacts in the fabrication of ITO/GaAs Schottky diodes; the wax was removed by a brief dip in tricholoroethylene (TCE). However, their method of protecting the In metal is not compatible with the fabrication process involved here.

In the next step, ITO was deposited on the entire surface of the samples by reactive r.f. sputtering in a Ar/O₂ plasma using the Nordiko 1500 system. The conditions for ITO deposition were as follows: base pressure = 1×10^{-6} torr, total pressure during sputtering = 5×10^{-3} torr, partial pressure of oxygen, P_{O₂} = 7.3×10^{-3} , r.f. power = 150W, pre-conditioning time = 30 minutes, and the deposition time = 30 minutes. These conditions produced ITO films which were approximately 3000Å thick.

Following sputtering, further photolithography was used to deposit the TLM patterns by sequential thermal evaporation and lift-off process on the ITO films covering the conductive mesas; the TLM pads were (50 x 100) μm^2 and had linear spacings of 10 to 70 μm between them. The metalisation scheme used was Ni/AuGe/Ni/Au. The fabrication steps for the samples without the In layer were completed by removing the unwanted ITO by using the metal pads as a mask for wet chemical etching in HCl. Figure 6.25a and b show a schematic diagram of the fabricated ITO/n⁺ GaAs and ITO/In/n⁺ GaAs ohmic contacts respectively :

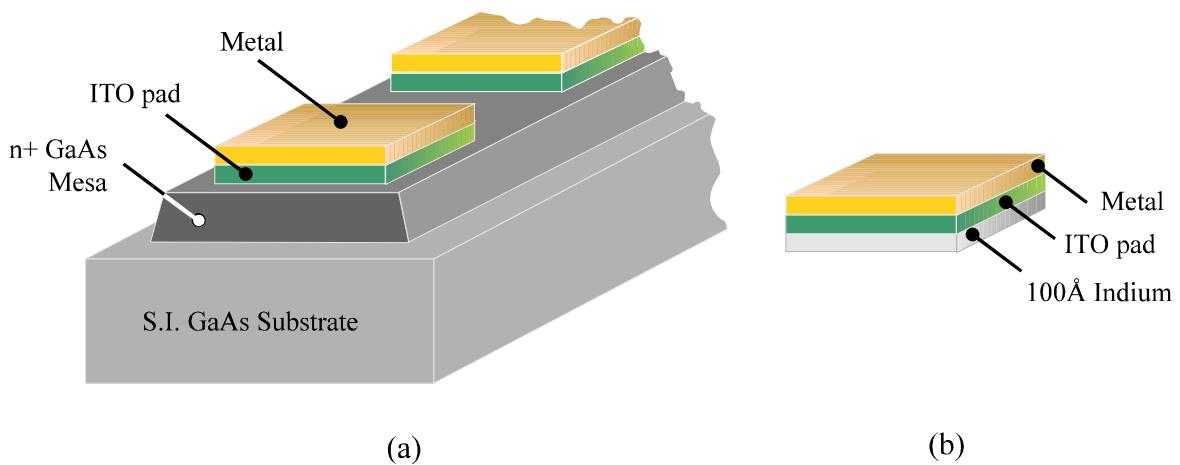


Figure 6.25: Schematic diagram of an ITO ohmic contact to n⁺ GaAs layer; (a) shows part of such a contact fabricated for TLM measurements while (b) shows the addition of a thin layer of Indium between the ITO and the conductive layer.

In case of the ITO/In/n⁺-GaAs ohmic contacts, wet chemical etching was not suitable for the reasons described earlier. In addition, it was evident that the dry etch rate of Au was greater than that of ITO and therefore the Ni/AuGe/Ni/Au metal pads were unsuitable as a mask. Therefore a 1500Å thick layer of Al, which has a much slower etch rate in the Ar plasma than either the ITO or Au, was used as the final metal on top of the Au. This allowed the required dry etching of the unwanted ITO with Al as the protective mask. The conditions for the RIE in Ar were as follows: pressure = 1.2×10^{-2} torr, Ar flow rate = 55 and r. f. power = 100W, etch time = 15 minutes.

Following fabrication of the required TLM patterns, the contacts were annealed using various methods:

- a) heat treatment under forming gas ambient in a tube furnace for temperatures ranging from 400°C to 500°C for periods of up to 30 minutes
- b) heat treatment under a nitrogen ambient in the rapid thermal annealer at 500°C for 30 to 90 seconds

After each treatment step, the I-V characteristics of two adjacent TLM pads were plotted on the HP4145B SPA to monitor the effect. Although the series resistance, R_s , of the contacts decreased, the plots continued to demonstrate “Schottky-like” behaviour at low voltages as shown in Figure 6.26.

It is seen from Figure 6.26 that the R_s of the ITO contacts reduce as a result of the conventional annealing techniques. This can be attributed to a number of factors which include the reduction in the resistivity of the ITO film and recovery of sputter damage in the GaAs epitaxial layer. The breakdown voltage of the highly conductive mesa layer was seen to have increased from 6V (typical for $N_D = 10^{18} \text{ cm}^{-3}$) to a few kV following sputtering; annealing at 400°C for 30 minutes reduced this value to approximately 20V - typical for a doping density of mid 10^{16} cm^{-3} . Although some recovery is evident, as expected from earlier work on Schottky contacts annealed at 340°C, full damage restoration has not occurred. Thus a rectifying behaviour typical of an ITO/n-GaAs with 10^{16} cm^{-3} doping was observed due to a barrier at the ITO/semiconductor interface. Comparable results were also obtained by the rapid thermal annealing (RTA) technique. It is assumed that short annealing is insufficient to cause any significant changes to the sputter damaged layer. Cunningham *et al* [185] have reported similar retainment of rectifying behaviour of Indium Oxide contacts to relatively lowly doped ($N_D = 10^{17} \text{ cm}^{-3}$) GaAs substrates despite RTA at temperatures reaching 700°C.

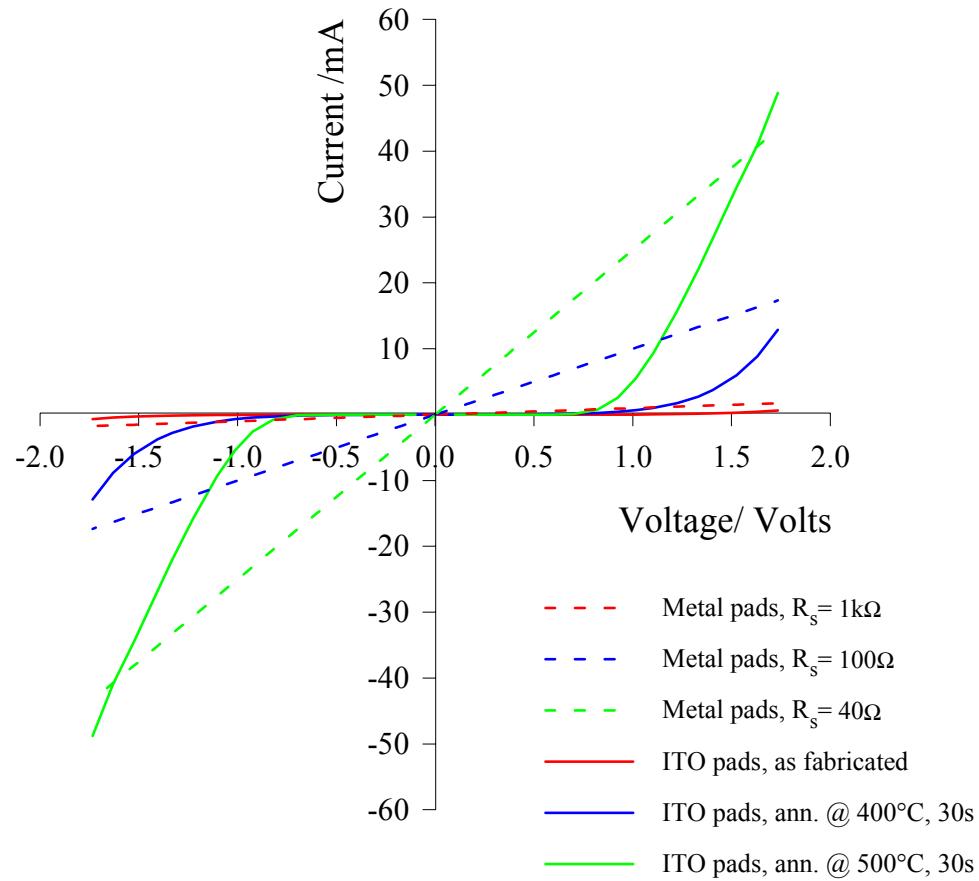


Figure 6.26: Typical I-V plots for two adjacent TLM pads with ITO contacts (solid lines) and metal contacts (dotted lines) as a result of annealing by conventional methods

Hence a “step-wise” annealing procedure was adopted to produce “linear” ohmic behaviour similar to the metal/GaAs contacts. The actual annealing scheme involves a step-like sequence as shown in Figure 6.27. Annealing was carried out in the tube furnace in a forming gas ($10\%\text{H}_2 + 90\%\text{N}_2$) ambient. The maximum temperature applied at each stage was approximately 500°C .

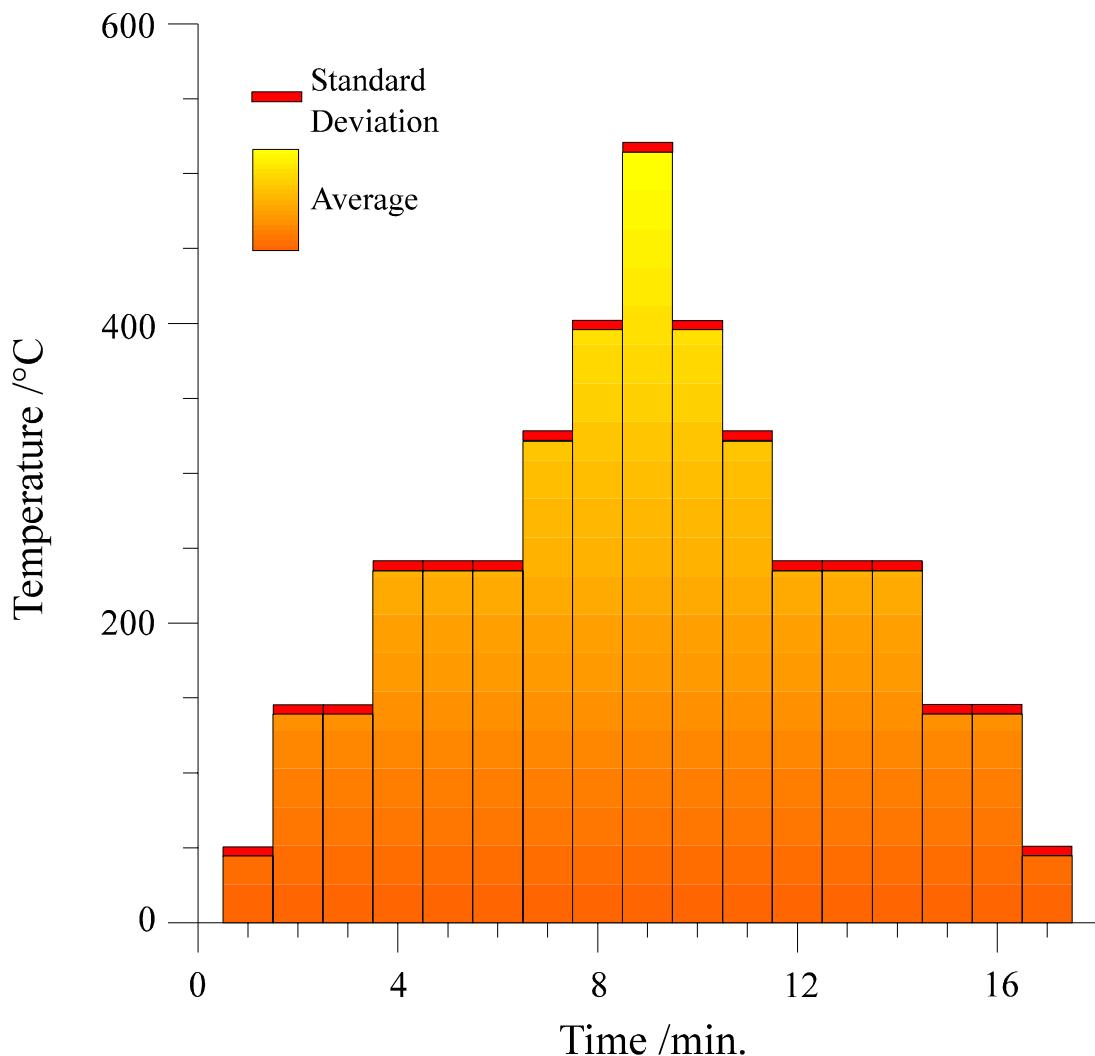


Figure 6.27: Bar chart showing the annealing sequence of the ITO/semi-conductor contacts; the average temperature and the standard deviations are plotted versus time.

The effect of high temperature annealing to the ITO films was discussed in section 5.3; it was shown that there is a minimal change in transparency due to the annealing treatments. The addition of a 100Å thick layer of In between the ITO and the conductive mesa (as shown in Figure 6.25b) is expected to reduce the effective transparency of the ohmic contact. In order to determine this effect, a 100Å layer of In was thermally evaporated on a microscope glass cover slide; the required thickness of ITO film was then deposited by reactive r.f. sputtering. Figure 6.28 shows the results. It is seen that although the transmittance of the composite film is significantly reduced from 90% to approximately 75%, this is restored to the original value after the first annealing stage.

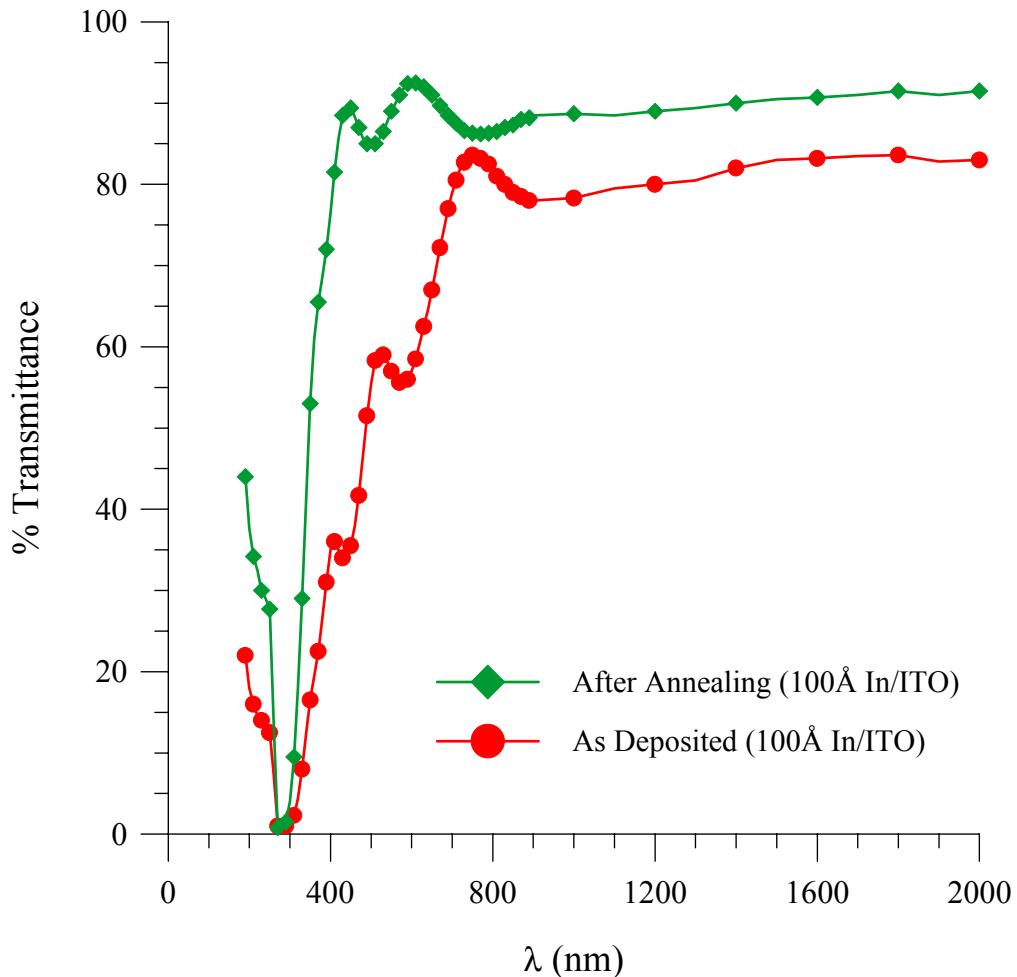


Figure 6.28: Effect of a 100 \AA thick layer of In between the glass and ITO on the transmittance

Finally, a set of TLM mesa/pad structures were prepared using conventional metal pads on the respective n⁺-GaAs and p⁺-GaAs mesas for comparison. These were identical in size and spacing to the ITO-TLM patterns. For the n-type contacts, the following metalisation scheme was achieved by sequential resistive thermal evaporation of Ni (50 \AA)/ AuGe (300 \AA)/ Ni (100 \AA)/ Au (1000 \AA) without breaking the vacuum; for the p-type contacts, Au (300 \AA)/ Zn (300 \AA)/ Au (1000 \AA) was deposited in a similar manner. Following photolithography and prior to loading in the evaporation chamber, the samples were chemically cleaned in 10% HCl for 15 seconds. Both these sets of contacts were annealed at 400°C for 30 seconds using RTA in N₂ ambient.

6.2.1.1.2 Results and Comparison with conventional Contacts

The TLM theory and setup has been discussed in section 4.1. Recall that the specific contact resistance, ρ_c , calculated using the contact end resistance, is given by:

$$\rho_c = \frac{R_c^2 w^2}{R_{sk}} \quad (\text{eqn. 6.7})$$

where

R_c = contact resistance,

w = width of the contact pad

R_{sk} = modified sheet resistance directly under the ITO contact pad

R_{sk} is given by:

$$R_{sk} = \frac{2w}{s} (R_c - R_e) \quad (\text{eqn. 6.8})$$

where,

s = length of the contact pad

R_e = end contact resistance

R_e can be calculated from the resistance measurements of R_{12} , R_{23} and R_{13} corresponding to the resistances of three adjacent pads. In practice, if the total resistance between two pads is plotted as a function of the separation between them, the slope gives the value of (R_{sh}/w) while the y-axis intercept gives $2R_c$. In addition to these parameters, the transfer resistance, R_t , is often used as a figure of merit in the related literature. R_t is the product of the contact resistance R_c and w , the pad width.

In a good ohmic contact, following annealing, the sheet resistance of the material directly under the pad is heavily modified and significantly reduced in comparison to the sheet resistance, R_{sh} , of the starting material. Therefore, before annealing, R_{sh} and R_{sk} should be similar in value if the material directly under the pad has not been modified as a result of simply depositing the pad metals for example; following annealing, R_{sk} is typically ten or twenty times lower while R_{sh} remains unchanged.

After annealing, the measured contact resistance as a function of pad spacing showed a linear dependence. Figure 6.29 shows the specific contact resistance, ρ_c , as a function of annealing stages for ITO contacts to n^+ -GaAs and In/n^+ -GaAs. Here each “annealing stage” refers to

one full cycle of the annealing scheme shown in Figure 6.27; thus stage 2 refers to two consecutive cycles and so on.

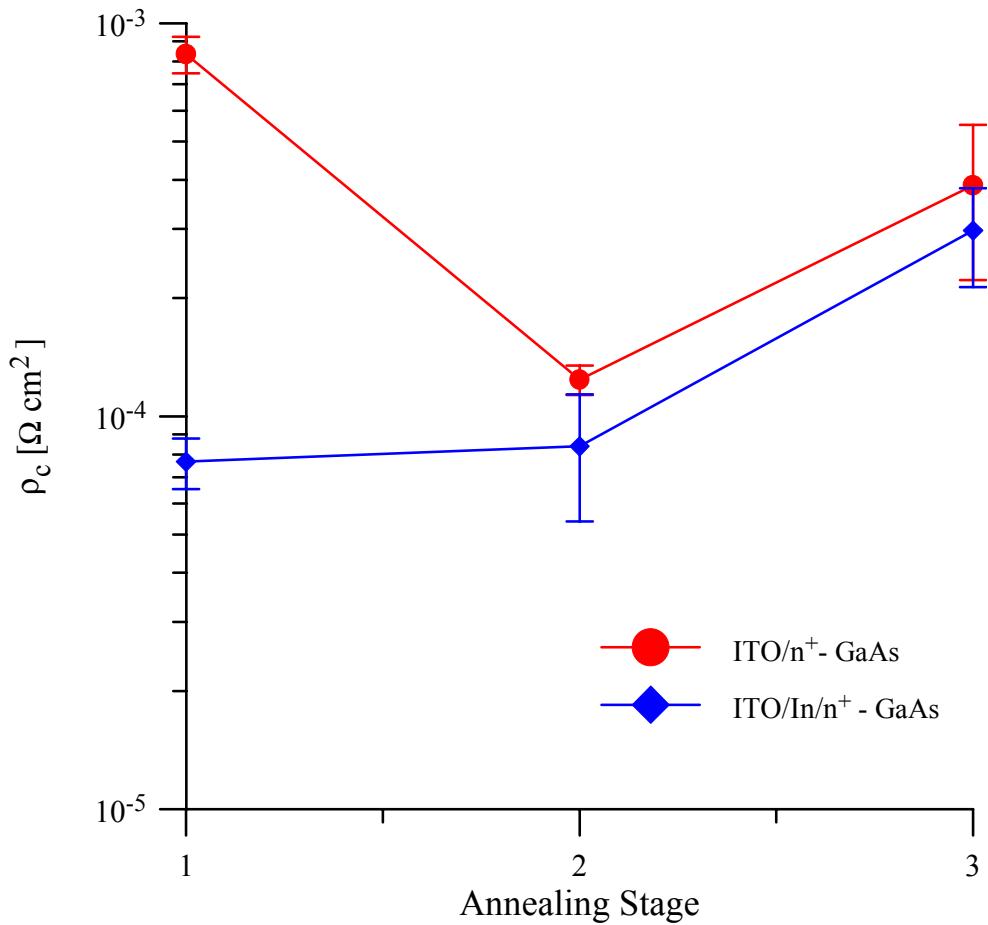


Figure 6.29: Specific contact resistance, ρ_c , of ITO and ITO/In contacts to n^+ GaAs substrates as a function of annealing stages

The best transfer resistance, R_t , and the specific contact resistances, ρ_c , and their corresponding R_{sh} and R_{sk} values achieved in each case are summarised in Table 6.13; corresponding results obtained for a conventional contact is also shown for comparison. As mentioned earlier, prior to annealing, the ITO contacts showed rectifying behaviour and were not measurable using the TLM method. The R_t also shows a minima after the first stage of annealing. Hence only one annealing stage was used during the fabrication of devices with transparent ITO ohmic pads on n^+ - GaAs contact layers.

Contact	$R_t [\Omega\text{mm}]$	$\rho_c [\Omega\text{cm}^2]$	$R_{sh} [\Omega/\square]$	$R_{sk} [\Omega/\square]$
ITO/n ⁺ -GaAs	0.68 ± 0.01	$(1.2 \pm 0.1) \times 10^{-4}$	60.2 ± 2.1	10.2 ± 1.2
ITO/In/n ⁺ -GaAs	0.49 ± 0.02	$(7.6 \pm 0.1) \times 10^{-5}$	52.1 ± 1.1	6.3 ± 0.7
(Au/Ni/AuGe/Ni)/n ⁺ -GaAs	0.10 ± 0.01	$(3.1 \pm 0.7) \times 10^{-5}$	38.8 ± 1.0	2.3 ± 0.4

Table 6.13: Summary of ohmic parameters for ITO/n⁺ - GaAs contacts with and without a thin intermediate In layer and comparison with conventional opaque metal/n⁺-GaAs contacts

From Table 6.13, it is seen that the insertion of the intermediate layer of In helps improve the ohmic contact although it is not a known dopant in GaAs. However, Lakhani *et al* [169] have suggested that In alloyed to n-GaAs forms a graded InGaAs heterojunction giving rise to ohmic behaviour. After the post deposition annealing, it forms a thin layer of InGaAs which results in a superior ohmic contact with ITO.

In the conventional n-type Ni/AuGe/Ni/Au ohmic contact, Ge is the main dopant species which is said to be driven into the underlying n-type semiconductor by the heat treatment to form a n⁺⁺-GaAs interface [26] resulting in ohmic behaviour through current transport predominantly by the tunneling mechanism. In the transparent contacts, Sn, thermally dissociated from the stoichiometric compound Indium Tin Oxide, is most likely to be responsible for forming a good non-rectifying contact. Sn, like Ge, is known to be an amphoteric shallow donor in n-GaAs [26,186]. It is seen that the ITO contacts have comparable ohmic characteristics to their conventional counterparts.

The R_{sh} values for a given conductive substrate should not change as a result of annealing or having different ohmic pads. Therefore, it is interesting to note that the sheet resistance of the ITO mesas is consistently higher than that for the thermally evaporated contacts suggesting the retention of some sputter induced damage. Given the low sheet resistance obtained for the ITO film itself following similar heat treatment, it is this damage which is most likely to account for the relatively slight increase in the resistance of the transparent contacts.

Although Zn, Be and sometimes Mg are usually chosen as acceptors for p-type semiconductors, but for practical purposes, the Au/Zn/Au multilayered contact is by far the most widely used. Despite the absence of any obvious dopant species in the ITO, the main reason behind realising good p-type transparent ohmic contacts is likely to be due to the high

substrate doping alone. The corresponding specific contact resistance, as a function of annealing stages for ITO contacts to p⁺-GaAs is shown in Figure 6.30.

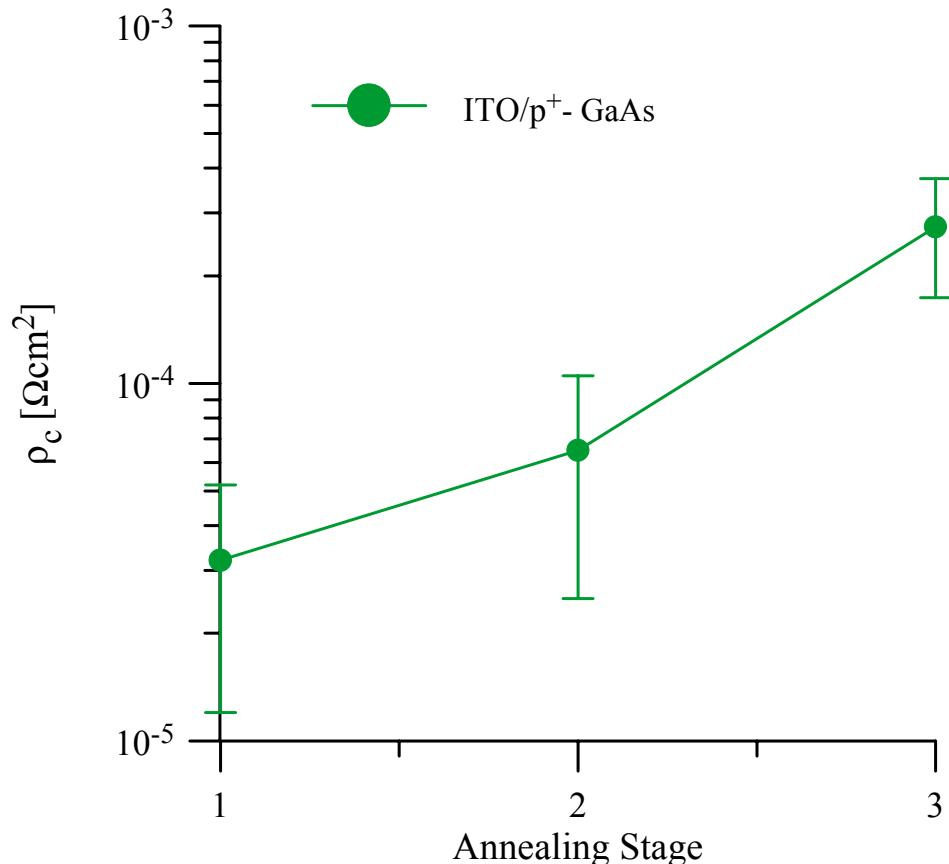


Figure 6.30: Specific contact resistance, ρ_c , of ITO contacts to p⁺ GaAs substrates as a function of annealing stages

The best transfer resistance, R_t , and the specific contact resistances, ρ_c , achieved are summarised in Table 6.14.

Contact	$R_t [\Omega\text{mm}]$	$\rho_c [\Omega\text{cm}^2]$	$R_{sh} [\Omega/\square]$	$R_{sk} [\Omega/\square]$
ITO/p ⁺ -GaAs	0.55 ± 0.03	$(3.2 \pm 0.1) \times 10^{-5}$	156.1 ± 15.7	13.8 ± 2.8
(Au/Zn/Au)/p ⁺ -GaAs	0.07 ± 0.01	$(5.1 \pm 0.2) \times 10^{-6}$	138.5 ± 6.6	6.7 ± 0.2

Table 6.14: Summary of ohmic parameters for ITO/p⁺ - GaAs contacts and comparison with conventional opaque metal/p⁺-GaAs contacts

As for the n-type contacts, the transparent ITO contacts are comparable to their opaque counterparts. It is should be noted that the conventional p-type ohmic contacts obtained here

are similar to those fabricated in our laboratory which is amongst some of the best results ever reported for Au/Zn/Au contacts on highly (carbon) doped p⁺-GaAs substrates [187]. Although the sputter damage evidently has a less significant effect on the sheet resistance of the p⁺-GaAs substrate than in the case of the n⁺-GaAs substrate, the higher specific contact resistance and transfer resistance of the transparent contact must be due to a combination of the absence of any acceptor species in ITO and retention of sputter induced damage.

In comparison with the ITO/n⁺-GaAs ohmic contact, it is seen that the ITO/p⁺-GaAs contact is marginally better. Again, this is most likely due to the p⁺-GaAs test wafer being ten times more highly doped than the n⁺-GaAs samples used in this study.

6.2.1.2 Contacts to Highly Doped InGaAs Epitaxial Layers

ITO was deposited on highly doped InGaAs epitaxial layers to study the ohmic properties of the ITO/n⁺ InGaAs interface with its potential application in the fabrication of ITO emitter contact InP/InGaAs HPTs.

6.2.1.2.1 Fabrication and Post Deposition Annealing

The InGaAs samples used in these experiments consisted of a S. I. InP substrate with MOCVD grown lattice matched n⁺ In_{0.53}Ga_{0.47}As epitaxial layers. Like the n⁺-GaAs layers, the InGaAs test wafers were obtained by chemically etching a InP/InGaAs HBT wafer until the highly doped sub-collector was reached. The subsequent fabrication and post deposition annealing procedure for the ITO/n⁺-InGaAs ohmic contacts were similar to those for the n⁺ and p⁺ ITO/GaAs ohmic contacts. Typical values for doping and thickness of the highly doped InGaAs layers are summarised in Table 6.15 below :

Sample	Doping [cm ⁻³]	Thickness [nm]	Substrate
n ⁺ InGaAs	3x10 ¹⁸	600	400μm S.I. InP(Fe doped)

Table 6.15: Typical values for doping and thickness of the InGaAs samples used for appraising ITO ohmic contacts.

6.2.1.2.2 Results and Comparison with Conventional Contacts

Figure 6.31 shows the specific contact resistance as a function of annealing stages for ITO contacts to the n^+ -InGaAs layers grown on S.I. InP substrates.

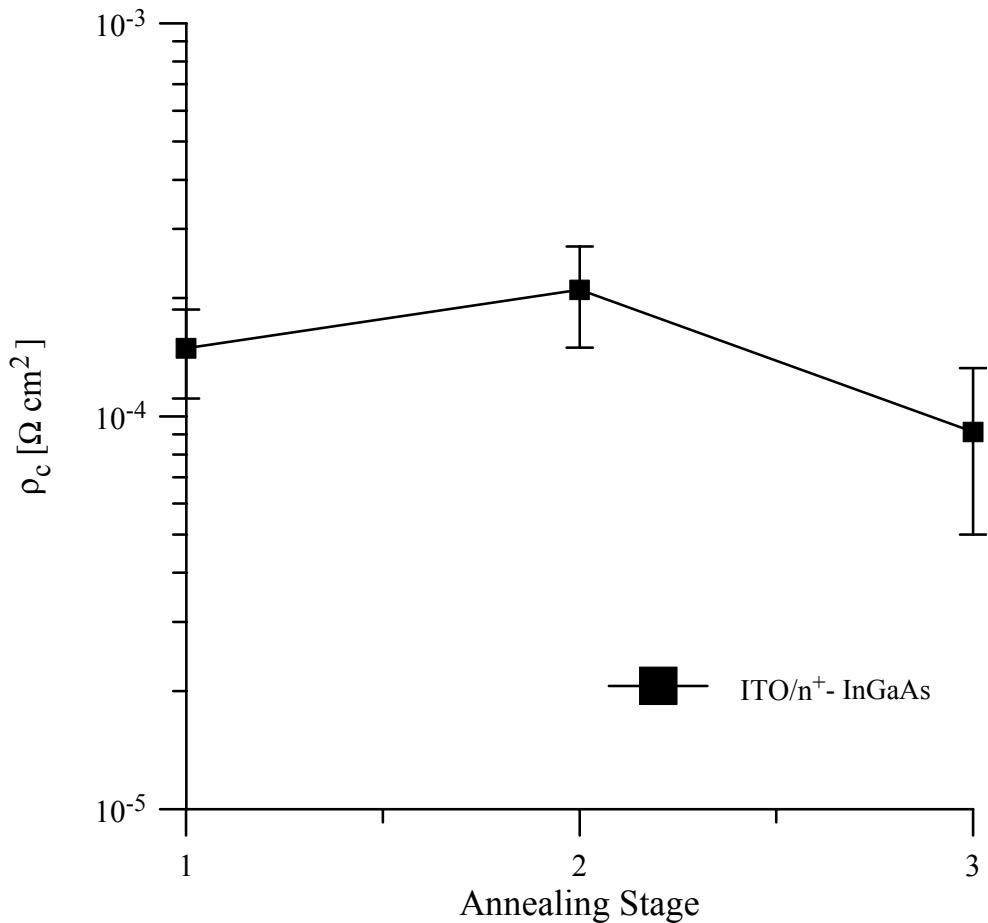


Figure 6.31: Specific contact resistance, ρ_c , of ITO contacts to n^+ InGaAs substrates as a function of annealing stages

The best transfer resistance, R_t , and the specific contact resistances, ρ_c , achieved are summarised in Table 6.16:

Contact	$R_t [\Omega \text{mm}]$	$\rho_c [\Omega \text{cm}^2]$	$R_{sh} [\Omega/\square]$	$R_{sk} [\Omega/\square]$
ITO/ n^+ -InGaAs	0.37 ± 0.1	$(7.1 \pm 0.6) \times 10^{-5}$	39.3 ± 3.2	8.0 ± 1.5
(Au/Ni/AuGe/Ni)/ n^+ -InGaAs	0.12 ± 0.01	$(5.4 \pm 0.8) \times 10^{-6}$	37.4 ± 1.0	3.2 ± 0.3

Table 6.16: Summary of ohmic parameters for ITO/ n^+ - InGaAs contacts and comparison with conventional opaque metal/ n^+ -InGaAs contacts

The doping mechanisms involved here are similar to those in the n^+ -GaAs substrate.

6.2.1.3 Surface Morphology of ITO Ohmic Contacts

In the fabrication of small geometry microwave devices, the surface morphology of the ohmic contact is of particular importance. An uneven surface can reduce the ease of subsequent wire bonding and degrade the edge-definition where tolerances are very strict. However, the wetting action of metallic compounds on III-V semiconductors is low and the contact material tends to separate into islands [25]. This adhesion problem is also called “mounding” or “balling-up” and is usually associated with the n-type AuGe contact [188]; although adhesion layers such as Ni or Pt, which do not form eutectics with the contact metals, have been used to circumvent this problem, this is still a topic which is far from resolved. Morphology problems can also arise from re-evaporation of constituents at high temperatures as Zn in the Au/Zn/Au p-type contact.

Figure 6.32 shows a Scanning Electron Microscope (SEM) photomicrograph of three types of ohmic contacts on a GaAs substrate: metal on ITO/n⁺-GaAs, Au/Zn/Au on p⁺-GaAs and finally Ni/AuGe/Ni/Au on n⁺-GaAs. It should be noted that following ITO annealing using the scheme shown in Figure 6.27, further metalisation and chemical etching steps were carried out to deposit the opaque p and n-type contacts on p⁺-GaAs and n⁺-GaAs respectively. A final single annealing step was carried out by RTA at 400°C for 30 seconds.

Figure 6.32: SEM Photomicrograph showing the contrast between the smooth surface morphology of an metal/ITO/n⁺-GaAs and the rough (Ni/AuGe/Ni/Au)/n⁺-GaAs contact.

It is seen from Figure 6.32 that there is significant “balling-up” on the surface of the n-type; the diameter of an average “mound” is approximately $5\mu\text{m}$ - comparable to, if not larger than, the dimensions involved in emitter finger widths of microwave HBTs. This effect is reduced but still present in the p-type contact.

By contrast, however, the metal on the ITO/n⁺-GaAs surface is smooth. This suggests that there is no liquid phase reaction involved in the latter ohmic contact and ITO acts like a capping (such as Ti/Au) or a diffusion barrier (such as ZrB₂) [189] layer preventing the intermixing of the top-most Au layer with the substrate causing the balling effect. Its demonstrated excellent surface morphology and edge definition is an added advantage in the fabrication of small geometry optoelectronic devices. This observation is further correlated by the fact that Sn present in ITO is also known to take part in solid phase reactions to n-GaAs in the formation good ohmic contacts. However, like other solid phase schemes, such as Pd/Ge or Pd/Sn, the resistance is higher than that obtained for the Ni/AuGe/Ni/Au liquid phase n-type contact.

6.2.2 Realisation of ITO Contacts to HPT Emitters

Given that photo transistors offer the possibility of light detection and amplification in a single device, renewed interest has been aroused in these devices as detectors, particularly with the advent of the Heterojunction Bipolar Transistor (HBT). Studies using such HBTs with opaque emitter contacts demonstrate the suitability of these devices as photo detectors in terms of optical performance where signal to noise ratios in excess of 30 dB have been obtained [95,190,191]; HBTs used as phototransistors are known as HPTs. The optical gain of any photo transistor depends on the coupling efficiency, the collection efficiency and its internal gain; in the HPT structure, there lies an inherent trade-off between the speed and the collection efficiency. However, by using a transparent emitter contact, the coupling efficiency can be significantly improved thereby raising the overall gain-bandwidth of the device correspondingly.

In this section the use of Indium Tin Oxide (ITO) as the transparent ohmic contact to the emitter of such HPTs is presented. As mentioned elsewhere in this thesis, a transparent contact overcomes the processing difficulties associated with opaque ring electrodes where near micron structures need to be fabricated. AlGaAs/GaAs, InGaP/GaAs and InP/InGaAs HPTs have been fabricated using ITO as the emitter contact. To the best of our knowledge, the work on InP/InGaAs HPTs with ITO emitter contacts was first reported by ourselves [2]. The I-V, C-V, and optical characteristics of HBTs and HPT's fabricated from these three different material systems and the advantages associated with their fabrication and

performance are compared and discussed in the following pages. In addition, advantages and disadvantages of top illuminated vs. edge coupled HPTs is also considered.

6.2.2.1 Fabrication of conventional HBTs and ITO Emitter Contact HPTs

A set of AlGaAs/GaAs, InGaP/GaAs and InP/InGaAs HBT devices were fabricated using standard photolithographic and wet chemical mesa etching steps. Layer structures of the samples are shown in Table 6.17 to Table 6.21 respectively:

No.	Layer	Material	Dopant	Doping [cm ⁻³]	Thickness [Å]
8	Cap	n ⁺ - GaAs	Si	2 x 10 ¹⁸	3,500
7	Graded Emitter	Al _x Ga _{1-x} As; (x=0.3 to 0)	Si	2 x 10 ¹⁸	400
6	Emitter	Al _{0.3} Ga _{0.7} As	Si	3 x 10 ¹⁷	1,500
5	Graded Emitter	Al _x Ga _{1-x} As; (x=0 to 0.3)	Si	3 x 10 ¹⁷	225
4	Base	p ⁺ - GaAs	C	4 x 10 ¹⁹	1,000
3	Collector	n - GaAs	Si	5 x 10 ¹⁵	10,000
2	Sub-collector	n ⁺ - GaAs	Si	> 5 x 10 ¹⁸	7,000
1	Substrate	S. I. GaAs	Undoped	-	400μm

Table 6.17: Layer Structure for graded AlGaAs/GaAs wafer (no. 3075-3)

No.	Layer	Material	Dopant	Doping [cm ⁻³]	Thickness [Å]
8	Cap	n ⁺ - GaAs	Si	5.0 x 10 ¹⁸	1,900
7	Graded Emitter	Al _x Ga _{1-x} As; (x=0.3 to 0)	Si	5.0 x 10 ¹⁷	200
6	Emitter	Al _{0.3} Ga _{0.7} As	Si	5.0 x 10 ¹⁷	1,500
5	Graded Emitter	Al _x Ga _{1-x} As; (x=0 to 0.3)	Si	5.0 x 10 ¹⁷	200
4	Base	p ⁺ - GaAs	C	2.0 x 10 ¹⁹	900
3	Collector	n - GaAs	Si	2.0 x 10 ¹⁶	5,000
2	Sub-collector	n ⁺ - GaAs	Si	5.0 x 10 ¹⁸	10,000
1	Substrate	S. I. GaAs	Undoped	-	400μm

Table 6.18: Layer Structure for graded AlGaAs/GaAs HBT wafer (no. 1-1408)

No.	Layer	Material	Dopant	Doping [cm ⁻³]	Thickness [Å]
6	Cap	n ⁺ - GaAs	Si	2±0.2 x 10 ¹⁸	1,000
5	Emitter	n - In _{0.51} Ga _{0.49} P	Si	3±0.3 x 10 ¹⁷	4,000
4	Base	p ⁺ - GaAs	C	5±0.5 x 10 ¹⁹	800
3	Collector	n - GaAs	Si	7±0.7 x 10 ¹⁵	10,000
2	Sub-collector	n ⁺ - GaAs	Si	> 5 x 10 ¹⁸	7,000
1	Substrate	S. I. GaAs	Undoped	-	400µm

Table 6.19: Layer Structure for the InGaP/GaAs Wafer (no. 15894-2)

No.	Layer	Material	Dopant	Doping [cm ⁻³]	Thickness [Å]
8	Cap	n ⁺ - GaAs	Si	3 x 10 ¹⁸	1,500
7	Emitter 2	n ⁺ - In _{0.5} Ga _{0.5} P	Si	2 x 10 ¹⁸	200
6	Emitter 1	n - In _{0.5} Ga _{0.5} P	Si	3 x 10 ¹⁷	1,000
5	Spacer	GaAs	Undoped	-	25
4	Base	p ⁺ - GaAs	C	3 x 10 ¹⁹	800
3	Collector	n - GaAs	Si	5 x 10 ¹⁶	5,000
2	Sub-collector	n ⁺ - GaAs	Si	3 x 10 ¹⁸	5,000
1	Substrate	S. I. GaAs	Undoped	-	400µm

Table 6.20: Layer Structure for the InGaP/GaAs Wafer (no. DK-136)

No.	Layer	Material	Dopant	Doping [cm ⁻³]	Thickness [Å]
7	Cap	n ⁺ - In _{0.53} Ga _{0.47} As	Si	3.0 x 10 ¹⁸	1,000
6	Emitter	n - InP	Si	5.0 x 10 ¹⁷	3,000
5	Base	p ⁺ - In _{0.53} Ga _{0.47} As	Zn	6.0 x 10 ¹⁸	2,500
4	Collector	n - In _{0.53} Ga _{0.47} As	Si	2.3 x 10 ¹⁶	4,000
3	Sub-collector	n ⁺ - In _{0.53} Ga _{0.47} As	Si	3.0 x 10 ¹⁸	6,000
2	Buffer	InP	Undoped	-	10,000
1	Substrate	S. I. InP	Fe	-	400µm

Table 6.21: Layer Structure for the InP/InGaAs (no. 3-089)

Large geometry HBT devices were fabricated based on the circular triple-mesa design using the standard photolithography and lift-off techniques. Figure 6.33 shows the plan view of a typical $100\mu\text{m}$ HBT device. Using this design, the emitter/base and base/collector areas can be obtained as $7.85 \times 10^{-5} \text{ cm}^2$ and $4.27 \times 10^{-4} \text{ cm}^2$ respectively.

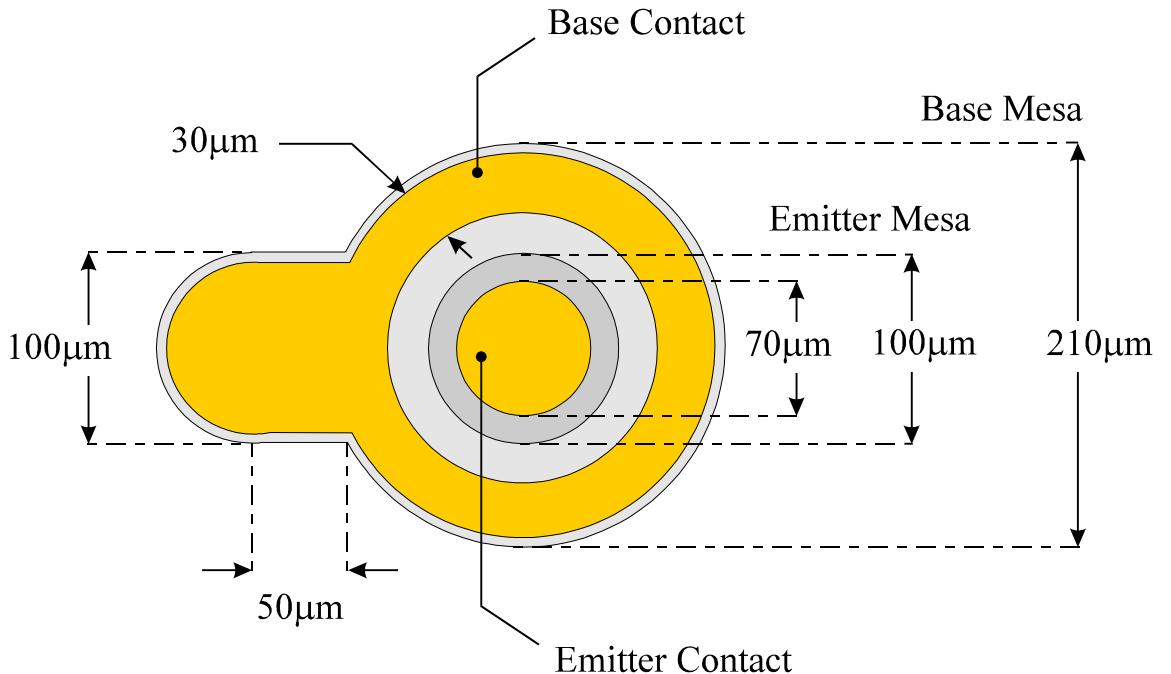


Figure 6.33: Scale diagram of a HBT with $100\mu\text{m}$ diameter emitter

In case of the conventional HBT devices, the fabrication process begins with the deposition of the emitter metal contact on the bare wafer; this n-type metalisation scheme consists of 50 Å Ni / 300 Å AuGe / 100 Å Ni / 1000 Å Au. This step is followed by mesa etching to the base and deposition of the p-type contact metals consisting of 300 Å Au / 300 Å Zn / 1000 Å Au. Finally, a second mesa etch step is used to reach the highly doped sub-collector and deposition of another n-type metal contact layer. The fabrication step is completed by a single rapid thermal annealing (RTA) at 400 °C for 30 seconds. This final annealing step is not applied in case of the InP/InGaAs HBT devices because these devices already have low ohmic contacts without the annealing; furthermore, the annealing causes these devices to short out.

In the fabrication of the HPTs with transparent ITO emitter contacts, the above procedure is slightly modified. For the AlGaAs/GaAs and InGaP/GaAs devices, both of which have a n^+ -GaAs cap layer, a thin layer of In is used between the ITO and the semiconductor in order to improve the ohmic contact. This was seen from our experimental results which were discussed in section 6.2.1 of the thesis. Therefore, a circular dot of In (100 Å thick) is

deposited by thermal evaporation on the n⁺-GaAs cap layer of the AlGaAs/GaAs or InGaP/GaAs sample using standard photolithography and lift-off process. ITO is then deposited onto the n⁺-GaAs cap layers by reactive r.f. sputtering followed by dry etching for emitter contact definition. The samples were then alloyed to obtain good ITO/In/n⁺-GaAs ohmic contact. For the InP/InGaAs devices, the fabrication process starts with the r.f. sputter deposition of ITO on the n⁺ - InGaAs cap layer. This is followed by emitter contact definition and alloying to achieve a good ITO/n⁺ - InGaAs ohmic contact as in the case of AlGaAs/GaAs or InGaP/GaAs devices.

Thus, for the ITO emitter contact HPTs, once the transparent contact is deposited, defined and alloyed, further fabrication consists of depositing a conventional n-type metal contact on the ITO. This is followed by exactly the same processing steps as in the fabrication of conventional HBTs. Thus Au/Zn/Au and Ni/AuGe/Ni/Au metalisation systems are used to make contacts to the base and collector layers respectively. Finally, while the AlGaAs/GaAs devices were annealed using RTA at 400°C for 30 sec., no further annealing was carried out on the InP/InGaAs HPTs in the final stage of the fabrication. Figure 6.34 shows the photo-micrograph of such an InP/InGaAs HPT device after fabrication:

Figure 6.34 : Photo micrograph of a completed InP/InGaAs HPT with transparent ITO emitter ohmic contact.

Individual devices were packaged on T05 transistor headers and all I-V measurements were carried out using a HP4145B semiconductor parameter analyser (SPA) while the C-V measurements were done using a HP4284A precision LCR meter. Responsivity measurements were performed by mounting the headers on an optical bench and using 630nm, 780nm and 1310nm variable power solid state lasers (for the AlGaAs/GaAs and InP/InGaAs HPTs respectively) in conjunction with the SPA. The electrical base current input from the SPA was set to zero during the optical measurements, and the output collector current was recorded at various incident optical power levels.

6.2.2.2 Electrical Properties of HBTs with Opaque and Transparent Contacts

The measured electrical (d.c.) properties of the HBTs in this study are presented and analysed here. In each case, the mean value with the respective spread of various parameters for several otherwise identical devices are used. At first a comparison between the opaque and transparent set of devices is made; this is followed by a comparison between the HBTs fabricated from the different material systems.

6.2.2.2.1 AlGaAs/GaAs Devices

The common emitter output characteristics of a typical N-p-n AlGaAs/GaAs HBT with conventional metal contacts is plotted in Figure 6.35. It is seen that these HBTs have excellent saturation characteristics with low output conductance typical for GaAs-based devices.

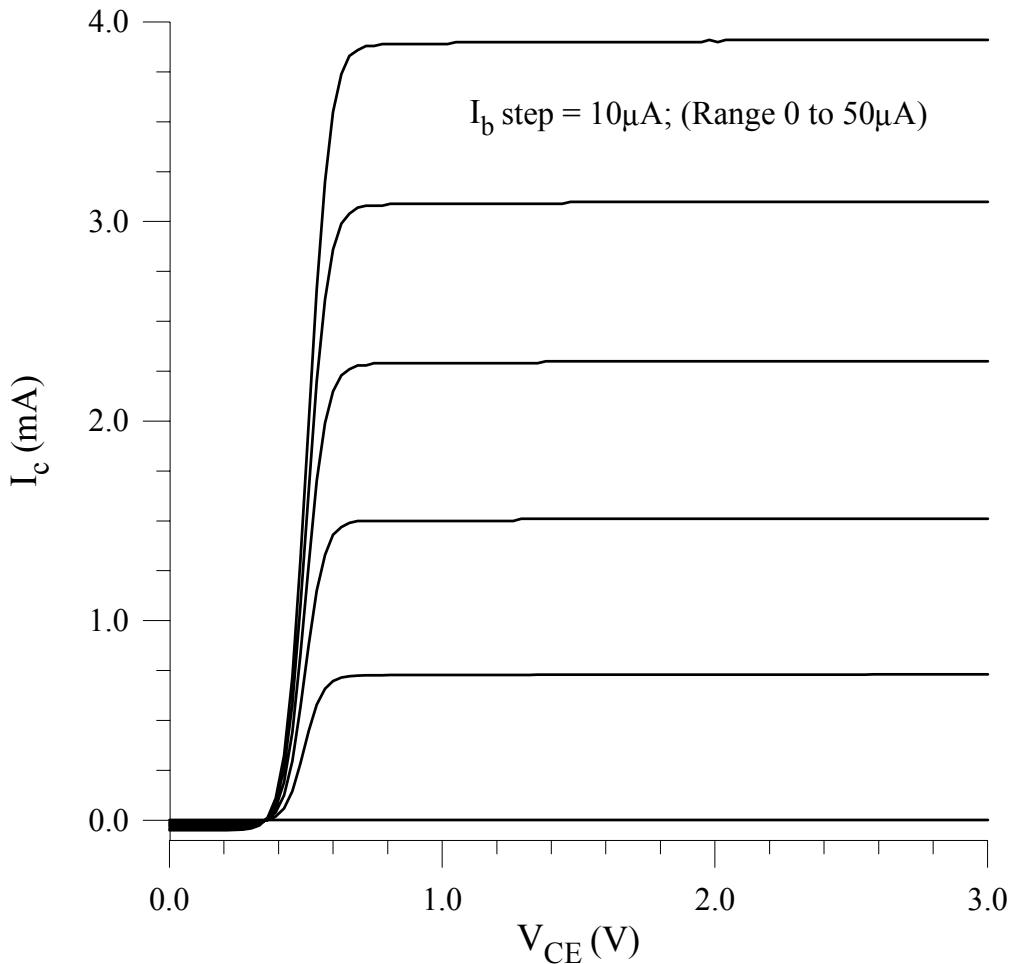


Figure 6.35: Common emitter output characteristics of a conventional AlGaAs/GaAs HBT (on wafer no. 3075-3)

For these HBTs, a common emitter offset voltage, ΔV_{CE0} , (measured with $I_b \approx I_c \approx 0$) of 405mV was observed. This value is more than an order of magnitude greater than the ΔV_{CE0} for a homojunction device which is typically 10 mV. The large ΔV_{CE0} in HBTs is due to the inherent difference between the turn on voltages, V_t , of the base-emitter heterojunction and the base-collector homojunction [192]. The difference in the built-in potentials has been attributed and experimentally confirmed to be due a potential spike at the base emitter hetero-interface by Lee *et al* [192]. In the presence of such a spike the electrons have to surmount the barrier by thermionic emission (much like transport across a Schottky barrier) whereas transport of carriers in a homojunction is dictated essentially by a diffusion mechanism. Other researchers have reported the use of controlled grading at the heterojunction to reduce the spike [193,194] or employed another hetero-interface at the base collector [195] in order to minimise the offset voltage. The V_t is related to but not equal to the built-in potentials, V_{bi} , of the respective p-n hetero and homo junctions. In addition to V_{bi} differences, the final

variation in the V_t also depends on the difference between total series resistances of the two (base-emitter and base collector) diodes in question. Thus the offset voltage is given by:

$$\Delta V_{CEo} = V_{t(B-E)} - V_{t(B-C)} \quad (\text{eqn. 6.9})$$

where,

$V_{t(B-E)}$ = base-emitter turn-on voltage

$V_{t(B-C)}$ = base-collector turn-on voltage

In addition to the above factors, Tiwari *et al* [196] have also reported that if there is significant recombination current present in the base, the asymmetry of the areas of the two junctions can also contribute to the offset voltage by between $[kT/q \times \ln(\text{area ratio})]$ and $[2kT/q \times \ln(\text{area ratio})]$. In case of the transistors in this study, this value could therefore be between 45mV to 90mV.

The Early voltages ($> 400V$) are higher than those expected from a BC182 homojunction Silicon bipolar transistor (typically 130 volts) and demonstrates considerably lower degree of base width modulation in the HBTs. This is to be expected given the extremely high base dopings in the latter devices. We have observed AlGaAs/GaAs HBTs with forward Early voltages as high as 1300 volts.

A maximum d.c. current gain of 76.6 was measured at a collector current of 100mA corresponding to a current density of $1.3 \times 10^3 \text{ A/cm}^2$. The ideality factors of the base and collector currents, n_{Ib} and n_{Ic} , were 1.29 and 1.12 respectively; the Gummel plot for these devices is shown in Figure 6.36. A base ideality factor close to unity indicates either the dominance of a base bulk or extrinsic surface recombination effect while domination of recombination in the space charge region at the base emitter hetero-interface yields a n_{Ib} closer to 2 [197]. A collector ideality factor of greater than unity, which is unusual for graded emitter AlGaAs/GaAs HBTs, suggests that the collector current is not a simple diffusion current and that there is a large conduction band offset limiting this current as expected from an abrupt base emitter junction.

The output characteristics for the transparent emitter contact devices were very similar to those shown in the previous figure. The various d.c. parameters for these two sets of devices are summarised in Table 6.22 for comparison.

Parameter	Conventional Device	Device with ITO Contact
β , d.c. Gain	76.6 ± 6.2	60 ± 7.6
n_{Ib} , Base current ideality factor	1.29 ± 0.05	1.30 ± 0.07
n_{Ic} , Collector current ideality factor	1.12 ± 0.01	1.10 ± 0.02
R_{ee} , (Emitter contact resistance) [Ω]	4.32 ± 0.60	24.2 ± 5.2
R_{cc} , (Collector contact resistance) [Ω]	4.22 ± 0.49	4.7 ± 0.5
ΔV_{CEo} , Offset Voltage [mV]	405 ± 45	547 ± 56
Forward Early Voltage [V]	427.7 ± 13.4	406.4 ± 15.3

Table 6.22: Extracted electrical parameters for AlGaAs/GaAs HBTs on wafer no. 3075-3

Few notable differences between the devices with opaque and transparent contacts become apparent from Table 6.22. The greatest amongst these is the emitter contact resistance R_{ee} , which was found to be as much as five times greater for the latter devices in comparison to their opaque counterparts. If the total contact resistance, R_s , is considered to be due of the resistance of the ITO film, R_{ITO} and that of the emitter cap layer immediately underneath it, R_{Cap} , then:

$$R_s = R_{ITO} + R_{Cap} \quad (\text{eqn. 6.10})$$

where, R_{ITO} is given by:

$$R_{ITO} = \frac{\rho_{ITO} L}{A} \quad (\text{eqn. 6.11})$$

and

$$\begin{aligned} \rho_{ITO} &= \text{resistivity of ITO after annealing} = 14.6 \times 10^{-4} \Omega\text{cm} \text{ (see section 5.3.)} \\ L &= \text{thickness of ITO film} = 1500\text{\AA} \\ A &= \text{emitter surface area} = 7.85 \times 10^{-5} \text{ cm}^2 \end{aligned}$$

hence,

$$R_{ITO} = 0.3 \text{ m}\Omega$$

similarly, the resistance of the cap layer was found to be

$$R_{Cap} = 0.03 \text{ m}\Omega$$

taking a value of 1900\AA for its thickness and $1.2 \times 10^{-4} \Omega\text{cm}$ as the modified resistivity of the cap layer under the ohmic contact (obtained from measured $R_{sk} = 6.3 \Omega/\square$, see section 6.2.1).

This shows that high series resistance cannot be attributed to the resistance of the ITO layer or to the cap layer resistance alone. It is also apparent from this calculation that the total contact resistance of the conventional devices also have other resistive components, albeit much less significant in comparison to the r.f. sputtered contacts. The additional resistance in the transparent contact must therefore be due to some sputter induced damage to layers deeper than the cap layer. It was also observed that the thin layer of In helps reduce this effect because preliminary devices without this intermediate metallic film had even larger R_{ee} than those reported here. More detailed study is necessary to investigate this source of resistance and further reduction in the emitter resistance may be achieved by using a thicker layer of indium without causing significant reduction to the transmittance of the ITO contact.

Figure 6.36 shows the Gummel plot for these devices.

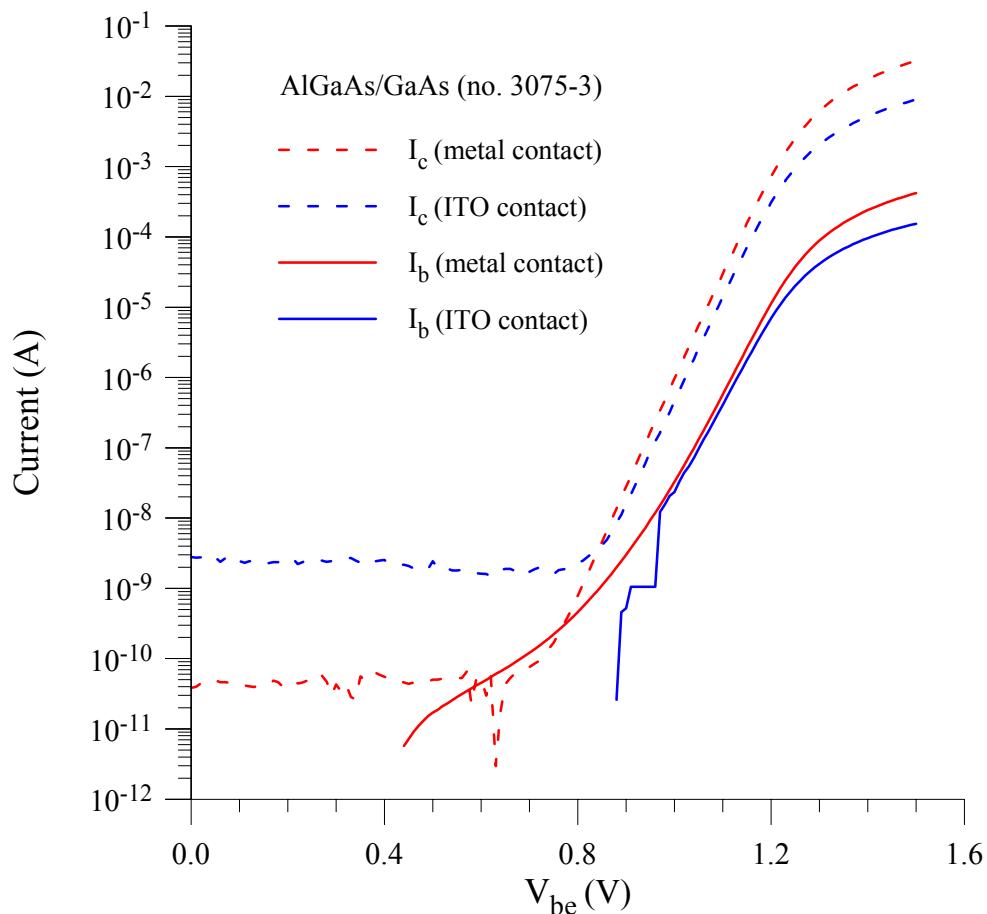


Figure 6.36: Gummel Plots for AlGaAs/GaAs devices (wafer no. 3075-3) with and without ITO emitter ohmic contacts.

It is seen that the I_c in the linear region of the Gummel plot is slightly lower than that of the opaque devices. The final value of I_c is limited by the larger emitter series resistance. However the overall reduction in I_c vs. V_{be} in comparison with the metal contact devices again points to the likelihood of possible damage caused to the emitter layer during r.f. sputtering which was not fully recovered during the ohmic contact annealing. As a result, the measured d.c. gain, β is consistently lower for the ITO emitter contact devices. This is discussed later in section 6.2.2.2.4.

A relatively reduced forward Early voltage was also observed for the transparent emitter contact devices. This can be due to a reduced base doping as result of the ITO deposition. As seen in the analysis of the ITO/n⁺ GaAs Schottky diode, the r.f. sputtering is most likely to give rise to a donor like effect. An increase in the number of ionised donors in the p⁺ base would have the same electrostatic effect as a reduction in the number of acceptors and hence the doping concentration. The reduction in the forward Early voltage would be consistent with such a phenomenon.

The results of capacitance voltage (C-V) measurements on these devices will now be presented. The bias range for the C-V measurements was between 0 and -2V. The extracted emitter and the collector doping profiles for the AlGaAs/GaAs HBTs with the conventional and the ITO emitter contacts are plotted in Figure 6.37 and Figure 6.38 respectively.

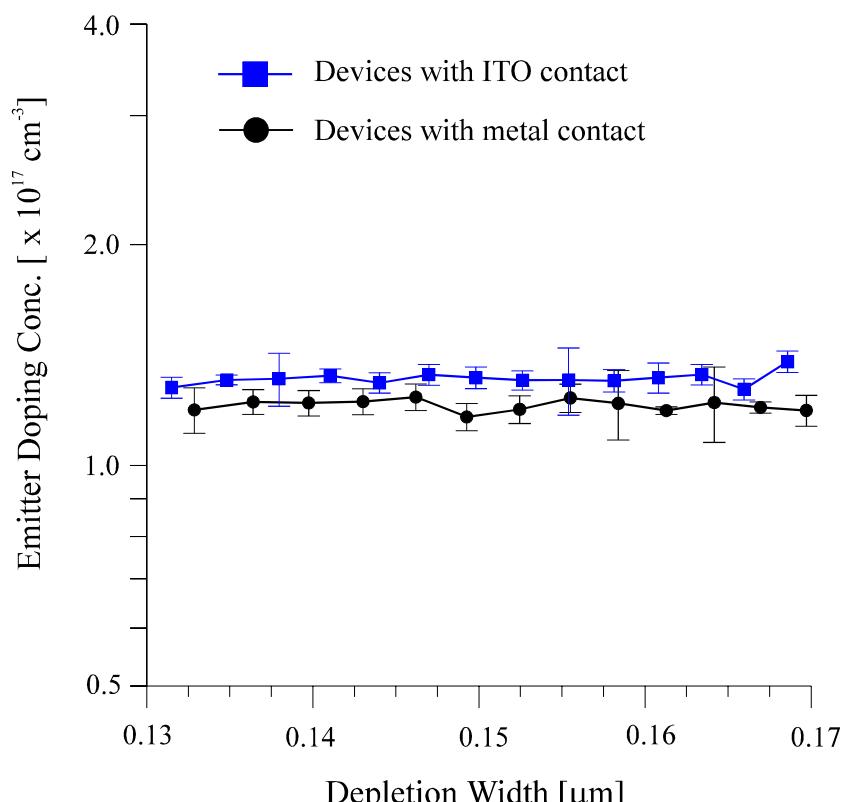


Figure 6.37: Emitter doping profile extracted from C-V measurements for AlGaAs/GaAs devices (wafer no. 3075-3) with and without ITO emitter ohmic contacts.

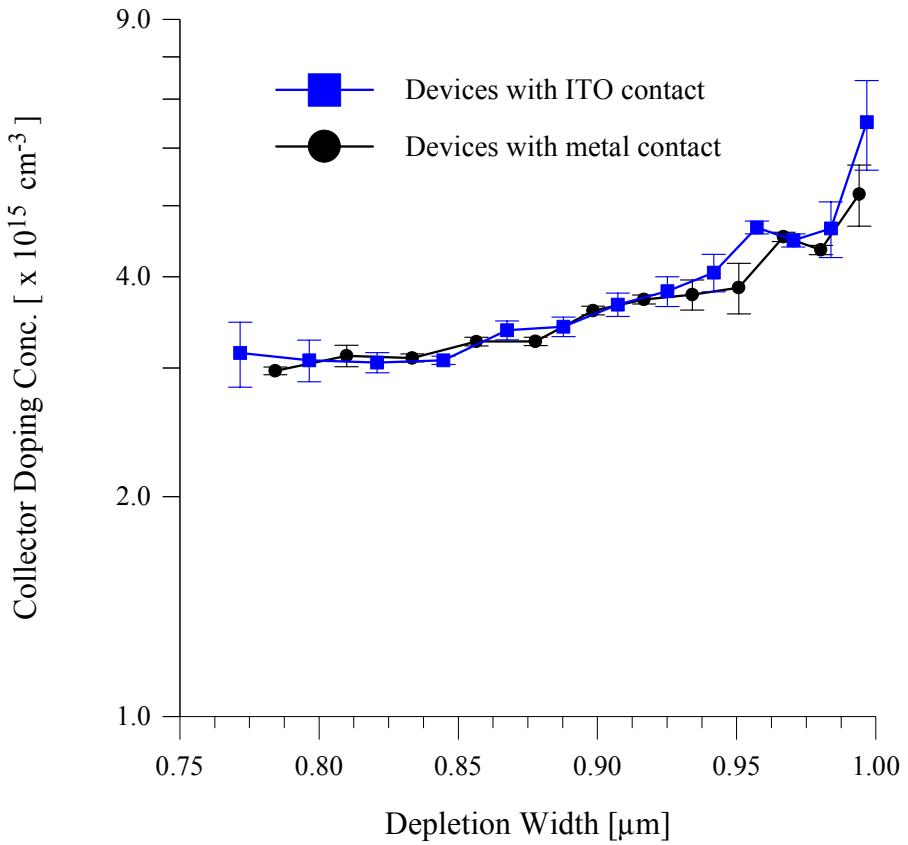


Figure 6.38: Collector doping profile extracted from C-V measurements for AlGaAs/GaAs devices (wafer no. 3075-3) with and without ITO emitter ohmic contacts.

The effect of a higher emitter series resistance in the ITO emitter contact devices was assumed not to have any effect on the capacitance measurement as per the findings discussed earlier in section 6.1.2.4. The emitter doping profiles are flat in comparison with the collector profiles. The higher doping in the emitter means that as the reverse bias is increased to its limit, the depletion region does not go beyond the bulk of the AlGaAs emitter into the GaAs cap layer for example. This observation is consistent with specifications for the wafer no. 3075-3 shown in earlier. Figure 6.37 also shows that the majority of the emitter is already depleted even at zero bias with the depletion region edge at approximately 0.13 μm for both sets of devices. In contrast however, Figure 6.38 shows that the collector profiles rise sharply as the depletion region, swept by the applied reverse bias, approaches the highly doped sub-collector region. The relatively lower collector doping results in the larger zero bias depletion width, 0.77 μm. The measured data for these plots suggest that the collector is fully depleted with a reverse bias of approximately - 0.9V

From these figures it is evident that the values for the measured and the specified doping concentrations are similar within the boundaries of experimental errors. It is also seen that emitter doping profile for the ITO devices is approximately 20% higher than their

conventional counterparts, whereas the difference between the collector dopings is much less significant at approximately 1%. Therefore, these results suggest that there is a noticeable change on the doping profiles of HBTs due to r.f. sputtering and that this does indeed give rise to a donor like effect in the affected regions. Furthermore, as there is no significant change in the collector doping profile, it is reasonable to assume that the sputtering effects are confined before the collector layer. Since the C-V profiling technique cannot yield the doping profile of the already highly doped p⁺ GaAs base region, it is not possible to make definite conclusions based on these measurements on the effects of r.f. sputtering on that region.

Parameter	Conventional Device	Device with ITO Contact
C _{BEo} , Base-emitter zero bias cap. [pF]	6.43 ± 0.08	6.54 ± 0.07
C _{BCo} , Base-coll. zero bias cap. [pF]	6.32 ± 0.03	6.34 ± 0.09
V _{bi(B-E)} , Base-emitter built-in pot. [V]	1.54 ± 0.03	1.62 ± 0.01
V _{bi(B-C)} , Base-collector built-in pot. [V]	1.29 ± 0.01	1.28 ± 0.01
N _{DE} , Emitter doping conc. [cm ⁻³]	(1.10 ± 0.08) x 10 ¹⁷	(1.31 ± 0.04) x 10 ¹⁷
N _{DC} , Collector doping conc. [cm ⁻³]	(3.11 ± 0.11) x 10 ¹⁵	(3.15 ± 0.32) x 10 ¹⁵
MJE (Emitter-base grading)	0.5 (abrupt)	0.5 (abrupt)
MJC (Base-collector grading)	0.5 (abrupt)	0.5 (abrupt)

Table 6.23: Extracted C-V parameters for AlGaAs/GaAs HBTs on wafer no. 3075-3

The various other C-V parameters are summarised in Table 6.23 for comparison. It is seen that the base-emitter built-in potential, V_{bi(B-E)}, is greater (by approximately 200mV) than that of the base-collector V_{bi(B-C)}. This is partly due to the emitter doping being larger than that of the collector, but primarily because of the presence of the considerably large AlGaAs/GaAs heterojunction conduction band offset ΔE_C , as shown in (eqn. 6.12). As mentioned earlier, this difference in the two built-in potentials also contributes towards the larger offset voltage in HBTs.

Although the quoted values above for the built-in potentials were extracted from plots of 1/C² vs. the applied reverse voltage V_R, the analytical values for V_{bi(B-E)} heterojunction [198] and the V_{bi(B-C)} homojunction are given by:

$$V_{bi(B-E)} = E_{gB} + \Delta E_C + \frac{kT}{q} \ln \left(\frac{N_{DE} N_{AB}}{N_{cE} N_{vB}} \right) \quad (\text{eqn. 6.12})$$

which can be also expressed as (see Appendix D2),

$$V_{bi(B-E)} = \Delta E_C - \frac{\Delta E_g}{2} + \frac{kT}{2q} \ln\left(\frac{N_{cB} N_{vE}}{N_{cE} N_{vB}}\right) + \frac{kT}{q} \ln\left(\frac{N_{DE} N_{AB}}{n_{iB} n_{iE}}\right) \quad (\text{eqn. 6.13})$$

and,

$$V_{bi(B-C)} = \frac{kT}{q} \ln\left(\frac{N_{AB} N_{DC}}{n_{iB}^2}\right) \quad (\text{eqn. 6.14})$$

where

E_{gB} = Bandgap of Base material (GaAs), in eV

N_{cE}, N_{vE} = Density of states in the emitter conduction and valence bands respectively

N_{cB}, N_{vB} = Density of states in the base conduction and valence bands respectively

n_{iE} = intrinsic carrier concentration in $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ emitter ($= 2.50 \times 10^3 \text{ cm}^{-3}$)

n_{iB} = intrinsic carrier concentration in GaAs base (or collector) ($= 1.79 \times 10^6 \text{ cm}^{-3}$)

and all other symbols have their usual meaning

Values of $V_{bi(B-E)}$ and $V_{bi(B-C)}$ obtained from these equations, using the measured doping concentrations, compare very well with those extracted experimentally. The equations also indicate that a larger emitter doping in the transparent contact devices would give rise to a larger $V_{bi(B-E)}$ as is the case in practice.

The grading of the two junctions were also obtained from the C-V measurements which indicate both junctions as being abrupt. This is despite the emitter being nominally graded; however, interpreted in conjunction with experimentally measured the I-V parameters (large ΔV_{CEo} and $n_{ic} > 1$), it is likely that the emitter was imperfectly graded.

Table 6.24 shows a comparison of extracted electrical parameters for another set of AlGaAs/GaAs HBTs fabricated (on wafer no. 1-1408) with and without ITO contacts. These devices have considerably lower β than the previous set of devices. As expected from a base emitter junction with proper compositional grading, the collector ideality factor is very close to unity while the offset voltage is noticeably reduced in comparison with the previous set of devices. It is worth noting that the nominal values for the emitter and the base dopings, which play a part in determining the built-in potential of the heterojunction, are comparable for both wafers and is unlikely to contribute to the difference in the measured offset voltages.

Parameter	Conventional Device	Device with ITO Contact
β , d.c. Gain	12.7 ± 0.7	10.7 ± 0.8
n_{Ib} , Base current ideality factor	1.16 ± 0.06	1.36 ± 0.01
n_{Ic} , Collector current ideality factor	1.01 ± 0.05	1.01 ± 0.03
$R_{ee'}$ (Emitter contact resistance) [Ω]	4.65 ± 0.61	28.1 ± 3.6
$R_{cc'}$ (Collector contact resistance) [Ω]	5.10 ± 0.45	4.84 ± 0.36
ΔV_{CEo} , Offset Voltage [mV]	343.0 ± 7.5	278.0 ± 14.7
Forward Early Voltage [V]	347.5 ± 7.1	325.0 ± 10.7

Table 6.24: Extracted electrical parameters for AlGaAs/GaAs HBTs on wafer no. 1-1408

When comparing the opaque and transparent devices, some of the common features with the previous set are that the gain and the forward early voltage are lower while the $R_{ee'}$ is greater for the ITO devices. However, unlike the previous set where n_{Ib} was approximately 1.3 for both conventional and sputtered devices, it is seen here that the base ideality factor has significantly increased from 1.16 to 1.36 for the latter devices with the ITO contact. This indicates a shift of the dominant base current component from base bulk recombination to space charge recombination at the emitter interface. It is possible that sputtering has induced intrinsic surface interface states causing this effect. Given the depth of the base emitter interface in these devices is 3,600Å in comparison to 5,625Å for the previous set, the likelihood of sputter damage to the shallower hetero-interface is greater. It may be argued that this effect did not become apparent in the previous set of devices as those were already dominated by SCR recombination at the base emitter heterojunction.

6.2.2.2 InGaP/GaAs Devices

InGaP/GaAs devices have several advantages over their AlGaAs/GaAs counterparts. These include selective etching of the InGaP emitter which makes not only fabrication considerably easier but it also yields devices with more uniform characteristics for a given wafer. This is evident from the measured d.c. parameters of the devices used in this study as shown in Table 6.25 and Table 6.26. The conduction band offset, ΔE_C , is smaller while the valence band offset, ΔE_V , is larger for the InGaP/GaAs hetero-interface - conditions which are ideal for the performance of an HBT. A more detailed comparison between the various HBT material systems is presented later in this section. As shown by (eqn. 6.12), a smaller ΔE_C would yield a smaller $V_{bi(B-E)}$ which in turn would reduce the collector emitter offset voltage, ΔV_{CEo} . The

ΔV_{CEo} for the InGaP/GaAs devices in this study range from approximately 200mV (wafer no. 15894-2) to as low as 50mV (wafer no. DK-136). The larger offset value in this case results from a combination of higher emitter doping and lower collector doping in the former set of devices giving rise to a larger $V_{bi(B-E)}$ and a smaller $V_{bi(B-C)}$.

Parameter	Conventional Device	Device with ITO Contact
β , d.c. Gain	45.2 ± 0.5	39.0 ± 2.7
n_{Ib} , Base current ideality factor	1.13 ± 0.01	1.11 ± 0.05
n_{Ic} , Collector current ideality factor	1.01 ± 0.01	1.01 ± 0.01
$R_{ee'}$ (Emitter contact resistance) [Ω]	4.58 ± 0.37	14.8 ± 4.6
$R_{cc'}$ (Collector contact resistance) [Ω]	4.62 ± 0.22	4.8 ± 0.7
ΔV_{CEo} , Offset Voltage [mV]	190 ± 10	197 ± 9
Forward Early Voltage [V]	370 ± 23	356 ± 15

Table 6.25: Extracted electrical parameters for InGaP/GaAs HBTs on wafer no. 15894-2

Devices on both InGaP/GaAs HBT wafers indicate a near unity collector ideality factor suggesting the overwhelming domination of diffusion mechanism in the collector current transport. The base ideality factors are also low enough (approximately 1.1) to disregard domination of SCR recombination at the emitter base hetero-interface. Thus, the measured low ideality factors and the low offset voltages are consistent with a lower ΔE_C ; it is worth noting that these effects are also expected from a well graded AlGaAs/GaAs emitter base HBT which attempts to remove the restrictive influence of the potential spike from the otherwise large conduction band offset.

Much of the discussion and analysis used in the presentation of the results for the AlGaAs/GaAs HBTs is also applicable in the comparison between opaque and transparent InGaP/GaAs devices. The ITO devices have lower β and higher $R_{ee'}$ in all cases.

Parameter	Conventional Device	Device with ITO Contact
β , d.c. Gain	16.2 ± 1.8	12.8 ± 1.5
n_{Ib} , Base current ideality factor	1.09 ± 0.03	1.25 ± 0.07
n_{Ic} , Collector current ideality factor	1.01 ± 0.01	1.04 ± 0.04
R_{ee} , (Emitter contact resistance) [Ω]	4.37 ± 0.46	21.6 ± 0.8
R_{cc} , (Collector contact resistance) [Ω]	4.83 ± 0.71	5.06 ± 0.62
ΔV_{CEo} , Offset Voltage [mV]	48.4 ± 7.2	64.5 ± 8.5
Forward Early Voltage [V]	306.8 ± 11.2	262.3 ± 13.5

Table 6.26: Extracted electrical parameters for InGaP/GaAs HBTs on wafer no. DK-136

A final feature which becomes more apparent is the relationship between the effect of r.f. sputter induced damage on the base emitter interface and its depth from the surface of the wafer. It is seen from Table 6.26 that the base ideality factor for ITO contact devices fabricated on wafer no. DK-136 with a shallower base of 2725\AA is 1.25 in comparison to 1.09 of their opaque counterparts indicating sustaining of sputter damage giving rise to increased SCR recombination at the heterojunction; in contrast, the difference in the n_{Ib} between ITO and metal contact devices is insignificant for the wafer with the deeper base of 5000\AA as shown in Table 6.25.

6.2.2.2.3 InP/InGaAs Devices

The InP/InGa_{0.53}As_{0.47} material system received a great deal of attention because of its bandgap of 0.75eV which is sensitive to wavelengths universally used for long haul optical fiber cables. Thus this system has wide ranging implications for uses in the field of optical telecommunications. Also its superior transport properties with respect to the AlGaAs/GaAs system makes it one of the strongest competitors.

Like their InGaP/GaAs counterparts, this material system also offers the advantages associated with selective etching during device fabrication. For the HBTs fabricated in this study, a low common emitter offset voltage (measured when $I_b \approx I_c \approx 0$) of 61mV and collector/emitter breakdown voltage of 5.5V were observed. However, it was evident from the output characteristics that InP/InGaAs HBTs have rather poor saturation characteristics with high output conductance unlike the complete saturation observed in typical GaAs-based

devices. This is due to the high multiplication factor and the low breakdown voltage associated with the low band gap of the InGaAs material.

Figure 6.39 shows the measured current gains vs. collector current for InP/InGaAs HBT devices with metal and ITO emitter contacts at $V_{CE} = 2V$. A maximum current gain of 30 was measured at a collector current of 50 to 70mA corresponding to a current density of approximately $9 \times 10^2 A/cm^2$. From this figure it is also evident that the gain for the ITO devices is lower than those of the opaque devices and that this is throughout the entire range of the collector current.

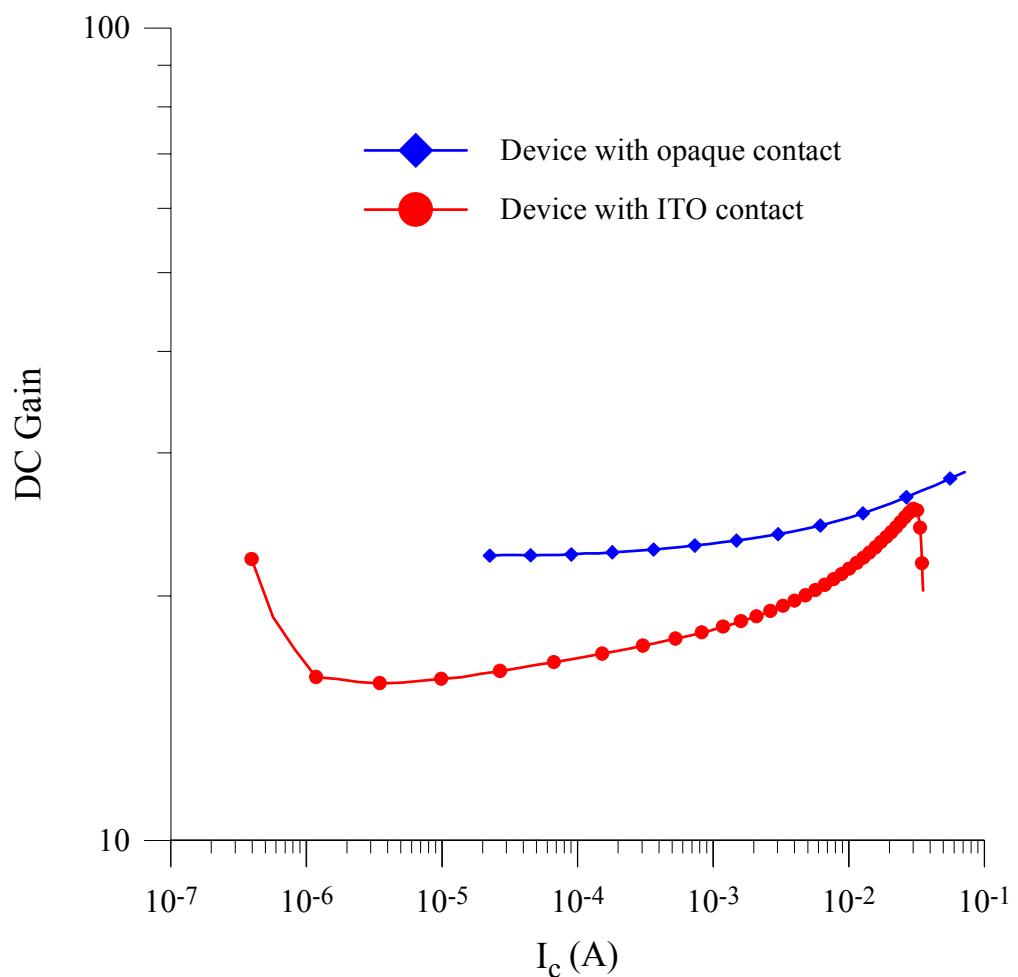


Figure 6.39: Measured current gains vs. collector current for InP/InGaAs HBT devices with an opaque and a ITO emitter contact ($V_{CE} = 2V$).

Ideality factor of the collector and base were 1.01 and 1.11 respectively, indicating that the base current was dominated by the bulk recombination in base while there are no potential barriers in the base emitter junction deviating the collector current from the dominant diffusion mechanism. In case of the ITO devices, there is no change in the n_{lc} while there is a small but notable increase in n_{lb} to 1.18 indicating a presence of SCR recombination at the

base emitter junction. Following from previous discussion on AlGaAs/GaAs and InGaP/GaAs, this increase can be attributed to sputter damage during ITO deposition. The depth of the base emitter hetero-interface is 4000\AA and thus the damage sustained is less than in devices with shallower base emitter junctions (I-1408 and DK-136). Recall, the effect of sputter damage was not noticeable for base interfaces deeper than 5000\AA .

As seen from Table 6.27, the difference between the d.c. gains of the transparent and the opaque devices is the smallest for the InP/InGaAs devices as is the emitter series resistance, $R_{ee'}$, when compared to the devices fabricated in the other material systems. The $R_{ee'}$ for the metal contact devices is 3 to 4 times greater than those for the previously presented AlGaAs/GaAs and InGaP/GaAs HBTs. This is because while the ohmic contacts on those devices were annealed, no annealing was carried out on InP/InGaAs devices with conventional metal ohmic contacts.

Parameter	Conventional Device	Device with ITO Contact
β , d.c. Gain	29.7 ± 0.2	27.5 ± 1.5
n_{Ib} , Base current ideality factor	1.11 ± 0.02	1.18 ± 0.04
n_{Ic} , Collector current ideality factor	1.01 ± 0.01	1.01 ± 0.01
$R_{ee'}$ (Emitter contact resistance) [Ω]	15.6 ± 4.5	19.6 ± 5.3
$R_{cc'}$ (Collector contact resistance) [Ω]	4.8 ± 0.30	4.83 ± 1.22
ΔV_{CEO} , Offset Voltage [mV]	60.0 ± 0.5	56.7 ± 6.2
Forward Early Voltage [V]	80.6 ± 7.3	74.5 ± 8.0

Table 6.27: Extracted electrical parameters for InP/InGaAs HBTs on wafer no. 3-081

The small offset voltage reflects a good match between the turn-on voltages of the base emitter and the base collector junctions. Referring to (eqn. 6.12) it can be deduced that the $V_{bi(B-E)}$ is reduced by the small bandgap of the InGaAs base while according to (eqn. 6.14), the $V_{bi(B-C)}$ would also be expected to be small because of the intrinsic carrier concentration in this material which is 10^5 times greater than in GaAs. It can also be seen that the difference between the offset voltages of the opaque and ITO contact devices is minimal. This can be attributed to their closely matched emitter resistances, $R_{ee'}$.

6.2.2.2.4 Sputter Damage in HPT Devices

There is evidence of sputter damage in the HBTs. However, since the initial doping concentrations in the HBTs is several orders of magnitude greater than those of the diodes, its effect is not as noticeable in the device performance or the CV profiles.

Shallow damage at the surface of the cap layer adversely affects the ohmic properties. Annealing restores most of this damage, but the remaining damage acts as recombination centres at the interface of ITO/cap layer draining a small part of the emitter current. This then results in the observed increase in the emitter series resistance.

Deep damage in the HBTs affects the emitter-base junction and the base bulk respectively. Any non-ideal current transport across the emitter-base junction, in particular increased recombination, would result in an increase in the base ideality factor, n_{Ib} . Experimental results clearly show that devices with sputtered ITO contact have a larger n_{Ib} than their thermally evaporated metal contact counterparts. However, from the n_{Ib} it is not possible to ascertain the effect of damage in the bulk of the base. Increased recombination at the base-emitter junction would reduce the emitter injection efficiency whereas increased recombination in the base would reduce the base transport factor. A reduction in either or both of these two parameters would result in a lowered β of the device. Experimental data suggests lower β for the ITO devices. Thus the observed effects on the emitter series resistance, base ideality factor and the reduced gain provides evidence of both shallow and deep damage due to sputtering on the HBT samples as well. This is in agreement with our observation of the diode samples.

6.2.2.2.5 Comparison between AlGaAs/GaAs, InGaP/GaAs and InP/InGaAs HBTs

In this section, the electrical properties of HBTs fabricated on the three material systems are compared. In order to compare the turn on voltages, V_t , of the AlGaAs/GaAs HBTs, with typical InGaP/GaAs and InP/InGaAs HBTs, the collector currents of three devices with same geometry and conventional ohmic contacts were plotted as a function of base emitter voltage with $V_{BC} = 0$ as shown in Figure 6.40. It is seen that the InP/InGaAs HBTs exhibit a lower turn on voltage (0.2eV) compared to GaAs-based HBTs (0.8eV). This clearly demonstrates the advantage of InP-based HBTs for low power circuit applications, such as mobile telecommunications.

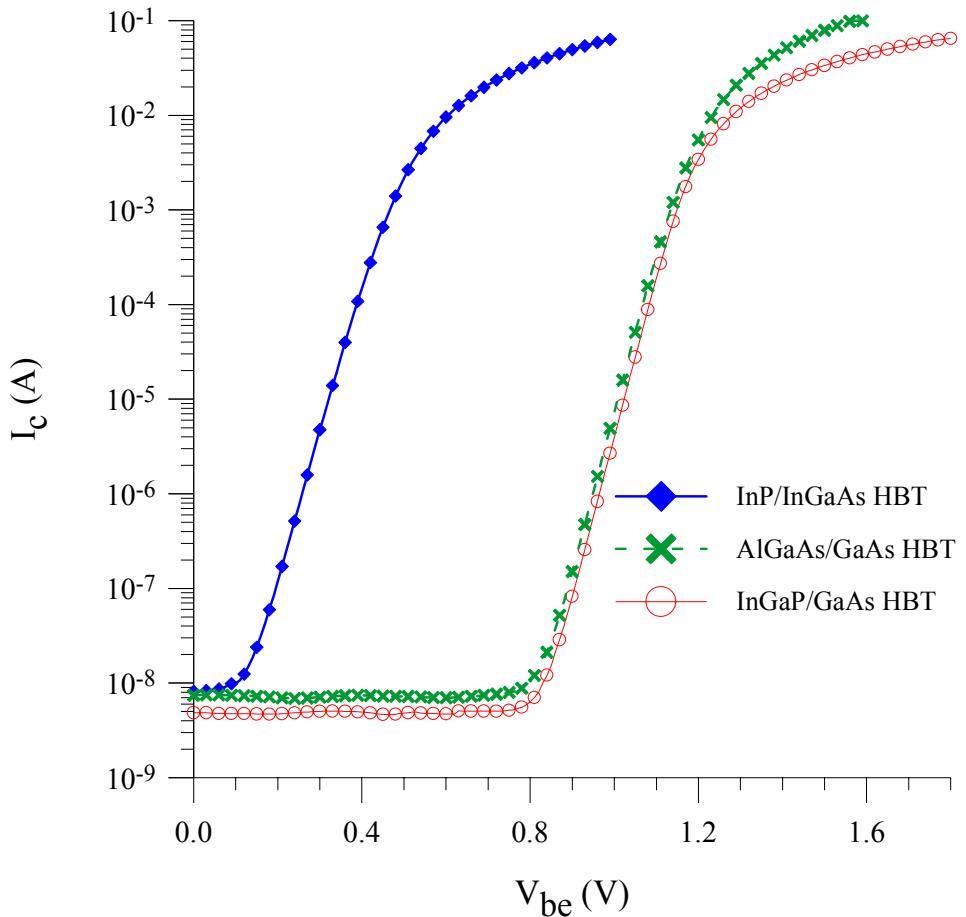


Figure 6.40: I_c versus V_{be} for AlGaAs/GaAs, InGaP/GaAs and InP/InGaAs HBTs. All devices have the same geometry and conventional ohmic contacts.

This difference in the turn on voltages is caused primarily by the difference in the band gap energies of the InGaAs and GaAs base materials. Assuming a unity base transport factor and negligible hole current due to back injection, the collector current is proportional to the minority carrier injected, n_{pb} , at the base emitter junction:

$$I_c \propto n_{pb} \exp\left(\frac{qV_{be}}{KT}\right) \quad (\text{eqn. 6.15})$$

If one measures the turn on voltage at a fixed collector current for all devices, using (eqn. 6.15) the difference in turn on, ΔV , in InGaAs and GaAs base materials can be found by :

$$\Delta V \approx \frac{KT}{q} \ln \left[\frac{\left(n_i^2 / N_A \right)_{\text{InGaAs}}}{\left(n_i^2 / N_A \right)_{\text{GaAs}}} \right] \quad (\text{eqn. 6.16})$$

where,

$$n_i(\text{InGaAs}) = 5.4 \times 10^{11} \text{ cm}^{-3}$$

$$n_i(\text{GaAs}) = 1.8 \times 10^6 \text{ cm}^{-3}$$

Since $(n_i)_{\text{InGaAs}}/(n_i)_{\text{GaAs}} = 10^5$ the contribution from the difference in the ratios of the base dopants (N_{AB}) can be assumed to be minimal; therefore, ΔV was estimated using (eqn. 6.16) to be 0.6V, which is in good agreement with the experimentally observed difference (0.6V).

The gain variation with respect to the collector current for all three devices is compared next. Figure 6.41 shows the normalised d.c. gains for devices fabricated in the three HBT material systems. It is evident that while the AlGaAs/GaAs β varies with I_c , the InGaP/GaAs shows little change with respect to I_c and the InP/InGaAs gain is almost independent of the collector current. This can be attributed to the low surface recombination velocity associated with the InGaAs material.

Much of this work has already been the subject of a journal publication [199].

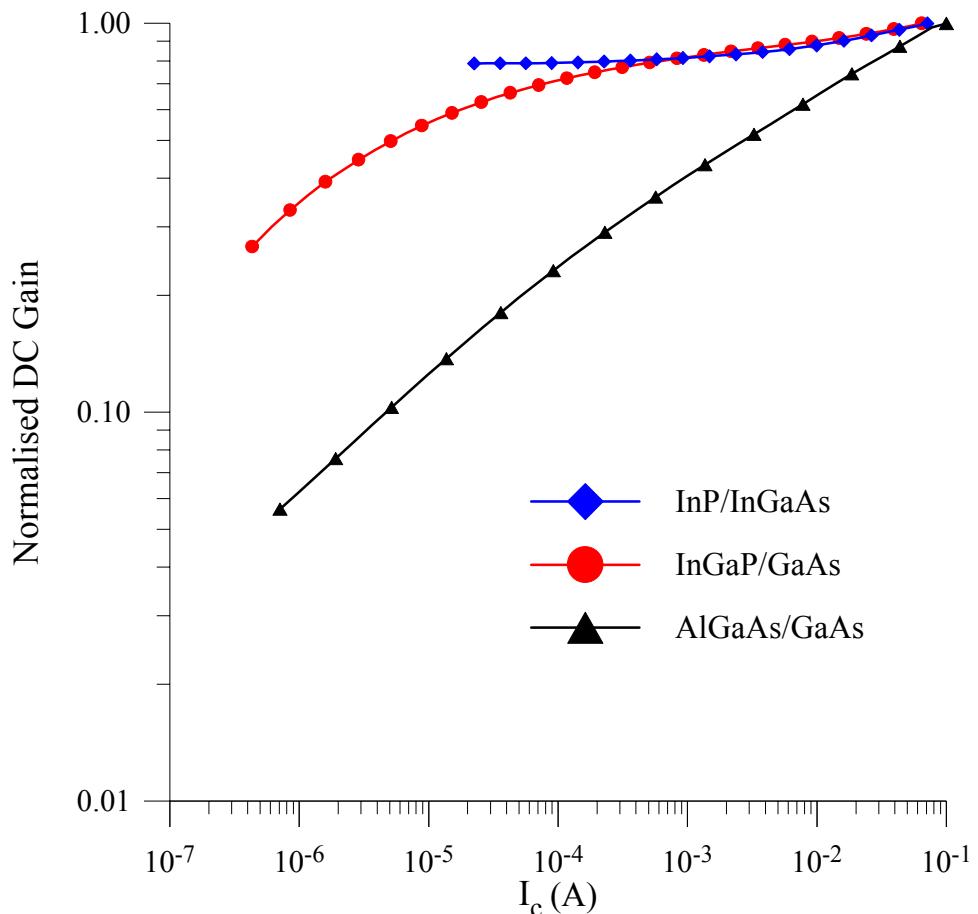


Figure 6.41: Normalised d.c. Gain versus I_c for AlGaAs/GaAs, InGaP/GaAs and InP/InGaAs HBTs. All devices have the same geometry and conventional ohmic contacts.

6.2.2.3 Optical Properties of HBTs

By using a transparent ITO emitter contact the performance of these devices improves significantly; this is particularly important in order to overcome practical difficulties in coupling optical radiation to microwave devices where emitter-base junction areas are in the order of a few $10\mu\text{m}^2$. The basic theory of the photo transistor was discussed earlier in sections 2.4 and 2.5; a schematic device structure of an InP/In_{0.53}Ga_{0.47}As HPT with transparent ITO emitter ohmic contact is shown in Figure 6.42. Incident photons pass through the ITO contact and the wide band gap emitter “window”; they are then absorbed in the base and collector regions of the HPT, creating electron-hole pairs. The photo generated holes accumulate in the base and alter the base-emitter potential so that electrons are injected from the emitter into the base. Internal gain is then achieved through normal transistor action when the base width w_b is less than the diffusion length of the injected electrons L_{nB} and whereby light absorbed affects the base current giving multiplication of photo current through the device [200].

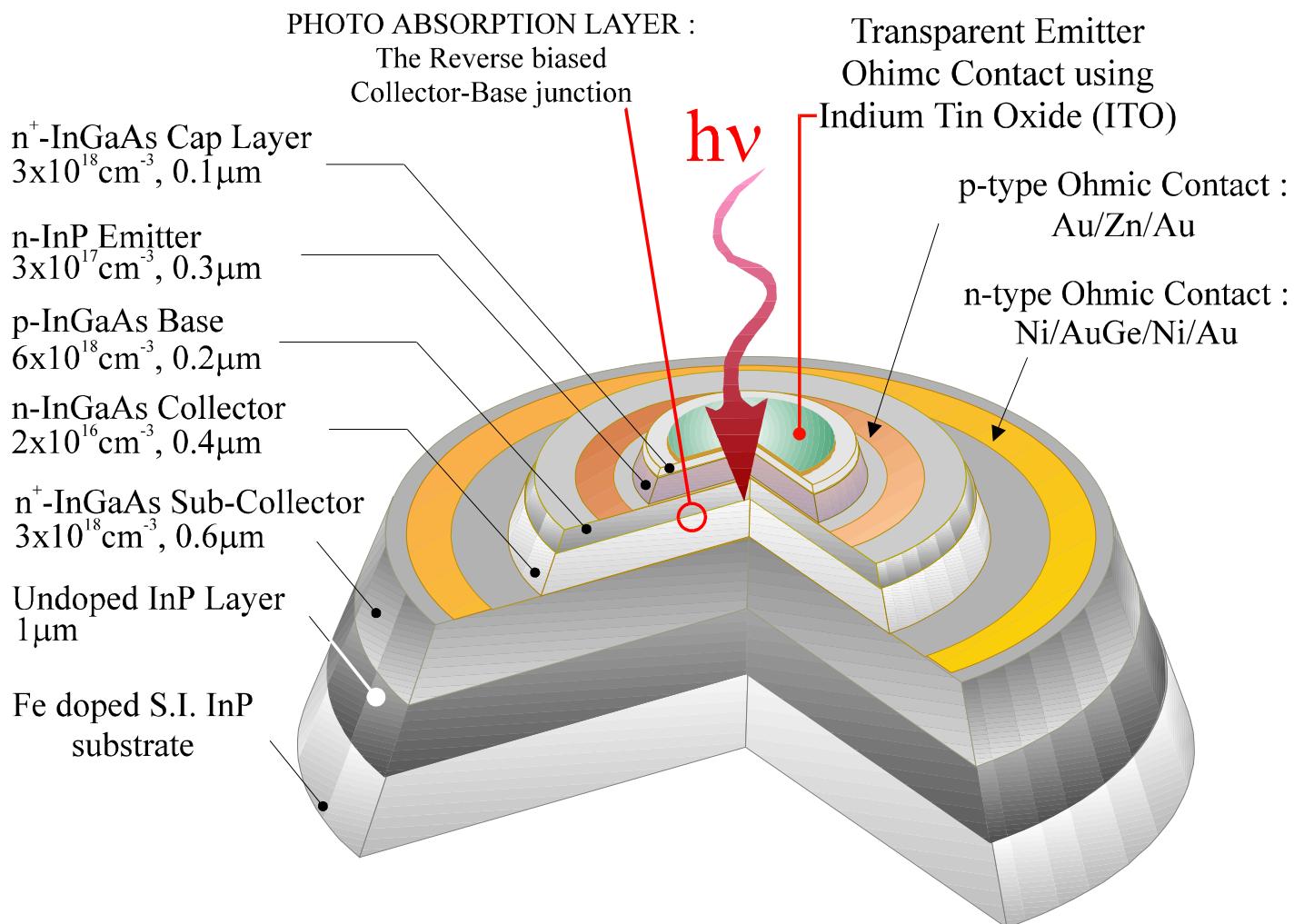


Figure 6.42: Schematic device structure of an InP/In_{0.53}Ga_{0.47}As HPT with transparent ITO emitter ohmic contact.

6.2.2.3.1 Output Characteristics

The measured common emitter electrical and optical characteristics of an InP/InGaAs HPT with ITO emitter contact is shown in Figure 6.43. Recall that the conventional ohmic contacts of these devices were not annealed and as a result have large emitter series resistance; its effect is apparent in the slope of the collector current. Otherwise, there is no noticeable difference in the device output characteristics with the base terminal physically disconnected or having base lead connected but the electrical base current, I_b set to zero. The wavelength of the optical signal was 780 nm.

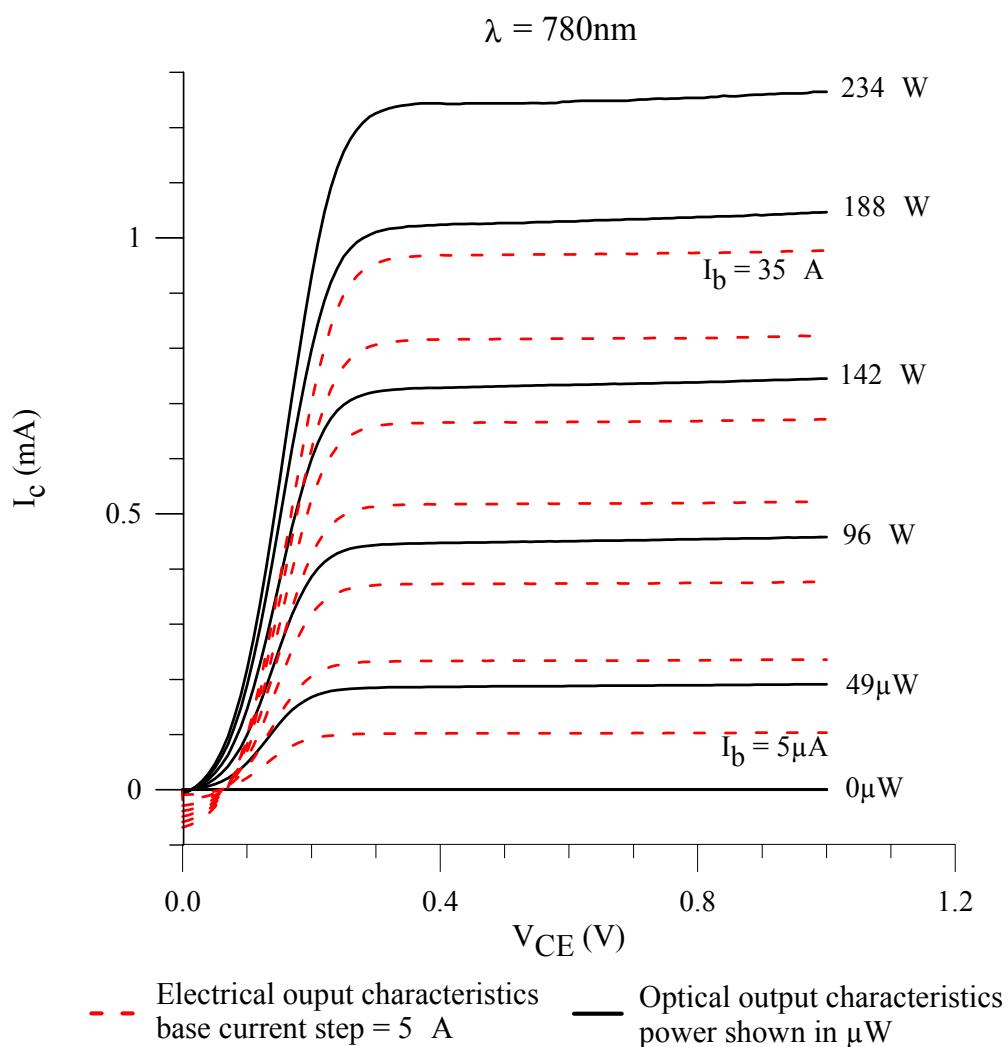


Figure 6.43: Measured common emitter electrical and optical characteristics of an optically transparent emitter contact InP/InGaAs HPT fabricated using ITO. $\lambda = 780\text{nm}$.

These results show that there is no significant degradation of the active substrate layers or the device characteristics as a result of r.f. sputtering used in the ITO deposition apart from those already discussed in section 6.2.2.2.4. It is also seen that at a constant illumination, the collector current is constant with the applied voltage indicating that there is no base width modulation or avalanche multiplication in the base/collector region. Figure 6.43 also shows that the HPT can be controlled both optically and electrically or by a combination of both sources. This represents the potential to use a single device for the simultaneous detection and amplification of an optical signal as well as its subsequent coupling with an electrical signal in a single device.

Another notable feature of Figure 6.43 is that there is a shift in the collector offset voltage, ΔV_{CEo} , of the electrical and optical output of the photo transistor. Whereas the ΔV_{CEo} is approximately 60mV for the electrical mode, the corresponding measured value for the optical output curves is 15mV. Recall that ΔV_{CEo} arises from the inherent differences in the turn-on voltages of the emitter-base heterojunction and the base-collector homojunction. A lowering in $V_{t(B-E)}$ or an increase in $V_{t(B-C)}$ as a result of the induced photo voltage across either of these two junctions respectively could explain the apparent reduction in the offset voltage of the photo transistor. However, in view of the accepted HPT operation theory, it is likely that the actual turn on voltages for the junctions remain unchanged. Because the photo voltage across the base emitter is such that it seeks to forward bias that junction, the electrical voltage, which is the voltage which affects the ΔV_{CEo} , required to turn on the p-n junction is much smaller.

Figure 6.44 shows the optical characteristics generated by illuminating the device with a 1310 nm laser. This shows the suitability of these devices for operation at telecommunication wavelengths. It can be seen that for a comparable incident optical power, the corresponding electrical output of the HPT is approximately five times greater than when it was illuminated by a 780 nm solid state laser. Another less desirable feature of this plot is that the slope of the output I-V curves is less and less steep at high current levels and is indicative of a presence of large emitter series resistance. This resistance, as discussed earlier, is associated with the ITO deposition process involving r.f. sputtering. No other obvious deleterious effects are noticed in the optical output characteristics of HPTs with transparent ITO emitter contacts.

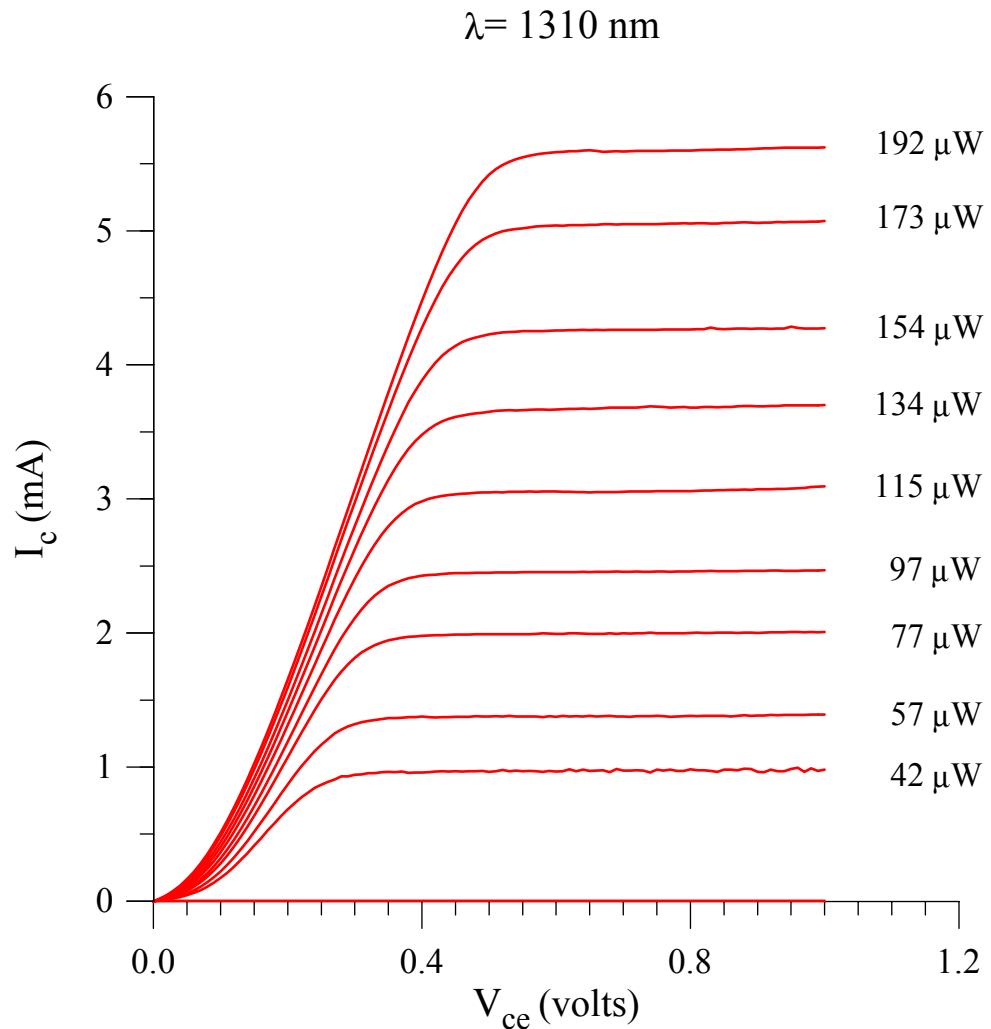


Figure 6.44: Measured optical output characteristics of an ITO emitter contact InP/InGaAs HPT.

The d.c. current gain, β of the InP/InGaAs HPT was found to be 28 which is similar to those of devices fabricated on the same substrate material using conventional opaque emitter ohmic contacts. In order to understand the relationship between the optical gain and the d.c. current gain, the responsivity of the base-collector p-n junction diode was measured; note that this junction can also be effectively treated as a p-i-n photo diode. The experimental setup was kept the same as that for the HPT optical characterisation; the emitter terminal was electrically disconnected and the base terminal was activated. As before, a series of forward and reverse I-V plots were made under known optical illumination levels and the respective optical responsivities were calculated. These were then compared with the responsivity of the device operating under the three terminal device mode.

Figure 6.45 shows the ratio of the responsivity of the InP/InGaAs HPT to the responsivity of the base-collector photo diode vs. optical power at $\lambda = 780$ nm. From eqn. 2.46 (see section 2.5), this ratio is approximately equal to β , and is shown to be the case by our experimental

results. Similar measurements were made for a set of AlGaAs/GaAs HPTs and found to confirm the relationship between the optical gain G , the electrical gain β and the photo diode responsivity at a given wavelength.

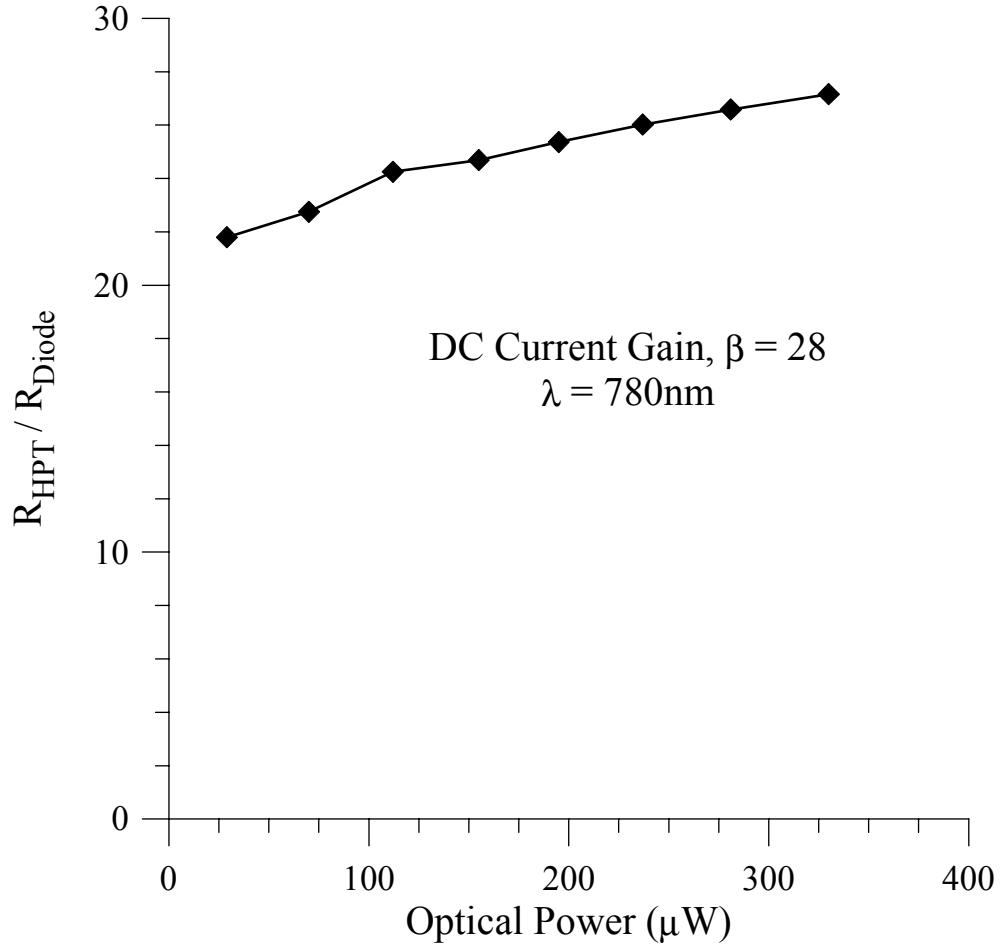


Figure 6.45: Ratio of the responsivity of the InP/InGaAs HPT to the responsivity of the base-collector photo diode vs. optical power at $\lambda = 780$ nm.

Since Figure 6.45 is also representative of the optical gain G , the relative flatness of this ratio versus the incident optical power should be noted. Given the similarly flat features of the d.c. current gain of these InP/InGaAs HPTs presented earlier in the thesis, one can conclude that SCR recombination in the base-emitter junction does not have any significant effect on the optical gain. In the presence of such “defect currents” the responsivity at low optical power would be significantly reduced as reported by many previous workers [112,191,201].

6.2.2.3.2 Spectral Response and Absolute Responsivity

Figure 6.46 shows the measured and simulated spectral response, normalised to the maxima, of the ITO emitter contact InP/InGaAs HPT. The measured spectral response is divided by

the blackbody radiancy (from the tungsten filament lamp in the monochromator) corresponding to each wavelength or is ‘deconvoluted’ to observe the actual device characteristics at various wavelengths.

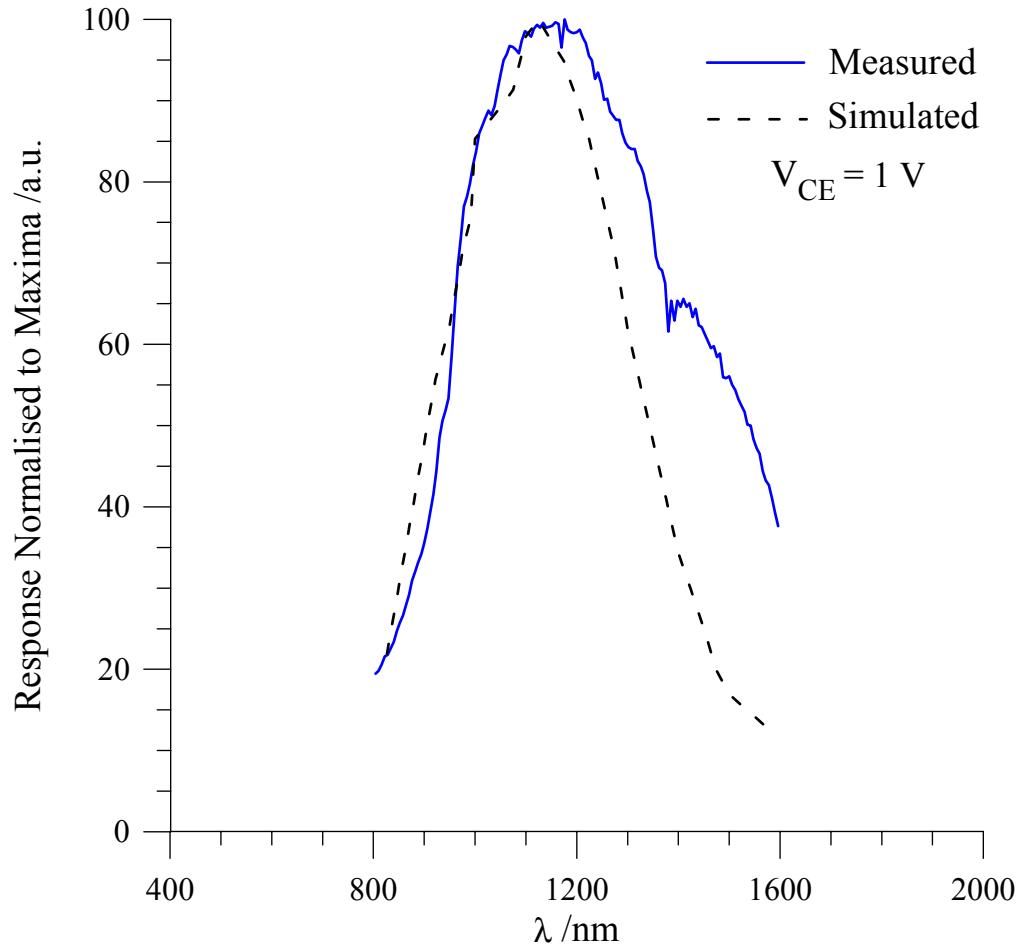


Figure 6.46: Measured and simulated spectral response, S_λ , of ITO emitter contact InP/InGaAs HPT

The long wavelength cut-off is determined by the absorption edge of the narrow-bandgap base and collector. For $In_{0.53}Ga_{0.47}As$ this corresponds to a wavelength of approximately $1.65\mu m$. At shorter wavelengths ($< 0.95\mu m$), the photoresponse is limited by absorption in the InP emitter [202] as well as the ITO transmission and the monochromator grating efficiencies. The dip in the spectral response at around 1400nm corresponds to atmospheric absorption of radiation from the monochromator and is not a reflection of the device characteristic. This atmospheric absorption in the wavelength range $1340\text{-}1450\text{nm}$ is most likely due to moisture and CO_2 [203]. The suitability of the InP/InGaAs devices for operation at 1310 nm and 1550 nm wavelengths is again clearly demonstrated in Figure 6.46.

The simulation model is discussed in detail in section 6.3 and has been the subject of a journal publication [204]. However, using this model, the adverse effect of the InGaAs cap

layer on the opto-coupling to the active base-collector layers was identified. A notable portion of the long wavelength ($\lambda > 960$ nm) incident photons are absorbed in this first layer of the InGaAs material before arriving at the active absorption layers. Further study and optimisation is required to minimise this effect which reduces the overall coupling efficiency without sacrificing the good ohmic properties that are associated with the InGaAs cap layer. Any mismatch between the simulation and the measured data is due to the uncertainties in the literature for the optical properties of the materials used, the lack of absolute device layer dimensions and the atmospheric absorption around 1400 nm.

It is seen that the peak responsivity for these InP/InGaAs HPTs is around the 1200 nm wavelength. From a telecommunications applications perspective, ideally the peak should correspond to 1550 nm. In order to achieve this, the overall width of the active absorption region (the base and the collector thicknesses) need to be increased. As increasing the base width would swiftly reduce the device gain [201], the collector layer thickness would be the most suitable parameter which should be tuned to further tailor these devices for this particular application.

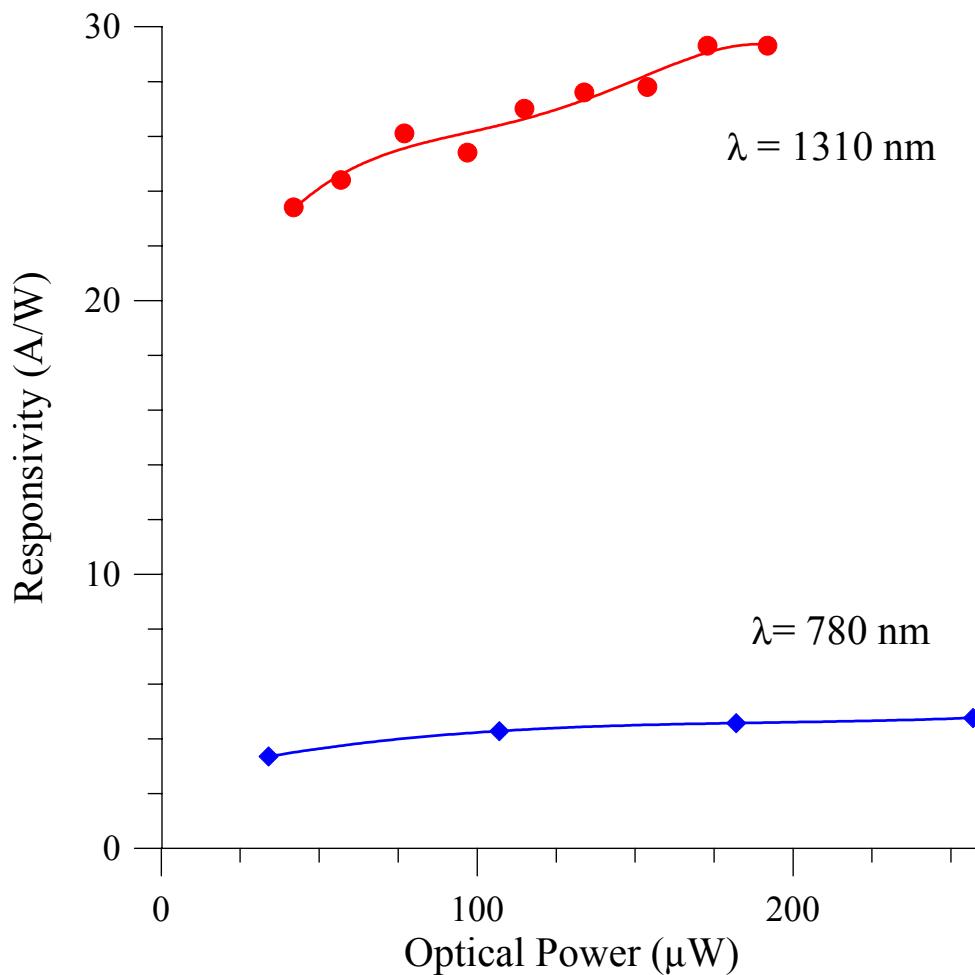


Figure 6.47: Responsivity vs. optical power for InP/InGaAs HPT at $\lambda = 780$ nm and 1310 nm.

Device responsivities of up to 30A/W and 22A/W at 1310 nm and 1550 nm wavelengths respectively were suggested by the spectral response measurements normalised to 780 nm. Figure 6.47 shows the measured absolute responsivities vs. optical power for InP/InGaAs HPT at $\lambda = 780$ nm and 1310 nm respectively. The responsivity of these HPTs at $\lambda = 780$ nm was 5.4A/W, and as expected, the responsivity at $\lambda = 1310$ nm was found to be 28A/W. This is about five times the value at 780 nm as shown in the normalised spectral response in Figure 6.46. Although greater absolute responsivities have been reported for opaque InP/InGaAs HPT devices [95,190], our low values can be attributed to the relatively low internal d.c. current gains of the devices rather than poor external optical coupling efficiency.

Finally, the measured and normalised spectral response of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ (wafer no. 1-1408) and $\text{InP}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (wafer no. 3-089) HPTs with ITO emitter contacts are presented in Figure 6.48 for comparison.

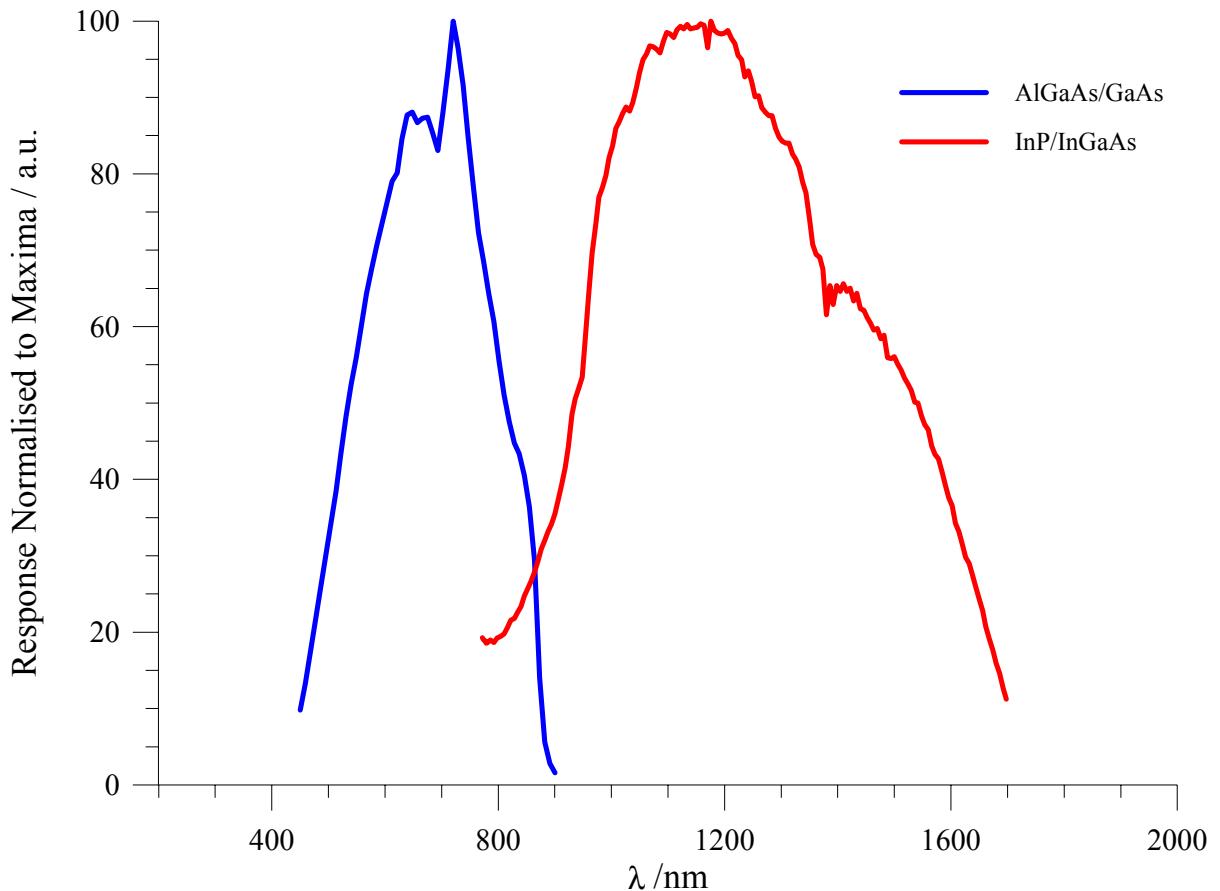


Figure 6.48: Measured spectral response, S_λ , of ITO emitter contact $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ (wafer no. 1-1408) and $\text{InP}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (wafer no. 3-089) HPTs.

Apart from the obvious difference in the bandwidth of the respective spectral response for the HPTs fabricated from the two different material systems, there is in fact a similarity between

them. In contrast with some of the results in the literature, both AlGaAs/GaAs and InP/InGaAs HPTs used in this study have spectral responses which rise gradually to a rounded peak and drop off steadily. Spectral response for HPTs made from these material systems as well as other semiconductor compounds have been studied by a number of workers: [82,112,205] (AlGaAs/GaAs); [202] (InP/InGaAs); [206,207] (InP/InGaAsP); and [84] (GaAs/Ge). Much of their work involved devices with very wide device layers (which were typically 5 to 6 times greater than those in the devices used in this study). As a result, the responses in the literature have very sharp edges and often a flat peak. While the rapid drop at the higher wavelengths is attributable to a thick absorption layer, a sharp rise at the lower wavelengths is most likely due to the absence of a narrow band gap cap layer over the emitter “window” in most of the early studies reported in the literature.

In these devices, absorption begins in the cap layer, followed by the emitter, then the cumulative base/collector volume. Photo generated electron-hole pairs in the cap and the emitter layer do not undergo amplification by the transistor action, and therefore only give rise to a relatively small response. On the other hand photons absorbed in the active region are amplified and are represented in the peak of the response. Therefore, the electrical gain of the photo transistor plays a significant part in shaping the overall spectral response; the other parameters include the material system, the thickness of the layers and other design constraints.

This point is illustrated in the results presented in Figure 6.48. The AlGaAs/GaAs device has a relatively low gain of 10 compared to nearly 30 of its InP/InGaAs counterpart. The spectral response largely due to the wide gap $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ material is represented in the shoulder to the left of the peak on the first curve; in case of the second curve belonging to the InP/InGaAs device, the spectral response due to the InP material is hidden under the amplified response from the InGaAs base/collector and hence there is no similar shoulder on the left hand side of the peak.

6.2.2.3.3 Top versus Edge Coupling and Design Considerations

In the absence of transparent contacts, coupling from the top becomes increasingly difficult as the emitter contact area is reduced in order to maximise the device bandwidth. Furthermore, for devices with non-absorbing collectors, such as double heterojunction bipolar transistors (DHBTs), very little absorption occurs when the incident light is introduced from the top. The situation is similar to TG-HEMTs where the vertically stacked thin absorption layers do

not provide sufficient depth for adequate photo generation and collection. This principle is further discussed in the following section, 6.3.

Therefore, by introducing the light from the edge of a HPT overcomes some of the limitations referred to earlier. Collection of photo-generated electron-hole pairs is maximised as the absorption volume now extends laterally across the device rather than vertically down it and therefore stretches over several carrier diffusion lengths. Wake *et al* have demonstrated high speed InP/InGaAs HPTs with quantum efficiencies of around 50% at an incident wavelength of 1480nm [95]. Inherent optical wave guiding is achieved in this structure since the absorption volume consisting of InGaAs is effectively clad by InP emitter and substrate; this is because InP has a lower refractive index than InGaAs.

A drawback, however, of this system is that the combined heights of the base and the collector ($0.5\mu\text{m}$) is still only a fraction of the minimum achievable laser beam diameter (for a lensed fiber this is $> 2\mu\text{m}$). As a result the coupling efficiency is greatly reduced. An investigation with the InGaP/GaAs HBTs with ITO contacts fabricated in this study to examine this effect however showed that the overall quantum efficiency at 780 nm for these devices was 50% and 40% for top and edge illumination respectively (discarding electrically induced gain of the device). However, it should be noted that these devices do not have a wide bandgap substrate which serves as a waveguide. Hence, a more careful comparison needs to be performed using InP/InGaAs devices at an appropriate wavelength where the InP is effectively transparent and the InGaAs material is highly absorbing. Since the absorption edge of InP is approximately 920 nm ($E_g = 1.35 \text{ eV}$) a 1310 nm laser would be highly suitable.

The external coupling efficiency in the edge coupled device can be increased by introducing a InGaAsP quaternary sub-collector below the InGaAs collector [208]. The InGaAsP has a refractive index which is between that of InGaAs and the InP semi-insulating layer. Thus introducing a thick InGaAsP based sub-collector not only increases the absorption volume but also acts as an additional optical waveguide to further improve the quantum efficiency. It should be noted that insertion of this additional layer in the InP HPTs also has the same potential advantage for a top illuminated device with a transparent emitter ohmic contact. A rigorous theoretical investigation of the performance limits of conventional p-i-n photo detectors when illuminated from the top and from the edge has been carried out by Kato *et al* [209].

6.3 Spectral Response of Photodetectors

In photo detectors the efficiency as a function of wavelength λ strongly depends on the absorption coefficient $\alpha(\lambda)$ [210]. The struggle to improve individual devices as well as integrate a number of functions on a single chip has led to a need to better understand the associated material properties. Therefore, accurate values of the refractive index, n , and the absorption coefficient of the materials used in the device structure are needed for proper device tailoring. A knowledge of these properties and their variation with material composition and wavelength is fundamental to the understanding of almost any conceivable travelling wave device [211].

Since the optical properties of materials vary according to their composition, only the systems with demonstrated importance in optoelectronics and device performance i.e. technological relevance will be considered. In the case of AlGaAs/GaAs HBTs, the preferred system consists of 27% Al and 73% Ga in the high bandgap $\text{Al}_{0.27}\text{Ga}_{0.73}\text{As}$ emitter which is lattice matched to the underlying GaAs base. On the other hand, InP/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ HBTs are usually grown on Fe doped InP substrates. Hence, the collector and base materials have to be lattice matched to InP; the preferred composition in this case is 53% In and 47% Ga in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap, base, collector and sub-collector layers.

In this section the refractive indices of the materials are first presented followed by the respective absorption coefficients. A table showing the minority carrier diffusion lengths in each of these materials is also shown. A model, to simulate the measured spectral response, S_λ , based on the principles of light transmission, absorption and reflection in different semiconductor materials is presented for the first time and shown to have extremely good correlation with the experimental data.

6.3.1 Spectral Properties of Relevant Materials

Device parameters such as the doping concentrations, the semiconductor layer thickness as well as the material properties such as the absorption coefficients, α , and the refractive indices, n , were used from the literature for the purpose of simulation [212,213,214,215]. A 100% collection efficiency is assumed for any electron-hole pairs photo generated inside the depletion region or within a diffusion length from it in the bulk material.

Figure 6.49 shows a plot of the experimentally measured refractive indices vs. wavelength for GaAs, AlGaAs, InP and InGaAs materials; the relevant data was obtained from the literature.

It is clearly seen that for the AlGaAs/GaAs system, the refractive index for the narrower bandgap material is greater than that of the large bandgap counterpart. This property is often used to design solid state optical waveguides, rather like optical fibers, to confine light inside a narrow bandgap material which is inserted between two layers of large bandgap material. The same can be noticed for the InP/InGaAs system. Indeed, this property is often a prime advantage for edge coupled optical detectors such as double heterojunction phototransistors made from the latter system.

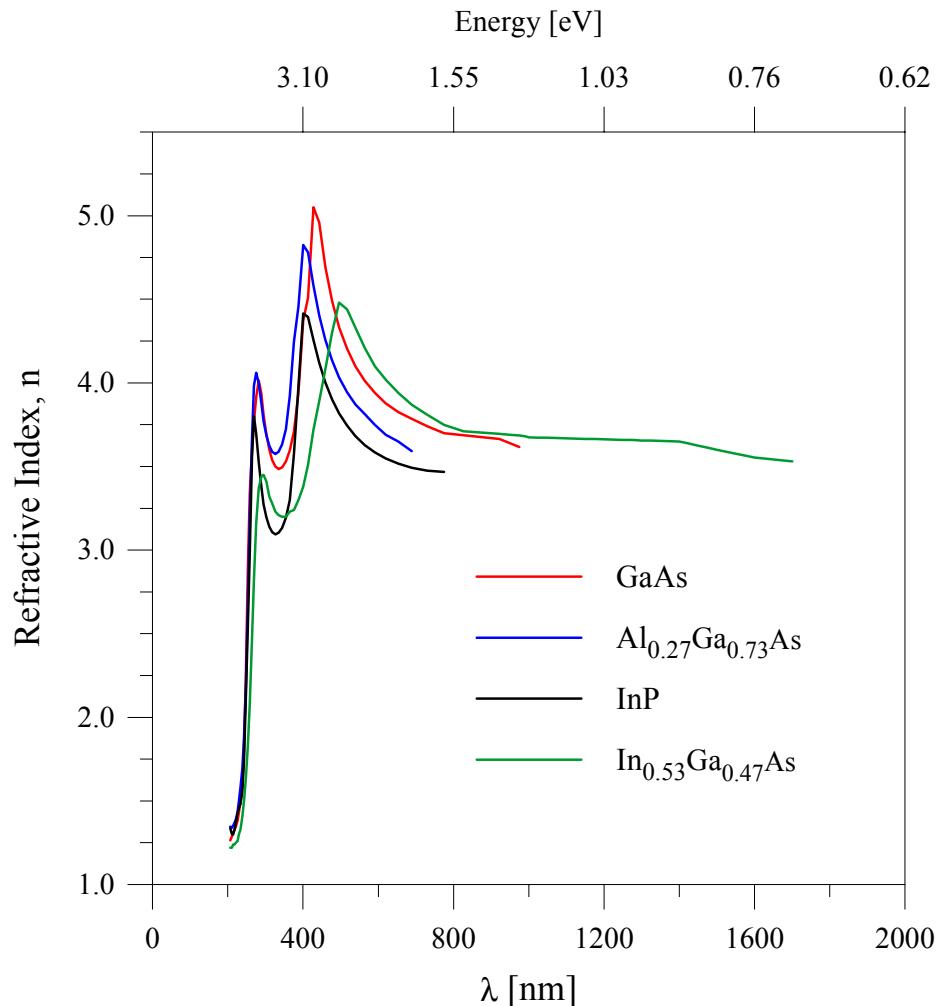


Figure 6.49: A comparison of the refractive indices for various semiconductor materials as a function of wavelength. (After ref. [212-215])

The optical data used for GaAs and $\text{Al}_{0.27}\text{Ga}_{0.73}\text{As}$ layers were obtained from the work by Aspnes *et al* [216]. 2 to 3 μm thick layers of AlGaAs were grown on Cr doped semi-insulating GaAs substrates by LPE. This work provides room-temperature pseudo-dielectric and related optical function data for $\text{Al}_x\text{Ga}_{1-x}\text{As}$ alloys for compositions x from 0.00 to 0.80 in steps of approximately 0.10. Hence, for the data used in the model in the case of GaAs, x is assumed to be zero and in the case of AlGaAs, x is assumed to be 0.3. The data was measured using an automatic rotating analyser spectro-ellipsometer. The authors report that

the detailed analysis of similar samples showed that typical differences between actual and target Al compositions do not exceed 0.03. Furthermore, they conclude that the data are accurate to within 2% of peak values for $x \leq 0.5$, the region of relevance for this study.

The optical data for InP is obtained from the work by Forouhi *et al* [213]. These spectral functions are deduced by indirect methods: they are determined through measurements of one or more extrinsic optical parameters which depend on them such as reflectance, transmittance and phase angle. Typical methods for determining the functions include: Kramers-Kronig analysis, comparison of measured and theoretical reflectance values, spectroscopic ellipsometry and modulation spectroscopy.

Finally, the data for InGaAs lattice matched to InP is based on the table by Adachi [214] for $\lambda \leq 0.83 \mu\text{m}$ and the work by Jenkins *et al* [215] for $1.0\mu\text{m} \leq \lambda \leq 1.7\mu\text{m}$. The table by Adachi relies on high precision pseudo-dielectric function spectra ellipsometrical measurements at room temperatures on LPE grown InGaAs materials.

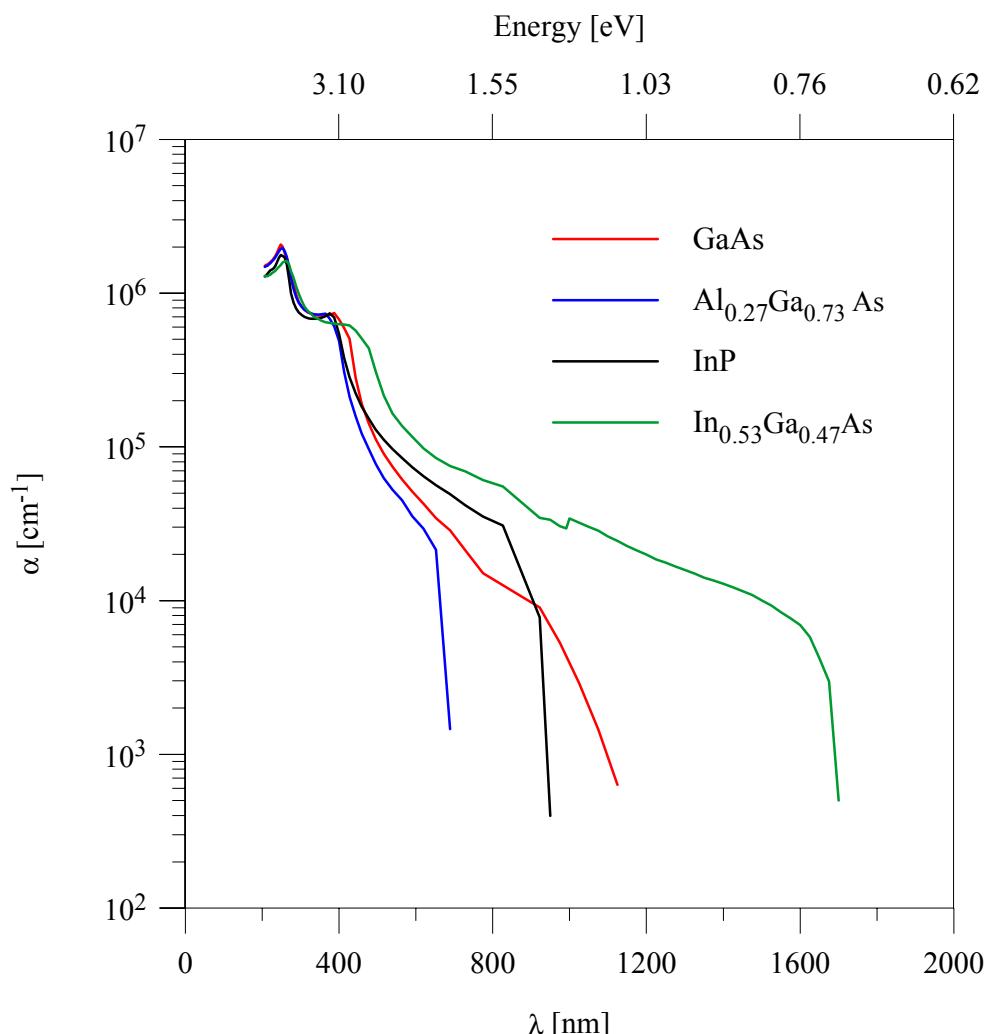


Figure 6.50: A comparison of the absorption co-efficients, α , versus the wavelength for various semiconductor materials. (After ref. [212-215])

Figure 6.50 shows the optical absorption co-efficients, α , for GaAs, AlGaAs, InP and InGaAs materials as a function of wavelength. From these plots, it is apparent that the absorption drops sharply at the edge of the respective bandgaps of each of these materials.

In addition to considering the optical properties, it is instructive to consider the electrical diffusion properties of these materials since almost all photo detection significantly depends on the diffusion fields in the absorption volumes. These are listed in Table 6.28:

Material	Doping Concentration [cm ⁻³]	Minority Carrier Diff. Length [μm]	References
n - GaAs	2x10 ¹⁶ (N _D)	1.8 (hole)	217
n ⁺ - GaAs	2x10 ¹⁸ (N _D)	1.2 (hole)	217
p ⁺ - GaAs	1x10 ¹⁹ (N _A)	2.5 (electron)	218
n - Al _{0.27} Ga _{0.73} As	1x10 ¹⁷ (N _D)	0.3 (hole)	219, 220
n - InP	3x10 ¹⁷ (N _D)	0.24 (hole)	221, 222
n - In _{0.53} Ga _{0.47} As	2x10 ¹⁶ (N _D)	0.4 (hole)	223, 224
p ⁺ - In _{0.53} Ga _{0.47} As	1 - 4x10 ¹⁹ (N _A)	0.4 - 4.0 (electron)	223, 225, 226

Table 6.28: Minority Carrier Diffusion Lengths of Various Materials

The doping densities in the above table have been chosen to represent the actual layers in the detector devices as closely as possible. Wherever data for exact specification was not found, the closest value with respect to doping concentration or in case of ternary materials the percentage composition was selected.

It should be noted that the minority carrier diffusivity is much more difficult to determine than the majority-carrier mobility [227]. Workers often extrapolate majority carrier mobility values to minority carrier values at the same doping level. For example to estimate the minority electron mobility at doping level N_A, one uses the electron mobility in n-type material at doping density N_D.

6.3.2 Spectral Response Model for a Monolayer Detector

As discussed earlier in Chapter 2, a semiconductor photo detector is capable of detecting only radiation with photon energy, $h\nu$, greater than the bandgap, W_g , of the device material. If however, $h\nu$ is much greater than W_g , then the absorption will take place entirely near the surface. This is because as the photon energy increases, their penetration depth decreases. Hence, the electron hole pairs created by absorbing the high energy photons near the surface of the detecting device (i.e., away from the junction or the adjacent diffusion fields) will recombine with majority carriers before diffusing into the depletion layer. This event does not contribute to the current flow and is not detectable.

Assuming the basic principles of optical detection are applicable, photo generation takes place where incident photons with super bandgap energies create electron-hole pairs; however, for these photo generated pairs to give rise to an external current, they must be collected before recombination leads to their annihilation. This can only occur if the photo generation takes place within the absorption volume which consists of the depletion region and the two diffusion regions on either side of it. As Table 6.28 demonstrates, the materials involved in this study, AlGaAs, GaAs, InP and InGaAs all have a diffusion length typically in the region of a few micrometers while the devices have active layers which have thicknesses usually a fraction of or smaller than these values. This means that in all cases the photo generation takes place within the absorption volume, hence justifying the assumption of a 100% collection efficiency. Let us consider one of the layers of the photo transistor, layer 2, bounded at 'A' by layer 1 and at 'B' by layer 3 as shown in Figure 6.51 below:

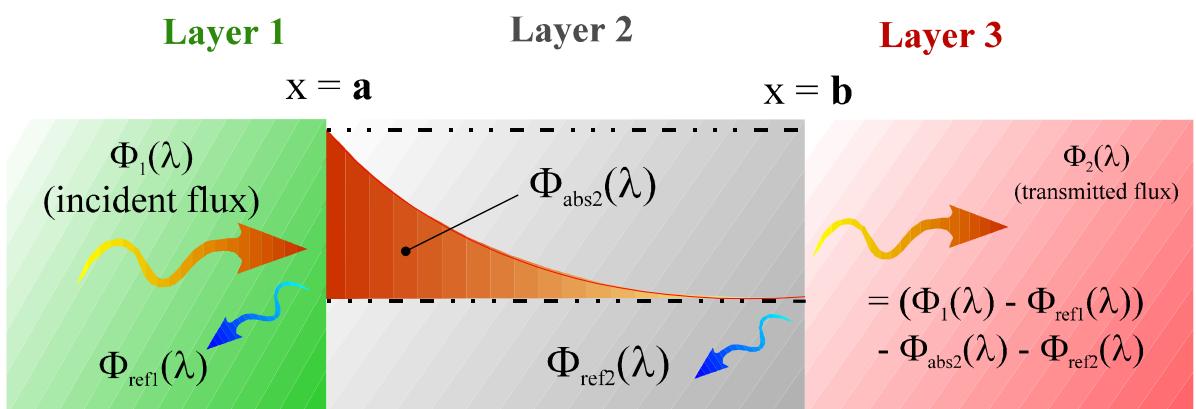


Figure 6.51: Schematic of optical flux propagation, absorption and reflection for a multilayered semiconductor device

Each of these layers is assumed to have homogenous material properties and constant doping concentration. Thus the flux absorbed as a function of the wavelength, λ , for layer 2, $\Phi_{\text{abs}2}(\lambda)$, can be expressed as:

$$\Phi_{\text{abs}2}(\lambda) = [\Phi_1(\lambda) - \Phi_{\text{Refl}}(\lambda)] \times \{\exp^{-[a\alpha_2(\lambda)]} - \exp^{-[b\alpha_2(\lambda)]}\} \quad (\text{eqn. 6.17})$$

where,

- Φ_1 = the incident flux from layer 1 at the layer1/layer 2 interface
- α_2 = the absorption coefficient of layer 2,
- a = the distance of the first boundary of layer 2 from the air/ITO interface
- b = the distance of the second boundary of layer 2 from the air/ITO interface
- Φ_{refl} = the reflected flux from layer 1 at the layer1/layer 2 interface;
this is given by [132]:

$$\Phi_{\text{refl}}(\lambda) = \left[\frac{(n_2 - n_1)}{(n_2 + n_1)} \right]^2 \quad (\text{eqn. 6.18})$$

where,

- n_1 = refractive index of layer 1 at a given λ
- n_2 = refractive index of layer 2 at a given λ

In the case of layer 1, here being the ITO contact, the incident flux is calculated from the measured transmission spectrum of the ITO layer and the two reflections at the air/ITO and ITO/cap interfaces.

Thus, for a given device made of a homogeneous material (e.g. GaAs), the thickness required to absorb a given fraction of the incident light increases sharply as its absorption co-efficient, α , drops (or as the penetration depth increases). As shown earlier in Figure 6.50, for most direct bandgap semiconductors, the absorption co-efficient sharply drops near the band edge. The effect of a change in α is clearly demonstrated in Figure 6.52 by plotting the fraction of the incident light absorbed vs. absorption layer thickness (difference between 'b' and 'a') using (eqn. 6.17) for three different values of the absorption coefficient.

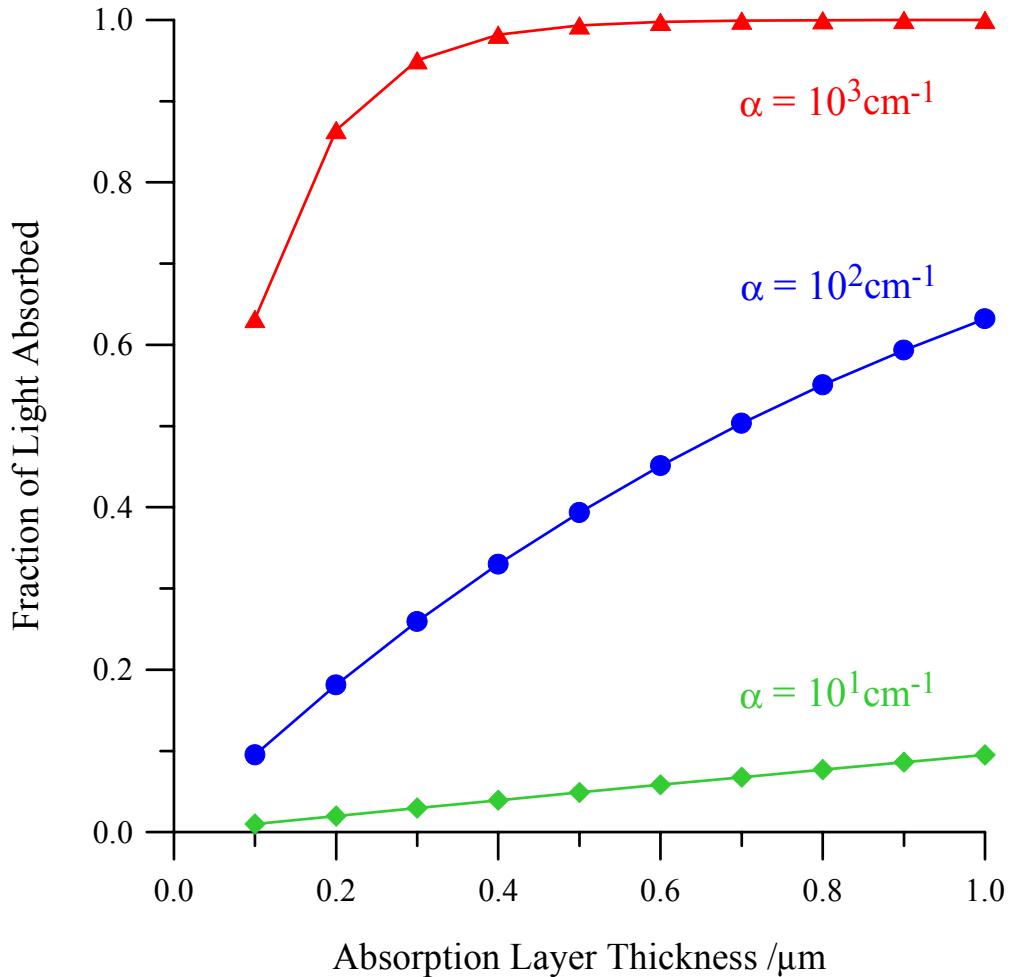


Figure 6.52: Calculated effect of absorption thickness on the amount of light absorbed for different values of absorption co-efficients

Conversely, as the energy of the incident photons approaches the band edge of the semiconductor material, thicker and thicker absorption layers are required in order to produce a given number of photo generated electron hole pairs. Taking these factors into account, it follows that for a given material system at a given wavelength the response is greater for the structure which has the thicker absorption region. Figure 6.53 shows the simulated effect of altering only the absorption thickness on the spectral response of a photo detector.

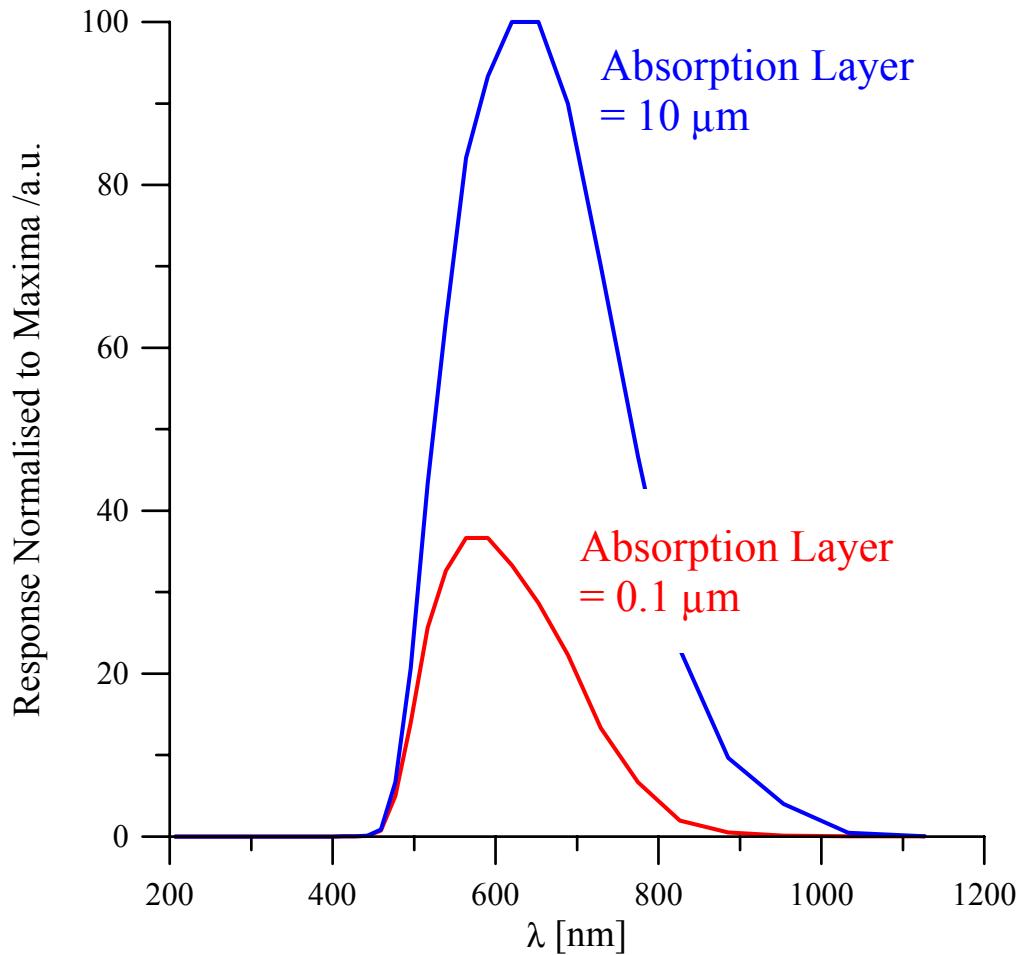


Figure 6.53: Calculated effect of absorption layer thickness on the spectral response for a monolayer detector

It is seen from Figure 6.53 that not only is the overall peak of the response reduced as a result of having a thinner absorption layer, but there is also a distinct shift in its shape. Reducing the thickness by an order of magnitude shifts the peak to a lower wavelength corresponding to a higher energy. This is because for a thinner absorption layer, only the photons with high energy (or for which the material has higher absorption co-efficients) have the optimum match between the (low) penetration depth and the absorption thickness. Therefore there is a fundamental influence on the spectral response of a photo detecting device purely arising its geometrical dimensions. Hence, this model is able to exploit yet another design parameter for such a device to optimise and tailor its response according to specific requirements.

6.3.3 Spectral Response of an ITO/n-GaAs Schottky Diode

In order to demonstrate the model, the measured and simulated spectral responses of an ITO/n-GaAs Schottky photo diode will now be presented. This device is so chosen as it consists of a single material (n-GaAs) absorption layer. The structure of the device is the same as those presented earlier in section 6.1.2.

Figure 6.54 below shows the measured and simulated results of the spectral response of such an ITO/n-GaAs Schottky diode:

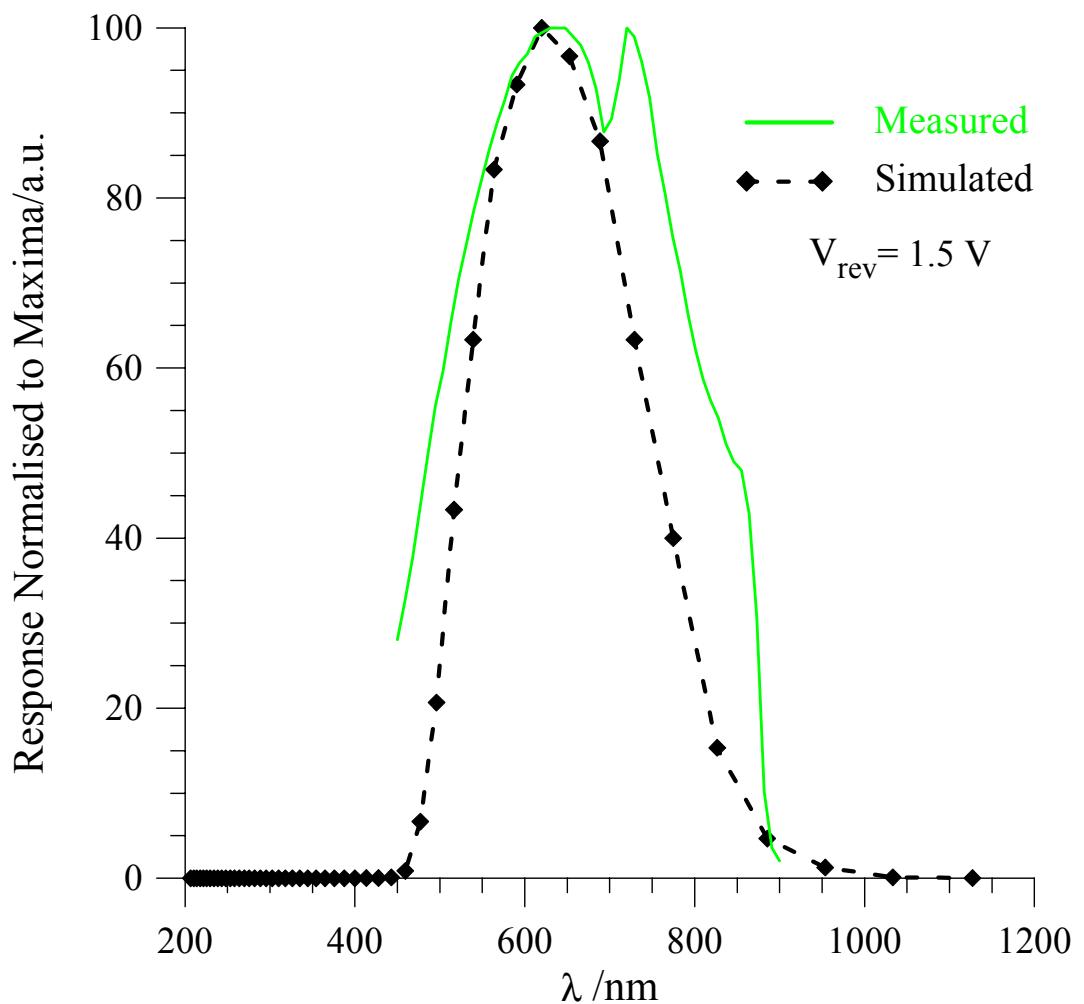


Figure 6.54: Comparison between measured and simulated Spectral Response of an ITO/n-GaAs Schottky Diode

This device is represented by modifying (eqn. 6.17) and using the basic principles to determine the amount of actual absorption in the active layer of the photo diode. Therefore, the responsivity, R as a function of the wavelength, λ for the Schottky diode is given by:

$$R(\lambda) = \Phi_o(\lambda) \times [1 - R_1(\lambda)] \times T_{ITO}(\lambda) \times (1 - R_2(\lambda)) \times \Phi_{abs}(\lambda) \quad (\text{eqn. 6.19})$$

where, at a given wavelength,

- Φ_o = the flux incident at the air/ITO surface
- R_1 = reflection caused at the air/ITO interface
- T_{ITO} = transmission of ITO
- R_2 = reflection caused at the ITO/GaAs interface
- Φ_{abs} = flux absorbed in the semiconductor active layer (calculated using (eqn. 6.17))

The spectral response, S_λ , can thus be found by integrating over the entire operational wavelength range :

$$S_\lambda = \int R(\lambda) d\lambda \quad (\text{eqn. 6.20})$$

6.3.4 Spectral Response of a HPT with ITO Emitter Contact

For the HPT the generic equation (eqn. 6.20) is used for each layer in succession with the appropriate values of α , n and the layer thickness to determine the theoretical absorption; in order to calculate the absorption in each layer, any reflection and absorption in previous interfaces and layers is thus accounted for. Subsequently, the device responsivity at a particular wavelength is given by:

$$R_{HPT}(\lambda) = \Phi_{cap}(\lambda) + \Phi_{emitter}(\lambda) + \Phi_{collector}(\lambda) + \beta[\Phi_{base}(\lambda) + \Phi_{collector}(\lambda)] \quad (\text{eqn. 6.21})$$

where

Φ_{cap} , $\Phi_{emitter}$, Φ_{base} and $\Phi_{collector}$ are the respective fluxes absorbed in the (n^+ -GaAs or n^+ -InGaAs) cap layer, the (n -AlGaAs or n -InP) emitter, the (p^+ -GaAs or p^+ -InGaAs) base and the (n -GaAs or n -InGaAs) collector at a given wavelength, while β is the common emitter current gain of the transistor.

Hence, the spectral response, S_λ , is found by integrating (eqn. 6.21) over the entire operational wavelength range:

$$S_\lambda = \int R_{HPT}(\lambda) d\lambda \quad (\text{eqn. 6.22})$$

The simulated and measured spectral responses of the AlGaAs/GaAs (wafer no. 1-1408) HPTs are shown in Figure 6.55. The corresponding plot for the InP/InGaAs (wafer no. 3-089) devices was shown in section 6.2.2.3.1 (see Figure 6.46).

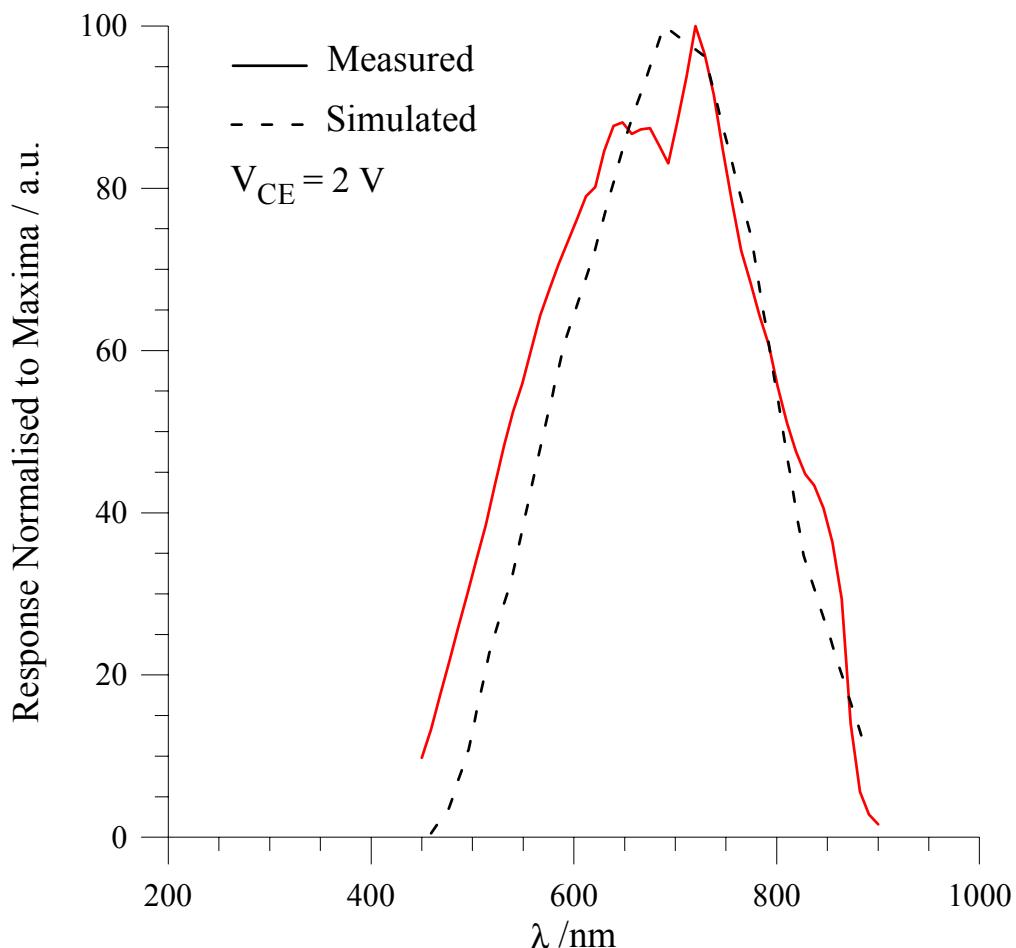


Figure 6.55: Measured and simulated spectral response, S_λ , for AlGaAs/GaAs HPT devices with ITO emitter contact ($V_{CE} = 2V$).

Some of the apparent mismatch between the simulation and the measured data is due to the uncertainties in the literature, the lack of absolute device layer dimensions and non-linear effects of the monochromator around 800nm (for the AlGaAs/GaAs case) and the atmospheric absorption around 1400nm (for InP/InGaAs devices) as discussed in section 6.2.2.3.

7. Conclusion

In order to investigate the use of optically transparent indium tin oxide (ITO), a range of technological steps were developed and optimised during the course of this study. These include reactive r.f. sputtering, reactive ion etching, careful optimisation for producing ideal Schottky contacts, annealing for producing good ohmic contacts using ITO and metal ohmic contacts on ITO itself. A number of novel optoelectronic devices were fabricated as a result including: transparent metal contact Schottky photo diode [228], transparent gate HEMT (TG-HEMT) [79], transparent electrode VCSELs [88] and LEDs and transparent emitter contact HPTs [2].

7.1 ITO Deposition

A reactive r.f. sputtering technique using an argon/oxygen mixture was utilized for the deposition of the Indium Tin Oxide films from a hot pressed target. A number of deposition parameters and their effects on the films were studied in detail. In particular the partial pressure of gaseous oxygen, PO_2 , in the plasma and the r.f. power, directly affecting the deposition rate, were found to be amongst the most influential. While the conductivity was found to be inversely proportional to the exponential of the PO_2 , the transparency reduced significantly in the absence of sufficient oxygen. The r.f. power was directly proportional to the film conductivity. These parameters were then optimised to maintain the desired combination of high transparency and conductivity properties of the films and to minimise sputter damage to the substrate material constituting the active device layers. The critical values for PO_2 and the r.f. power used were 14×10^{-3} (at a total pressure of approximately 10 mTorr) and 150W respectively.

Using this technique, highly conductive uniform ITO films were obtained. The as deposited sheet resistance, R_{sh} , was typically $340 \Omega/\square$ which reduced to $27 \Omega/\square$ after annealing. These values correspond to resistivities of $190 \times 10^{-4} \Omega\text{cm}$ and $15 \times 10^{-4} \Omega\text{cm}$ respectively and compare favourably to those in the literature. Above 90% transmittance was achieved for these ITO films over the 500nm to 2000nm wavelength range. This corresponds to 2.48eV to 0.62eV energy range which covers majority of the III-V compound semiconductors such as AlAs, AlGaAs, GaAs, InP and InGaAs as well as Si and Ge. For a typical ITO film, the value of the bandgap calculated from the transmission spectra was found to 3.8eV, which is in close agreement with previously published work.

7.2 ITO-based Microfabrication

Driven by the need to produce near micron structures with ITO films, a number of experiments were carried out to develop a suitable method for micro-patterning these films. Due to the energetic species inside the sputtering chamber, resulting in baking of the photoresist, liftoff lithography was rendered unsuitable. Wet chemical etching involving a number of chemicals, such as HCl, HNO₃ etc., in various strengths as well as Zn dust as a catalyst were tried and were also found to be unsatisfactory for this delicate application. Finally a selective dry etching technique based on reactive ion etching (RIE) with Ar gas was developed; a 1000Å thick layer of Al metal was used as the mask. As well as having a very good selective etch ratio of greater than 4:1 for Al:ITO, the use of Ar as the plasma gas is both cheaper and safer. Two micron fingers were successfully produced using this etching technique. The optimum r.f. power and the chamber pressure RIE system was found to be 100W and 11mtorr respectively.

Two distinct sets of post deposition annealing techniques were developed. One of these was to obtain an ITO/n-GaAs Schottky diode with rectifying contact with low series resistance while retaining the diode parameters for a good device. A two step process extended over several hours was used to ensure the reduction of ITO film resistivity and the recovery of sputter damage from the substrate without affecting the rectifying properties of the device. A five hour anneal at 240°C followed by another five hours at 340°C in a N₂ ambient was found to produce these desired results.

The other annealing technique was developed to produce a heterojunction photo transistor with essentially an ohmic contact to the emitter cap layer. Given that the stringent requirement not to destroy a rectifying junction is no longer applicable, the realisation of an ITO ohmic contact proved to be more difficult than at first imagined. Traditional annealing techniques with RTA or dual alloying methods were unable to produce good uniform ohmic contacts. Thus a new technique involving a step-like annealing method was employed. Samples were at first gently heated at lower temperatures (240°C) for relatively longer periods (3 minutes) and gradually the annealing temperature was increased to up to 500°C where it was placed for a shorter time (1 minute); the sample was cooled using the reverse temperature/time combination.

Using both these techniques, the resultant ITO resistivity was found to be approximately 14x10⁻⁴ Ωcm. This compares well with the published data.

Bearing in mind the need to form large metal pads for connection to external circuits, a set of experiments were performed to assess various metalisation schemes for making contacts to the ITO films themselves. These metalisation systems were Ni/AuGe/Ni/Au, Ni/Al and Ni/AuGe/Ni/Ti/Au; as well as the ohmic properties, mechanical adhesion was also a factor in these assessments. It was concluded that in the absence of an adhesion promoting layer such as Ni, the use of say only a layer of Au was unsuitable. Comparing the electrical properties of the three metalisation systems investigated, it is noticeable that their unalloyed characteristics were very similar (R_{sk} and ρ_c in the region of $50\Omega/\square$ and $3 \times 10^{-4} \Omega\text{cm}^2$ respectively) despite the fact that the sheet resistances of the corresponding ITO material varies over a much greater range ($1273 \Omega/\square$ to $665 \Omega/\square$). The R_{sk} after alloying for all three metalisations lie approximately in the range 1 to $2 \Omega/\square$ while ρ_c lie in the range 3 to $8 \times 10^{-5} \Omega\text{cm}^2$. Thus all three systems are equally suited for contacting ITO films as there is very little difference between them.

7.3 Optically Transparent Schottky Diodes

Following thorough cleaning and pre-metalisation chemical etch to the surface of MBE (Si) grown, n-GaAs wafers with $N_D = 1.4 \times 10^{16} \text{ cm}^{-3}$, $1.75\mu\text{m}$ thick active layers, near ideal Schottky diodes were produced using Au and Al as the metal contacts. The ideality factor, n , the barrier height, ϕ_{bo} , and the modified Richardson constant, A^{**} , for the Au/n-GaAs devices were 1.04, 0.84 eV and $12.5 \times 10^6 \text{ Am}^{-2}\text{K}^{-2}$; the corresponding values for the Al/n-GaAs diodes were 1.08, 0.77 eV and $16.0 \times 10^4 \text{ Am}^{-2}\text{K}^{-2}$. These values for both sets of devices are in good agreement with the findings of other researchers. The Schottky diodes were also characterised over a wide temperature range to provide a thorough understanding of their d.c. performance. The results analysed using a simulation model involving the influence of various current transport mechanisms at different temperatures. Excellent agreement was found between the measured and the simulated data.

In the quest for replicating near ideal Schottky diodes with an ITO film replacing the conventional metal contact in the previous set of diodes, numerous experiments were performed to finally achieve the desired goal. As well as thoroughly cleaning the wafer prior to ITO deposition, a number of sputtering parameters had to be optimised. Some of these, such as r.f. power and PO_2 and the relevant post-deposition annealing techniques, have already been discussed earlier. In addition, a thin layer of Indium metal, 100\AA , deposited between the ITO and the semiconductor was found to be effective in shielding the substrate from sputter damage. Thus ITO/n-GaAs Schottky photo diodes were realised with the following characteristics: $n = 1.1$, $\phi_{bo} = 0.76 \text{ eV}$, dark current at $-2\text{V} = 50 \text{ nA}$, series

resistance = 25.8Ω , responsivity to 780 nm radiation = 0.57 A/W and an external quantum efficiency, $\eta = 91.5\%$. These are amongst some of the best results obtained thus far and compare better than many reported in the literature for similar devices. Thus near ideal, ITO/n-GaAs Schottky diodes with low leakage current, low series resistance and high responsivity have been fabricated on n-GaAs epitaxial layers.

The effect of mesa etching, r.f. power, use of a thin layer of indium and gradual annealing at 340°C have been studied and optimised to produce near ideal photo diodes. Mesa etching significantly reduces the surface leakage current thus suppressing the dark current. Increasing the r.f. power reduces the sheet resistance of the ITO film but causes greater damage to the substrate; this damage can be minimised by depositing a thin layer of indium on the GaAs substrate prior to sputtering and the damage can be removed by gradual annealing.

A detailed C-V analysis was carried out to separate the effects of sputter damage from associated series resistance. It was concluded that sputtering causes two types of damage:

- (a) donor like effect at the surface results from knocking of Arsenic atoms by relatively large Argon ions in the plasma
- (b) damage induced traps due to high velocity particles penetrating deeper into the substrate are thought to be the cause of a progressively falling free charge carrier profile.

This requires further detailed study to understand both the cause and the nature of these defects.

These novel ITO/n-GaAs devices were then subject to cryogenic measurements similar to their conventional opaque counterparts. From the measurements, the modified Richardson constant, A^{**} , for these devices were found to be $1.3 \times 10^4 \text{ Am}^{-2}\text{K}^{-2}$, and to the best of our knowledge this is the first time it is being reported for ITO/n-GaAs devices produced by reactive r.f. sputtering.

Having thus obtained relatively large ITO/n-GaAs Schottky photo diodes, high speed diodes can be achieved by shrinking the active region; parasitic capacitances and leakage currents can be reduced by a combination of proton bombardment and mesa etch isolation techniques.

7.4 Transparent Gate HEMTs

As an extension of the work with ITO/n-GaAs Schottky diodes, a set of novel pseudomorphic HEMTs with a transparent gate (TG-HEMT) were fabricated using transparent indium tin oxide for the first time. These AlGaAs/InGaAs/GaAs pseudomorphic HEMTs (pHEMTs)

with ITO gate electrodes have an optical responsivity greater than 5A/W corresponding to an external quantum efficiency of greater than 800% for an incident radiation of $\lambda = 780\text{nm}$. A set of conventional devices were also fabricated for comparison using opaque Ti Schottky gates. This was performed in collaboration with another researcher in the group to demonstrate the viability of such devices and greater detail is available in [229].

7.5 Optically Transparent ITO Ohmic Contacts

The next part of this thesis involved the fabrication of good ITO ohmic contacts to highly conductive n and p type layers ($N_D = 5 \times 10^{18} \text{ cm}^{-3}$, $N_A = 5 \times 10^{19} \text{ cm}^{-3}$) of GaAs and n-type InGaAs layers ($N_D = 3 \times 10^{18} \text{ cm}^{-3}$). The objective was to realise good transparent contacts to the emitter of HBTs for vertical illumination of an optical signal. The TLM method was used for assessing the quality of these contacts. In each of these cases, the transparent ohmic contacts were compared to ohmic contacts made from conventional metals on the same substrates to enable a direct comparison to be made.

For the ITO/n⁺-GaAs contacts, the insertion of a thin layer of In metal between the semiconductor and the transparent film was found to be very effective in enhancing the ohmic properties of the contact. Although initially this reduced the transparency to nearly 60%, this parameter was restored to above 90% following the ohmic contact annealing scheme discussed earlier. It is believed that In acts as a doping species in n-type GaAs thereby reducing the specific contact resistance. The best transfer resistance, R_t , and the specific contact resistances, ρ_c , achieved in each case were as follows: $R_t = 0.68 \Omega\text{mm}$, $\rho_c = 1.2 \times 10^{-4} \Omega\text{cm}^2$ (n⁺-GaAs); $R_t = 0.49 \Omega\text{mm}$, $\rho_c = 7.6 \times 10^{-5} \Omega\text{cm}^2$ (In/n⁺-GaAs). Thus the superior quality of the ITO/In/n⁺-GaAs over the ITO/n⁺-GaAs ohmic is clearly demonstrated [230]. The corresponding values for the conventional contacts realised using the Ni/AuGe/Ni/Au metalisation system, were as follows: $R_t = 0.10 \Omega\text{mm}$, $\rho_c = 3.1 \times 10^{-5} \Omega\text{cm}^2$.

The values achieved for these parameters in case of the ITO/p⁺-GaAs contacts and their conventional counterparts fabricated using Au/Zn/Au metalisation system were $R_t = 0.55 \Omega\text{mm}$, $\rho_c = 3.2 \times 10^{-5} \Omega\text{cm}^2$ (ITO); and $R_t = 0.07 \Omega\text{mm}$, $\rho_c = 5.1 \times 10^{-6} \Omega\text{cm}^2$ (conventional) respectively. Although comparably good transparent ohmic contacts were achieved on p⁺-GaAs substrates, the increased difference between the transparent and their opaque counterparts is attributable to the absence of any obvious dopant species in the ITO contacts. Despite this absence, the main reason behind realising good p-type transparent ohmic contacts is likely to be due to the high substrate doping alone.

The results for the ITO/n⁺-InGaAs contacts and their conventional counterparts were as follows: R_t = 0.37Ωmm, ρ_c = 7.1x10⁻⁵ Ωcm² (ITO); and R_t = 0.10 Ωmm, ρ_c = 3.1x10⁻⁵ Ωcm² (conventional).

A brief surface morphology examination of the ITO contacts and subsequent comparison with the conventional metal contacts revealed some interesting results. It was seen that there was significant “balling-up” on the surface of the conventional contacts to the n⁺-GaAs substrates. The diameter of an average “mound” is approximately 5μm - comparable to, if not larger than, the dimensions involved in emitter finger widths of microwave HBTs. This effect is reduced but nevertheless it is still present in the p-type contact. By contrast, the metal on the ITO/n⁺-GaAs surface was smooth suggesting that there is no liquid phase reactions involved in the latter ohmic contact and ITO acts like a capping (such as Ti/Au) or a diffusion barrier (such as ZrB₂) layer preventing the intermixing of the top-most Au layer with the substrate causing the balling effect. Its demonstrated excellent surface morphology and edge definition is an added advantage in the fabrication of small geometry optoelectronic devices. This observation is further correlated by the fact that Sn present in ITO is also known to take part in solid phase reactions to n-GaAs in the formation of good ohmic contacts. However, like other solid phase schemes, such as Pd/Ge or Pd/Sn, the resistance is higher than that obtained for the Ni/AuGe/Ni/Au liquid phase n-type contact.

7.6 Optically Transparent HPTs

The penultimate part of the study concerned the study of heterojunction bipolar transistors fabricated on three different material systems: AlGaAs/GaAs, InGaP/GaAs and InP/InGaAs respectively [231]. This was followed by realisation of their counterparts fabricated using transparent ITO as the emitter contact. The measured electrical (d.c.) properties of the HBTs were then analysed. At first a comparison between the opaque and transparent set of devices was made; this was followed by a comparison between the HBTs fabricated from the different material systems. This electrical performance analysis was followed by an extensive study of the suitability of these devices as phototransistors [232]; a very brief demonstrational work was performed to compare the results of vertical illumination versus edge illumination.

One of the consistent findings from the electrical study was that the emitter series resistance for the ITO emitter contact devices was higher than those with conventional metal contacts. This directly affected a number of other parameters of the transparent emitter contact transistors such as the offset voltage which was higher compared to their conventional

counterparts. Further investigation revealed that the high series resistance could not be attributed to the resistance of the ITO layer or to the cap layer resistance alone. It also became apparent that the total contact resistance of the conventional devices also had other resistive components, albeit much less significant in comparison to the r.f. sputtered contacts. The additional resistance in the transparent contact must therefore be due to some sputter induced damage to layers deeper than the cap layer. It was also observed that the thin layer of In helps reduce this effect because preliminary devices without this intermediate metallic film had even larger R_{ee} . More detailed study is necessary to investigate this source of resistance and further reduction in the emitter resistance may be achieved by using a thicker layer of indium without causing significant reduction to the transmittance of the ITO contact.

A study of the Gummel plot showed that the overall reduction in I_c vs. V_{be} in comparison with the metal contact devices again points to the likelihood of possible damage caused to the emitter layer during r.f. sputtering which was not fully recovered during the ohmic contact annealing. This deep damage results in an increased base ideality factor suggesting increased SCR recombination at the base-emitter junction and also possibly greater base bulk recombination; As a result, the measured d.c. gain, β is consistently lower for the ITO emitter contact devices.

A study involving the C-V measurements on both these sets of devices suggested that there was a noticeable change on the doping profiles of emitter layers in the HBTs due to r.f. sputtering and that this does indeed give rise to a donor like effect in the affected regions. Recall, this is consistent with the findings of the work on the ITO/n-GaAs Schottky photo diodes. Furthermore, as there is no significant change in the collector doping profile, it was assumed that the sputtering effects are confined before the collector layer. Since the C-V profiling technique cannot yield the doping profile of the already highly doped p^+ GaAs base region, it is not possible to make definite conclusions based on these measurements about the effects of r.f. sputtering on that region.

A final feature of this work is the relationship between the effect of r.f. sputter induced damage on the base-emitter interface and the depth of this junction from the surface of the wafer. For example in the work with the InGaP/GaAs HBTs, it was seen that the base ideality factor for ITO contact devices fabricated on a wafer with a shallower base of 2725Å (this figure being the sum of the cap and the emitter layers) is 1.25 in comparison to 1.09 of their opaque counterparts indicating presence of sputter induced damage giving rise to increased SCR recombination at the heterojunction; in contrast, the difference in the n_{Ib} between ITO and metal contact devices is insignificant for the wafer with the deeper base of 5000Å. These results were also consistent with the work on the AlGaAs/GaAs HBTs on two

wafers with slightly different structures. The depth of the base/emitter hetero-interface for the InP/InGaAs was 4000Å and thus the damage sustained is less than in devices with shallower base/emitter junctions. Recall, that the effect of sputter damage was not noticeable for the base interfaces deeper than 5000Å.

Like their InGaP/GaAs counterparts, the InP/InGaAs material system also offers the advantages associated with selective etching during device fabrication resulting in uniform device characteristics across the wafer; this desirable property is reduced in case of the AlGaAs/GaAs HBT fabrication where no suitable selective etchants are available. The InP/InGaAs HBTs fabricated in this study, a low common emitter offset voltage (measured when $I_b \approx I_c \approx 0$) of 61mV and collector/emitter breakdown voltage of 5.5V were observed. However, it was evident from the output characteristics that InP/InGaAs HBTs have rather poor saturation characteristics with high output conductance unlike the complete saturation observed in typical GaAs-based devices. This is due to the high multiplication factor and the low breakdown voltage associated with the low band gap of the InGaAs material.

In order to compare the turn on voltages, V_t , of the AlGaAs/GaAs HBTs, with typical InGaP/GaAs and InP/InGaAs HBTs, the collector currents of three devices with same geometries but different material systems were plotted as a function of base emitter voltage with $V_{bc} = 0$. It is seen that the InP/InGaAs HBTs exhibit a lower turn on voltage (0.2eV) compared to GaAs-based HBTs (0.8eV). This clearly demonstrates the advantage of InP-based HBTs for low power circuit applications, such as mobile telecommunications [199].

From a comparison of the respective gain plots of the devices on different material systems, it was evident that while the AlGaAs/GaAs β varied with I_c , the InGaP/GaAs showed little change with respect to I_c and the InP/InGaAs gain is almost independent of the collector current. This was attributed to the influence of various recombination processes in the base-emitter junctions of these devices and also the lower surface recombination velocity associated with the InGaAs material.

Optical output results showed that there is no degradation of the active substrate layers or the device characteristics as a result of r. f. sputtering used in the ITO deposition. It was also shown that a HPT can be controlled both optically and electrically or by a combination of both sources representing the potential to use a single device for the simultaneous detection and amplification of an optical signal as well as its subsequent coupling with an electrical signal in a single device. Much of the optical characterisation work was based only on the InP/InGaAs devices.

A notable feature of the output characteristic of the InP/InGaAs HBTs with ITO emitter contacts was the significant reduction in the collector offset voltage optical output of the photo transistor to 15mV from 60mV in its electrical mode of operation. This reduction is related to the absence of the finite base resistance in case of the optical mode where no active base contact is required.

In order to understand the relationship between the optical gain and the d.c. current gain, the responsivity of the base-collector p-n junction diode was measured and compared with the responsivity of the device operating under the three terminal device mode. A plot of the ratio of the responsivity of the InP/InGaAs HPT to the responsivity of the base-collector photo diode vs. optical power at $\lambda = 780$ nm showed that this is approximately equal to β , in agreement with conventional analysis of photo transistor operation. Similar measurements were made for a set of AlGaAs/GaAs HPTs and found to confirm the relationship between the optical gain, the electrical gain β and the photo diode responsivity at a given wavelength.

The optical characterisations also involved the measurement and analysis of the spectral response of these novel HBTs with ITO emitter contacts over the relevant wavelength ranges. The AlGaAs/GaAs devices showed an operational range spanning over $\lambda = 450$ to 900 nm while for the InGaAs/InP devices this was from 800nm to 1700 nm.

In both cases, the long wavelength cut-off is determined by the absorption edge of the narrow-bandgap base and collector. For $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ this corresponds to a wavelength of approximately 1650 nm. At shorter wavelengths (< 950 nm), the photoresponse is limited by absorption in the InP emitter as well as the ITO transmission and the monochromator grating efficiencies. The dip in the spectral response at around 1400nm corresponds to atmospheric absorption of radiation from the monochromator and is not a reflection of the device characteristic. This atmospheric absorption in the wavelength range 1340-1450nm is most likely due to moisture and CO_2 . The suitability of the InP/InGaAs devices for operation at 1310 nm and 1550 nm wavelengths was clearly demonstrated.

Finally, initial experiments comparing the benefits of edge coupling versus top coupling showed that up to 40% of the incident beam is lost in the former mode. Device structures need to be redesigned to suit the edge coupling mode. Further work is required to provide more quantitative analysis.

7.7 Spectral Response Model

A spectral response model was developed for the first time to understand, analyse and finally to optimise the performance range of these HBTs [233]. Device parameters such as the doping concentrations, the ITO and the semiconductor layer thickness as well as the material properties such as the absorption coefficients, α , the refractive indices, n , and the generation efficiency were used from the literature for the purpose of simulation. A 100% collection efficiency was assumed for any electron-hole pairs photo generated inside the depletion region or within a diffusion length in the neutral material. The spectral responses of the ITO/n-GaAs Schottky diodes and the AlGaAs/GaAs, InP/GaAs phototransistors are simulated and compared to measured data for the first time. In all cases, very good correlation between the model and the measured results were obtained [204].

The results presented in this thesis provide valuable insight into the use of optically transparent ITO for use in a wide range of optoelectronic devices as well as the respective optimisation. A list of publications arising from this work is presented in Appendix A.

8. Further Work

The following work is recommended as a follow-up to this study:

1. Further analysis of the ITO film, particularly a surface study using AFM or similar instrument.
2. DLTS measurements on the devices with ITO contacts to quantify/assess the sputter induced damage to the underlying epitaxial layers and substrate if any. In particular study in detail the nature and the cause of the damage deep into the semiconductor substrate as suggested by CV profiling. An experiment may be designed to incur the sputter damage and remove the ITO deposit chemically; then re-deposit a metal Schottky contact and repeat the CV profiling in order to isolate any possible effects due to the ITO layer. The damage study should also be extended to HBT wafers to examine its effect on highly doped substrates.
3. Further study the effect of varying the thickness of the indium film between the ITO and the semiconductor to understand its effect on sputter damage limitation and thus enhancement of device performance.
4. Fabrication of small geometry ITO/n-GaAs Schottky diodes with improved series resistance followed by a test of their small signal performance.
5. Fabrication and testing of small geometry ITO emitter contact InP/InGaAs HPTs
6. Incorporate the spectral response model with existing HBT current-voltage models to further understand the optical performance of heterojunction phototransistors in particular the trade-offs involved in top versus edge illumination.

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Appendix A: List of Publications

A.1 Journal / Letter Publications

1. “Optically Transparent Indium Tin Oxide (ITO) Ohmic Contacts in the Fabrication of Vertical Cavity Surface-Emitting Lasers”, M. A. Matin, A. F. Jezierski, S. A. Bashar, D. E. Lacklison, T. M. Benson, T. S. Cheng, J. S. Roberts, T. E. Sale, J. W. Orton, C. T. Foxon and A. A. Rezazadeh, *Electronics Letters*, Vol. **30**(4), 1994, pp. 318-320
2. “Optically Transparent ITO Emitter Contacts in the Fabrication of InP/InGaAs HPTs”, S. A. Bashar and A. A. Rezazadeh, *IEEE Transactions on Microwave Theory and Techniques*, Vol. **43**, No. 9, 1995, pp. 2299-2303
3. “Fabrication and Spectral Response Analysis of AlGaAs/GaAs and InP/InGaAs HPTs with Transparent ITO Emitter Contacts”, S. A. Bashar and A. A. Rezazadeh, *IEE Proceedings on Opto-electronics*, Vol. **143**, Issue 1, (February) 1996, pp. 89-93
4. “InP Based HBTs for Optical Telecommunications - Invited Paper”, A. A. Rezazadeh, H. Sheng and S. A. Bashar, *International Journal of Optoelectronics*, Vol. **10**, no. 6, 1996, pp. 489-493

A.2 Publications in Conference, Colloquium and Workshop Proceedings

1. “Realisation of Fast Photoreceivers Based on ITO/n-GaAs Schottky Diodes”, S. A. Bashar and A. A. Rezazadeh, *Proceedings of IEE Colloquium on Optical Detectors and Receivers*, London, UK, October, 1993
2. “Transparent Indium Tin Oxide (ITO) Ohmic Contacts to both p and n GaAs for Surface-emitting Lasers”, A. F. Jezierski, M. A. Matin, S. A. Bashar, T. S. Cheng, D. Lacklison, T. Foxon, T. M. Benson, M. Heath, J. Orton and A. A. Rezazadeh, *IEEE/LEOS Annual Meeting Proceedings*, San Jose, USA, 15th-18th November, 1993
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5. “Fabrication and Characterisation of a Transparent Gate HEMT Using Indium Tin Oxide”, A. H. Khalid, S. A. Bashar and A. A. Rezazadeh, *Proceedings of IEEE International Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications - EDMO*, London, UK, 14th November, 1994, pp. 99-104

6. "Transparent Emitter Contacts to InP/InGaAs HPTs for Long Haul Optical Telecommunications Applications", S. A. Bashar and A. A. Rezazadeh, *Proceedings of IEEE International Conference on Telecommunications*, Bali, Indonesia, 3rd-5th April, 1995, pp. 320-323
7. "Analysis and Modeling of Spectral Response for GaAs Schottky Diodes and InP/InGaAs HPTs Fabricated Using Indium Tin Oxide", S. A. Bashar and A. A. Rezazadeh, *Proceedings of The 5th European Heterostructure Workshop*, Cardiff, UK, 17th-19th September, 1995
8. "Characterisation of Transparent ITO Emitter Contact InP/InGaAs Heterojunction Bipolar Transistors", S. A. Bashar and A. A. Rezazadeh, *Proceedings of IEEE International Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications - EDMO*, London, UK, 27th November, 1995, pp. 76 - 81
9. "Noise Properties of AlGaAs/GaAs HPTs with Transparent ITO Emitter Contacts", N. B. Lukyanchikova, N. P. Garbar, M. V. Petrichuk, A. A. Rezazadeh and S. A. Bashar, *Proceedings of IEEE International Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications - EDMO*, Leeds, UK, 25th - 26th November, 1996, pp. 50 - 55
10. "Noise Characterization of AlGaAs/GaAs HBTs with Different Emitter Contacts", N. B. Lukyanchikova, N. P. Garbar, M. V. Petrichuk, A. A. Rezazadeh and S. A. Bashar, *Proceedings of IEEE International Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications - EDMO*, London, UK, 24th - 25th November, 1997, pp. 157 - 162

Appendix B: Processing Steps for Liftoff and Etch Lithography

Ideal sample size for processing: between 1cm x 1cm and 2.5cm x 2.5cm.

B.1 Steps for Liftoff lithography

No.	Name	Conditions/Comments
1	De-greasing	Clean in TCE, acetone, methanol - at 60°C for 10 mins. in each (skip TCE if this is not the first photolithography stage)
2	Rinse	Rinse in running D.I. water for 5 minutes
3	Pre-bake	Blow dry sample then bake at 160°C for 30 mins.
4	Photoresist (P.R.)	Apply P.R. (Shipley 1400-27) to entire surface using a clean pipette; spin at 4,500 rpm for 35 secs. to obtain a film thickness of app. 1µm.
5	Soft bake	Bake sample at 70°C for 30 minutes, then allow sample to cool prior to alignment
6	Prepare Mask	Clean mask in acetone and blow dry carefully in N ₂ , then place mask facing down in the aligner
7	Alignment	Carefully remove any P.R. residue from the back of sample using acetone prior to placing sample on the aligner tray; insert and then raise the tray to bring the sample into “contact”; lower slightly to the “separation” position to facilitate alignment; once satisfactory alignment to the mask has been achieved, carefully raise the tray to the “contact” position once again.
8	UV Exposure	Expose using UV light for 15 secs.
9	Chlorobenzene	Soak in chlorobenzene (inside the fume cupboard) for 4 mins. then carefully blow dry using N ₂
10	Post bake	Bake sample at 70°C for a further 15 mins.
11	Develop	Soak in a 1 Microposit developer : 1 H ₂ O solution for roughly 1 min; check under microscope to ensure “windows” have opened adequately; do a final soak in a fresh developer solution for a further 15 secs to remove trace P.R.
12	De-oxidise	Finally, etch in 10% HCl solution for 15 secs. prior to metalisation.

Table B1: Processing steps for lift-off lithography

B.2 Steps for Etch lithography

No.	Name	Conditions/Comments
1 - 4		Same as lift-off lithography, see Table B1
5	Soft Bake	Bake sample at 95°C for 30 minutes, then allow sample to cool prior to alignment
6 - 8		Same as lift-off lithography, see Table B1
9	Develop	Soak in a 1 Microposit developer : 3 H ₂ O solution for roughly 90 secs.; check under microscope to ensure “windows” have opened adequately; do a final soak in a fresh developer solution for a further 15 secs to remove trace P.R.
10	Hard Bake	Bake sample at 115°C for 30 minutes, then allow sample to cool prior to etching in required solution

Table B2: Processing steps for etch lithography

Appendix C: SPA Settings for Device Parameter Extractions

C.1 Settings for Schottky diode parameter extractions

Device configuration: positive terminal to SMU1; negative terminal to SMU3.

Channel Definition					Source Set-up		
Channel	Name		Source		Var1	Var2	
	V	I	Mode	Function			
SMU1	VF	IF	V	VAR1	VF	-	
SMU2	-	-	-	-	Sweep Mode	linear	
SMU3	V	I	COM	CONST	Start	-2.0V	
SMU4	-	-	-	-	Stop	1.0V	
					Step	0.01V	
					No. of steps	301	
					Compliance	100mA	
		Constant		Source	Compliance		
V COM		0.0V		105.0mA			

Table C1.1: Typical SPA settings for measuring the output characteristics of a Schottky diode

C.2 Settings for HBT parameter extractions

Device configuration: emitter to SMU1; base to SMU2; collector to SMU3.

Output characteristics

Channel Definition					Source Set-up		
Channel	Name		Source		Var1	Var2	
	V	I	Mode	Function			
SMU1	VE	IE	COM	CONST	Name	VCE	
SMU2	VB	IB	I	VAR2	Var2	IB	
SMU3	VCE	IC	V	VAR1	Sweep Mode	linear	
SMU4	-	-	-	-	Start	0.0V	
					Stop	3.0V	
					Step	0.03V	
					No. of steps	101	
					Compliance	100mA	
		Constant		Source	Compliance		
VE COM		0.0V		105.0mA			

Table C2.1: Typical SPA settings for measuring the output characteristics of a HBT
Gummel plot

Channel Definition					Source Set-up		
Channel	Name		Source		Name	Var1	Var2
	V	I	Mode	Functio n		VB	-
SMU1	VE	IE	COM	CONST	Sweep Mode	linear	-
SMU2	VB	IB	V	VAR1	Start	0.0V	-
SMU3	VCE	IC	V	VAR1'	Stop	1.6V	-
SMU4	-	-	-	-	Step	0.01V	-
					No. of steps	160	-
					Compliance	100mA	-
					VAR1' ratio = 1, VAR1' offset = 0.0V		
					Constant	Source	Compliance
					VE COM	0.0V	105.0mA

Table C2.2: Typical SPA settings for measuring the Gummel plot of a HBT

DC Gain, β

Channel Definition					Source Set-up		
Channel	Name		Source		Name	Var1	Var2
	V	I	Mode	Functio n		VB	-
SMU1	VE	IE	COM	CONST	Sweep Mode	linear	-
SMU2	VB	IB	V	VAR1	Start	0.1V	-
SMU3	VCE	IC	V	CONST	Stop	3.9V	-
SMU4	-	-	-	-	Step	0.05V	-
					No. of steps	77	-
					Compliance	100mA	-
					Constant	Source	Compliance
					VE COM	0.0V	105.0mA
					VCE V	3.0V	100.0mA

Table C2.3: Typical SPA settings for measuring the DC gain of a HBT

Emitter contact resistance, R_{ee} ,

Channel Definition					Source Set-up		
Channel	Name		Source		Name	Var1	Var2
	V	I	Mode	Function		IB	-
SMU1	VE	IE	COM	CONST	Sweep Mode	linear	-
SMU2	VB	IB	I	VAR1	Start	0.0A	-
SMU3	VCE	IC	I	CONST	Stop	5.0mA	-
SMU4	-	-	-	-	Step	10μA	-
					No. of steps	501	-
					Compliance	2.0V	-

Appendix D: Mathematical Derivations

D.1 Two derivations for the doping concentration, N_D .

The capacitance, C , of Schottky diode as a function of the applied bias, V_{app} , (see section 4.3) is given by:

$$C = \frac{\epsilon_0 \epsilon_r A}{\sqrt{\frac{2\epsilon_0 \epsilon_r}{qN_D} (V_{bi} - V_{app})}} \quad (\text{eqn. D1.1})$$

Therefore,

$$\frac{1}{C^2} = \frac{2}{qN_D \epsilon_0 \epsilon_r A^2} \cdot (V_{bi} - V_{app}) \quad (\text{eqn. D1.2})$$

D1.1 The first derivation

Differentiating (eqn. D1.2) w.r.t. V_{app} yields:

$$\frac{d(1/C^2)}{dV_{app}} = \frac{-2}{qN_D \epsilon_0 \epsilon_r A^2} \quad (\text{eqn. D1.3})$$

Rearranging in terms of N_D :

$$N_D = \frac{-2}{q\epsilon_0 \epsilon_r A^2} \cdot \frac{dV_{app}}{d(1/C^2)} \quad (\text{eqn. D1.4})$$

D1.2 The second derivation

Simplifying (eqn. D1.1) gives:

$$C = \sqrt{\frac{qN_D \epsilon_0 \epsilon_r A^2}{2}} \cdot \frac{1}{\sqrt{(V_{bi} - V_{app})}} \quad (\text{eqn. D1.5})$$

Differentiating (eqn. D1.5) w.r.t. V_{app} yields:

$$\frac{dC}{dV_{app}} = \sqrt{\frac{qN_D \epsilon_o \epsilon_r A^2}{2}} \cdot \left(\frac{1}{2} (V_{bi} - V_{app})^{-3/2} \right) \quad (\text{eqn. D1.6})$$

But from (eqn. D1.5),

$$\frac{1}{\sqrt{(V_{bi} - V_{app})}} \text{ or } (V_{bi} - V_{app})^{-1/2} = \frac{C}{\sqrt{\frac{qN_D \epsilon_o \epsilon_r A^2}{2}}} \quad (\text{eqn. D1.7})$$

Hence, substituting (eqn. D1.7) in (eqn. D1.6), we obtain:

$$\begin{aligned} \frac{dC}{dV_{app}} &= \sqrt{\frac{qN_D \epsilon_o \epsilon_r A^2}{2}} \cdot \left(\frac{1}{2} \left(\frac{C}{\sqrt{\frac{qN_D \epsilon_o \epsilon_r A^2}{2}}} \right)^3 \right) \\ &= \frac{1}{2} \frac{C^3}{\left(\sqrt{\frac{qN_D \epsilon_o \epsilon_r A^2}{2}} \right)^2} \\ &= \frac{C^3}{qN_D \epsilon_o \epsilon_r A^2} \end{aligned} \quad (\text{eqn. D1.8})$$

Rearranging in terms of N_D :

$$N_D = \frac{C^3}{q\epsilon_o \epsilon_r A^2} \left(\frac{dC}{dV_{app}} \right)^{-1}$$

(eqn. D1.4)

D.2 Derivation of built-in potential at the base-emitter heterojunction, $V_{bi(B-E)}$, of a HBT

The analytical expression for $V_{bi(B-E)}$ is given by:

$$V_{bi(B-E)} = E_{gB} + \Delta E_C + \frac{kT}{q} \ln \left(\frac{N_{DE} N_{AB}}{N_{cE} N_{vB}} \right) \quad (\text{eqn. D2.1})$$

which can be re-written as:

$$V_{bi(B-E)} = E_{gB} + \Delta E_C + \frac{kT}{q} \ln\left(\frac{N_{DE} N_{AB}}{n_{iB} n_{iE}}\right) + \frac{kT}{q} \ln\left(\frac{n_{iB} n_{iE}}{N_{CE} N_{VB}}\right) \quad (\text{eqn. D2.2})$$

But recall that,

$$n_{iB} = \sqrt{N_{cB} N_{vB}} \cdot \exp\left(\frac{-qE_{gB}}{2kT}\right) \quad (\text{eqn. D2.3})$$

and,

$$n_{iE} = \sqrt{N_{cE} N_{vE}} \cdot \exp\left(\frac{-qE_{gE}}{2kT}\right) \quad (\text{eqn. D2.4})$$

Thus, the final term in (eqn. D2.2) can be expressed as:

$$\begin{aligned} \frac{kT}{q} \ln\left(\frac{n_{iB} n_{iE}}{N_{CE} N_{VB}}\right) &= \frac{kT}{q} \ln\left(\frac{\sqrt{N_{cB} N_{vE}} \cdot \exp\left(\frac{-q(E_{gB} + E_{gE})}{2kT}\right)}{\sqrt{N_{cE} N_{vB}}}\right) \\ &= \frac{kT}{2q} \ln\left(\frac{N_{cB} N_{vE}}{N_{cE} N_{vB}}\right) - \frac{1}{2}(E_{gB} + E_{gE}) \end{aligned} \quad (\text{eqn. D2.5})$$

And therefore, (eqn. D2.2) can now be written as:

$$\begin{aligned} V_{bi(B-E)} &= E_{gB} + \Delta E_C + \frac{kT}{2q} \ln\left(\frac{N_{cB} N_{vE}}{N_{cE} N_{vB}}\right) + \frac{kT}{q} \ln\left(\frac{N_{DE} N_{AB}}{n_{iB} n_{iE}}\right) - \frac{1}{2}(E_{gB} + E_{gE}) \\ &= \frac{E_{gB} - E_{gE}}{2} + \Delta E_C + \frac{kT}{2q} \ln\left(\frac{N_{cB} N_{vE}}{N_{cE} N_{vB}}\right) + \frac{kT}{q} \ln\left(\frac{N_{DE} N_{AB}}{n_{iB} n_{iE}}\right) \end{aligned} \quad (\text{eqn. D2.6})$$

But since, $E_{gE} > E_{gB}$, and

$$\begin{aligned} \Delta E_g &= E_{gE} - E_{gB} \\ -\frac{\Delta E_g}{2} &= \frac{E_{gB} - E_{gE}}{2} \end{aligned} \quad (\text{eqn. D2.7})$$

Hence we obtain the desired expression for the V_{bi} of a heterojunction:

$$V_{bi(B-E)} = \Delta E_C - \frac{\Delta E_g}{2} + \frac{kT}{2q} \ln\left(\frac{N_{cB} N_{vE}}{N_{cE} N_{vB}}\right) + \frac{kT}{q} \ln\left(\frac{N_{DE} N_{AB}}{n_{iB} n_{iE}}\right)$$

(eqn. D2.8)