Reduction of recombination current in CdTe/CdS solar cells

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(Received 5 June 1995; accepted for publication 24 July 1995)

A study of the current–voltage behavior of recombination current in CdTe/CdS solar cells has shown that the reverse saturation current, J_0, and the diode quality factor, A, are correlated. Our better devices typically have low values of both A and J_0. Spectral response data indicate that devices with a gradual decline in quantum efficiency beginning at about 600 nm show better performance than devices with a sharp drop at the CdS band gap of 510 nm, which is interpreted as an indication that mixing between CdS and CdTe during processing reduces the amount of recombination current at the interface. © *1995 American Institute of Physics.*

Recent advances in the conversion efficiency of polycrystalline CdTe/CdS solar cells,[1,2] the highest being a 15.8% cell fabricated at the University of South Florida,[3] have renewed interest in the pursuit of CdTe as a low cost material for the production of solar cells for terrestrial applications.[4] One of the most crucial aspects to making further improvements in these devices is to develop a clear understanding of the operating principles of the CdTe/CdS junction. Previous studies have advanced our level of understanding,[5–7] but several important issues regarding device performance remain unresolved. Also, it is important to know how these junction properties are influenced by processing conditions. In this letter we present results that provide new insights to performance as well as correlation to processing.

The structure of our solar cells is glass/SnO_2/CdS/CdTe/backcontact. The close spaced sublimation (CSS) process is used for CdTe deposition and the CdS is deposited by chemical bath (CBD) or CSS. Details of the processing conditions have been presented elsewhere.[8,9] The general equation for solar cell J–V characteristics is

$$J = J_0(e^{q(V-JR_s)/AkT} - 1) + \frac{V-JR_s}{R_{sh}} - J_L, \tag{1}$$

where R_s and R_{sh} are the series and shunt resistances, A the "diode quality factor," J_0 the reverse saturation current, and J_L the light generated current. Our initial objective was to demonstrate that when all parameters were measured properly, all aspects of device performance could be simulated in a self-consistent manner with this straightforward, classical equation.

The values of R_s and R_{sh} in the dark and in the light are estimated by taking the reciprocal of the slope of the J–V curve at 90 mA forward current (above the short circuit current I_{sc}) and at -0.2 V reverse bias, respectively. Since we have not seen any significant voltage dependent collection in reverse bias for our samples, we take $J_L = J_{sc}$ as a constant in the equation.

The two macroscopic parameters that describe the performance of the main junction are A and J_0. We have investigated several methods that have been proposed to calculate these parameters,[10,11] but we have found that the most consistent and reliable measurement of these values is to take the slope and y intercept of the dark log J vs V data between 0.2 and 0.6 V. Outside of this range of voltages, shunt and series resistances influence the J–V behavior. A and J_0 values for a large number of our cells are shown in Fig. 1.

It is clearly seen that low A values are correlated with low J_0 values. The data point furthest to the right on the graph (A=1.90) actually represents 4 different devices that had the same A and J_0 values. Our better cells tend to appear in the lower left region of Fig. 1, having low values of both A and J_0. This trend is demonstrated in Fig. 2, where the fill factor$\times V_{oc}$ product is plotted versus the diode quality factor. The efficiencies of these devices ranged from 10% to 15%. The reason for plotting fill factor$\times V_{oc}$ on the y axis rather than efficiency is that the impact of processing conditions and junction parameters on the value of J_{sc} is less dramatic than differences in absorption produced by different CdS thicknesses. Fill factor and V_{oc} are the parameters that are most directly affected by the values of A and J_0. The spread in the data is in part due to differences in series resistance between samples which can cause variations in the fill factor by a percent or two. In addition, A and J_0 may change under light exposure, and the magnitude of that change varies from device to device. This issue will be discussed in more detail in a future publication.

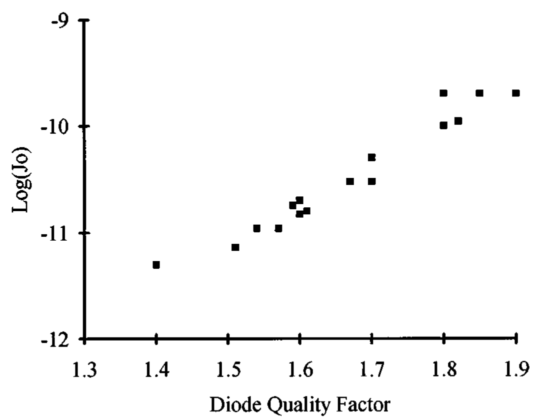

FIG. 1. Correlation between A and J_0.

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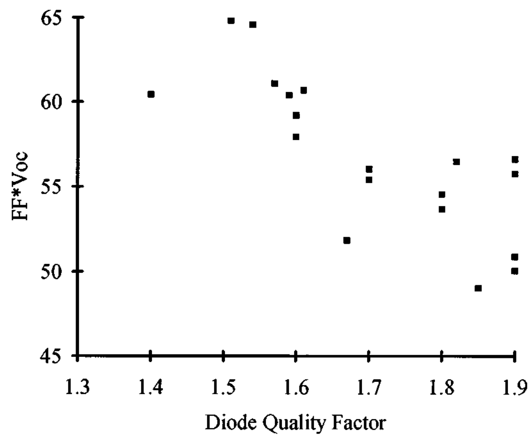

FIG. 2. Correlation of device performance with diode quality factor.

Figure 3 illustrates another trend that we have observed in spectral response behavior. The CdS layer for the first sample [Fig. 3(a)] was deposited by CSS. In this cell, a sharp drop in quantum efficiency (QE) is seen at the CdS band gap of 510 nm. The values of A and J_0 for this sample are 1.85 and 2×10^{-10} A/cm^2. The sample had an open circuit voltage of 805 mV and an efficiency of 10.3%. The second sample [Fig. 3(b)], with CBD CdS, has no sharp feature at 510 nm. Instead, a gradual decline in QE is seen beginning at approximately 600 nm. The performance of this sample is far better. The A and J_0 values were 1.54 and 1×10^{-11} A/cm^2, $V_{oc}=849$ mV, and $\eta=14.1\%$.

The magnitude of the QE in the short wavelength region of the spectral response is controlled primarily by CdS thickness. However, it has been our experience that devices produced with CBD CdS typically have the shape of Fig. 3(b) in this region, while CSS CdS samples tend to exhibit sharper drops in QE at the CdS band gap. Other authors have proposed that interdiffusion of CdS and CdTe can occur during processing.[12,13] We believe that mixing of the two materials for CBD cells has passivated the CdTe/CdS interface and reduced the number of defects that act as recombination centers. This in turn has increased the carrier lifetime that influences A and J_0. By processing our devices in a manner that promotes mixing, we are able to consistently produce high performance devices.

As Fig. 1 shows, the ''macroscopic'' device parameters A and J_0 are not completely independent. J_0 may be expressed as

$$J_0=\frac{qn_iW}{\sqrt{\tau_p\tau_n}}\times F, \tag{2}$$

where W is the space charge width, τ the carrier lifetimes, and F the fraction of the space charge width over which recombination is taking place. Sah, Noyce, and Shockley[14] have shown that for recombination centers with a single energy level, the effective width over which recombination occurs is kT/qE, where E is the electric field in the space charge region. This treatment also indicates that the voltage dependent portion of the recombination rate is affected by the energy level of the recombination centers and the ratio of the carrier lifetimes τ_{p0}/τ_{n0}. It is the common dependency of A and J_0 on carrier lifetimes that is the source of the correlation between them. Our data further indicate that devices with sharper drops in the spectral response at the CdS band gap have higher A and J_0 values and poorer performance. We interpret this as being due to a decrease in carrier lifetime. This is in agreement with recently published results of time resolved photoluminescence measurements in which a strong dependence of V_{oc} on minority carrier lifetime was demonstrated.[15] A more detailed model of junction behavior will be discussed in a future publication.

We have demonstrated the correlation between the diode quality factor and reverse saturation current for high efficiency CdTe solar cells that are dominated by recombination current. The relationship between these two parameters is due to their common dependency on carrier lifetimes. Low A and J_0 values are most desirable for the best device performance. Our spectral response data are believed to indicate that an effective way to reduce the dark recombination current and improve device performance is to cause mixing between the CdTe and CdS.

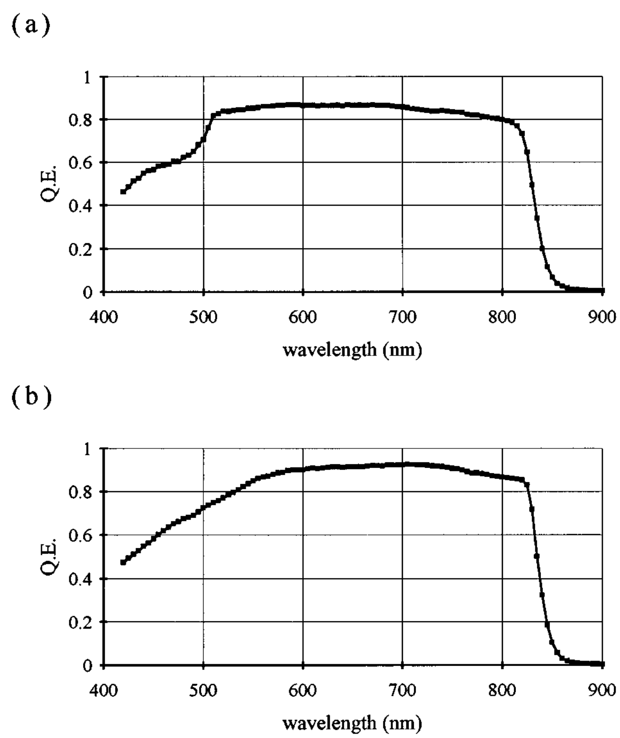

FIG. 3. Spectral response of (a) a 10% efficient cell and (b) a 14% cell.

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