



Rectification in CdS/TCO bilayers

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ABSTRACT

The origin of process-induced rectification in CdS/ITO and CdS/SnO₂ bilayers has been investigated. Both pre-treatment of the transparent conducting oxide (TCO) substrates and post-growth treatment of the bilayers were explored for both oxidising and reducing conditions. In/CdS/TCO structures were used for *I*–*V* testing, and the CdS layers were verified as being pinhole-free using a test employing a rectifying Au/CdS contact. Whilst neither pre-oxidation nor reduction of any TCO substrate failed to induce rectification in CdS/TCO, oxidation of CdS always induced rectification, regardless of the substrate type. This was attributed to oxidation of CdS (confirmed by Auger electron spectroscopy), and the results are consistent with a band diagram postulated for the CdO/CdS/ITO structure. Recommendations are made for the fabrication of CdTe/CdS/TCO solar cells.

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1. Introduction

It is a central tenet of the thin film PV device fabrication methodology to create devices by deposition of (cheap) polycrystalline materials, which are then annealed or heat processed in order to somehow normalise their stoichiometry to generate efficient p–n junctions. Given the correct choices of material, e.g. CdS as a naturally n-type partner layer, the progress can be eased, and the need for more sophisticated processing, e.g. intentional doping, can be reduced. Nevertheless, the complete devices and individual layers of devices are the subjects of processing/performance studies, which are sometimes empirical and sometimes represent back-tracking in order to establish the means by which they are effective. In this work we examine the behaviour of CdS layers deposited on transparent conducting oxide (TCO) layers, as is used in the fabrication of CdTe/CdS/TCO/glass solar cells. For device fabrication, this whole structure is invariably subjected to post-growth treatment involving chloride species, most usually CdCl₂. However, some laboratories choose to subject the CdS/TCO/glass combination to an intermediate processing step. In particular this study refers to the work of Alamri and Brinkman [1] in which air annealing of this combination of layers lead to rectifying behaviour, when the TCO was indium–tin–oxide (ITO), but the samples remained Ohmic when the TCO was SnO₂. Alamri and Brinkman attributed this behaviour to a change in

work function of the buried ITO surface on processing, which caused the junction to change from Ohmic to rectifying. An increase in work function of ~ 1 eV on oxidation was demonstrated elsewhere [2] and its inclusion in the CdS/ITO junction is sufficient to cause the observed changes to the junction type. This was considered to be the origin of poor performance of CdTe solar cells grown on ITO substrates. Such changes were neither expected nor observed in the case of the more stable SnO₂ substrates. Here we test Alamri and Brinkman's explanation by (a) pre-annealing TCO substrates before overgrowth with CdS in an attempt to change their work function and promote either Ohmic or rectifying behaviour at the CdS/TCO interface and (b) post-growth annealing of the CdS/TCO couples in order to re-examine Alamri and Brinkman's results.

The wider literature and experience of the response of CdS layers to post-growth annealing provide a context for the study; there are reports of annealing of the layers in oxidising (oxygen [1–3]), reducing (hydrogen containing [4–8]) and neutral (nitrogen, helium or argon [3,4–6,7–9]) atmospheres. In a photoluminescence study, Goto et al. [3] reported that annealing of CdS in air, and particularly in oxygen, caused a reduction in defect luminescence. Since annealing under nitrogen caused an increase in such levels, the paper concluded that annealing in oxygen may be beneficial for device performance. On the other hand, annealing under reducing conditions has been found to induce profound physical changes to CdS thin films. Hydrogen annealing at moderate temperatures (200–250 °C) has been shown to cause significant decreases in resistivity [4] attributed to grain boundary passivation, this being reversed at higher temperatures (300 °C) on account of stoichiometry changes. Other authors [5] attribute the resistivity drop to reduction of oxides, re-crystallisation and

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the presence of CdCl₂, and the increase to the formation of voids. Reduction of the CdS prior to CdTe growth has also been observed to influence the transport mechanism [8], depletion region width and diode ideality factor [6] with such treatment being recommended to increase device performance.

Given Alamri and Brinkman's findings, and the range of recommendations with regard to CdS annealing in the literature, there are therefore grounds for the further investigation presented in this work. Finally it should be mentioned that thin films of CdS are known to be prone to pinholing. Since the characterisation in this work relies on *I*–*V* measurement of thin test structures, a method of testing for pinholes in CdS was established in order to validate the findings. This makes use of the fact that In/CdS forms an Ohmic contact [1], while Au/CdS is a rectifying junction [10].

2. Experimental

2.1. Sample Preparation: bilayers, pre- and post-growth treatment

The growth, annealing and contacting details for all samples studied are shown in Table 1. Growth of CdS films was undertaken by close space sublimation (CSS), with the source temperature being 650 °C, and the substrate temperature in the range 490–550 °C. The films were grown on 5 × 5 cm² ITO/glass substrates supplied by Delta Tech and SnO₂/glass “TEC 8” supplied by Pilkington.

For the work on ITO/glass substrates, annealing took place either (a) prior to CdS growth i.e. pre-annealing of the ITO substrates or (b) post-growth. For the pre-annealing (a) the ITO/glass substrates were heated in a CSS reactor in one of two gaseous ambients: (i) 100 Torr of O₂ or (ii) 15 Torr of H₂+60 Torr of N₂. In both cases the substrates were heated to 400 °C for 10–40 min using a substrate heater only. One further pre-annealing run under O₂ was undertaken at 550 °C for 40 min in order to investigate the effects of more severe oxidising conditions.

After annealing, the TCO substrates were allowed to cool in the chamber and the system was flushed with N₂ to remove the annealing ambient prior to CdS deposition. It should be noted that for the H₂+N₂ annealing, vacuum was not broken prior to the CdS deposition, as the CdS source remained in the CSS chamber during

Table 1

Annealing details for the samples investigated. Sample 1 had Au/ITO contacts i.e. without CdS film. Sample 2 had In/CdS/ITO, with both CdS and ITO layers being as-grown. Samples 3–11 had the ITO treated prior to over-growth with CdS, while 12 and 13 were treated after CdS had been deposited. Samples 14 and 15 had In/CdS/SnO₂ structure with as-grown and oxidised CdS, respectively.

Sample	TCO	Treatment type	Treatment conditions			<i>I</i> – <i>V</i> curve
			Gas	<i>T</i> (°C)	Time (min)	
1	ITO	As-grown	–	–	–	Ohmic
2	ITO	As-grown	–	–	–	Ohmic
3	ITO	Pre-CdS	O ₂	400	10	Ohmic
4	ITO	Pre-CdS	O ₂	400	20	Ohmic
5	ITO	Pre-CdS	O ₂	400	30	Ohmic
6	ITO	Pre-CdS	O ₂	400	40	Ohmic
7	ITO	Pre-CdS	O ₂	550	40	Ohmic
8	ITO	Pre-CdS	H ₂ +N ₂	400	10	Ohmic
9	ITO	Pre-CdS	H ₂ +N ₂	400	20	Ohmic
10	ITO	Pre-CdS	H ₂ +N ₂	400	30	Ohmic
11	ITO	Pre-CdS	H ₂ +N ₂	400	40	Ohmic
12	ITO	Post-CdS	O ₂	400	40	Rectifying
13	ITO	Post-CdS	H ₂ +N ₂	400	40	Ohmic
14	SnO ₂	As-grown	–	–	–	Ohmic
15	SnO ₂	Post-CdS	O ₂	400	40	Rectifying

annealing. However, in the case of O₂ annealing the source was removed prior to annealing to protect it from oxidation and replaced for the CdS growth step.

To study the post-growth treatment (b) of CdS, the CdS/ITO films were deposited on non-treated substrates and annealed for 40 min at 400 °C in either 100 Torr of oxygen or the same H₂+N₂ mixture as used in (a). Similar post-growth annealing runs were done on CdS/SnO₂ for comparison.

All samples were finally contacted with a matrix of 16 In dots (2 mm diameter), which was applied by thermal evaporation at a pressure of ~10^{−5} Torr. Indium was used since it makes an Ohmic contact with CdS [1], allowing any rectification behaviour to be credited to the CdS/ITO interface. Dark *I*–*V* characteristics were measured using a computer controlled Keithley source meter.

2.2. Testing the coverage of the CdS film

The presence of pinholes in the CdS film may result in misleading *I*–*V* curves for the In/CdS/ITO structure. If In has a direct contact with the ITO at some areas of the sample, the resulting *I*–*V* curves will be Ohmic regardless of the junction type at the CdS/ITO interface. Therefore, it was an essential requirement that the coverage of the CdS film be tested before undertaking the study.

In this work a method of testing the CdS film continuity was devised. It is well known that Au makes a Schottky contact with CdS [10]. Hence, a structure comprising Au/CdS/ITO should always display rectifying behaviour even when the CdS/ITO junction is Ohmic. However, when pinholes are present in CdS, a direct Ohmic contact will be established between Au and the TCO, and the *I*–*V* curves will be Ohmic. Moreover, Au was also evaporated directly on as-grown Delta Tech ITO (sample 1). The aim of this control was to measure the resistance of the direct contact between Au and the ITO in order to compare it with the resistance of other Ohmic contacts in this study.

2.3. Materials analysis

Instrumental methods of physical and chemical analysis were applied to CdS in order to evaluate changes that occurred to it during annealing. Surface structure was evaluated by grazing incidence XRD, while surface and the bulk chemistries of the layers were evaluated by AES and SIMS, respectively. The latter were undertaken by Loughborough Surface Analysis Ltd.

3. Results

3.1. Continuity of the CdS films

Fig. 1 illustrates the use of the Au-contact method to test for the presence of pinholes in CdS. The sample chosen had been shown to be Ohmic when tested using In contacts. Nevertheless, the contact in Fig. 1a is rectifying, which indicates that there is no Ohmic shorting through CdS, with the rectifying behaviour being due to the Au/CdS interface as expected. On the other hand, the contact in Fig. 1b (from another part of the same sample) behaves as if it is Ohmic, and this must be due to a short circuit through CdS. It may therefore be concluded that the method is capable of detecting pinholes in CdS.

In assessing the quality of CdS/TCO layers it was found that (i) of the two brands of ITO tested, CdS grown on Delta Tech showed pinholing in only 10% of contacts, whereas another brand suffered from 56% of contacts having pinholes, and (ii) the

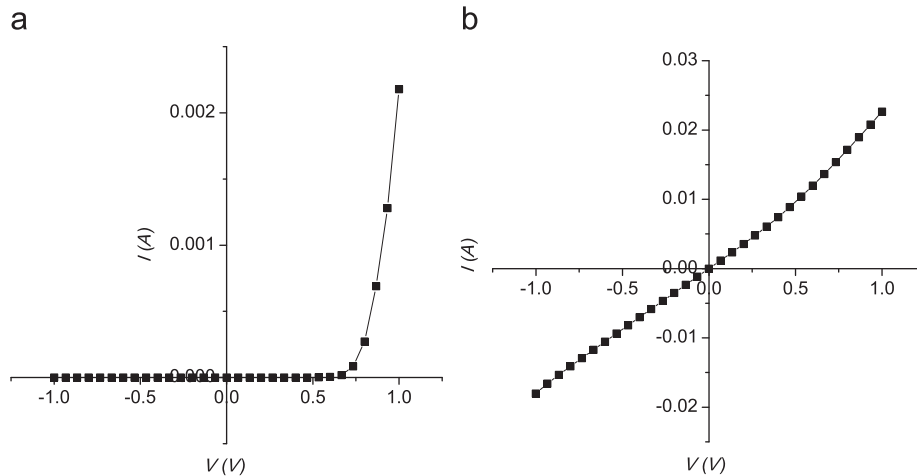


Fig. 1. I - V curves for (a) an Au/CdS/ITO structure showing rectifying behaviour, indicating that the CdS layer was pinhole free, and (b) Ohmic behaviour of another dot on the same sample indicating the presence of pinholes.

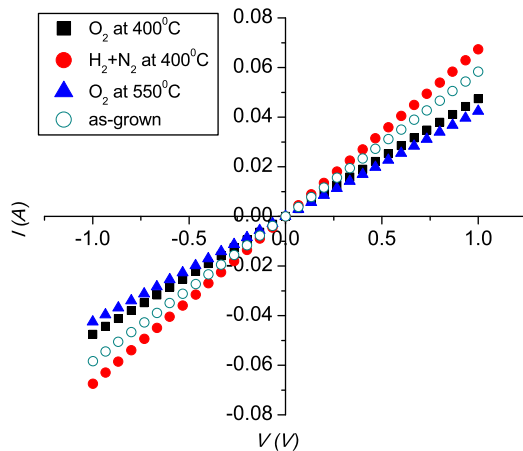


Fig. 2. Typical results showing Ohmic behaviour of the In/CdS/ITO structure. The ITO was either as-grown (hollow circles, sample 2) or pre-treated in (a) O₂ at 400 (squares, sample 6), (b) H₂ at 400 (solid circles, sample 11) or (c) O₂ at 550 °C (triangles, sample 7).

incidence of pinholes was dependent on the position on a given $5 \times 5 \text{ cm}^2$ substrate, with the central $2 \times 2 \text{ cm}^2$ part being of greater integrity. Samples for experiments were therefore chosen with this in mind. Furthermore, for all experiments, interspersed matrices of both Au and In dots were applied to the samples, with each In dot being surrounded by 4 Au dots. In this way it was possible to verify the local quality of CdS near any individual In dot. An additional safeguard was for the I - V behaviour to be tested on up to 16 In dots from each sample. In this way all the results presented in the remainder of this paper were verified as being reproducible and for pinhole free CdS.

3.2. CdS films grown on pre-treated ITO substrates

I - V curves for all CdS samples grown on either as-grown or pre-treated ITO substrates (both oxidised and reduced at 400 °C for between 10 and 40 min) and then contacted with In were found to be linear i.e. Ohmic. Typical examples selected from the curves for samples 2, 6, 7 and 11 (see Table 1) are shown in Fig. 2. This finding indicates that it was not possible to manipulate the CdS/ITO junction behaviour from being Ohmic to rectifying by means of oxidising or reducing the ITO. A possible explanation is that the samples were all normalised after pre-treatment by ramping up the ITO temperature

to ~ 550 °C for the overgrowth with CdS. This was tested by oxidising a further ITO sample at ~ 550 °C for 40 min in oxygen, but this too yielded an Ohmic response.

Nevertheless, the resistances of the samples did conform to those expected from their exposure to oxidising and reducing conditions. The sequence was that the most strongly oxidised sample was the most resistive (sample 6, $21.5 \pm 3.9 \Omega$) with a transformation to more conductive behaviour accompanying more reducing conditions (sample 11, $15.3 \pm 3.2 \Omega$). This is expected as a result of the promotion of oxygen vacancies by reduction, and indicates that overgrowth by CdS could not have effected a complete transformation of the ITO after it had been annealed.

3.3. Post-growth annealed CdS/ITO films

The post-growth treated CdS/ITO samples showed a different behaviour. The CdS/ITO annealed in a H₂+N₂ ambient typically had Ohmic behaviour as shown in Fig. 3a. All the 16 In dots on sample 13 had the same Ohmic I - V characteristics with a resistance of $17.7 \pm 3.2 \Omega$. Since pinholing was ruled out, the CdS/ITO junction itself is therefore considered to be Ohmic.

On the other hand, the shape of the I - V curves of In/CdS/ITO using O₂-annealed CdS changed dramatically as shown in Fig. 3b. This treatment caused the I - V curves to change from being Ohmic (for non-treated CdS-based samples) to fully rectifying. This behaviour implies that a significant change had happened to at least one of the two interfaces in the tested structure (i.e. the In/CdS or CdS/ITO interface).

3.4. Post-growth annealed CdS/SnO₂ films

The results of the I - V testing of In/CdS/SnO₂ structures both before and after post-growth annealing of the CdS in O₂ are shown in Fig. 4a and b, respectively. While the as-grown structure is almost Ohmic, the oxidation has introduced rectifying behaviour. The appearance of this is contrary to Alamri and Brinkman's findings for CdS/SnO₂ and is discussed later.

3.5. Structural and compositional analysis

The next stage was to investigate compositional changes due to the post-growth oxidation of the CdS/ITO samples. The GIXRD results for as-grown and annealed CdS films are shown in Fig. 5. It is seen that no new peaks appeared, indicating that there were no

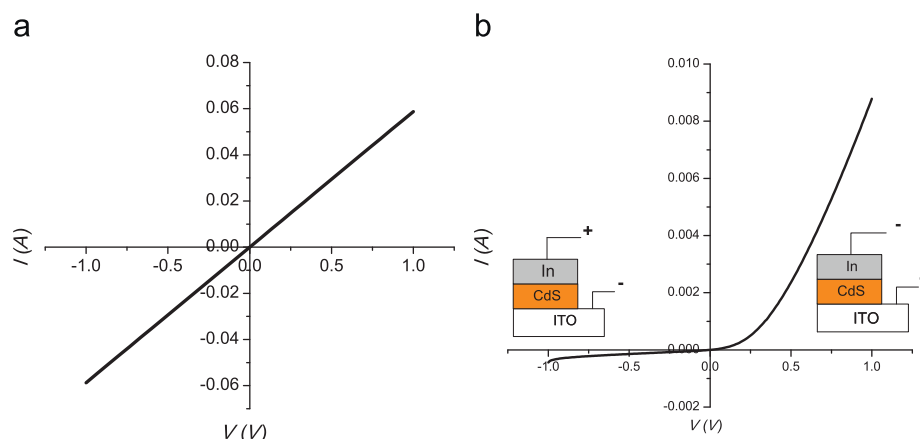


Fig. 3. I - V curves for post-growth annealed CdS/ITO contacted with In. (a) H_2+N_2 treated CdS displaying Ohmic behaviour (sample 13). (b) O_2 -annealed CdS showing rectifying behaviour (sample 12). In (b) the polarity of the electrodes used to record the I - V curves is shown. The field in this structure has opposite sense to that in a full CdTe/CdS solar cell.

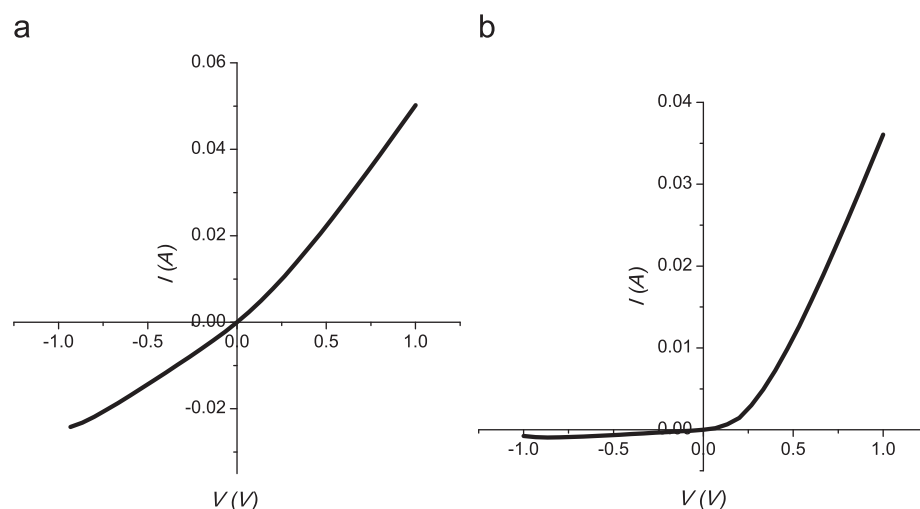


Fig. 4. I - V characteristic behaviour for the In/CdS/SnO₂ structure for (a) as-grown and (b) post-growth oxidised CdS.

new crystalline phases. However, the preferred orientation of annealed (hexagonal) CdS seems to be slightly affected. For example, the 002 orientation was more pronounced after annealing while the intensity for 103 slightly decreased.

Fig. 6a shows a comparison of the In profiles from SIMS profiling. For both films there is evidence of In diffusion into CdS from the ITO. However, for the annealed sample, the In concentration is higher and the diffusion has penetrated more deeply into CdS.

Fig. 6b shows the SIMS depth profiles of oxygen in both the as-grown and the O_2 -treated CdS films. In both samples the curves are comparable. Throughout the bulk of the films there is a low background signal, which rises rapidly at the CdS/ITO interface. The apparent small peak at the layer surface may be genuine, but since such peaks are known to appear from plasma start-up artifacts in SIMS, this was further investigated by AES (Fig. 7). While there was evidence of a small oxygen peak for the as-grown sample, AES showed the CdS surface was very significantly oxidised for the case of the treated sample, the peak being 3 times higher.

4. Discussion

Having established that CdS films of good quality could be identified and selected for experiments, results of the I - V tests as

a function of the processing are now discussed. It is a significant finding that none of the oxidising and reducing treatments applied to the ITO films prior to the CdS growth had any influence on junction performance, which was always found to be Ohmic. This is contrary to what might be expected from work function considerations, with an increase of ~ 1 eV being expected on going from reduced to oxidised ITO and this being sufficient to change the junction type. In principle, this failure may be due to re-normalisation of the ITO on being heated from the treatment temperature of 400 °C to the CdS growth temperature of 550 °C (under a residual nitrogen pressure of 0.5 Torr). However, oxidation at 550 °C also failed to effect a change, and moreover the resistivity data indicated that the CdS/ITO films followed the trends expected for oxidised and reduced ITO. Overall, while we cannot rule out the possibility that the rectification might be engineered by treating this ITO, we consider modification of the overlying CdS to be a stronger candidate for the behaviour observed by Alamri and Brinkman [1].

Of the analytical tests, AES was the most revealing, and indicated that the treatment in oxygen caused oxidation of the CdS surface, and the effect may be expected to be independent of the substrate type. This result is consistent with reports from a number of authors [11–13] that oxidation of CdS surfaces results in the formation of a CdO surface layer. Moreover, in this work,

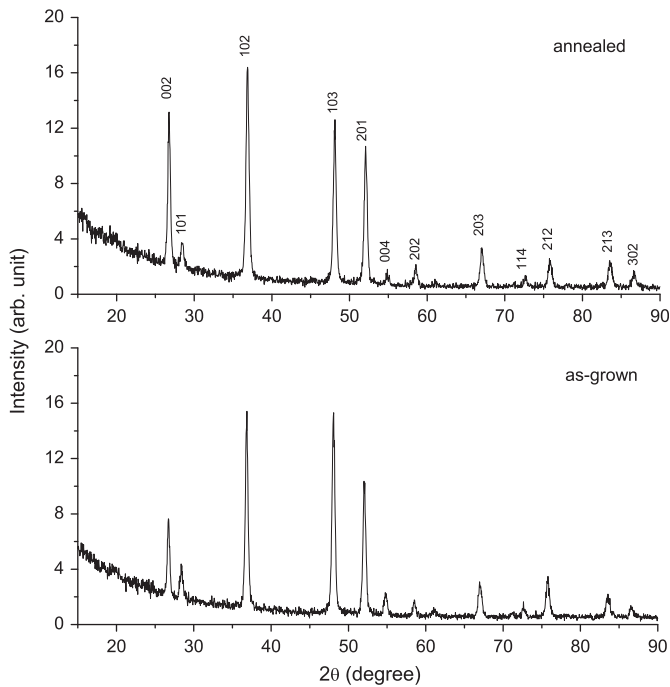


Fig. 5. GIXRD for two CdS/ITO samples: annealed in O_2 (upper) and as-grown (lower) indexed as for the wurtzite phase of CdS. There is no evidence of formation of a new phase after annealing. The samples were identical to samples 2 and 12, respectively.

oxidation caused both CdS/ITO and CdS/SnO₂ to change from Ohmic to rectifying, whereas only the former changed in Alamri and Brinkman's study. CdO is a degenerate semiconductor having a band gap close to that of CdS. The possibility that it is in fact the CdO/CdS junction that accounts for rectification is now explored with the aid of a band diagram postulated for the interfaces in the In/CdO/CdS/ITO structure.

Table 2 shows the values of work function (ϕ), electron affinity (χ) and band gap (E_g) used. There is some disagreement in the literature concerning the band gap of CdO. It is reported to be in the range ~ 2.2 – 2.5 eV for thin films [14–20]; however, as it may depend on grain size [17], it can have higher values for CdO nanostructures e.g. up to 3.69 eV [21]. The value of CdO E_g used was chosen to be 2.4 eV.

The band diagram shown in Fig. 8 indicates that electrons may flow freely from both CdS into the (degenerate) ITO and from CdO into the In contact (Ohmic behaviour of In/CdO has been confirmed by experiment [22]). However, electrons would face an energy barrier ($\phi_{CdO/CdS}$) when they flow from CdO to CdS: this is an n^+/n junction. In fact the polarity of the field of this junction is consistent with the sense of rectification of the complete In/CdS/ITO junction identified by the experiment and shown in Fig. 3. Such a junction has a field that is in the opposite sense to that of the CdTe/CdS p – n junction, and would act to decrease the efficiency of solar cells.

5. Conclusion

It is concluded that Alamri and Brinkman's hypothesis that annealing of CdS/ITO modifies ITO [1] is insufficient to explain the oxidation induced rectification, and that it is instead due to the formation of CdO. This is supported by the finding here that oxidation induced rectification could be demonstrated for both CdS/ITO and CdS/SnO₂, indicating that it is CdS that is modified and not the buried CdS/TCO interface. (It is possible that Alamri

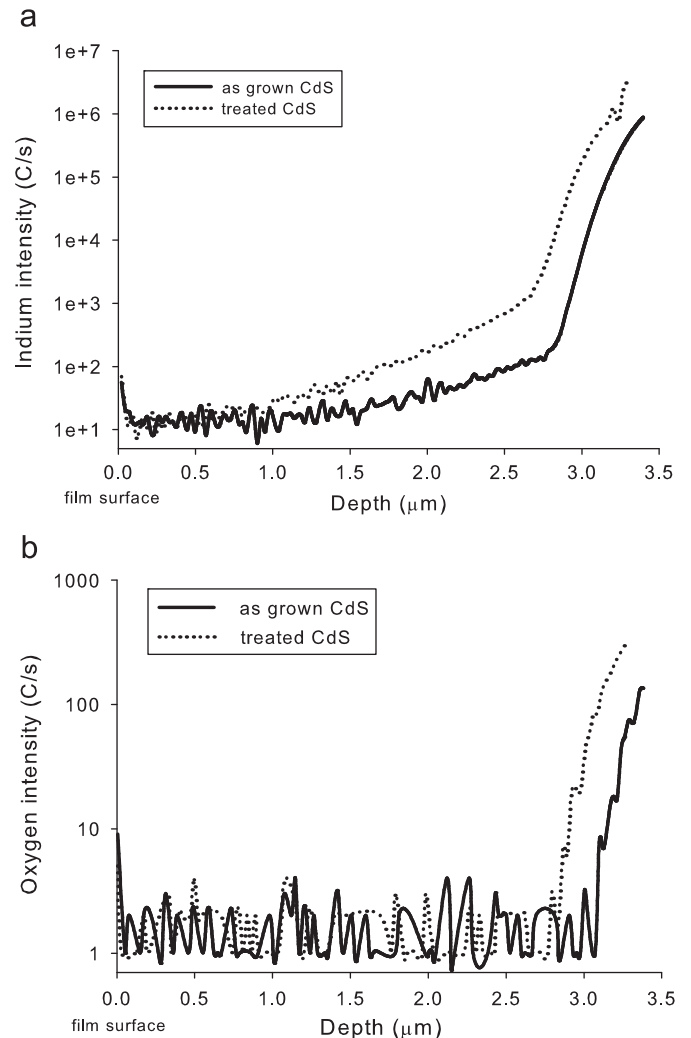


Fig. 6. SIMS depth profiles of (a) In and (b) oxygen recorded from as-grown and O_2 -treated CdS/ITO films (400 °C for 40 min under 100 Torr of O_2). Displacement of the curves is due to differences in CdS thickness at each sampling point.

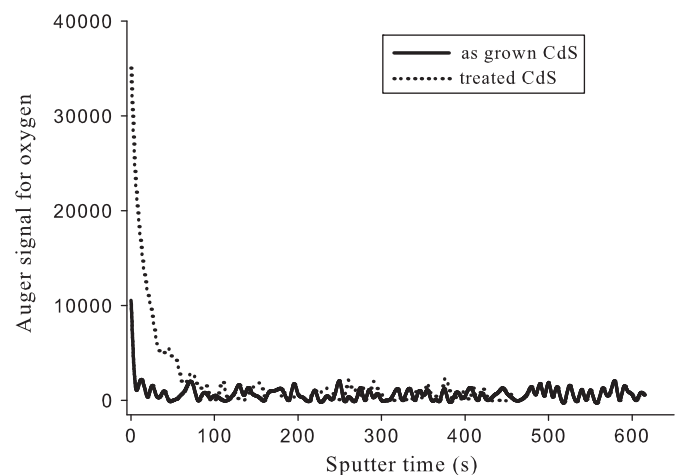


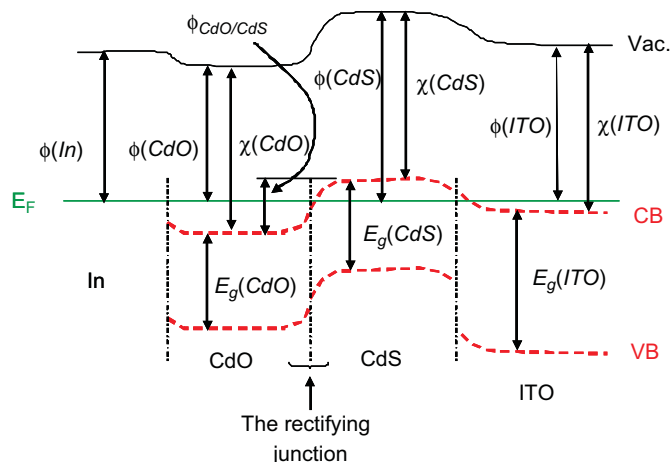
Fig. 7. Auger depth profile for oxygen in both as-grown and O_2 -treated CdS/ITO films (400 °C for 40 min under 100 Torr of O_2). This confirms the presence of a higher concentration of oxygen on the surface of annealed CdS.

and Brinkman's Ohmic result for CdS/SnO₂ was the result of pinholes in CdS.) Further evidence for this is that a recent study (employing photoelectron spectroscopy and sputtering depth

Table 2

Work functions, electron affinities and band gaps of the materials used in the band diagram postulated to explain rectification in oxidised CdS/ITO layers.

	CdS	CdO	ITO	In
Work function	5.0	3.4	4.0	4.12
ϕ (eV)	[24]	[25]	[2]	[26]
Electron affinity	4.5	4.5	4.7	–
χ (eV)	[27]	[25]	[28]	–
Band gap	2.4	2.4	3.6	–
E_g (eV)	[27]	[12]	[29]	–

**Fig. 8.** Proposed band alignments of the In/CdO/CdS/ITO junctions.

profile to investigate band offset of the TCO/CdS interface) [23] has shown that post-growth oxidation of CdS/ITO does not change the band alignment of the interface itself. The experimental finding that CdTe/CdS cells grown on ITO have poorer performance than those on SnO_2 is more likely to be due to out-diffusion of In (confirmed here by SIMS) than to a change in the CdS/ITO band line-up as suggested in [1]. Indeed, In is a known donor in CdTe.

While literature gives contrary indications as to the benefits of treating CdS under oxidising or reducing conditions, the implication of this study for CdTe/CdS solar cell manufacture is that formation of an oxide layer on CdS is to be avoided, since it will create a field at the resulting CdO/CdS junction that is in opposition to that at the p–n junction. Such a field might be expected to reduce device efficiency, presuming that the structure survives over-growth by CdTe and the subsequent device processing.

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