Growth and process optimization of CdTe and CdZnTe polycrystalline films for high efficiency solar cells

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Abstract

Polycrystalline CdTe solar cells with efficiencies of approximately 10% were achieved by metal organic chemical vapor deposition growth of CdTe on glass/SnO_2/CdS substrates. An *in situ* pre-heat treatment of the CdS substrate at 450 °C in an H_2 ambient was found to be essential for high performance devices because it removes oxygen-related defects on the CdS surface. This heat treatment also results in a cadmium-deficient CdS surface which may, in part, limit the CdTe cell efficiency to 10% owing to cadmium vacancy related interface defects. The $CdCl_2$ treatment used in CdTe cell processing was found to promote grain growth, reduce series resistance and interface state density, and change the dominant current transport mechanism from thermally assisted tunneling and recombination via interface states to recombination in the depletion region. These beneficial effects resulted in an increase in the CdTe/CdS cell efficiency from around 2% to approximately 9%. In addition to the CdTe cells, polycrystalline 1.7 eV CdZnTe films were grown by molecular beam epitaxy for tandem cell applications. CdZnTe/CdS cells processed using the standard CdTe cell fabrication procedure resulted in 4.4% efficiency, high series resistance, and a band gap shift to 1.55 eV. Formation of Zn–O at and near the CdZnTe surface was found to be the source of high contact resistance. A saturated dichromate etch instead of the Br_2:CH_3OH etch prior to contact deposition was found to solve the contact resistance problem. The $CdCl_2$ treatment was identified to be the cause of the observed band gap shift owing to the preferred formation of $ZnCl_2$. A model for the band gap shift along with a possible solution using an overpressure of $ZnCl_2$ in the annealing ambient is proposed. Development of a sintering aid which promotes grain growth and preserves the optimum 1.7 eV band gap is shown to be the key to successful wide gap CdZnTe cells.

1. Introduction

Thin film polycrystalline cell efficiencies higher than 20% can be achieved using a tandem cell design. For a two-cell tandem design, the optimum band gaps for the top and bottom cells are 1.7 eV and 1 eV respectively [1]. Considerable progress has been made in the area of the bottom cell, with small-area $CuInSe_2$ cell efficiencies in excess of 14% having been reported recently [2]. However, a compatible wide band gap (1.7 eV) material for the top cell has not yet been developed. CdTe and CdZnTe alloys are considered for top cell applications. CdTe is a promising polycrystalline wide

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band gap material that has given small-area single-cell efficiencies in excess of 12% [3]. However, the CdTe bandgap is 1.45 eV, instead of 1.7 eV which is the optimum for the top cell. Thus, there are two approaches for realizing the goal of 20% efficient polycrystalline cells with a tandem structure. The first approach involves improving CdTe cell efficiencies in excess of 15% and augmenting that with a small amount of power from the bottom cell. The second approach involves developing a 1.7 eV bandgap CdZnTe top cell with an efficiency of approximately 10% to take greater advantage of the bottom cell efficiency owing to higher subgap transmission. This paper describes the investigation of growth and process optimization of CdTe and CdZnTe cells in order to understand the efficiency-limiting defects and mechanisms. Future directions are suggested to improve their efficiencies to a point where they can be a potential candidate for approximately 20% efficient tandem cells.

2. Experimental details

2.1. Film growth

CdTe films were grown on CdS/SnO_2/glass substrates by metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). In the MOCVD growth dimethylcadmium was used as the cadmium source, and diallyltellurium and diisopropyltellurium were used as the tellurium sources. The CdTe films were grown at a substrate temperature in the range 300–400 °C with a reactor pressure of 250 Torr. The Cd/Te ratio in the growth ambient was varied from 0.4 to 4.0. MBE CdTe and $Cd_{1-x}Zn_xTe$ ($x=0.35$, will be referred to as CdZnTe in the paper) films were grown using a Varian Gen II MBE system and elemental sources were used for all constituents having a purity of at least 99.999%. The substrates were baked out at 250 °C for 3–4 h before film growth. The substrate temperature was kept at 275 °C for 30 min to initiate film growth and was increased to 300 °C for the remainder of the run [4].

2.2. Cell fabrication

P–i–n front-wall solar cells were fabricated at AMETEK Applied Materials Laboratory. After a dip in a saturated $CdCl_2$:CH_3OH solution, the CdTe/CdS structures were annealed at 400 °C for 30 min in air. Annealed films were etched in bromine–methanol solution for 5 s followed by an evaporation of 1000 Å of copper-doped p^+–ZnTe film. Small-area (8 mm^2) nickel contacts were evaporated to form an ohmic contact [5].

P–n CdTe cells were fabricated by treating the CdTe films with $CdCl_2$ followed by an air anneal at 400 °C for 30 min. Contact to the p-CdTe was made by a sequential evaporation of 100 Å of copper and 400 Å of gold followed by an anneal at 150 °C in argon atmosphere for 90 min. Finally, bromine–methanol etch was performed on the entire structure to etch off any residual cadmium and tellurium oxides [6].

2.3. Material and device characterization

Electrochemical surface photovoltage (SPV) measurement, Auger electron spectroscopy (AES), X-ray photoelectron spectroscopy (XPS), and transmission measurements were used for optical, physical and chemical characterization of the films. Current–voltage–temperature (*J–V–T*), frequency-dependent capacitance–voltage (*C–V*), and bias-dependent spectral response measurements were used to characterize device properties.

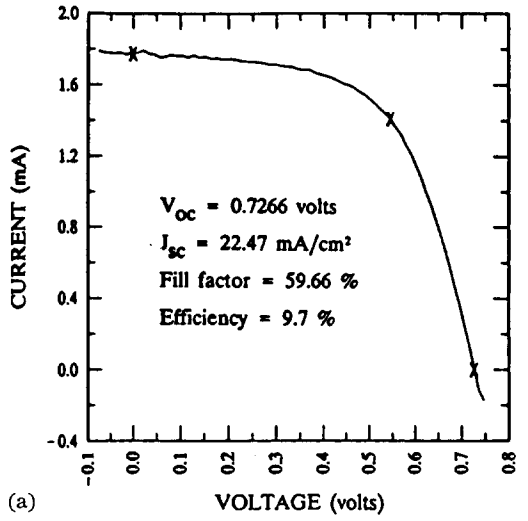
3. Results and discussion

3.1. CdTe solar cells

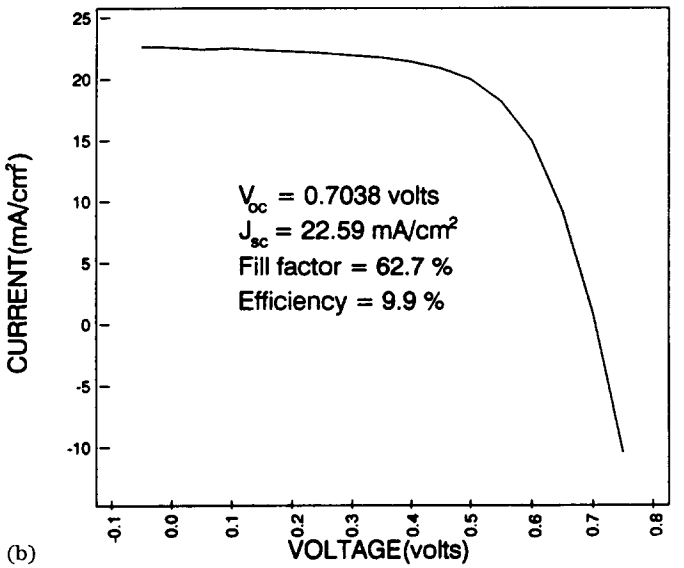
Figures 1 and 2 show the comparison of light current–voltage (*I–V*) and bias-dependent spectral response of 9.7% efficient p–i–n and 9.9% efficient p–n CdTe cells. The cell parameters are similar, and in both cases the spectral response is fairly uniform with sharp cut-off indicating that bulk recombination does not play a major role in the collection efficiency in either cell. However, the spectral responses of both cells show a strong wavelength-independent bias dependence, suggesting that defects at the CdS–CdTe interface are limiting the performance of these cells by making the interface recombination velocity sensitive to applied bias [7].

Attempts were made to improve the interface quality by (a) controlling the CdTe film deposition conditions, (b) adjusting CdTe stoichiometry and (c) varying the *in situ* pre-heat treatment of CdS in hydrogen atmosphere prior to CdTe deposition. Figure 3 shows the light *I–V* curves for CdTe cells with CdS substrates annealed at different temperatures. It clearly shows that a preheat treatment improves both the open-circuit voltage V_{oc} and the fill factor FF but does not change the short-circuit current density J_{sc}. The best results, $V_{oc}=0.68$ V, $J_{sc}=20.5$ mA cm^{-2}, and FF = 0.56, were obtained for substrates annealed at 450 °C for 15 min. The fact that J_{sc} did not change and V_{oc} and FF increased with heat treatment suggests that improved cell performance results from better interface quality. Capacitance *vs.* frequency measurements confirmed that the interface quality was improved after the preheat treatment. Cells fabricated with no pre-heat treatment of CdS not only showed higher absolute capacitance but also a stronger frequency dependence which is generally indicative of the active role of interface states [8].

The fact that the 10% efficient cells subjected to this pre-heat treatment at 450 °C for 15 min showed a strong bias dependence in the spectral response, suggests that pre-heat treatment is necessary but not sufficient to eliminate the detrimental effects of interface recombination. In order to understand the source of these defects, XPS and AES measurements were performed on various CdS films before and after the pre-heat treatment. XPS data (Fig. 4) showed that the pre-heat treatment was able to remove a significant amount of oxygen from the CdS surface. Since it is known that oxygen adsorbed on the surface of CdS gives rise to recombination centers



(a)



(b)

Fig. 1. Comparison of light *I–V* data of (a) a 9.7% efficient p–i–n cell and (b) a 9.9% p–n MOCVD-grown CdTe cell.

[9], it is reasonable to state that oxygen-induced defects on the CdS surface could be responsible for the large number of interface states and poor performance of the untreated cells.

However, depth-resolved AES measurements made on the annealed CdS film showed that 450 °C heat treatment in hydrogen causes the CdS surface to become cadmium deficient ([Cd]/[S] < 1) in addition to removing oxygen [8]. It is well known that cadmium deficiency in CdS gives rise to an acceptor type defect level which is situated at 0.26 eV above the valence band [10].

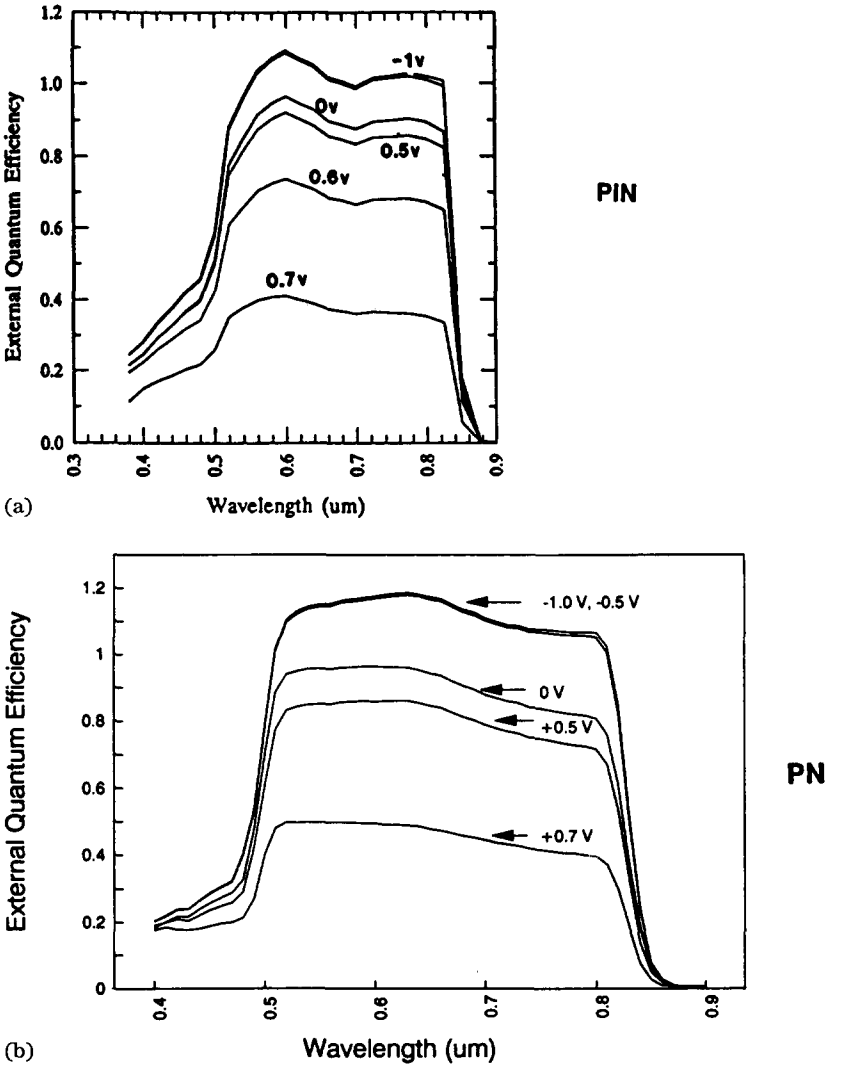


Fig. 2. Comparison of bias-dependent spectral response data of (a) a 9.7% p–i–n cell and (b) a 9.9% p–n CdTe cell.

This can produce a high resistivity CdS surface layer, which is known to reduce V_{oc} and FF in $CuInSe_2$/CdS solar cells [11]. A similar mechanism is possible in CdTe/CdS cells, which may in part be responsible for limiting the efficiency to 10%.

Since cadmium deficiency in CdS is a potential source of interface defects, one way of reducing such defects is to grow CdTe in cadmium-rich conditions. This was attempted by gradually increasing the [Cd]/[Te] ratio in the vapor from 0.4 to 4.0. The 10% efficient cells were grown with a [Cd]/[Te] ratio of 0.4, in a cadmium-deficient ambient. The SPV responses of these films

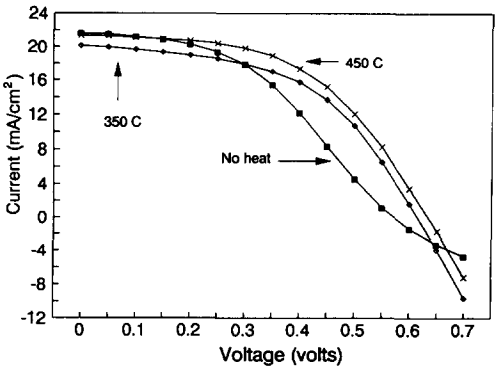


Fig. 3. Light *I–V* data of CdTe/CdS solar cells fabricated on CdS/SnO_2/glass substrates annealed at different temperatures.

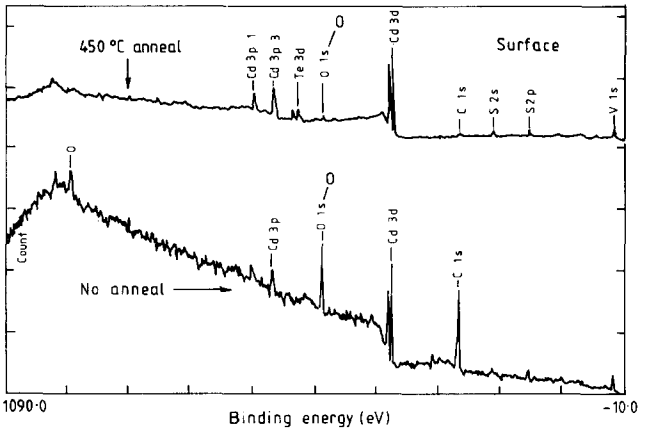


Fig. 4. XPS data on the surfaces of CdS substrates before and after annealing at 450 °C in hydrogen atmosphere inside the MOCVD reactor.

were measured with light incident on the CdTe film side. Figure 5 shows electrochemical SPV spectra of CdTe films grown on CdS with various [Cd]/[Te] ratios. In order to separate the electrolyte–CdTe junction contribution from the CdTe–CdS interface contribution, only the SPV response in the long wavelength region is shown in the figure. It is interesting to note that the cadmium-rich films show a significant increase in the SPV, suggesting that the excess cadmium in the CdTe film is eliminating the cadmium deficiency at the CdS–CdTe interface. Since the SPV response is an indicator of V_{oc}, it is possible to expect higher V_{oc} on films grown under cadmium-rich conditions compared with 9.7% efficient CdTe cells grown in a tellurium-rich ambient. The films are now being subjected to the standard post-deposition 400 °C for 30 min air anneal for cell fabrication. If the higher SPV response is maintained throughout the cell processing, then we should

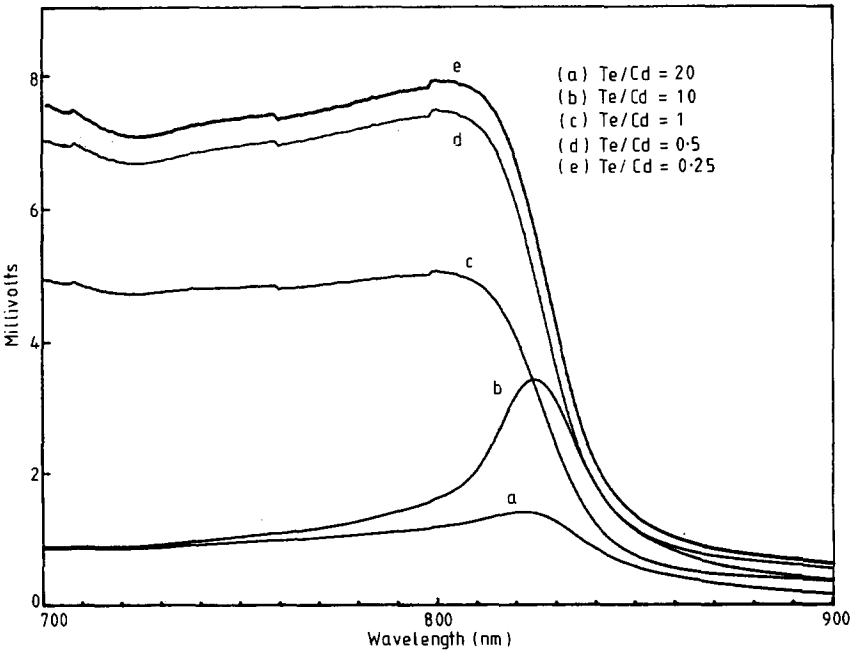


Fig. 5. Surface photo voltage spectra of CdTe films grown by MOCVD on CdS/SnO_2/glass substrates with different [Cd]/[Te] ratios.

be able to attain a higher V_{oc} and efficiency compared with the 10% efficient cells.

In order to estimate the maximum attainable efficiency as a result of the improved quality of the CdTe–CdS interface, model calculations were performed using a collection function approach. This was done by first calculating the collection function (ratio of zero bias quantum efficiency to quantum efficiency at different bias voltages) as a function of applied bias using bias-dependent spectral response data (Fig. 2). The losses in V_{oc} and FF due to the collection function were calculated according to [7, 11]:

$$\Delta V_{oc} = (AKT/q) \ln \eta V_{oc}$$

$$\Delta FF = (V_{mp}/V_{oc})(1 - \eta V_{mp})$$

where A is the ideality factor, η is the collection function, and V_{mp} is the voltage at the maximum power. For a 9.7% efficient MOCVD CdTe cell, the calculated losses in V_{oc} and FF were 0.05 V and 0.12 respectively. In addition, reverse bias spectral response measurements indicate (Fig. 2) an additional loss of at least 10% (1.5 mA cm^{-2}) in J_{sc} due to interface recombination. If these losses can be eliminated by improving the interface quality then we project that cell efficiencies of 13.5% can be achieved from the MOCVD CdTe cells.

A further improvement in efficiency can be achieved by eliminating the loss due to absorption of high energy photons in the thick (1500 Å) CdS

window layer. The 10% cells had approximately 1500 Å of CdS on SnO_2, and the estimated loss in J_{sc} due to absorption is 4 mA cm^{-2} [5]. This results in an additional loss of 0.02 V and 0.08 in V_{oc} and FF respectively. Thus, by eliminating this loss mechanism along with the interface recombination, it is possible to achieve 18% efficient CdTe cells. Attempts are being made to deposit thin CdS films by the chemical immersion method [12]. We have successfully grown CdS films in the thickness range 400–1400 Å by controlling the immersion time and have found an appreciable improvement in the transmission of 400 Å CdS film in the short wavelength range. Thus a combination of optimum pre-heat treatment, proper [Cd]/[Te] ratio, and thin CdS films should yield a significant improvement in the MOCVD CdTe cell efficiency.

3.2. CdZnTe solar cells

Polycrystalline CdZnTe films with a 1.7 eV band gap were successfully deposited by MBE onto CdS/SnO_2/glass substrates [4]. However, CdZnTe solar cells fabricated by the identical process sequence used successfully for high efficiency CdTe cells gave efficiencies of only around 4.4%. In addition, the CdZnTe band gap shifted from 1.7 eV to 1.55 eV and the series resistance (around 2–6 Ω cm^2) was 3–5 times higher than in the counterpart CdTe solar cells. Detailed investigations were conducted to understand and remove the source of these problems.

In order to find and eliminate the source of high resistance, depth-resolved AES and XPS measurements were performed near the CdZnTe surface after annealing (400 °C for 30 min in air without the $CdCl_2$ treatment) and subsequent chemical etching to investigate process-induced changes in the CdZnTe surface which can prevent the formation of good ohmic contacts [13]. XPS analysis and AES profiles in Fig. 6 show that without any post-anneal chemical etch, a significant amount of Cd–O, Te–O and Zn–O are present at and below the CdZnTe surface. After an etch in Br_2:CH_3OH, which was used in the standard cell fabrication prior to ZnTe/Ni back-contact deposition, both cadmium and tellurium oxides were removed from the surface but the Zn–O remained at and below the surface, responsible in part for the high series resistance. In addition, the CdZnTe surface is not as tellurium rich ([Te]/[Cd+Zn] ≈ 1.2) as the counterpart CdTe surface where the [Te]/[Cd] ratio is approximately 1.5–2. It has been suggested that a tellurium-rich surface can facilitate the ohmic contact formation on p-type CdTe [14].

In an attempt to remove the Zn–O and make the CdZnTe surface tellurium rich, various chemical etchants were investigated. Figure 6 shows that a post-anneal saturated dichromate ($K_2Cr_2O_7$:H_2SO_4) etch removed the near-surface region that contained Zn–O and yielded a tellurium-rich surface layer approximately 0.15 μm thick with little or no detectable trace of cadmium, zinc or oxygen. *C–V* measurements made on the dichromate-etched surface confirmed a much higher carrier concentration of around 2×10^{17} cm^{-3} in the tellurium-rich surface layer which gradually dropped down to the bulk

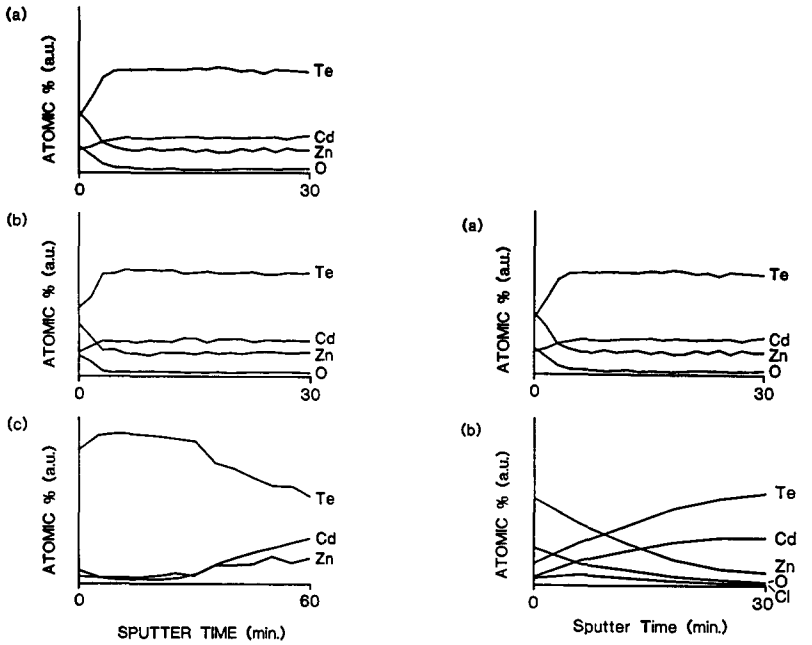


Fig. 6. Auger depth profiles of air-annealed CdZnTe films after (a) no post-anneal etch, (b) Br_2:CH_3OH etch, and (c) saturated dichromate etch.

Fig. 7. Auger depth profiles of air-annealed CdZnTe films (a) without $CdCl_2$ treatment and (b) with $CdCl_2$ treatment.

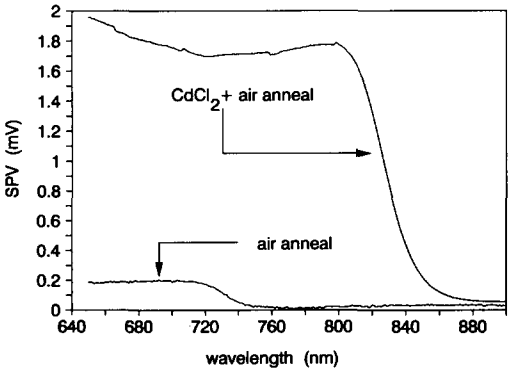


Fig. 8. Electrochemical surface photovoltage spectra of air-annealed CdZnTe/CdS structures with and without the $CdCl_2$ treatment.

doping concentration of around 5×10^{15} cm^{-3} over a distance of 0.15 μm [13]. This should eliminate the contribution from high contact resistance to the measured high series resistance.

The next step was to investigate the process-induced band gap shift observed in processed CdZnTe films. AES depth profiles shown in Fig. 7 and the SPV spectra in Fig. 8 after the standard air anneal, with and without

the $CdCl_2$ treatment, clearly demonstrate that it is not the air anneal itself, but the $CdCl_2$ treatment coupled with the air anneal that is responsible for the band gap shift. The cells were fabricated with the $CdCl_2$ treatment. The Auger profiles show that after the $CdCl_2$ treatment, out-diffusion of zinc from the bulk toward the surface occurs which reduces the bulk zinc content and decreases the band gap, as demonstrated by the shift in the cut-off edge toward the longer wavelength in the SPV spectra of Fig. 8. A proposed model for the phenomenon stems from the fact that, thermodynamically, the formation of $ZnCl_2$ is preferred over $CdCl_2$ [15]. Therefore, introducing $CdCl_2$ onto the surface and into the CdZnTe bulk triggers the formation of $ZnCl_2$ which has a much higher vapor pressure and lower melting point (318 °C [15]) than $CdCl_2$, resulting in the out-diffusion of zinc. This process, where cadmium from the $CdCl_2$ substitutes for lattice zinc, resulting in $ZnCl_2$ formation can be described by the following equation:

$$Cd_{1-x}Zn_xTe + yCdCl_2 \rightleftharpoons Cd_{1-x+y}Zn_{x-y}Te + yZnCl_2$$

If $y > x$, all of the zinc will be consumed and CdZnTe will reduce to CdTe.

SPV data (Fig. 8) taken on the CdZnTe/CdS structures show that if the $CdCl_2$ treatment is bypassed to preserve the band gap, a very weak photoresponse is observed, resulting in only 1%–2% efficient cells. However, the SPV data clearly show that incorporation of $CdCl_2$ during the processing of CdZnTe cells resulted in much higher photovoltages but the cut-off edge (or band gap) shifted from 1.7 V to 1.55 eV. The $CdCl_2$ treatment was also found to reduce the series resistance of the CdZnTe/CdS cells by a factor of about 10.

In order to investigate both the need for and the beneficial effects of the $CdCl_2$ treatment on CdTe-based polycrystalline solar cells, experiments were first conducted on p–i–n CdTe solar cells fabricated with and without the $CdCl_2$ treatment to eliminate the complication due to the presence of zinc. We have shown elsewhere [16] that the $CdCl_2$ treatment is essential for high efficiency MBE-grown CdTe cells because it promotes CdTe grain growth from approximately 0.1 μm to approximately 1 μm, resulting in an increase in V_{oc} from 385 to 720 mV, J_{sc} from 10.5 to 23.1 mA cm^{-2}, FF from 0.32 to 0.51 and cell efficiency from 1.3% to 8.6%. Other investigators have observed similar improvements due to the $CdCl_2$ treatment [6, 17]. In addition to quantifying the improvements in cell parameters, attempts were made to understand the effects of the $CdCl_2$ treatment on bulk properties, interface quality and carrier transport mechanisms. The CdTe/CdS SPV response in Fig. 9 showed a significant increase over the entire long wavelength range of 700–880 nm for cells annealed with $CdCl_2$ compared with cells annealed without $CdCl_2$. Since in our SPV measurements, light is incident on the back side (not the sun side) of the CdTe cell structure, the long wavelength photons near the CdTe cut-off (around 840 nm) are absorbed in the CdTe region near the CdTe–CdS interface. Hence, the significant increase in SPV response clearly supports an improved interface quality due to $CdCl_2$-induced grain growth. This is not surprising since grain growth

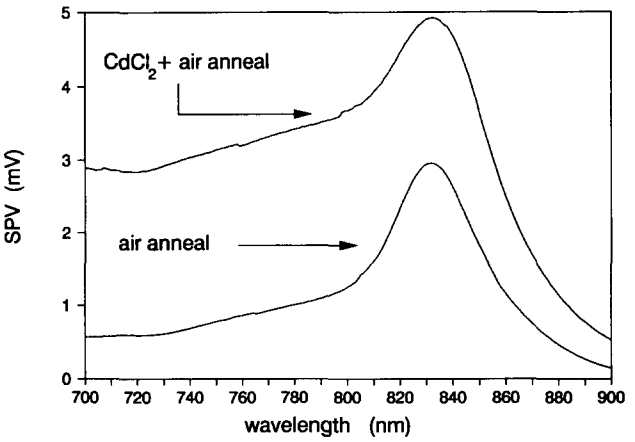


Fig. 9. Electrochemical surface photovoltage spectra of air-annealed CdTe/CdS structures with and without the $CdCl_2$ treatment.

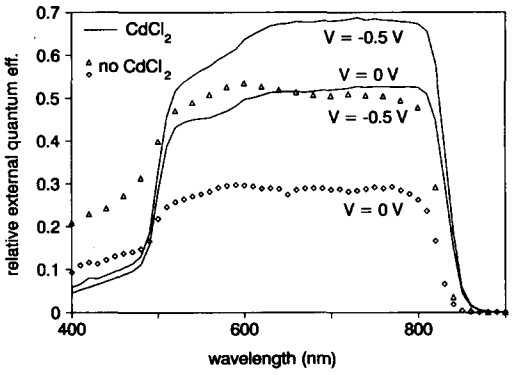


Fig. 10. Bias-dependent spectral response of completed Ni/ZnTe/CdTe/CdS/SnO_2/glass solar cells with $CdCl_2$ (solid lines) and without $CdCl_2$ (symbols). The applied reverse bias values are noted.

reduces the number of grain boundaries intersecting the interface which should result in reduced interface state density. Spectral response measurements shown in Fig. 10 also revealed a significant increase in bulk and interface quality due to the $CdCl_2$ treatment. The spectral response of a p–i–n device is generally dominated by interface recombination since the bulk is essentially depleted. Figure 10 shows that even after the $CdCl_2$ treatment, the spectral response showed an appreciable bias dependence with much higher response at 0.5 V applied reverse bias. This is indicative of the fact that even though the $CdCl_2$ treatment significantly improves the interface quality, it does not completely eliminate those interface states which can increase the interface recombination velocity.

Temperature dependent dark *J–V* measurements were performed to identify and quantify changes in the fundamental current transport properties

due to the improved interface quality. CdTe/CdS cells, with and without $CdCl_2$ treatment, were analyzed by fitting the J–V–T data to equations governing various transport mechanisms such as direct and multi-step tunneling [18], thermally assisted tunneling [19, 20], depletion region recombination [21], interface recombination [22], etc. It was determined that without the $CdCl_2$ treatment, current transport is dominated by thermally assisted tunneling of holes from the CdTe into interface states followed by interface recombination, characterized by an activation energy of 0.56 eV and $J_0 = 4.7 \times 10^{-7}$ A cm^{-2}. For cells treated with $CdCl_2$, the dominant mode of current transport was found to shift from a tunneling–interface recombination mechanism to recombination via traps within the CdTe depletion region, indicating substantial reduction in interface state density. This change is manifested in an increase in the activation energy for current transport from 0.56 eV to 0.85 eV which results a significantly lower J_0 value of 2.6×10^{-9} A cm^{-2}, accounting for the observed increase in V_{oc} from 385 mV to 720 mV.

Having established quantitatively the beneficial effects of the $CdCl_2$ treatment on CdTe material and device properties, in addition to the detrimental (band gap shift) effects on CdZnTe, it became evident that a sintering aid other than straight $CdCl_2$ is essential for obtaining efficient CdZnTe solar cells. However, some combination involving $CdCl_2$ may be a good choice since the $CdCl_2$ treatment results in partial grain growth (determined from scanning electron microscopy measurements) and significantly lower series resistance yielding a much higher photoresponse (Fig. 8). Since the band gap shift appears to result from the substitution of cadmium for zinc, attempts were made to control the band gap shift and induce grain growth by dipping the CdZnTe films in various solutions of $CdCl_2 + ZnCl_2$ in methanol prior to air annealing at different temperatures. Only limited success was obtained using this method since the $ZnCl_2$ readily evaporates into the anneal ambient at temperatures greater than 320 °C, leaving $CdCl_2$ alone which results in a partial band gap shift. For lower anneal temperatures (less than 320 °C), negligible band gap shift occurs but this is accompanied by little or no grain growth and poor photoresponse. Attempts are underway to anneal $CdCl_2$-treated CdZnTe surfaces in a $ZnCl_2$ overpressure ambient using a closed system to prevent the outdiffusion of zinc and induce grain growth. In this system, $ZnCl_2$ is heated in a separate boat next to the CdZnTe sample. Thus, development of a sintering aid that can promote CdZnTe grain growth without the bandgap shift remains the major obstacle for the success of wide band gap CdZnTe cells for tandem cell applications.

4. Conclusions

MOCVD grown polycrystalline CdTe solar cells with efficiencies of aproximately 10% were demonstrated using both p–i–n and p–n structures. *In situ* pre-heat treatment of glass/SnO_2/CdS substrates at 450 °C for 15 min prior to CdTe deposition was found to be essential for high performance

devices because it removes oxygen and related defect states. The heat treatment also simultaneously makes the CdS surface cadmium deficient, resulting in cadmium vacancy-related interface states because of which even the 10% efficient cells show a strong bias-dependent spectral response and lower V_{oc} and FF compared with the best reported [5] cells. Preliminary model calculations suggest that the removal of these states can increase the cell efficiency from 10% to 13.5%. Photon absorption in the CdS film also limits the cell performance and elimination of this loss mechanism can result in efficiencies in excess of 18%.

The CdTe process sequence cannot be used to fabricate efficient CdZnTe cells because it results in high resistance and a band gap shift from the desired value of 1.7 eV to 1.55 eV. The contribution to the high series resistance from the non-ohmic back contact was solved by using a saturated dichromate instead of the $Br:CH_3OH$ post-anneal etch, which resulted in a p-type surface doping concentration of 2×10^{17} cm^{-3}. It is shown that $CdCl_2$ is essential for high efficiency CdTe solar cells because it promotes grain growth which improves bulk collection, reduces interface state density, and eliminates the tunneling of carriers through the interface to improve V_{oc}, J_{sc} and efficiency. However, the use of a $CdCl_2$ dip prior to air anneal was established to be the main source of the observed band gap shift in CdZnTe due to $ZnCl_2$ formation by substitution of cadmium for lattice zinc. This also resulted in incomplete grain growth in CdZnTe since much of the $CdCl_2$ was consumed by this process. Development of an alternative sintering aid, which induces grain growth but prevents the band gap shift, is the key to the success of wide gap polycrystalline CdZnTe solar cells for tandem cell applications.

Acknowledgments

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