Solar Energy Materials and Solar Cells 28 (1993) 305–316
North-Holland

Solar Energy Materials and Solar Cells

Preparation and characterisation of electrodeposited n-CdS/p-CdTe thin film solar cells

S.K. Das and G.C. Morris

Department of Chemistry, University of Queensland, Brisbane, Qld 4072, Australia

Received 4 June 1992; in revised form 31 July 1992

Cadmium sulphide and cadmium telluride films have been electrodeposited for n-CdS/p-CdTe solar cells. Cell efficiency varied considerably from 9.5% to 11.5% for each deposition set. The reverse saturation currents of 9.5% and 11.5% cells at 298 K were 25 and 6.7 nA cm^{-2}, respectively. The cells with higher efficiency has a lower number of interface states than the less efficient cells. The 11.5% cell had interface states (N_{IS}) of 3×10^{10} cm^{-2} eV^{-1} at zero volt bias in dark and when it was illuminated with 35 mW cm^{-2} light at zero volt bias N_{IS} increased by two orders to 1.2×10^{12} cm^{-2} eV^{-1}. At higher frequency the large voltage intercept of the Mott–Schottky plot indicates the existence of the near intrinsic layer of the polycrystalline heterojunction.

1. Introduction

CdS/CdTe heterojunction thin film solar cells are one of the promising photovoltaic devices for low cost large area terrestrial applications. Several workers have studied CdS/CdTe cells prepared by different techniques. Highly efficient polycrystalline CdS/CdTe cells have been fabricated by different techniques, viz. screen printing [12], close-spaced vapor transport [3–6], electrodeposition [7–14], vacuum evaporation [15], chemical vapor deposition [16], sintering [17], etc. In our laboratory we have prepared thin film n-CdS/p-CdTe cells by electrodeposition onto ITO coated substrates.

The electrodeposition process is suitable because of its advantage as a low cost technique. The cathodic electrodeposition of CdTe films from aqueous electrolytes was first carried out by Panicker, Knaster and Kroger [18] who demonstrated that uniform films with controlled stoichiometry could be obtained using the simple electrodeposition technique. They described the effect of rest potential and the temperature of the bath solution on the properties of the film. In this paper we present the preparation and characterisation of our electrodeposited n-CdS/p-CdTe solar cells.

Correspondence to: S.K. Das, Department of Chemistry, University of Queensland, Brisbane, Qld 4072, Australia.

2. Cell fabrication:

The cell fabrication steps consists of the following main steps:

(a) Electrodeposition of a 100 nm thick CdS film onto cleaned ITO/glass substrate (10 Ω/□, purchased from Hoya Corporation, Japan).

(b) Electrodeposition of an about 2 μm thick CdTe film onto freshly prepared CdS film.

(c) Annealing of the CdS/CdTe structure at 400°C for the type conversion of n-CdTe for the formation of the n-CdS/p-CdTe heterojunction.

(d) Chemical etching of the surface of the CdTe film followed by hydrazine hydrate treatment and metallization for the electrical contact to CdTe.

2.1. Electrodeposition of CdS films

A 0.2 M Cd^{2+} solution was made using $CdCl_2 \cdot H_2O$ dissolved in Milli-Q water with a resistivity of 18 MΩ cm. The bath solution was electropurified at 5 mV more positive potential than the measured cadmium potential for about 12 h at 90°C. Sodium thiosulphate (AR grade) was added to make a 0.01 M $S_2O_3^{2-}$ solution. The pH was adjusted to around 2.5 by adding HCl (BDH chemicals).

The ITO/glass substrate was cleaned by a sequence of steps which include ultrasonic washing in organic solvents and Milli-Q water and isopropanol vapour degreasing. The substrate holder was made of teflon by which the contact to ITO/glass was made by a platinum pressure plate which was connected to the external circuit.

A clear CdS film of 25 cm^2 and 100 nm thickness was deposited at 40 mV more positive potential than the measured cadmium potential (approximately −620 mV with respect to the saturated calomel electrode, SCE) in about 2 h.

2.2. Electrodeposition of CdTe films

A 2.5 M Cd^{2+} solution was made by using $3CdSO_4 \cdot 8H_2O$, $CdCl_2 \cdot H_2O$ (for Cl doping) and Milli-Q water. The solution was electropurified at 10 mV more positive potential than the measured cadmium deposition potential for about 12 h at 90°C. The pH was adjusted to around 2. The inclusion of tellurium ions into the solution was performed by injecting Te ions ($HTeO_2^+$) from a 5N pure Te rod. The Te concentration was adjusted to 120 ppm which was confirmed by using a computer controlled atomic absorption spectrometer (Varian AA300). The CdTe film of around 2 μm thickness was deposited in about 2 h at a quasi-rest potential, QRP of +25 ±5 mV relative to the measured cadmium deposition potential using a split anode system (Te and C). The Te electrode acted as both calomel electrode and source of $HTeO_2^+$ in the solution. The concentration of $HTeO_2^+$ ions was kept constant by adjusting the current split through the anode system.

2.3. Cell completion

After electrodeposition of the CdTe film the glass/ITO/CdS/CdTe structure was dried by nitrogen gas and kept in vacuum for several hours and then annealed

at 400°C for 15 min for the type conversion of n-CdTe to p-CdTe for the formation of the n-CdS/p-CdTe heterojunction. After cooling down to room temperature the CdTe surface was etched for 2 s with potassium dichromate/sulphuric acid (1:1) solution followed by a 15 min hydrazine hydrate treatment. The film was once again cleaned with Milli-Q water and dried by nitrogen gas flow and then immediately transfered to the vacuum system (10^{-6} Torr) for copper and gold deposition. Several cells of 2 mm diameter were made after deposition of 2 nm of Cu and 100 nm of Au. Silver paste was applied to the gold and ITO layer to obtain mechanical strength.

3. Results and discussion

3.1. Current–voltage measurements

Current–voltage measurements were obtained by a computer controlled system with a 300 W oriel solar simulator to produce 1000 W m^{-2} AMl radiation tested by a Si-cell which was calibrated at the Solar Energy Research Institute, SERI, USA.

The electrical characteristics of the cells were obtained by using the diode equation

$$J = J_0\{\exp[q(V - iR_s)/AkT] - 1\}, \quad (1)$$

where J_0 is the reverse saturation current, q is the electronic charge, R_s is the series resistance, A is the diode quality factor, k is the Boltzmann constant and T is the temperature.

Fig. 1 shows the J–V characteristic under 1000 W m^{-2} AMl radiation for cell A and cell B having efficiencies 9.5% and 11.5%, respectively. The cell efficiency was defined as the ratio of electrical power out and light power in. The output power

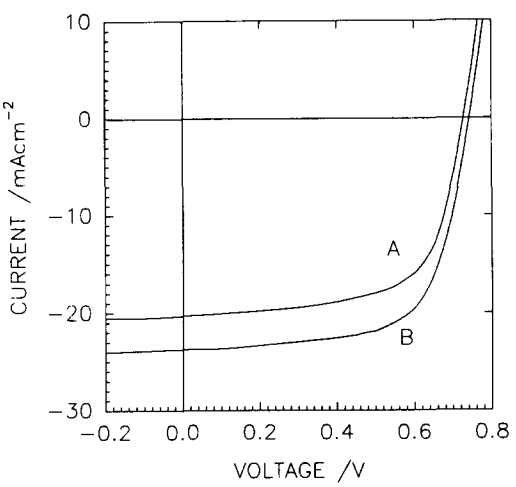

Fig. 1. Current density versus voltage (J–V) characteristics under 1000 W m^{-2} solar simulation for two cells. Efficiency of cell A: 9.5%; cell B: 11.5%.

was the product of the open circuit voltage V_{oc} and short circuit current and fill factor. The cell parameters of cell A and cell B were as follows:

cell A: $V_{oc} = 727$ mV, $J_{sc} = 20.4$ mA cm^{-2}, FF = 0.64, efficiency = 9.5%,

cell B: $V_{oc} = 746$ mV, $J_{sc} = 23.7$ mA cm^{-2}, FF = 0.65, efficiency = 11.5%.

It has been observed that in each set of deposition of 25 cm^2 area the cell efficiencies varied considerably from 9.5% to 11.5%. This variation of cell efficiency was probably due to the variation of growth of CdS and CdTe throughout the substrate from top to the bottom due to the resistance of the ITO substrate and the gradient of the circulation of the bath solution from bottom to the top as the liquid was stirred by a simple teflon coated cylindrical stirrer at the bottom. In our earlier papers [12,13] we have explained in detail how the different growth conditions of CdTe on controlling the QRPs of the deposits and the concentrations of cadmium and tellurium of the bath solution affect the quality of the cells of different sets of deposition. X-ray photoelectron spectroscopy (XPS) showed that all of the films from top to bottom had a stoichiometry similar to a CdTe single crystal to the accuracy permitted by XPS (about 10%). Secondary ion mass spectroscopy (SIMS) had previously [19,20] shown that the CdTe film as described had fewer impurities than a single crystal purchased as 99.9999% pure. Therefore the variation of cell efficiency even for a single set of deposition was not directly related to the impurities of the CdTe film.

The contact resistivity of the cell was measured using the relation

$$R_s = R_c + k/\Phi, \tag{2}$$

where R_s is the series resistance, R_c is the light independent contact resistance and k/Φ is the light dependent resistance. Plotting R_s as a function of $1/\Phi$, where Φ was changed by calibrated neutral density filters the contact resistance, R_c, was the intercept of the R_s axis at $1/\Phi = 0$. The contact resistivities of different cells lie between 0.5 and 1.2 Ω cm^2. This variation is probably due to the variation of the surface of the CdTe deposit due to the unintentional variation of the growth as mentioned before.

Fig. 2 shows the log J–V plot of cell B at different temperatures. The extrapolation of the curve up to $V = 0$ gives the value of J_0 and the slope gave the value of the diode quality factor, A. The parameters J_0 and A are the direct indicators of the dependence of the solar efficiency on the electrical transport properties of the junction and reflect the properties of the depletion layer and junction properties. The cell with a better junction is associated with lower J_0 values for a given diode factor. The value of J_0 and A at 298 K for cell B is 6.7 nA/cm^2 and 2.0, respectively.

Fig. 3 shows the temperature dependence of the diode quality factor, A. The figure shows that the diode quality factor decreases with increasing temperature. This effect was also observed by other workers [21] in polycrystalline CdS/CdTe solar cells.

The reverse saturation current can be written as

$$J_0 = J_{00} \exp(-E_a/kT), \tag{3}$$

where E_a is the activation energy and J_{00} is a weak function of temperature.

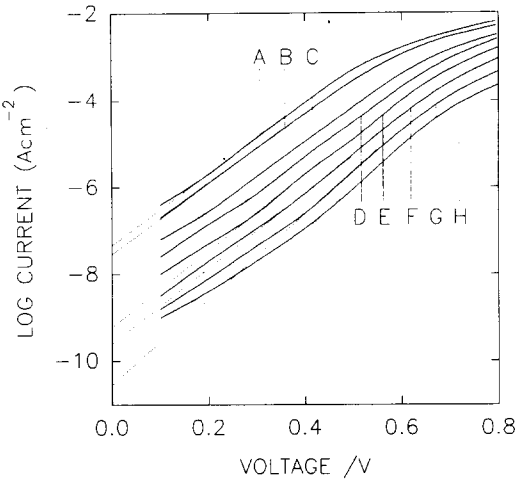

Fig. 2. Current density versus voltage ($J-V$) characteristics in the dark for cell B of fig. 1 for different temperatures (A) 329 K, (B) 320 K, (C) 298 K, (D) 285 K, (E) 273 K, (F) 261 K, (G) 248 K, (H) 232 K.

Fig. 4 shows the plots of log J_0 versus $1/T$ for cell A and cell B. The slopes of each graph gave the value of E_a separately for cell A and cell B. The activation energy for cell B for the measured temperature range was 0.59 eV and that for cell A above 270 K was 0.67 eV. Mitchell et al, [22] observed 0.59 eV as the activation energy above 300 K for their CdS/CdTe cell of which CdS had been deposited on single crystal CdTe. The product AE_a at room temperature for cell B was 1.18 eV which is fairly close to the value of the built-in potential of 1.1 eV as measured by capacitance measurement and also measured by other workers [5]. In fig. 4 plot (B)

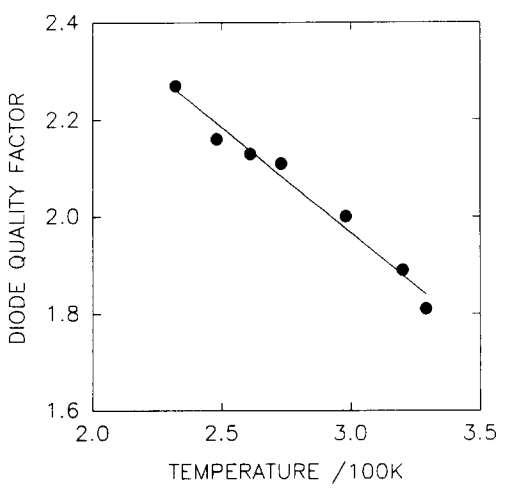

Fig. 3. Temperature dependence of the diode quality factor of cell B of fig. 1.

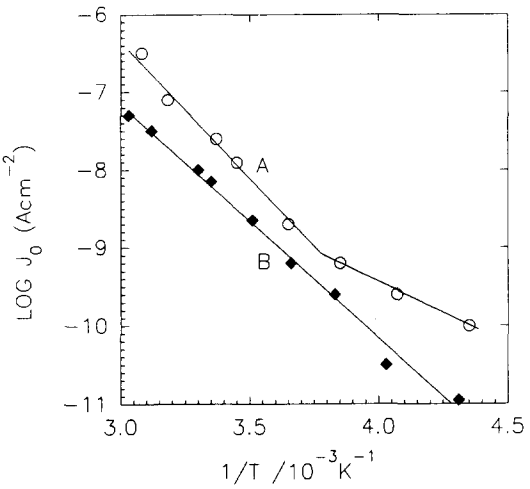

Fig. 4. Temperature dependence of the saturation current of cell A and cell B of fig. 1.

for the whole range of measured temperatures and plot (A) above 270 K show the strong temperature dependence indicating the current flow is controlled by a thermally activated process, presumably interface recombination. In the case of cell A below lower temperature (< 270 K) J_0 is less dependent on temperature which indicates that the current flow is also controlled by tunnelling and was probably due to the interface states caused by the high number of grain boundaries and voids of CdTe near the junction. The higher number of grain boundaries and voids in CdTe of less efficient cells was observed clearly in scanning electron micrographs of the less efficient cells. Anthony et al. [23] also observed a similar type of log J_0 versus $1/T$ graph like that of our cell A for their CdS/CdTe/graphite cell of which CdTe had been deposited by CSVT.

3.2. *Spectral response of the photocurrent*

Fig. 5 shows the external quantum yield (%) with wavelength of cell B. This figure indicates that the cell had about 15% more current collection at -1 V bias than at 0 V bias. At $+0.2$ V bias the current collection was decreased about 15% with a similar spectral dependence indicating a large carrier diffusion length.

3.3. *Morphology*

Fig. 6a shows the X-ray diffraction pattern of the annealed (400°C/15 min as a part of the cell fabrication) CdS film and displayed the reflection from the (002) and (103) planes. The CdS film had a hexagonal crystal structure. Fig. 6b shows the X-ray diffraction pattern of the annealed (400°C/15 min as a part of the cell fabrication) CdTe film and displayed peaks from the (111), (220), (311) and (400) planes. The film had a cubic structure with a lattice constant of 6.6 Å.

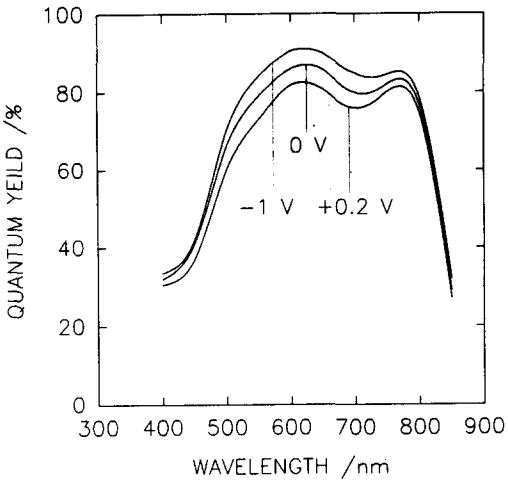

Fig. 5. Spectral response of cell B under different bias conditions.

Figs. 7a and 7b show electron micrographs of a 9.2% cell and a 11.1% cell, respectively. The CdTe deposit of 9.2% cell had smaller grains and more voids than the CdTe deposit of 11.1% cell which was more compact and had less grain boundaries.

3.4. Capacitance measurements

Fig. 8 shows the frequency dispersion of cell A and cell B. The less efficient cell A (9.5%) had a higher frequency dispersion than the higher efficiency cell B

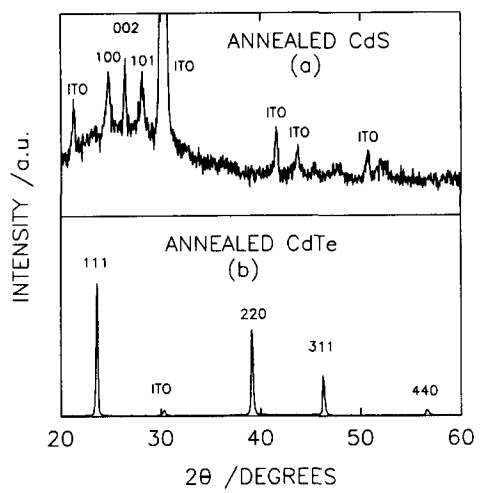

Fig. 6. X-ray diffraction patterns of (a) annealed (400°C/15 min) CdS film and (b) annealed (400°C/15 min) CdTe film.

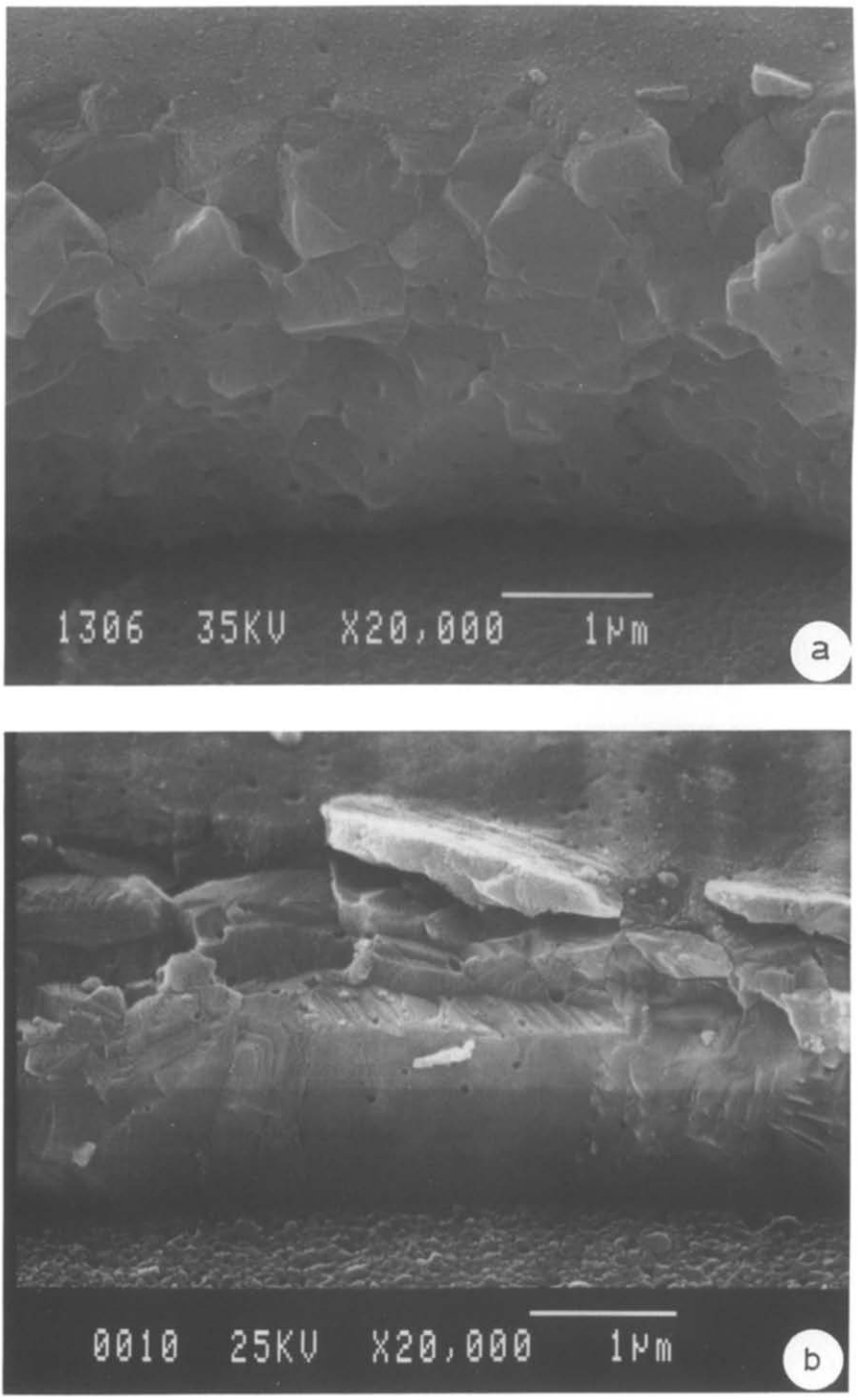

Fig. 7. Electron micrographs of CdS/CdTe structures of (a) the 9.2% cell and (b) the 11.1% cel

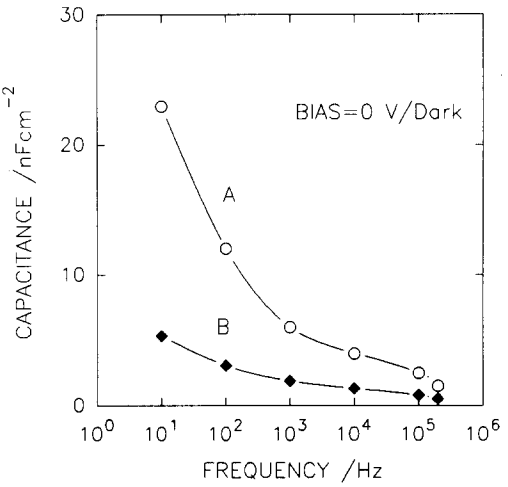

Fig. 8. Frequency dispersion of capacitance of cell A and cell B of fig. 1.

(11.5%). The cell associated with a wide range of energy levels and time constants show a high capacitance value at low frequency where more deep levels can respond to the AC signal.

The total number of states due to depletion and interface can be obtained from the measured capacitance at lower frequency whereas the capacitance at higher frequency is associated with depletion only. The number of interface states can be calculated from the measured capacitance at low and high frequency by using the relations [24]

$$N_{IS} = (C_{LF} - C_{HF})/q, \tag{4}$$

where N_{IS} is the total number of interface states, C_{LF} and C_{HF} are the measured capacitances at lower (≈ 10 Hz) and higher ($\approx 10^5$ Hz) frequency, respectively, q is the electronic charge.

Fig. 9 shows the dependence of the number of interface states with bias voltage for cell A and cell B. At zero volt/dark bias the number of interface states of cell B was 3×10^{10} cm^{-2} eV^{-1} which was one order lower than that of cell A. With negative bias the frequency dispersion was considerably less for both cells and indicated less bandgap states further from the junction.

When illuminated with light the capacitance particularly at lower freqency (≈ 10 Hz) increased rapidly with power due to the excitation of bandgap states responding to the AC signal. Fig. 10 shows the light power dependence of the interface states of cell B. The interface states increased rapidly with illumination. The number of interface states at 0 V bias at 0.7 mW cm^{-2} was 1.4×10^{11} cm^{-2} eV^{-1} and this value was increased to 1.2×10^{12} cm^{-2} eV^{-1} at 35 mW cm^{-2}.

Fig. 11 shows a Mott–Schottky plot of cell B at different frequencies (10, 10^2, 10^3 and 10^4 Hz) in the dark. The ionized charged density (N) was calculated from the slope of the curves using the relation $d(C^{-2})/dV = 2/q\epsilon N$, where ϵ is the

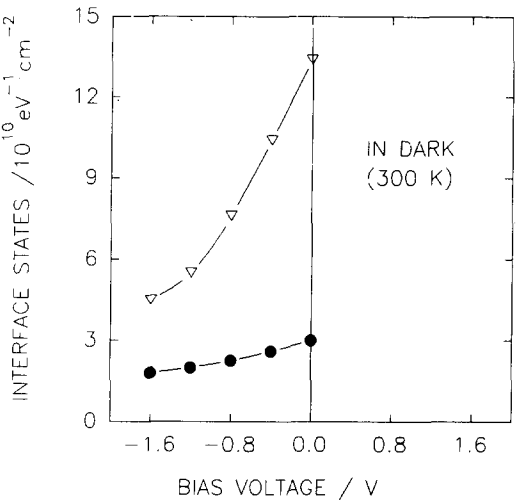

Fig. 9. Dependence of interfacial state density as a function of applied bias voltage of (▽) cell A and (●) cell B of fig. 1.

dielectric constant of CdTe. The ionized charged densities at 10, 10^2, 10^3 and 10^4 Hz are 20×10^{18}, 14×10^{15}, 5.4×10^{15} and 3.3×10^{15} cm^{-3}. The voltage intercept at $C^{-2} = 0$ gave the built-in-potential, V_{bi}. For 10 to 10^3 Hz frequencies the built-in potentials were nearly the same as 1.1 which is close to the value as measured from J–V–T plot. For 10^4 Hz frequency the voltage intercept was higher than 1.4 V. Because of the compensation characteristics of the polycrystalline materials the doping density is not spatially uniform and the existence of a

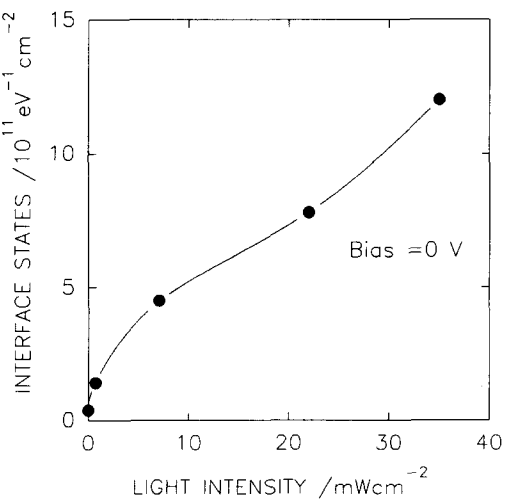

Fig. 10. Dependence of interfacial state density on illumination level at zero volt bias of cell B of fig. 1.

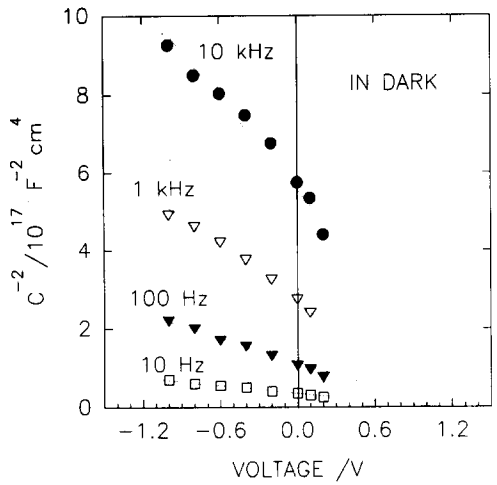

Fig. 11. Mott–Schottky plot of cell B of fig. 1 at different frequencies.

near intrinsic layer near the heterojunction is expected. The higher voltage intercept is due to the existence of the intrinsic layer inside the depletion layer. The thickness W_i of this intrinsic layer can be calculated by using the relation [25]

$$C^{-2} = 2(V_{bi} - V)/q\epsilon N + (W_i/\epsilon)^2, \tag{5}$$

The second term of r.h.s. of eq. (5) is due to the existence of the intrinsic layer. The value of this term was calculated after extrapolating the reverse bias of C^{-2} to voltage $V_{bi} = 1.1$ V as determined from the other C^{-2} versus voltage graphs at 10 to 10^3 Hz frequencies. The thickness of the intrinsic layer (W_i) of cell B was found to be 2 μm which is virtually the full width of the CdTe film.

4. Conclusion

Thin film n-CdS/p-CdTe solar cells have been fabricated from electrodeposited cadmium sulphide and cadmium telluride layers. 9.5% to 11.5% efficient cells were produced from each set of deposition. The activation energy of the 11.5% cell was 0.59 eV for the whole range of measured temperatures whereas that of the 9.5% cell was 0.67 eV above 270 K. The value of the diode quality factor decreases with increasing temperature. The reverse saturation current of the 9.5% and 11.5% cells were 25 and 6.7 nA/cm^2, respectively. The capacitance measurements indicate that the cell with the higher efficiency had a lower number of interface states than the less efficient cell. The number of interface states of the 11.5% cell in the dark at 0 V bias was 3×10^{10} cm^{-2} eV^{-1}. At 35 mW/cm^2 light intensity the number of interface states increased to 1.2×10^{12} cm^{-2} eV^{-1} at 0 V bias. Mott–Schottky plots at 10 to 10^3 Hz indicates the built-in potential to be 1.1 V. The large voltage intercept at 10^4 Hz frequency indicates the existence of the near intrinsic layer of the heterojunction.

Acknowledgement

The research was supported by the Energy Research Development Corporation and the Australian Research Committee. Electron micrographs were taken at the University's Electron Microscope Centre. XPS and SIMS results were taken at the Brisbane Surface Analysis Facility.

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