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Electrical characterization of vacuum-deposited n-CdS/p-CdTe heterojunction devices

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Abstract. The effects of post-deposition processes such as $CdCl_2$ dip and/or annealing in air on the material and device properties of vacuum-evaporated Au-CdTe/CdS-TO heterojunction solar cells have been investigated. The $CdCl_2$ dip followed by air annealing at 300 °C for 5 min improved the device efficiency significantly, resulting in decreased CdTe resistivity and enhanced grain size. The temperature-dependent current–voltage analysis indicated that above 280 K interface recombination dominates the current transport mechanism for the as-grown samples, while depletion region recombination starts to be dominant after annealing the samples with $CdCl_2$. Below 280 K multistep tunnelling is identified to be the dominant transport mechanism. Frequency-dependent capacitance–voltage studies revealed that after annealing with $CdCl_2$ the density of interface states decreases and the quality of the heterointerface improves. The capacitance of the CdS/CdTe heterojunctions has been analysed using a model based on the existence of a single dominant trap level, identified at 0.40 eV above the valence band with a concentration of 5.1×10^{15} cm^{-3}.

1. Introduction

The properties of CdTe make it a prime candidate for terrestrial photovoltaic applications with reported conversion efficiencies of almost 16% for CdS/CdTe thin film devices fabricated by a wide variety of techniques. The history of CdTe laboratory cell efficiencies has been given by Zweibel [1] and an overview of the CdTe thin film solar cells has been written by Bonnet [2]. The fabrication and characteristics of thin film II–VI photovoltaics with emphasis on the CdS/CdTe solar cells have been reviewed by Chu and Chu [3]. Most of the high-efficiency device preparation techniques involve the optimization of the properties of CdTe layer and the CdS/CdTe interface after the film deposition using some chemical and/or temperature processing. However, correlation of these processes, i.e. annealing in an oxygen-containing atmosphere at about 400–500 °C and/or introduction of $CdCl_2$ either during or after CdTe film growth, with the resulting film and device properties seems to vary with the CdTe deposition technique as well as with the specifics of the post-deposition treatments [4, 5]. The process induced and the preparation conditions effects have been investigated in detail for the sintered [6, 7], MOCVD and MBE grown [8, 9], screen printed [10] electrodeposited [11, 12] physical vapour deposited [13, 14] and CSS [15–17] CdS/CdTe devices and materials. Although the conventional vacuum evaporation has proved its potential as a low-cost technique, to our knowledge there is very limited publication on the processing effects on the material and device properties of CdS/CdTe thin film heterojunctions produced with this technique. There is still a lack of understanding of the electrical characterization, especially the junction transport properties of the vacuum-deposited CdS/CdTe structures, which is essential for the photovoltaic operation.

In this work, vacuum-evaporated CdS/CdTe heterojunctions are investigated to identify the specific effects of the post-deposition processing applied to CdTe on the electrical properties of the devices. Thin film CdS/CdTe devices have been prepared by the vacuum-evaporation of CdS and CdTe successively onto commercially available TO-coated glass substrates. Some of the devices were subjected to different post-deposition treatments such as $CdCl_2$ dipping and/or annealing to investigate the effects of post-annealing and $CdCl_2$ dipping on the device performance. Temperature-dependent dark current–voltage studies were carried out to identify the dominant current transport mechanisms before and after the treatments. The temperature- and frequency-dependent capacitance–voltage characteristics were analysed to understand the effects of interface states and traps on the vacuum-deposited CdTe films. The illuminated I–V characteristics were also measured to study factors affecting the device efficiency. The morphological and structural changes in the CdTe films with and without $CdCl_2$

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dipping were investigated by x-ray diffraction, reflection high-energy electron diffraction and scanning electron microscopy.

2. Experiment

2.1. Sample preparation

Conventional oil diffusion vacuum coating units operated at about 10^{-6} Torr have been employed for the deposition of CdS and CdTe thin layers. The cell fabrication process consists of the following main steps:

(i) Deposition of about 1 μm thick indium-doped CdS thin film onto the cleaned TO/glass substrate at about 200 °C. The TO-coated glass substrate has a nominal sheet resistance of 8–10 $\Omega\,\square^{-1}$ and transmission of 85–90%.

(ii) Deposition of about 2 μm thick CdTe film onto the freshly prepared CdS thin layer. The source and substrate temperatures were kept constant at 650 °C and 200 °C respectively.

(iii) Layers were then dipped in $CdCl_2$:CH_3OH (1:100) solution for 2–5 s before annealing in air at different temperatures in the range 300–400 °C for 5–10 min. Some of the samples from the same run were only annealed in air and some of them were left in their as-grown form to determine the effects of $CdCl_2$ and/or annealing on the CdTe material and device properties.

(iv) Etching the unprocessed and processed CdTe surface with $K_2Cr_2O_7$:H_2SO_4:H_2O (7 g:3 g:50 ml) solution followed by a deionized water rinse and blow dry in air.

(v) Completion of the device structure through evaporation of ohmic gold electrodes in a circular geometry with an area of about 0.03 cm^2.

2.2. Sample characterization

The temperature-dependent dark I–V measurements of the heterostructures were carried out in a bath-type LN_2 (liquid nitrogen) cryostat connected to the temperature controller unit of a DLS-82E system within the temperature range of 90–400 K. The temperature-dependent C–V measurements were carried out using the C–V mode of the DLS-82E system at 1 MHz frequency in the same temperature range. The frequency-dependent measurements were carried out using PAR124 lock-in amplifier operated in conjunction with a M184 current sensitive preamplifier in the frequency range of 6×10^2–2×10^5 Hz at room temperature. Solar cell data were determined by illuminated I–V measurements taken at room temperature under an illumination of 80 mW cm^{-2}. The films were also characterized by x-ray diffraction, RHEED and SEM. The resistivities of CdTe films parallel to the substrate were measured using a Keithley 8002A high-resistance test fixture.

3. Results and discussions

In order to quantify and improve the fundamental understanding of post-deposition process-induced effects on vacuum-deposited CdS/CdTe heterojunction devices, the samples were categorized as:

(A) Au–(etched)CdTe/CdS–TO (as-grown);
(B) Au–(etched+annealed)CdTe/CdS–TO);
(C) Au–(etched+annealed+$CdCl_2$-dipped)CdTe/CdS–TO).

The formation of a low-resistance ohmic contact to p-CdTe is difficult because of its large work function [18] and also due to the presence of a highly resistive surface layer. In the present study, gold has been used as the contact material to the chemically etched CdTe surface with dichromate solution and the contacts were found to be quite stable after heating them at 200 °C for 5 min in a nitrogen atmosphere.

It was found that the high resistivity of as-deposited CdTe films ($\geq10^{10}$ Ω cm) decreases systematically to a few 10^7 Ω cm when the annealing temperature and time increases in the specified range (section 2.1). Further increase in the annealing time and temperature led to the creation of pinholes as revealed from SEM studies, and the resulting short circuit paths made the measurement of resistivity difficult. Even though the lowest resistivities were obtained when the $CdCl_2$ dip was followed by air annealing at 400 °C for 10 min, the best device parameters are attained for the heterostructures annealed at 300 °C for 5 min after being dipped into $CdCl_2$ and then chemically etched with dichromate solution prior to Au contact evaporation.

RHEED, SEM and XRD studies confirmed that all the CdTe films are polycrystalline in nature and exhibit cubic zinc blende type structure. The spectrum of as-deposited films indicates strong preferential ordering of film crystallites along the [111] axis. Although the intensity of the {220} peak is high for the air annealed films, after the $CdCl_2$ dipping, the {111} planes were always found to be preferentially oriented parallel to the glass substrate. Estimated average grain size values, obtained from x-ray spectra were observed to increase from 75–85 nm for the as-grown and air annealed layers to about 100 nm for $CdCl_2$ processed films.

The details of the studies on the ohmic contact formation and the effects of the post-deposition processing on the electrical and structural properties of the CdTe have been discussed elsewhere [19]. Here we report only the results of the electrical characterization of the devices with an as-grown CdTe layer and after being annealed in air at 300 °C for 5 min with and without $CdCl_2$.

XRD and RHEED analysis showed that CdS films were polycrystalline, hexagonal wurtzite in structure and deposited with a preferred orientation with the {0002} planes parallel to the substrate. Film morphology studies with SEM analysis indicated that the average estimated grain size was about 45 nm. The resistivity values of the CdS layers were found to be in the range of 0.3–7.0 Ω cm.

3.1. Room temperature dark and illuminated I–V characteristics

The forward and reverse I–V plots of representative samples from groups A, B and C at room temperature are illustrated in figure 1. The forward current–voltage characteristics are expressed by the standard diode equation

$$I = I_0 \exp(qV/nkT) \qquad (1)$$

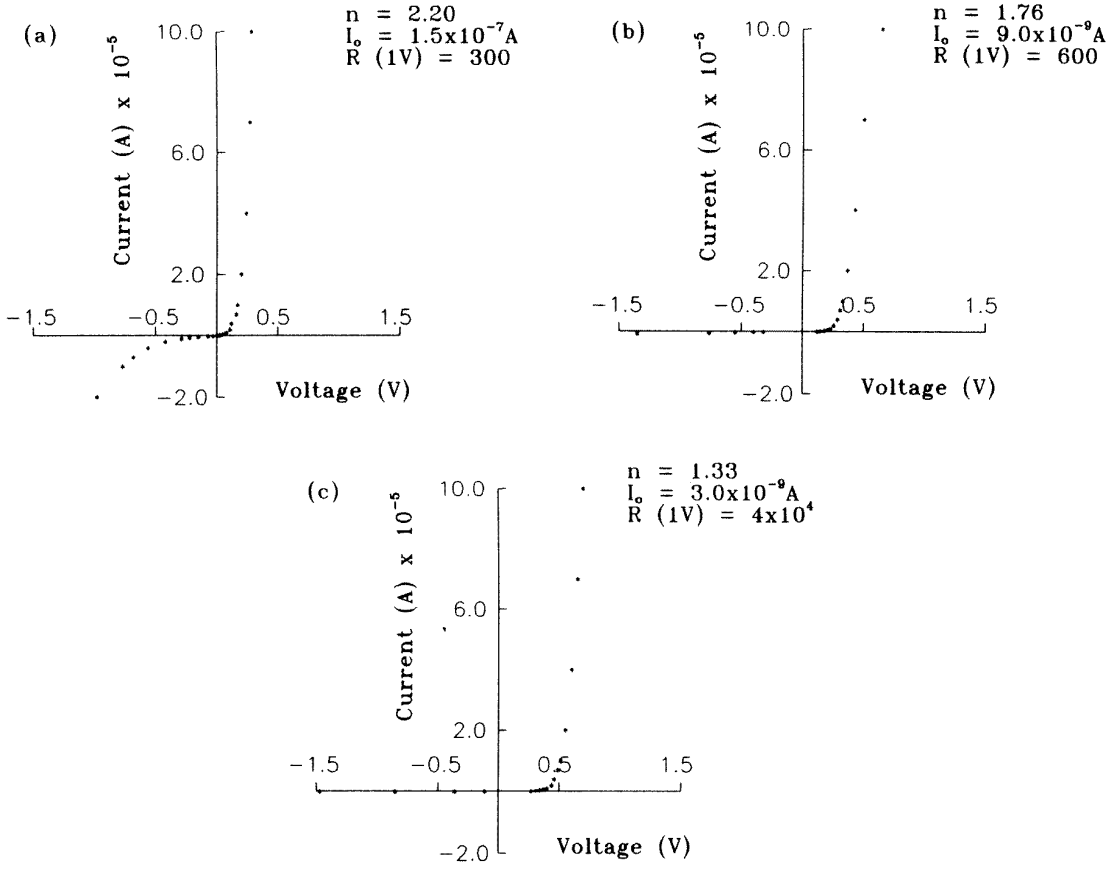

Figure 1. The room-temperature dark I–V characteristics of typical devices from groups (*a*) A, (*b*) B and (*c*) C.

where n is the diode ideality factor, I_0 is the reverse saturation current and k is the Boltzmann constant. The enhanced diode behaviour was consistently observed after annealing in air and $CdCl_2$ processing through the decrease in n, I_0 values and increase in the rectification factor R as observed in figure 1.

The illuminated I–V characteristics and the related photovoltaic parameters of the typical devices from groups A, B and C are given in figure 2. The performance characteristics of group A devices were very poor, which is probably due to the high resistivity of the CdTe layer. Even though the optimum annealing temperature and time (300 °C for 5 min) attained seems low to observe the enhancement of the p-type nature and the resistivity decrease when compared with the results of investigations of different groups [4, 20], an improvement in the photovoltaic parameters was observed under this annealing condition for our samples. The further increase in the annealing temperature and time decreased the photovoltaic efficiency, i.e. the short circuit current (I_{sc}), open circuit voltage (V_{oc}) and the fill factor (FF). For the efficiency calculations, contact optimization studies were not carried out and heterostructures have no antireflection coatings. Even though the highest efficiency attained in this work (6%) is low when compared with the results of other investigations on vacuum-deposited CdS/CdTe solar cells [13, 14], the main objective of this study is to explore the influence of the post-deposition treatments on the electrical characteristics of the vacuum-deposited CdS/CdTe heterostructures, which has not been done previously to our knowledge.

A substantial increase in V_{oc}, I_{sc}, FF was obtained when dipping the CdTe surface into $CdCl_2$ methanol solution was followed by annealing at 300 °C for 5 min in air. Obviously, introduction of $CdCl_2$ dipping into the processing step affects the CdS/CdTe interface, giving a remarkable increase in the device efficiency as discussed in section 3.2. The similar correlation between low n and I_0 values with higher solar cell efficiencies have been reported on CdTe/CdS solar cells deposited by the close space sublimation (CSS) technique [21]. $CdCl_2$ processing is known to induce recrystallization within the CdTe film leading to an increase in the average grain size, a decrease in intergrain pore size [7] and intermixing of CdS and CdTe forming a $CdTe_xS$ layer at the interface [14] which improves the electrical characteristics of the CdS/CdTe junction.

3.2. Temperature-dependent dark I–V characteristics

The typical forward log I–V characteristics of the devices from groups A, B and C at various temperatures in the

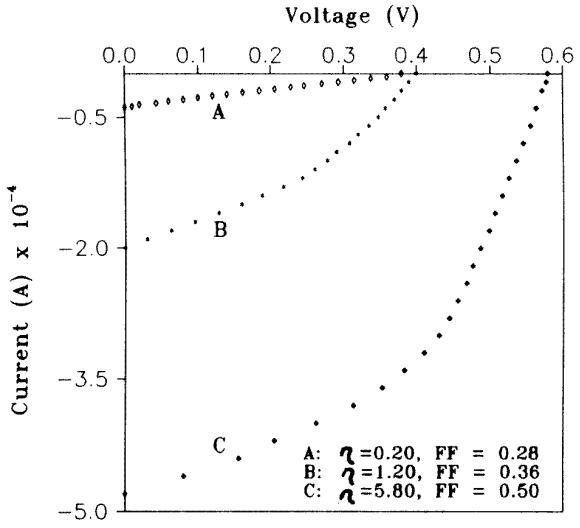

Figure 2. The illuminated I–V characteristics of the typical devices from groups A, B and C.

range of 90–400 K are given in figures 3(*a*), (*b*) and (*c*) respectively. The ideality factor n, the slope of the log I–V plot, α, and the reverse saturation current I_0 values evaluated at different temperatures from the I–V plots are collected in table 1. In order to identify the dominant current transport mechanisms through the junction, $\log I_0$ was plotted as a function of T^{-1} for the same samples and is illustrated in figure 4. The variations are found to be linear above 280 K, while they are far from being linear below that temperature, indicating the presence of two different transport mechanisms in these two different temperature ranges. Furthermore, the ideality factor n is almost constant above 280 K while the slope of the log I–V plot, α, is temperature insensitive below 280 K. All of these results are indicative of a thermally activated phenomenon above 280 K for which I_0 is expressed as

$$I_0 = I_{00} \exp(-\Delta E/kT) \tag{2}$$

where ΔE is the thermal activation energy of the process. From the slopes of $\log I_0$ versus T^{-1} plots for temperatures almost above 280 K, the activation energies were calculated to be about 0.40, 0.57 and 0.87 eV for samples A, B and C respectively. Junction recombination through the interface plane is known to be of particular importance in CdS/CdTe heterojunctions because of the large lattice mismatch (9.7%) [22]. For interface recombination-dominated current transport the value of n should be approximately unity because the carrier density in CdS is much larger than that of CdTe, and the product ΔEn should be around $V_{bi} = 1.18$ eV which is the built-in voltage of the junction [23]. If depletion region recombination dominates, the homogeneous distribution of recombination centres within the CdTe depletion region provides n values varying in between 1 to well above to 2 [24] and the slope of the log $(I_0T^{-2.5})$ versus T^{-1} plot must yield an activation energy approximately equal to half of the band gap of CdTe [8, 25].

For temperatures above 280 K, nearly constant $n \approx$ 2.08 values of group A samples result in a ΔEn product of 0.83 eV which is smaller than the expected value of V_{bi}. Although these results seem to eliminate the possibility of interface recombination, the low value of ΔE, relatively high I_0 values and the low rectification as observed from room-temperature plots indicate the presence of a high density of interface states and non-ideal junction formation. The validity of the depletion region mechanism seems doubtful since the slope of the log $(I_0T^{-2.5})$ versus T^{-1} plot gave an activation energy of around $\Delta E \approx 0.34$ eV which lies far from the expected value $(E_{gap}/2)$. Applying the same arguments and analysis to samples of group B, suggests that the thermally activated current transport mechanism is valid above 280 K with an almost constant n value of 1.97 and activation energy of $\Delta E \approx 0.57$ eV. The corresponding built-in voltage calculated from ΔEn is found to be 1.12 eV, which is close to the expected value. The validity of the depletion region recombination mechanism was also checked through the similar analysis given above. The activation energy is again quite low ($\Delta E \approx 0.54$ eV) compared with half of the CdTe bandgap, suggesting that depletion region recombination is not the dominant route.

With the above results, it is quite difficult to identify a single current transport mechanism across the junction for samples A and B, but interface state recombination seems most likely because of the high concentration of interface states located at or near the junction, as shown later from the C–V studies.

The analysis of I–V characteristics for group C devices (figure 3(*c*)) above 280 K gives the product of the average diode factor, $n \approx 1.33$ and the activation energy $\Delta E \approx 0.87$ eV as about 1.16 eV which is in close agreement with the expected value of V_{bi}. Hence, it is likely that the recombination process may be governed by the interface. Furthermore, the activation energy $\Delta E \approx 0.77$ eV calculated from the slope of the log $(I_0T^{-2.5})$ versus T^{-1} plot (figure 5) was almost equal to half of the CdTe bandgap of 1.51 eV obtained from optical transmission spectroscopy studies. Although both types (interface and depletion region) of recombination mechanism seem to be valid, the lowest I_0 values, best diode performances and the lowest diode ideality factors were obtained for this group, suggesting an improvement of the junction interface through a decrease in the interface state density, indicating that the depletion region recombination mechanism dominates. The effects of $CdCl_2$ dipping and air annealing on the current transport mechanism of molecular beam epitaxially grown CdTe/CdS heterojunctions have been investigated by Ringel *et al* [8]. It was reported that the $CdCl_2$ treatment changes the dominant current transport mechanism from interface recombination/tunnelling to depletion region recombination, suggesting a decrease in the density and the dominance of interface states following to $CdCl_2$ treatment. They have detected a hole trap within the CdTe depletion region of the $CdCl_2$ treated devices at 0.64 eV, which was addressed as the probable source of dominant recombination in these devices. In the relevant study the annealing temperature and time have been given as 400 °C and 35 min respectively. For our samples we have

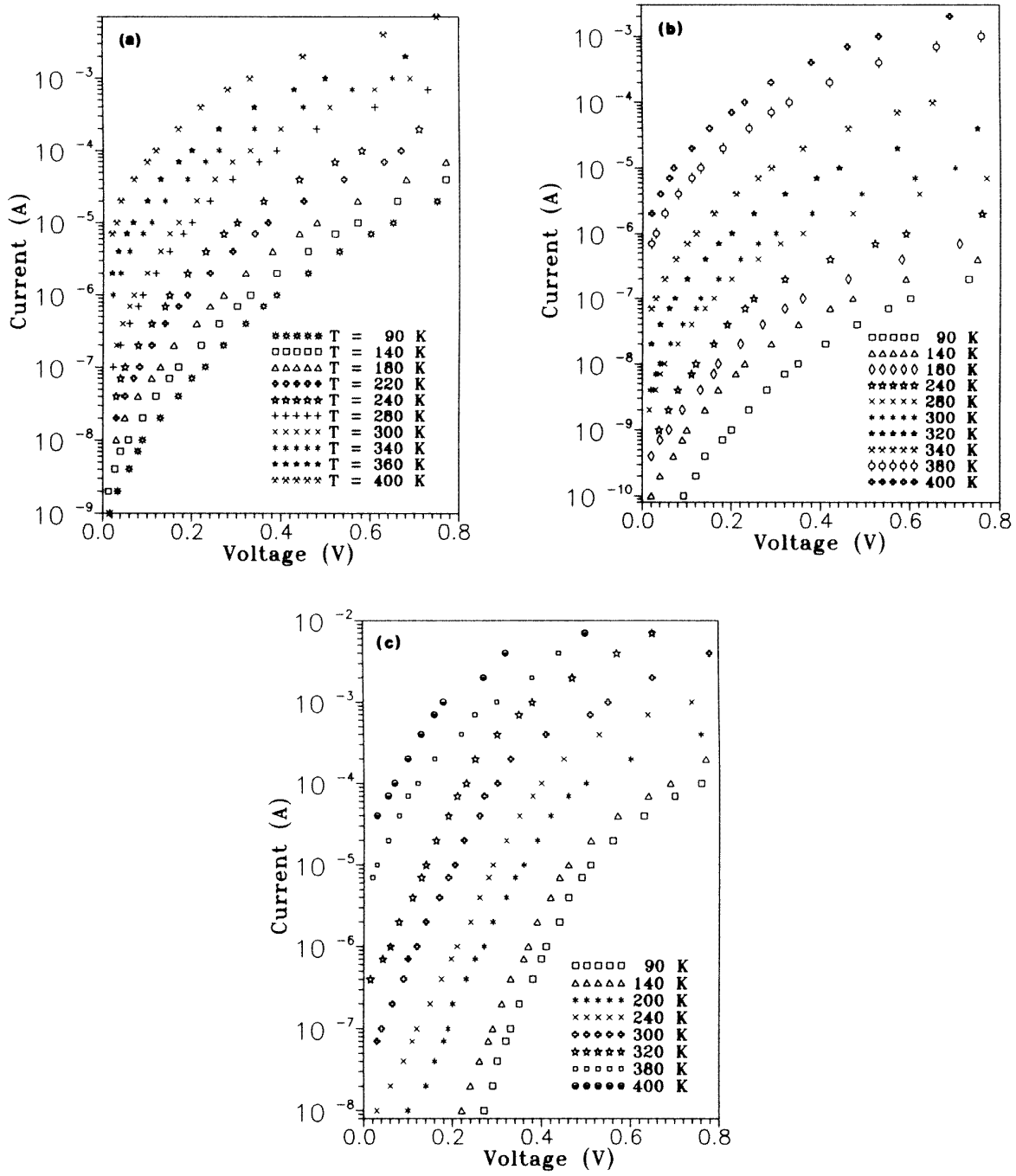

Figure 3. The dark forward current versus voltage characteristics of a typical device from group (*a*) A, (*b*) B and (*c*) C.

not only investigated the effects of $CdCl_2$ treatment, but also the effect of annealing on the electrical properties. Annealing of the samples at 300 °C for 5 min improves the diode behaviour and photovoltaic performances of the samples by an increase in the heterojunction barrier height from 0.40 eV to 0.57 eV and a decrease in the reverse saturation current from 3.4×10^{-7} to 1.3×10^{-8} A. $CdCl_2$ treatment further increases the heterojunction barrier height to 0.87 eV and decreases I_0 to 3×10^{-9} A, leading to a remarkable increase in the photovoltaic efficiency.

Below 280 K the slopes of the log I–V characteristics become temperature independent with almost constant α values of about 14.4, 16.8 and 27.0 for samples of group A, B and C respectively. This behaviour indicates that the tunnelling dominates the current transport which is expressed as [24]

$$I = I_{00}(\alpha V). \tag{3}$$

The reverse saturation current depends on the temperature through the empirical relation

$$I_0 = I_{00} \exp(\beta T) \tag{4}$$

Table 1. The I_0, n and α values for the samples of figure 2.

	I_0 (A)			n			α (V^{-1})		
T (K)	A	B	C	A	B	C	A	B	C
90	3.6×10^{-9}	4.5×10^{-11}	1.2×10^{-11}	8.70	8.24	4.77	14.8	15.6	27.0
120	5.8×10^{-9}	6.5×10^{-11}	2.8×10^{-11}	6.70	5.75	3.58	14.4	16.8	27.0
140	7.5×10^{-9}	2.3×10^{-10}	6.0×10^{-11}	5.80	5.15	3.06	14.2	16.2	27.0
180	2.0×10^{-8}	3.2×10^{-10}	1.9×10^{-10}	4.50	3.81	3.38	14.3	16.9	27.0
200	3.6×10^{-8}	4.8×10^{-10}	3.0×10^{-10}	4.14	3.35	2.23	14.0	17.3	26.0
220	6.0×10^{-8}	—	4.0×10^{-10}	3.68	—	1.95	14.3	—	27.0
240	9.5×10^{-8}	1.2×10^{-9}	5.0×10^{-10}	3.06	2.73	1.79	15.8	17.7	27.0
280	1.6×10^{-7}	3.8×10^{-9}	7.0×10^{-10}	2.16	1.97	1.35	19.2	20.9	30.6
300	3.4×10^{-7}	1.3×10^{-8}	3.0×10^{-9}	2.10	1.93	1.33	18.4	20.0	28.7
320	9.8×10^{-7}	3.2×10^{-8}	6.0×10^{-8}	2.10	1.97	1.33	17.2	18.4	27.0
340	1.8×10^{-6}	1.3×10^{-7}	6.0×10^{-7}	2.07	1.92	1.33	16.4	17.6	25.5
360	4.8×10^{-6}	—	—	2.03	—	—	15.8	—	—
380	—	1.4×10^{-6}	7.0×10^{-6}	—	1.99	1.24	—	15.3	24.2
400	1.8×10^{-5}	4.5×10^{-6}	3.5×10^{-5}	2.02	2.06	1.27	14.3	13.9	23.6

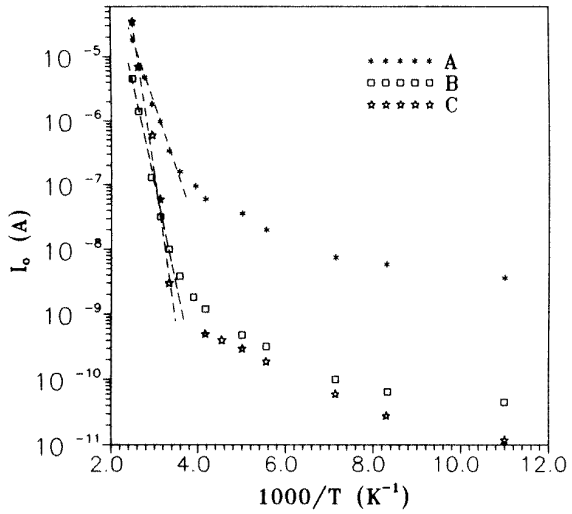

Figure 4. The dark current pre-exponential term versus T^{-1}.

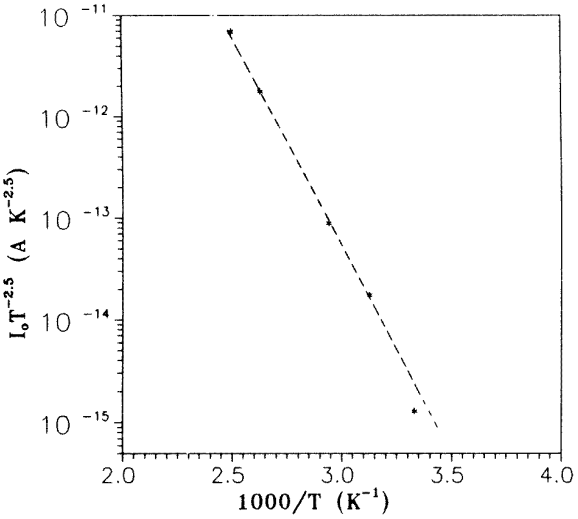

Figure 5. Plot of log ($I_0 T^{-2.5}$) versus T^{-1} in the temperature range between 300 to 400 K for group C devices.

where the empirical temperature coefficient β is found to be about 0.022 K^{-1} independent of the sample group considered. These results suggest that at low temperatures the transport is dominated by a tunnelling-type current transport. However, the acceptor concentration in the highly resistive CdTe layer is too low to allow direct quantum mechanical tunnelling through the energy barrier at the junction. Thus, a multistep tunnelling model such as that of Riben and Feucht [26] was found to give a satisfactory description of the temperature-dependent nature of the diode parameter n in this temperature range.

3.3. Capacitance–voltage characteristics

The capacitance of group A samples was almost independent of the applied reverse bias in the frequency and temperature ranges studied, indicating that the whole thickness of the highly resistive CdTe layer was depleted. At 1 MHz and room temperature, assuming that the capacitance at zero bias is the geometrical capacitance of the device, the depletion layer width w was calculated to be around 1.8 μm which was almost the whole thickness of the CdTe layer. Although the capacitance values were almost independent of the applied reverse bias, at a constant voltage, the room-temperature and high-frequency capacitances were strongly dependent on the measurement frequency and temperature indicating the presence of a considerable density of trap levels and interface states.

The capacitances of the group B and C samples were found to decrease with the applied reverse bias and this dependence decreased with increasing frequency and decreasing temperature. The typical room-temperature, high-frequency (1 MHz) capacitance–voltage variation for samples C is given in figure 6. As observed from the figure, C^{-2}–V variation is not linear in the voltage range studied, indicating the presence of the considerable number of deep

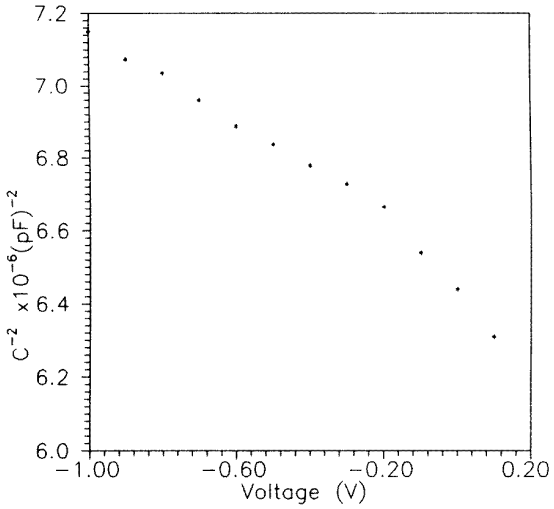

Figure 6. The C^{-2}–V characteristics of a typical group C device at 1 MHz.

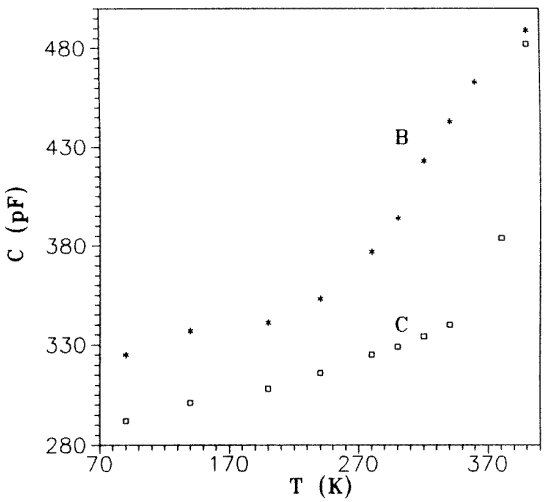

Figure 7. The C–T characteristics measured at 1 MHz.

levels. The high-frequency C–T variations of group B and C samples are shown in figure 7. The strong C–T variations just above room temperature can be ascribed to the effects of a high density of deep trap levels. Figure 8 shows the frequency dispersion curves of the same samples at room temperature. The frequency dispersion of capacitance of sample C is relatively low compared with that of air annealed group B samples and the capacitance saturates at $\sim 2 \times 10^3$ Hz which indicates a considerable decrease in the interface state density after $CdCl_2$ processing.

The model proposed by Schibli and Milnes [27] for n^+p junctions in the presence of a single dominant deep trap level, to identify the trap parameters, has been applied previously on Schottky barrier devices formed on both n- and p-type CdTe crystals [28] and on highly resistive n-type CdTe films obtained by electrodeposition [29]. The model considers theoretically the influence of deep levels on the capacitance of junctions.

When a low-frequency small-signal voltage is applied to the Schottky barrier formed on a highly resistive material, the contribution to the charge from the deep level becomes substantial. This charge increment q_{dc} is near the edge of the depletion region. At high frequencies, since the deep levels cannot follow the signal frequency, the charge increment q_f moves into the bulk and the measured capacitance decreases with increasing frequency. In the expression $C^{-1} = C_{dc}^{-1} + C_f^{-1}$, C is the overall capacitance expressed by the series combination of frequency-independent (bias-dependent) capacitance, C_{dc}, and frequency-dependent (bias-independent) capacitance, C_f. At low frequencies the capacitance saturates at value C_{dc}. The frequency-dependent capacitance, C_f, is given by [29]

$$C_f^2 = \frac{2\varepsilon q^2}{kT} N_t \frac{\omega_1}{\omega} \tag{5}$$

in which

$$\omega_1 = c_p N_v \exp\left(-\frac{q E_t}{kT}\right) \tag{6}$$

is the product of the hole capture probability, c_p, by the free hole density. In the above expressions N_t is the trap density, E_t is trap depth and ω is the angular frequency. The other symbols have their usual meanings. If the capture cross section is relatively temperature independent, the C_f versus T^{-1} variation yields half of the activation energy of the deep impurity.

The results of C versus T and C versus f measurements have been used for the investigation of the deep trap levels present in the CdTe layer of our CdS/CdTe, n^+p, heterojunctions assuming the density of the deep traps exceeds the density of the shallow level impurities. Evaluation of the results in terms of the proposed model showed that the model was only applicable to group C samples.

As observed from C–f plots illustrated in figure 8, the capacitance of group C sample saturated at around 2×10^3 Hz. The value of C_{dc} measured at 600 Hz was about 500 pF and used for the calculation of C_f from the measured C–f variations. Figure 9 shows the frequency dependence of C_f. It appears that C_f depends on the frequency as $C_f \propto f^{-0.48}$ which is very close to the theoretical variation of $f^{-0.5}$ given by equation (5). The temperature dependence of C_f at high frequency is plotted in figure 10 as log C_f versus T^{-1}. For temperatures lower than 300 K, the C_f values decreased only slightly with temperature, whereas at higher temperatures C_f showed a strong temperature dependence which led to the calculation of the trap depth of about 0.40 eV from equations (5) and (6). This level has previously been observed in CdTe and was attributed to a singly ionized Cd vacancy [30]. According to the proposed model, the break-point frequency, ω_B, is the frequency where $C_f = C_{dc}$ and is given by

$$\omega_B = \frac{4V_j q}{kT} \omega_1 \tag{7}$$

where V_j is the total junction voltage. In our case V_j is the built-in potential with a value of 1.16 eV. The break-point frequency is taken as $\omega_b \simeq 2\pi(3 \times 10^5)$ for the calculation

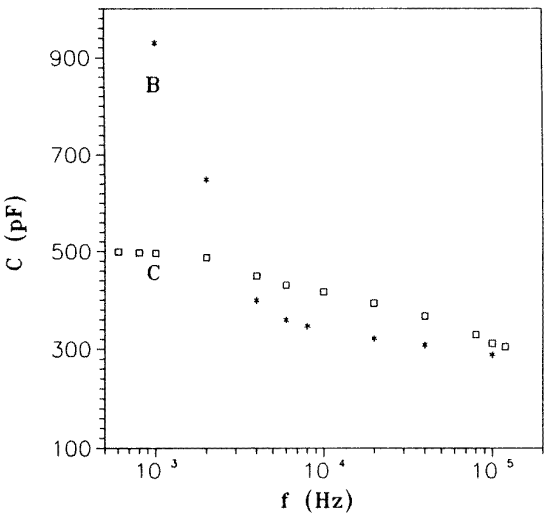

Figure 8. The zero bias C–f characteristics measured at room temperature.

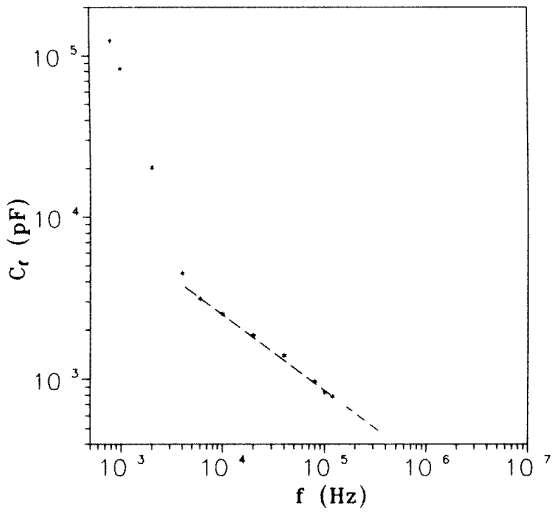

Figure 9. The C_f versus f characteristics of a typical group C device.

of w_1 using equation (7). The trap density, N_t, is estimated to be about 5.1×10^{15} cm^{-3} from the slope of the C_f^2 versus w^{-1} plot with the help of equation (5). The trap density was also calculated by using a depletion region width, w, of about 0.54 μm obtained from the C_{dc} value [29] and

$$w^2 = \frac{2\varepsilon V_{bi}}{qN_t}. \tag{8}$$

N_t is found to be about 4.5×10^{15} cm^{-3}.

4. Conclusion

The effects of different post deposition steps on the material and device properties of vacuum-deposited CdS/CdTe heterojunction devices have been analysed in detail. An improvement in the device efficiency was observed when

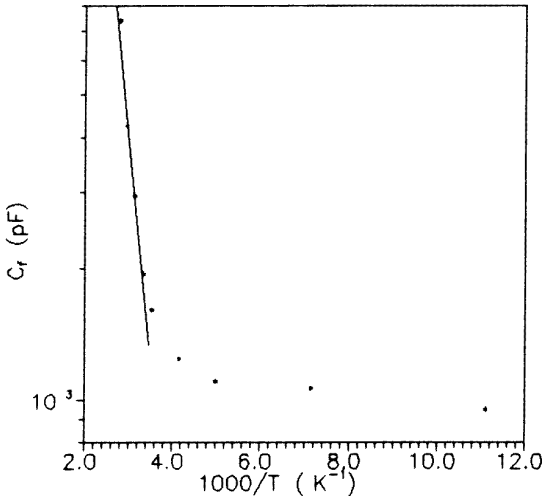

Figure 10. The C_f versus T^{-1} characteristics of a typical group C device.

samples were annealed in air with and without $CdCl_2$. The best solar cell parameters were obtained when the $CdCl_2$ treatment and annealing in air at 300 °C for 5 min was followed by chemical etching. At higher annealing temperatures, some short circuit paths were created, due probably to pinholes, which limited the cell efficiency.

The as-grown devices showed non-ideal junction formation owing to high reverse saturation current, series resistance and low rectification values. Due to the presence of a considerable density of interface states, the dark current transport was dominated by interface state recombination above ∼280 K for these samples. Even though interface quality was improved after annealing the samples in air, the dark current transport was still dominated by interface recombination. After the $CdCl_2$ treatment, the transport mechanism appeared to be dominated by depletion region recombination. This change was attributed to the decrease in the interface state density as observed from the frequency dispersion of the capacitance. The change in the transport mechanism resulted in an increase in the barrier height and reduced reverse saturation current values. Below about 280 K, the multistep tunnelling of carriers though the CdTe depletion region and subsequent recombination determined the current transport mechanism both before and after the post-deposition processing. The C–V measurements indicate the presence of a single dominant level at $E_v + 0.40$ eV in CdTe which is supposed to be due to a singly ionized Cd vacancy. Our studies reveal that annealing with $CdCl_2$ improves the interface and the film quality by decreasing the density of the interface states and improving the grain size and polycrystalline nature of the CdTe film.

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