

# The effect of the $\text{CdCl}_2$ treatment on CdTe/CdS thin film solar cells studied using deep level transient spectroscopy

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## Abstract

Thin film CdTe/CdS solar cells have been studied using deep level transient spectroscopy. The correlation-deep level transient spectroscopy (DLTS) technique was utilized as conventional analysis methods such as the boxcar-based approach were found to be inadequate under certain experimental conditions. The primary objective was to study the effect of a key processing step in the fabrication of thin film CdTe solar cells, namely the post-deposition heat treatment in the presence of  $\text{CdCl}_2$ . The substrate temperature as well as the ambient used during this process were varied around predetermined conditions for optimum solar cell performance, in order to identify performance-limiting defects, and in general improve our understanding of thin film CdTe solar cells. Solar cells without the  $\text{CdCl}_2$  heat treatment were also fabricated. A series of electron and hole traps were found in the various devices studied, with electron traps being present primarily in solar cells with limited performance.

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**Keywords:** CdTe/CdS solar cells; Post-deposition heat treatment; Deep level transient spectroscopy

## 1. Background

The need for cost effective and environmentally benign energy sources is becoming increasingly important. Thin film CdTe-based photovoltaics offer a viable option to meet cost and performance requirements, and commercialization of CdTe PV modules is underway by various CdTe PV module manufacturers [1]. The use of a heat treatment (HT) in the presence of  $\text{CdCl}_2$  is known to be beneficial in improving the performance of CdTe solar cells for various reasons. Among the improvements observed as a result of the  $\text{CdCl}_2$  HT is an increase in grain size typically observed in films with submicron size grains. Larger grain films (on the order of 1  $\mu\text{m}$  or larger) do not undergo a grain enhancement, rather elimination of smaller grains present in such films has been observed [2]. In addition, the  $\text{CdCl}_2$  HT has been found to affect the CdTe/CdS junction by enhancing the interdiffusion between the semiconductors leading to the formation of a  $\text{CdS}_{1-x}\text{Te}_x$  interfacial layer which is believed to improve current transport, as well as affecting the electronic structure of CdTe [3]. The presence of oxygen during the  $\text{CdCl}_2$  HT has been found

to be critical, as the amount of  $\text{O}_2$  appears to influence the degree of CdS consumption, i.e. the extent of CdS and CdTe interdiffusion [4].

Deep level transient spectroscopy (DLTS) is a powerful tool for the identification of deep levels in Schottky barriers and p–n junctions, by analyzing the temperature dependence of capacitance-transients caused by carrier emission processes from defect levels within the energy gap of a semiconductor. Its use has primarily benefited single crystalline devices and studies of thin film structures and, in particular, CdTe solar cells has been limited for various reasons. Thin film CdTe/CdS heterojunctions are significantly different than the ideal DLTS structure, the Schottky barrier, complicating their analysis with this technique, which is extremely sensitive to any capacitance change in the device under test. Discharge processes originating from parasitic capacitances in addition to the transient process corresponding to the thermal emission from traps can lead to signal distortion and erroneous results. Such parasitic capacitance sources in CdTe/CdS solar cells can originate from the back contact region and the device interface. Of the same concern is impurity migration along grain boundaries as well as native defect diffusion inside crystallites induced by the thermal and/or electrical perturbations during the DLTS measurement. Reversible changes as well as

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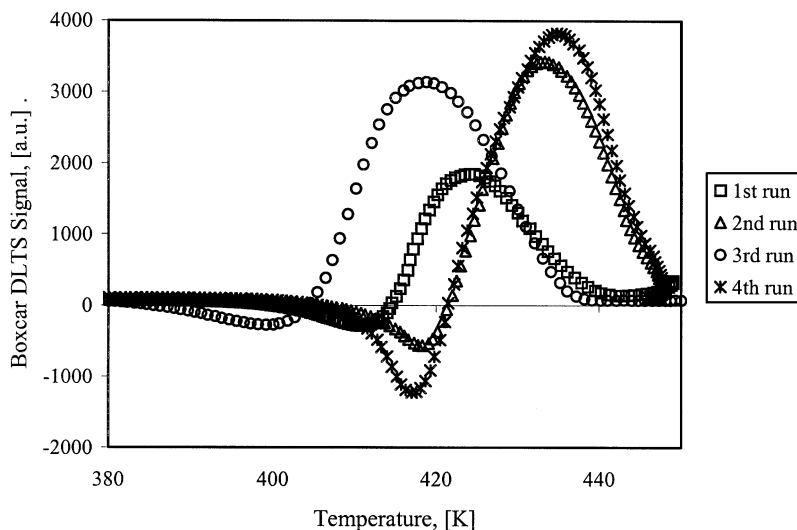


Fig. 1. Several boxcar DLTS spectra obtained under identical experimental conditions.

degradation in these devices have been previously observed [6,7].

## 2. Results and discussion

### 2.1. Device fabrication

Thin film CdTe/CdS solar cells were fabricated using procedures described previously [3,5]. Briefly, fluorine doped  $\text{SnO}_2$  (typically  $10 \Omega/\square$ ) was deposited by MOCVD on borosilicate glass substrates. The CdS films were deposited to a thickness of approximately 1000 Å by the chemical bath deposition technique, and CdTe was prepared using the close-spaced sublimation process. The  $\text{CdCl}_2$  HT was carried out in a tube furnace in inert (He) or  $\text{O}_2$ -containing ambient. The devices were coated with approximately 1  $\mu\text{m}$  of  $\text{CdCl}_2$  by evaporation, and subsequently annealed at temperatures ranging from 360 to 420 °C. After the  $\text{CdCl}_2$  HT the devices were briefly etched in a bromine/methanol solution before being masked and contacted with graphite paste doped with HgTe:Cu. For this study 12–16 solar cells, each with approximate area of 0.1  $\text{cm}^2$ , were fabricated on each substrate.

### 2.2. DLTS measurements

Initially the DLTS measurements were carried out using a Bio-Rad DL 4600 system, which utilizes the boxcar technique. However, the lack of consistency in the measured spectra led to significant changes in the measurement procedure. Fig. 1 shows a set of boxcar DLTS spectra obtained under identical conditions for electrical bias, filling pulse, rate window and temperature sweeps. The variations in these spectra suggest that the behavior of the particular device under test is changing significantly during the measurement process, and determination of trap specific information such as energy position, concentration and capture cross-section is not possible. Changes in the solar cell characteristics of a CdTe solar cell during a boxcar DLTS analysis in the temperature range of 100–450 K are summarized in Table 1, indicating decreases in both the open-circuit voltage ( $V_{oc}$ ) and fill factor (ff), as well as partial recovery after storage in the dark for 24 h. The observed changes in device performance were attributed to the combined effect of the temperature sweeps and the reverse bias applied to the CdTe solar cells during the DLTS measurements [8]. Limiting the DLTS temperature to 350 K resulted in essentially no changes in

Table 1

Changes in solar cell characteristics of a CdTe solar cell, for a boxcar DLTS run performed in the temperature range from 100 to 450 K

	Initial	After 1st run	After 2nd run	After 24-h recovery
$V_{oc}$ (mV)	841	813	805	813
ff (%)	68.4	64.1	63.8	66.5
$J_{sc}$ ( $\text{mA}/\text{cm}^2$ )	18.0	19.0	19.0	19.0

Table 2

Changes in solar cell characteristics of a CdTe solar cell, for a boxcar DLTS run performed in the temperature range from 100 to 350 K

	Initial	After 1st run	After 2nd run	After 24-h recovery
$V_{oc}$ (mV)	845	838	833	833
ff (%)	67.4	66.7	67.2	67.2
$J_{sc}$ ( $\text{mA}/\text{cm}^2$ )	21.0	21.0	21.0	21.0

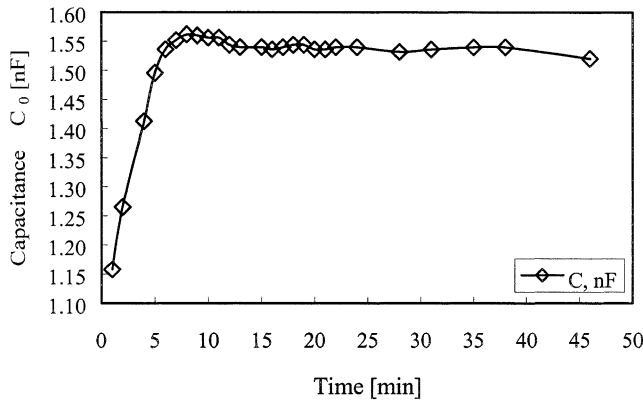


Fig. 2. The zero-bias capacitance of a CdTe solar cell after exposure to light.

device performance as the results listed in Table 2 indicate.

Capacitance–voltage measurements are also required during the DLTS analysis in order to calculate the defect concentration. During routine  $C$ – $V$  measurements it was observed that sample capacitance was very sensitive to light exposure. As the accuracy of the DLTS measurements depends on this device characteristic, the capacitance of several devices was monitored immediately after exposure to light. Fig. 2 describes the behavior of the capacitance at zero bias of one such device suggesting that sample storage in the dark prior to the start of the DLTS analysis for a period of 10–20 min is required for the sample capacitance to reach equilibrium. The background carrier concentration, which is needed for the calculation of trap concentration, also exhibited temperature dependence as indicated from  $C$ – $V$  measurements carried at temperatures in the range of 100–320 K [8].

Taking all the above issues into consideration a measurement system was developed for the DLTS analysis. The instrumentation has been described elsewhere [8]. Briefly, a Bio-Rad DL 4600 DLTS system was combined with an HP 4145B Semiconductor Parameter Analyzer, an HP 4194A Impedance Analyzer, and a Correlation DLTS system based on a National Instruments 5911 100 MHz Digitizer developed in-house for this study.

In order to further improve the resolution of the DLTS measurements and reduce the number of temperature cycles the cells are exposed to (and therefore minimize any changes in their characteristics), other approaches for the analysis of the capacitance transient data in addition to the boxcar method were considered. Taking into account that differentiation is a noise-producing process, and that a signal transient is not noise-free, any techniques involving data differentiation such as Isothermal DLTS were not considered [9]. Transform techniques provide the basis for true spectroscopy of

continuous distributions of exponential transients. The most popular rate window technique, better known as boxcar method, and the inverse Laplace transform belong to this category of transform techniques [10,11]. Based on signal processing theory, the best sensitivity is provided by a weighting function, which has the same form as the noise-free signal itself, and therefore for DLTS the weighting function should be a decaying exponential since the carrier emission process from most deep levels is also a decaying exponential [12]. Comprehensive analysis of previously published weighting functions indicated that the exponential correlator has a superior signal-to-noise ratio [12–14]. The correlation DLTS output vs. time spectra were calculated using

$$S(T, t_d) = t_c^{-1} \int_{t_d}^{t_d + t_c} f(t, \tau_s) W(t - t_d) dt \quad (1)$$

where  $f$  is the capacitance transient signal,  $\tau_s$  is the capacitance transient time constant,  $t_c$  is the duration of correlation,  $t_d$  is the delay time between the end of the filling pulse and the beginning of the correlation, and  $S$  is the output DLTS signal, with the ‘shifted-exponential’ reference weighting function given in the form of

$$W(t) = \exp(-t/t_0) - [1 - \exp(-t_c/t_0)] \quad (2)$$

where  $t_0$  is a reference time constant.

Additional details on the correlator and the overall DLTS analysis procedure can be found elsewhere [15]. Briefly, the measurement procedure consisted of the following major steps: (a) measure light and dark  $J$ – $V$  characteristics; (b) place device in the cryo-chamber and monitor its capacitance until it reaches equilibrium; (c) cool sample down to 100 K; (d) raise sample temperature in 10 °C intervals and perform dark  $J$ – $V$ ,  $C$ – $V$ , and capture the capacitance transient signal at each temperature; (e) perform a boxcar DLTS measurement while cooling the sample down to 100 K; (f) allow sample to warm up to room temperature and re-evaluate its dark and light  $J$ – $V$  characteristics. An example of a correlator DLTS spectrum obtained from a CdTe/CdS device studied in this work is shown in Fig. 3.

### 2.3. DLTS results

A summary of all defect levels measured during this work is included in Table 3, along with the most likely chemical origin assigned based on literature data. In order to study the effect of the CdCl<sub>2</sub> HT a series of devices were heat treated at different temperatures ranging from 360 to 420 °C in the presence of O<sub>2</sub>. The performance data ( $V_{oc}$  and  $ff$ ) and a summary of the DLTS measurements are listed in Table 4. Optimum

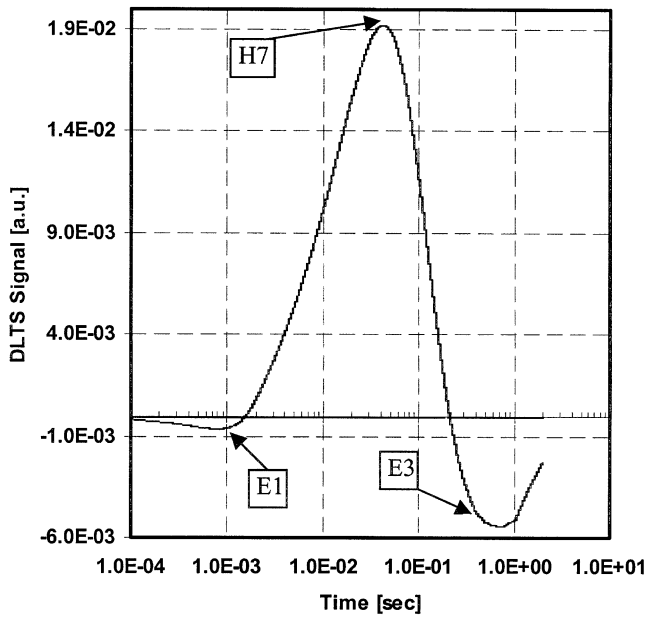


Fig. 3. Correlator generated DLTS spectrum for a CdTe sample at 300 K. Electron traps have negative amplitude values.

solar cell performance is obtained within the temperature range of 380–400 °C, and solar cell characteristics rapidly degrade for higher and lower temperatures. The primary difference in the defect structure among these devices is the presence of electron trap E1 and hole trap H7 in samples annealed under non-optimum conditions. The impact of these traps on device performance is not exactly clear at this time as in all cases their concentration was low (below  $1 \times 10^{14} \text{ cm}^{-3}$ ), and preliminary device modeling suggested that at these levels solar cell performance is not affected. However, the presence of these defects only in cells with poor characteristics, and the fact that they are not present in optimized devices suggests that they probably contribute to reduced device performance, and that to-date modeling efforts have not fully captured their impact. These defect levels are believed to be due to Cd vacancies ( $V_{\text{Cd}}$ ) and complex

defects involving  $V_{\text{Cd}}$  and Cl. The electron trap E1 may also be related to the effect of a shear stress field of a dislocation [16].

A similar experiment was performed where the CdTe/CdS solar cells were CdCl<sub>2</sub> heat-treated in inert ambient (He). Both solar cell performance and the DLTS results were very similar to those listed in Table 4 (samples annealed in O<sub>2</sub>) [14]. This suggests that the presence of O<sub>2</sub> does not affect the electronic defects in CdTe solar cells, or that the concentration of any O<sub>2</sub> related complexes is too low to be detected with this technique. Although from these results it appears that O<sub>2</sub> is not necessary for optimum performance, it has been reported that the amount of O<sub>2</sub> during the CdCl<sub>2</sub> treatment is important in determining the CdS consumption (in other words the extent of interdiffusion between CdS and CdTe) and, therefore, can affect the junction properties [4]. However, devices utilized in this work were fabricated at high temperatures (the CSS CdTe deposition was carried at substrate temperatures in the 580–620 °C range), which facilitate the formation of the interdiffused layer, and, therefore, O<sub>2</sub> is not necessary to promote the formation of the CdS<sub>1-x</sub>Te<sub>x</sub> interfacial layer.

Another important feature of the DLTS results listed in Table 4 is the fact that H8, which is believed to be due to Cd vacancies, is present in all devices, suggesting that Cd vacancies play a key role in determining the defect structure of this material. For devices fabricated without the CdCl<sub>2</sub> treatment (with Cu-based back contacts), only the hole trap identified as H6 was found. When ‘Cu-free’ contacts were used H6 was not detected [16]. It is, therefore, believed that H6 is related to Cu, and the fact that it is present in nearly all devices in Table 4, suggests that Cu is also an important impurity in these devices. It is possible that the hole traps located in the range of  $E_{\text{v}} + (0.27\text{--}0.35 \text{ eV})$  are all related to Cu, and the fact that this element is very mobile in CdTe and could move significantly during the analysis procedure has led to uncertainties in the calculation of the energy position.

Table 3  
Defects identified in CdTe solar cells investigated in this work

Defect level	$E_{\text{A}}$ (eV)	Suggested chemical origin as compiled from literature data
H1	0.120	$(V_{\text{Cd}}^{2-} - \text{Cl}_{\text{Te}}^{+})^{-}$ [17]
H2	0.140	$(V_{\text{Cd}}^{2-} - \text{Cu}_{\text{Te}}^{+})^{-}$ , $(2\text{Cu}_{\text{Cd}} - V_{\text{Te}}^{+})^{-}$ or complexes involving $V_{\text{Cd}}^{2-}$ or $V_{\text{Te}}^{+}$ [18]
H3	0.200	—
H4	0.320	$\text{Te}_{\text{Cd}}^{-}$ -complex, after CdCl <sub>2</sub> HT: $\text{Te}_{\text{Cd}}^{-} \rightarrow V_{\text{Cd}}^{2-} + \text{Te}_{\text{i}}$ [19]
H5	0.330	$\text{Ag}_{\text{Cd}}^{-}$ [17]
H6	0.270–0.350	$\text{Cu}_{\text{Cd}}^{+}$ ; $(\text{Cu}_{\text{i}}^{+} - 2\text{Cu}_{\text{Cd}})^{-}$ [20]
H7	0.430	Isolated $V_{\text{Cd}}^{2-}$ [21]
H8	0.760	Complex of $V_{\text{Cd}}^{2-}$ and an impurity [18]
E1	0.140	$\text{DX}_{2}$ -state of $(V_{\text{Cd}}^{2-} - \text{Cl}_{\text{Te}}^{+})$ [22]
E2	0.640	Isolated $\text{Cd}_{\text{i}}^{2+}$ [23]
E3	0.790	$(V_{\text{Cd}}^{2-} - 2\text{Cl}_{\text{Te}}^{+})^{0}$ [18]
E4	1.100	Isolated $V_{\text{Te}}^{+}$ [21]

Table 4

Summary of the  $V_{oc}$ , ff and DLTS results for CdTe cells CdCl<sub>2</sub>-treated at temperatures in the range of 360–420 °C

$T_{ANNEAL}^0$ (°C)	$V_{oc}$ (mV)	ff	$E_A$ (eV)	Defect level	$\sigma$ (cm <sup>2</sup> )	$N_T \times 10^{12}$ (1/cm <sup>3</sup> )
360	818	0.645	0.138	E1	1.0E–18	3.5
			0.454	H7	2.4E–14	6.0
			0.727	H8	4.2E–13	8.3
370	831	0.681	0.147	E1	3.1E–19	6.1
			0.320	H4-6	5.5E–18	7.9
			0.725	H8	1.2E–13	–
380	839	0.688	0.365	H4-6	4.8E–19	7.2
			0.765	H8	2.1E–12	–
390	850	0.712	0.336	H4-6	6.1E–18	3.4
			0.723	H8	8.1E–12	–
400	818	0.6683	0.321	H4-6	2.8E–18	16.0
			0.707	H8	9.1E–13	180
410	808	0.651	0.365	H4-6	4.8E–19	0.96
			0.452	H7	3.5E–14	2.2
			0.765	H8	2.1E–12	–
420	751	0.54	0.140	E1	2.9E–19	16.0
			0.323	H4-6	3.5E–18	32.0
			0.452	H7	3.5E–14	20.0
			0.707	H8	9.1E–13	45.0

The capture cross-section  $\sigma$  and trap concentration  $N_T$  are included; missing  $N_T$  values are for cases where the sample capacitance exceeded the instrument's maximum range.

### 3. Conclusions/Summary

A procedure for the DLTS characterization of CdTe/CdS thin film solar cells has been developed based on the correlator technique, in order to address device specific issues and improve the signal to noise ratio of the measurement process. A series of electron and hole traps have been identified. The effect of the post-deposition CdCl<sub>2</sub> HT on these thin film devices has been studied, and certain defect levels, namely those identified as E1 and H7 were found in devices processed under non-optimum conditions and which, therefore, exhibited lower solar cell performance. It was also found that the use of O<sub>2</sub> during the CdCl<sub>2</sub> HT does not affect the defect structure in CdTe. Although further studies for a self-consistent model to be derived are necessary, the results obtained from this work suggest that the CdCl<sub>2</sub> HT significantly influences the formation of defects in CdTe, with cadmium vacancies and chlorine related defects appearing to play a key role. These results emphasize the need for further evaluation of defects in CdTe-based thin film solar cells in order to advance our understanding of these devices and develop

the appropriate models and processes for additional improvements of the technology.

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