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Processing options for CdTe thin film solar cells

Brian E. McCandless *, Kevin D. Dobson

Institute of Energy Conversion, University of Delaware, Newark, DE 19716, USA

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Abstract

Processing options for addressing critical issues associated with the fabrication of thin film CdTe solar cells are presented, including window and buffer layer processing, post-deposition treatment, and formation of stable low resistance contacts. The paper contains fundamental data, engineering relationships and device results. Chemical surface deposited CdS and $Cd_{1-x}Zn_xS$ films are employed as the n-type heteropartner window layers. Maintaining junction quality with ultra-thin window layers is facilitated by use of a high resistance oxide buffer layer, such as SnO_2, In_2O_3 or Ga_2O_3, between the heteropartner and the transparent conductive oxide. Thermal annealing of the CdTe/CdS heterostructure in the presence of $CdCl_2$ and O_2 shifts the chemical equilibrium on the surface of the absorber layer, which influences the bulk electrical properties. Aspects of back contacting CdTe/CdS devices, including etching, Cu application, contact annealing, back contact chemistry and secondary contacts, are discussed. Two commonly employed etches used to produce a Te-rich layer, nitric acid/phosphoric acid mixtures and Br_2/methanol are compared, including the nature and stability of the final treated CdTe surface. The diagnostic abilities of the surface sensitive VASE and GIXRD techniques are highlighted. Various methods of Cu delivery are discussed with consideration to; reaction with Te, processing simplicity, processing time and possible industrial scale-up. Some aspects of back contact stability are presented, including discussion of apparent robust back contacts, which contain a thick Te component.

Keywords: Cadmium telluride; Thin-film; Solar cells; Contact; Processing

1. Introduction

Thin-film solar cells based on CdTe continue to show promise for terrestrial photovoltaic power generation. The optoelectronic properties of CdTe provide an ideal match to the solar spectrum for high conversion efficiency thin film devices (Loferski, 1956). Thin-film polycrystalline CdTe/CdS solar cell efficiencies have exceeded 15%, which is 65% of their theoretical values, and module efficiencies greater than 10% have been demonstrated for widely differing CdTe deposition technologies (McCandless and Sites, 2003). CdTe offers flexibility in device design in that it forms isostructural and isoelectronic alloys with other group II–VI compounds such as HgTe and ZnTe, thereby allowing the absorber layer band gap to be narrowed or widened for tandem cell and optical detector applications (Capper, 1994). The chemical stability of CdTe and its deployment in thin film modules for electrical energy production provides a mechanism to safely contain the cadmium by-products that originate in copper ore refining (Fthenakis and Zweibel, 2003).

While laboratory-scale research groups seek the CdTe performance and stability limits, manufacturing groups must also contend with the challenge of scaling-up the laboratory fabrication processes and finding ways

* Corresponding author. Tel.: +1-302-831-6240; fax: +1-302-831-6226.
E-mail address: bem@udel.edu (B.E. McCandless).

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Nomenclature

J_{sc}	short circuit current density, mA/cm^2	p	pressure, mTorr
V_{oc}	open circuit voltage, mV	p_{sat}	saturation pressure, Torr
d_fCdS	final thickness, nm	T	temperature, °C or K
J_o	recombination current, mA/cm^2	E_g	optical band gap, eV
FF	fill factor, %	ΔG_{rxn}	heat of reaction, kJ/mol
Eff	conversion efficiency, %	R_{oc}	slope of power curve near open circuit, mS/cm^2
D_{AB}	mass diffusivity of gas A in gas B, cm^2/s	Ω	incident beam angle for GIXRD, degrees
α	thermal diffusivity, cm^2/s	λ	wavelength, nm
τ_m	characteristic time for mass diffusion, s		
t_T	characteristic time for thermal diffusion, s		

to close the gap between small-area cell performance and module performance. For laboratory-scale research, the key issues with respect to cell performance are increasing the open circuit voltage (V_{oc}) beyond 850 mV, achieving short circuit current (J_{sc}) approaching 30 mA/cm^2, reducing V_{oc} sensitivity to the window layer configuration, and forming low resistance contacts to CdTe. Performance and stability cannot be treated exclusively, because viable processing schemes that give excellent short-term performance are not necessarily those which yield stable behavior over longer time under continuous or cyclic operation. Adapting research-scale fabrication processes to the manufacturing scale requires a detailed understanding of the function of each processing step, its dependence on up-stream processing variations, its influence on down-stream processing needs, and controlling these steps over large area. As this understanding matures, simple and robust processing alternatives can be developed that retain the salient features required for high performance and good stability.

This paper presents processing options for superstrate thin-film CdTe solar cells, with emphasis on critical processing steps: window/buffer layer fabrication; absorber layer processing and junction formation; and back contact formation. Specific techniques for depositing CdTe are not addressed, as these are covered extensively in published literature (McCandless and Sites, 2003). Results will be shown for laboratory-scale devices with CdTe films by physical vapor deposition (PVD) and vapor transport deposition (VT). Also, the discussion will be restricted to superstrate cells since these have demonstrated the highest performance and are presently under development by manufacturing groups, including First Solar and Canrom (both USA), and Antec (Germany). Cells made in the inverted configuration, with CdTe deposited onto a suitable substrate, have been fabricated by several groups and suffer from the same generic problems; low V_{oc} and FF, with poor electrical contact between the CdTe and the substrate (Birkmire et al., 1985).

2. Window layer

For superstrate thin film CdTe solar cells, the window layer is broadly defined as all the layers through which light passes before being absorbed in the CdTe, and the glass superstrate. The best junction performance, indicated by $V_{oc} \sim 850$ mV and FF $\sim 75\%$, is obtained using CdS as the heterojunction partner, with a band gap of 2.4 eV. It has been widely shown that the CdS layer in a superstrate CdTe/CdS cell contributes negligible photocurrent and therefore constitutes a photocurrent loss for the wavelength range from 300 to $\sim$520 nm (McCandless and Hegedus, 1991) despite the high absorption coefficient in CdS over this wavelength range, $>10^5$ cm^{-1}, the poor photoresponse is attributed in part to low hole lifetime and high recombination. Thus, parasitic optical absorption in the CdS layer is the predominant photocurrent loss, making it necessary to minimize the CdS film thickness in the device. Maintaining junction quality in superstrate structures with $d_{CdS} < 100$ nm depends on maintaining a uniform interface throughout processing to avoid formation of parallel junctions between CdTe and the transparent conductive oxide (TCO), which have a much higher recombination current, J_o, than CdTe/CdS. In practice, however, the occurrence of spatially non-uniform microscopic discontinuities in the CdS film increases with diminishing CdS film thickness, resulting in a decrease in V_{oc} with diminishing CdS thickness. This is shown in Fig. 1 for devices with PVD CdTe and $CdTe_{1-x}S_x$ absorber layers and CdS/ITO window layers (solid markers). Controlling the CdS thickness uniformity at the manufacturing scale requires control over the CdS deposition and CdS–CdTe interdiffusion during post-deposition processing. Deposition methods showing promise for controlling CdS film thickness <100 nm are chemical bath deposition (CBD) and chemical surface deposition (CSD), with the latter method giving very high chemical utilization of dissolved Cd species (McCandless and Shafarman, 2003). The CdTe–CdS

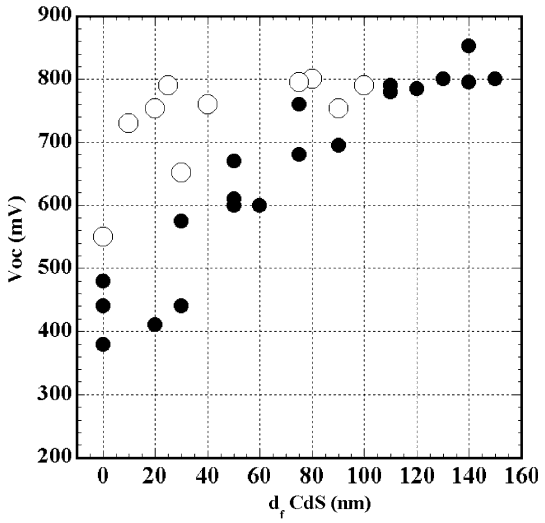

Fig. 1. V_{oc} versus final CdS film thickness for PVD CdTe/CdS and $CdTe_{1-x}S_x$/CdS cells without buffer layers (solid) and with buffer layers (open).

interdiffusion which occurs during the post-deposition $CdCl_2$ treatment of devices has been shown to primarily consist of CdS diffusion into CdTe; and the rate of CdS consumption depends greatly on the CdTe film grain size and the chemical ambient conditions (McCandless, 2001a,b). For CdTe/CdS couples treated in $CdCl_2$ vapor at 420 °C, the bulk diffusion coefficient was found to be $\sim 1\times10^{-8}$ cm^2/s and the grain boundary diffusion coefficient depended on the grain size, with typical values for PVD CdTe ~1 μm, resulting in grain boundary diffusion coefficient $\sim 1\times10^{-13}$ cm^2/s and a net CdS consumption rate of $<2\times10^{-10}$ gmol/cm^2 s, corresponding to an equivalent CdS thickness loss rate of <0.05 nm/s. For CdTe films with 4 μm diameter grains, deposited by either PVD or vapor transport deposition, typical CdS thickness loss rates less than 0.01 nm/s were measured. Such low rates can also be obtained in small-grain CdTe films, such as those obtained by electrodeposition (ED), by forming the native oxide $CdTeO_3$ in the CdTe film prior to the $CdCl_2$ treatment (McCandless et al., 2003).

Two options exist for maximizing photocurrent while retaining high junction quality: (1) employing a high resistance buffer layer between CdS and TCO to raise J_o in the CdTe/TCO junction and (2) using $Cd_{1-x}Zn_xS$ alloy films to widen the band gap and relax the thickness constraint. Table 1 lists AM 1.5 current–voltage (*JV*) device results for CdTe/CdS cells with CdTe deposited by PVD and high resistance oxide buffer layers between the TCO and CdS film. The buffer layers evaluated were SnO_2, In_2O_3 and Ga_2O_3. In all three cases, the buffer layers were fabricated by oxidation of thin films of Sn, In, or Ga deposited on TCO/glass. The cell results in Table 1 and the V_{oc} plot in Fig. 1 (open markers) demonstrate high J_{sc} and retention of junction quality for devices with CdS <100 nm. Incorporating a high resistance SnO_2 buffer layer on SnO_2/7059 has resulted in devices with conversion efficiencies >13% for evaporated CdTe.

Another approach to maximizing transparency in the window layer is replacing pure CdS with $Cd_{1-x}Zn_xS$, as reported in McCandless and Birkmire (2000a,b). Calculations suggest that addition of Zn to the interface can reduce valence band offsets (Wei et al., 2000) which may translate to higher V_{oc}. We fabricated devices with no buffer layer but with $Cd_{1-x}Zn_xS$ having low Zn content, $x \sim 0.05$, and obtained higher V_{oc} than for devices fabricated with non-alloyed CdS (Table 1).

3. Post-deposition treatments

Attaining high conversion efficiency from thin-film CdTe/CdS solar cells requires exposure of the CdTe/CdS

Table 1
AM1.5 *JV* results (28 °C) for PVD CdTe devices with 7059/ITO, 7059/ITO/buffer/CdS, 7059/SnO_2/buffer/CdS, and 7059/ITO/50 nm $Cd_{0.95}Zn_{0.05}S$ window layers

TCO	Buffer (nm/type)	d_f (CdS) (nm)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
ITO	None	0	440	25.0	47	5.0
ITO	None	50	590	23.9	47	6.6
ITO	None	110	790	20.3	70	11.3
ITO	20In_2O_3	30	652	23.9	52	8.1
ITO	50In_2O_3	<20	754	26.2	60	11.9
ITO	50In_2O_3	100	790	21.8	70	12.0
ITO	50Ga_2O_3	40	760	24.0	62	11.4
SnO_2	None	0	440	18.0	46	3.5
SnO_2	None	90	753	22.8	63	10.8
SnO_2	50SnO_2	<20	790	26.0	68	13.8
ITO	None	30$Cd_{0.95}Zn_{0.05}S$	750	23.2	62	10.8

All cells were processed with 580 °C, 5 min pre-anneal in argon and 420 °C, 15 min vapor $CdCl_2$ post-deposition treatments in dry air.

couple to chloride species during processing, which affects both chemical and electronic properties of the CdTe/CdS structure. Whether the chloride exposure occurs during film formation or during a post-deposition treatment depends on the process used to make the CdTe. The most commonly employed agent is the hygroscopic salt $CdCl_2$, which melts at 569 °C and boils at 963 °C. There have been a substantial number of studies of the effects of $CdCl_2$ treatment on CdTe/CdS devices (McCandless and Sites, 2003). In spray and screen-print processes, $CdCl_2$ is a component of the constituent materials. Annealing of these structures at high temperatures, 500–600 °C causes the $CdCl_2$ to act as a fluxing agent for recrystallization of the CdTe film. In processes using vapor-deposited films made by vapor transport deposition (VTD), physical vapor deposition (PVD), electrodeposition (ED), or close space sublimation (CSS), post-deposition treatment of the films with $CdCl_2$ at lower temperatures, from 350 to 450 °C, are found to promote intragrain recrystallization, grain coalescence and improve the electronic properties with respect to CdTe/CdS devices.

Until recently, the predominant method used to treat the films involved direct exposure of the CdTe surface to solid $CdCl_2$ applied via solution of $CdCl_2$ in methanol (wet $CdCl_2$) (McCandless and Birkmire, 1991) or by sublimation from a $CdCl_2$ source, either during heat treatment (McCandless et al., 1996) or prior to heating (Fischer et al., 1996) the CdTe/CdS structure. Alternative processes by treatment in Cl_2 or HCl vapor have also been examined, with the result that the CdTe surface is readily converted to $CdCl_2$ (Qu et al., 1996). The "wet" $CdCl_2$ surface treatment is effective for small-cell fabrication but has several disadvantages for large area manufacture, such as uniform delivery of the $CdCl_2$ and handling and safe disposal of the rinsate. To overcome these problems, vapor techniques were developed which can uniformly deliver the chloride species to the CdTe/CdS structure during the heat treatment without formation of post-treatment residues.

Two atmospheric pressure approaches for delivery of $CdCl_2$ vapor species were considered: diffusion in parallel-plate configuration (Fig. 2) and vapor transport via

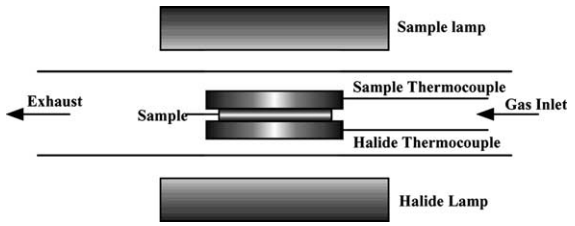

Fig. 2. Schematic of parallel $CdCl_2$ vapor treatment reactor. The sample is bounded above by a graphite susceptor and below by a hollow graphite susceptor containing $CdCl_2$ powder.

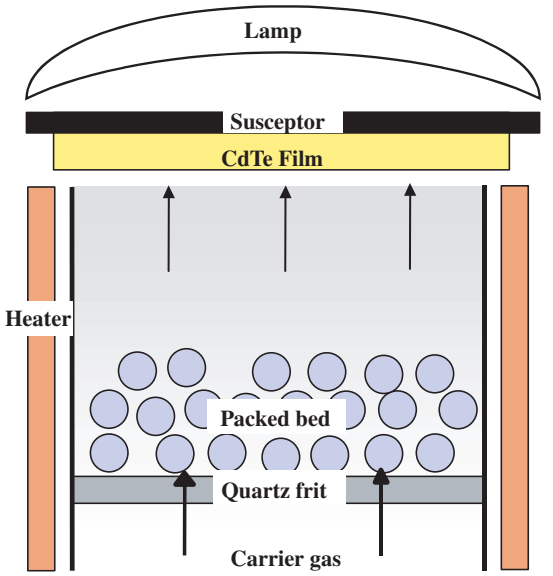

Fig. 3. Schematic depiction of carrier gas passing through a packed bed of $CdCl_2$.

carrier gas in a packed bed (Fig. 3). In both approaches, the diffusion of $CdCl_2$ through ambient gas is a critical aspect for estimating concentration at the film surface. In a static parallel-plate configuration, the separation is small; and diffusion calculations for $CdCl_2$ gas in N_2 and Ar ambients show that the characteristic time to reach equilibrium for 1 mm spacing at 400 °C is a few seconds. In the design of a packed bed delivery system, a steady state can be achieved, but the design critically depends on the carrier gas residence time compared to the characteristic thermal and mass diffusion time for the source particles. Also critical to operation of any vapor $CdCl_2$ system will be the composition of the carrier gas with respect to oxygen and water content. These components can contribute to ageing of the source thereby limiting the $CdCl_2$ partial pressure and changing the chemical reactions occurring at the CdTe surface (McCandless and Birkmire, 2000a,b).

3.1. Vapor chloride treatment—diffusion delivery

The reactor typically used for vapor $CdCl_2$ treatment consists of two parallel susceptors with independent temperature control. It has already been used for small-scale solar cell fabrication (McCandless et al., 1996; McCandless, 2001a,b) and to determine the solid state grain and grain boundary diffusion coefficients for CdS into CdTe thin films (McCandless et al., 2001; McCandless and Birkmire, 2000a,b). The lower susceptor contains solid $CdCl_2$ and the upper surface is the CdTe film undergoing the heat treatment (Fig. 2). The primary advantage of this reactor is the ability to

decouple the $CdCl_2$ concentration at the CdTe surface from the temperature of the CdTe surface. This is achieved by maintaining the $CdCl_2$ and CdTe surfaces at different temperatures. The temperature of the $CdCl_2$ surface determines the gas phase concentration of $CdCl_2$, while the temperature of the CdTe surface determines the reaction temperature. In this way it is possible to explore the effects of both temperature and $CdCl_2$ concentration on the CdTe heat treatment process. The concentration and temperature profiles of $CdCl_2$ in the heat treatment reactor are described as a function of z and t, where z is normal to the parallel $CdCl_2$ and CdTe surfaces, and t is time. The development of the temperature profile is described by (Bird et al., 1960).

$$\frac{\partial(\rho C_p T)}{\partial t} = \frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right) \tag{1}$$

where $T = T(z,t)$ is temperature, $C_p = C_p(T)$ is the heat capacity, $k = k(T)$ is the thermal conductivity, $\rho = pM/RT$ is the gas phase density, p is the system pressure (1 atm), M is the average molecular weight of the gas phase, and R is the ideal gas constant. Natural convection is minimized by maintaining the upper graphite susceptor (touching CdTe/CdS) at the same or higher temperature than the lower susceptor (containing $CdCl_2$). There is also a time-dependent concentration profile in the system, which is described by (Bird et al., 1960)

$$\frac{\partial c_A}{\partial t} = \nabla \cdot cD_{AB}\nabla x_A \tag{2}$$

where $c_A = c_A(z,t)$ is the concentration of component A ($CdCl_2$), and $D_{AB} = D_{AB}(p,T)$ is the diffusivity of component A in component B (air), and ∇x_A is the mole fraction gradient of component A. The $CdCl_2$ concentration at the source surface is specified by the parametric vapor pressure equation and thermodynamic constants (Knacke et al., 1997). Tabulated values of saturation pressure (P_{sat}) for CdTe, Cd, Te, CdS and $CdCl_2$ are presented in Table 2 and are depicted graphically in Fig. 4.

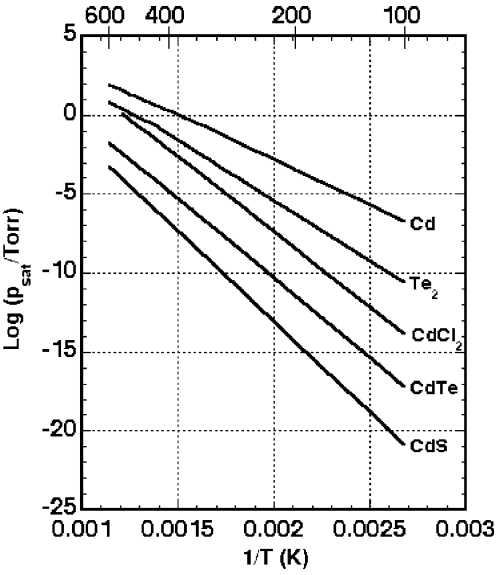

Fig. 4. Vapor–liquid–solid equilibria for CdTe, CdS, Cd, Te, and $CdCl_2$. The liquidus temperatures are $T_m^{Cd} = 321$ °C, $T_m^{Te} = 450$ °C, and $T_m^{CdCl_2} = 570$ °C. Parametric data from literature (Knacke et al., 1997).

It is obviously a tedious process to solve the coupled equations (1) and (2). If it can be shown that the characteristic times for both thermal and mass diffusion are short compared to the heat treatment time, the time derivatives of Eqs. (1) and (2) may be set to zero, and a simpler steady state solution may be obtained. The characteristic time for thermal diffusion, t_T, is given by

$$\tau_T = \frac{\ell^2 \rho C_p}{k} = \frac{\ell^2}{\alpha} \tag{3}$$

where ℓ is the length scale and α is referred to as the thermal diffusivity. The characteristic time is an order of magnitude estimate of the time required for the system to reach equilibrium. The length scale, ℓ, is simply the characteristic diffusion distance, in this case the separation between the $CdCl_2$ surface and the CdTe surface. We are also concerned with the characteristic time of the

Table 2
Saturation pressures (P_{sat}) for materials in the CdTe–CdS–$CdCl_2$ system, calculated from published parametric thermodynamic constants (Knacke et al., 1997)

T (°C)	P_{sat} (Torr)				
	CdTe	Cd	Te	CdS	$CdCl_2$
300	2.1E−08	0.0492	0.00038	8.4E−11	1.3E−05
350	5.2E−07	0.294	0.00455	3.4E−09	0.00027
400	7.9E−06	1.289	0.03758	7.7E−08	0.00361
450	8.2E−05	4.58	0.23019	1.1E−06	0.0329
500	6E−04	13.75	0.785	1E−05	0.222

Table 3
Thermal (α) and mass (D_{AB}) diffusivity for $CdCl_2$ in nitrogen ambient

T (°C)	α (cm^2/s)	D_{AB} (cm^2/s)
300	0.486	0.224
350	0.554	0.261
400	0.625	0.297
450	0.698	0.330
500	0.773	0.374

concentration profile development. The characteristic time for mass diffusion, τ_m, is given by

$$\tau_m = \frac{\ell^2}{D_{AB}} \tag{4}$$

Estimates of α and D_{AB} for nitrogen ambient are listed in Table 3 for the temperature range of Table 2, from 300 to 500 °C. The mass diffusion coefficient was determined using the Chapman–Enskog theory (Bird et al., 1960). The characteristic thermal and mass diffusive times are shown in Fig. 5 for different source to sample spacing. The time development of $CdCl_2$ concentration at the CdTe surface is shown in Fig. 6 for 400 °C at the same source to sample spacing as in Fig. 5. For typical source to sample spacing ~0.1 cm and treatment times of 20–30 min (1200–1800 s), the surface $CdCl_2$ vapor concentration is found to be comparable to the equilibrium saturation pressure. Similar results were calculated for argon and helium ambients.

3.2. Vapor chloride treatment—carrier gas delivery

For the case of a carrier gas passing through a fixed bed of subliming $CdCl_2$ spheres, as shown in Fig. 3, a steady state solution is needed (Bennett and Myers, 1982). Mass transfer in such a system occurs by molecular diffusion of $CdCl_2$ outward from the spherical surface into the stagnant medium and by ablation due to momentum transfer from the carrier gas to the surface of subliming $CdCl_2$. Assuming an isothermal packed bed with preheated carrier gas, the contribution to vapor concentration in the carrier gas along the bed depends on bed length, and for the gas to reach saturation, the characteristic diffusion time for $CdCl_2$ must be less than the residence time. For an isothermal bed of 0.1 cm diameter particles operating at 400 °C, with $D_{AB} = 0.297$ cm^2/s, we estimate that the linear velocity should be less than 5 cm/s. The mass flux from each sphere is given by:

$$J_{CdCl_2} = k\left(C^{surf}_{CdCl_2} - C^{gas}_{CdCl_2}\right) \tag{5}$$

For a subliming particle, the concentrations are determined by the partial pressures at the surface and in the adjoining medium. The mass transfer coefficient for a single sphere characterized by the Sherwood (Smith, 1970) and Schmidt (Hill, 1977) dimensionless numbers for momentum transfer and diffusivity:

$$k = \frac{D_{AB}}{d}\left[2 + 0.6\left(\frac{\mu}{\rho D_{AB}}\right)^{1/3}\left(\frac{dv\rho}{\mu}\right)^{1/2}\right] \tag{6}$$

where D_{AB} is the diffusivity of the $CdCl_2$ vapor in the carrier gas, d is the sphere diameter, μ is the bulk viscosity of the carrier gas, ρ is the carrier gas density, and v is the linear carrier gas velocity. Due to the relatively high vapor pressure and diffusivity of $CdCl_2$, a surprisingly thin layer is required to allow saturation pressure to be reached with ~0.1 cm particulates and 1–2 cm/s carrier gas velocity. Fig. 7 shows the positional dependence of the $CdCl_2$ partial pressure within a vapor generator, which during operation is in the vertical configuration of Fig. 3 to permit the $CdCl_2$ pellets to uniformly cover the supporting quartz frit, with the CdTe/CdS specimen to be radiatively heated from above. The IEC apparatus utilizes a 0.5 cm deep bed.

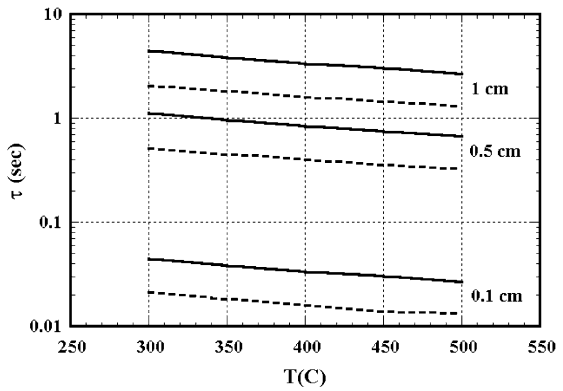

Fig. 5. Characteristic time versus temperature for thermal (dotted) and mass (solid) diffusion of $CdCl_2$ in nitrogen for different spacings.

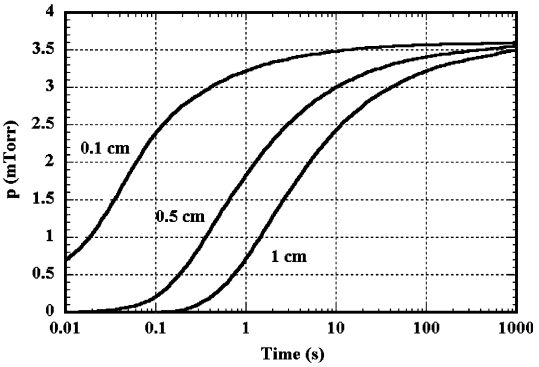

Fig. 6. Time development of $CdCl_2$ partial pressure at CdTe surface for 400 °C ($D_{AB} = 0.297$ cm^2/s).

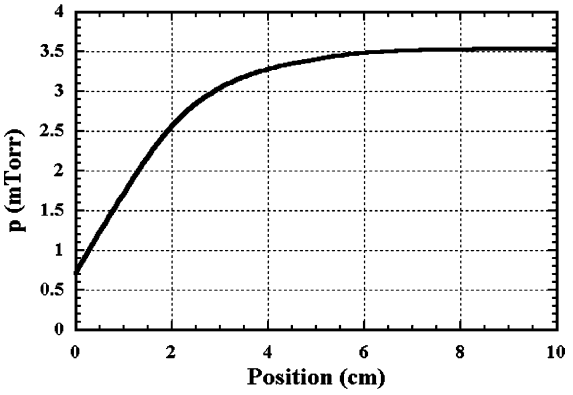

Fig. 7. $CdCl_2$ partial pressure versus position though a packed bed generator for operation at 400 °C with 0.1 cm spheres.

3.3. Vapor chloride—film and device results

Vapor $CdCl_2$ vapor treatments yield low surface residue and uniform device performance, making them an attractive alternative for large-scale processing. Fig. 8 shows glancing incidence X-ray diffraction (GIXRD) patterns of the surface of as-deposited, vapor $CdCl_2$ and wet $CdCl_2$ treated VT CdTe. The scans were made with Cukα X-ray source in asymmetric parallel-beam configuration, with incident beam angle of 1°, which samples a depth of 120 nm into CdTe. The $CdCl_2$ treatments were carried out at 420 °C for 20 min. For the vapor treatments, the $CdCl_2$ sources were maintained at 400 °C, which produces a $CdCl_2$ partial pressure of 3.5 mTorr. The GIXRD scan of the as-deposited CdTe shows, in addition to the usual CdTe reflections (1 1 1), (2 2 0), (3 1 1) and (4 0 0), a weak reflection at $2\theta = 27.5°$ which is a primary reflection of the native oxide TeO_2. The vapor treated sample exhibits the same pattern. The wet-treated sample, on the other hand, taken after a water rinse to remove $CdCl_2$, contains reflections from non-soluble phases, indexed as CdO ($2\theta = 33°$) and a different crystal form of $CdTeO_3$.

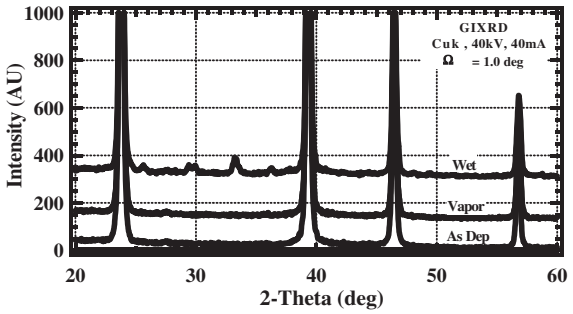

Fig. 8. GIXRD patterns taken at 1° incidence, of as-deposited, wet $CdCl_2$ treated and parallel plate vapor $CdCl_2$ treated VT CdTe films. Treatments were carried out at 420 °C for 20 min.

Devices were completed on the films shown above, by etching the CdTe surface with a three-step process (described below) using hydrazine to reduce oxides and produce a 10–30 nm thick Te layer and then depositing 3 nm Cu and 5 nm Au contacts. After contact processing, GIXRD scans show no detectable oxide phases. The AM 1.5 *JV* performance of the best device and the average of 8 devices made on each sample are listed in Table 4. With no $CdCl_2$ step, cells with 9% efficiency are obtainable but the *average* performance is much lower, due to low V_{oc} and FF, suggesting poor uniformity and junction quality. Higher performance and lower standard deviation was obtained for samples processed with $CdCl_2$ treatment. Although comparable standard deviations were found for the wet and parallel plate vapor treatments, the highest performance, with efficiency = 12%, $V_{oc} > 800$ mV and FF > 73%, was obtained with parallel-plate $CdCl_2$ vapor treatment. The cells made with packed bed $CdCl_2$ treatment had lower performance, with the lowest efficiency obtained on cells at the edge, where the effluent vapor stream mixes with ambient air. This shows that controlling the vapor phase composition across the entire sample is important to obtaining uniform device performance, and more optimization is necessary.

Table 4
Best and average (Avg) AM 1.5 *JV* results for devices fabricated from a single plate of production vapor transport deposited CdTe/CdS and treated at 420 °C using wet $CdCl_2$, parallel-plate vapor $CdCl_2$, packed bed ($L = 0.2$ cm) vapor $CdCl_2$, and no post-deposition treatment

Treatment	$CdCl_2$ Pressure (mTorr)		V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Eff (%)
Vapor $CdCl_2$ packed bed	2.5	Best	755	19.1	64.0	9.2
	2.5	Avg	735 ± 20	19.0 ± 0.4	61.0 ± 3	8.5 ± 0.6
Vapor $CdCl_2$ parallel plate	3.5	Best	805	20.3	73.2	12.0
	3.5	Avg	801 ± 5	20.2 ± 0.3	71.2 ± 2	11.6 ± 0.4
Wet $CdCl_2$	Solid	Best	782	20.1	68.5	10.8
	Solid	Avg	787 ± 5	20.0 ± 0.2	63.7 ± 2	10.0 ± 0.4
None	0	Best	700	20.6	64.8	9.3
	0	Avg	555 ± 90	20.5 ± 0.3	56.5 ± 5	6.4 ± 2.6

These results show that good device performance and uniformity can be obtained with vapor $CdCl_2$ treatment. The oxides CdO and $CdTeO_3$ on the surface are removed by the contacting process and thus do not impede the formation of low resistance contacts. Furthermore, we have found that CdTe films containing $CdTe_2O_5$ on the surface, formed by exposure of CdTe to humid ambient, do not yield good quality solar cells, indicated by low V_{oc} and FF. The oxidation process can affect the near-surface chemical equilibrium by removing disproportionate amounts of Cd or Te from the lattice, which will shift the defect vacancy content in the film. In CdTe, extremely small shifts in stoichiometry exert a strong effect on the p-type conductivity; Cd vacancies readily form acceptor complexes with dopants such as Cu and Cl, which enhances p-type conductivity. Thus, cells made with CdTe containing $CdTe_2O_5$ oxide may owe their inferior performance to a stoichiometric shift resulting in lower p-type conduction due to reduced Cd vacancy concentration.

4. Influence of chemical and structural properties on devices

The previous section shows that post-deposition treatment improves device performance considerably, with average efficiencies increasing from 6% to 11%. All high efficiency CdTe/CdS devices utilize such treatments; and the treatments modify the chemical and structural properties of the device structure, which in turn control the optical and electrical properties of the films. Post-deposition treatments at elevated temperatures in reactive chemical environments such as O_2 and $CdCl_2$ shift the chemical state of the films considerably compared to the as-deposited condition. This section summarizes the basis for this and the effect on device operation.

Over the past decade, detailed analysis of the interfacial region in moderate and high efficiency CdTe/CdS cells by X-ray diffraction (XRD), transmission electron microscopy (TEM) with microprobe (EDS), secondary ion mass spectroscopy (SIMS) and opto-electronic measurements have shown that the CdTe–CdS interface in a working device consists of $CdTe_{1-x}S_x/CdS_{1-y}Te_{1-y}$ alloys (McCandless and Sites, 2003). The interfacial values of x and y correspond to the solubility limits in the CdTe–CdS system at the device processing temperature. The $CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ alloys form via diffusion across the interface during CdTe deposition and post-deposition treatments and affect photocurrent and junction behavior. For the CdTe–CdS system, with $CdTe_{1-x}S_x$ and $CdS_{1-y}Te_y$ phases, the thermal dependence of the miscibility gap is well approximated by a cubic fit (McCandless et al., 2002):

$$x = (4.717e^{-2}) + (-3.104e^{-4})T + (9.543e^{-8})T^2 + (-3.687e^{-10})T^3 \quad (7)$$

$$y = (-1.684e^{-1}) + (1.172e^{-3})T + (-2.639e^{-7})T^2 + (2.348e^{-10})T^3 \quad (8)$$

The stable crystallographic forms of the solid alloys are zincblende (F-43m) structure for Te-rich $CdTe_{1-x}S_x$ and wurtzite ($P6_3mc$) structure for S-rich $CdS_{1-y}Te_y$. The zincblende–wurtzite transition in metastable films occurs at $x = 0.3$, and the lattice parameter within each structure type follows Vegard's rule. Metastable and equilibrated $CdTe_{1-x}S_x$ alloy films exhibit the same composition dependence of optical bandgap (E_g), with minimum $E_g = 1.39$ eV at the zincblende–wurtzite transition. The compositional dependence of the $CdTe_{1-x}S_x$ bandgap is described by (McCandless and Sites, 2003):

$$E_g(x) = 2.40x + 1.51(1-x) - bx(1-x) \quad (9)$$

where the bowing parameter, $b = 1.8$. Thus, for cells processed at ~500 °C, the $CdTe_{1-x}S_x$ composition is $x \sim 0.09$, and the corresponding absorber layer optical band gap is $E_g \sim 1.44$ eV. In correlating measurable properties in CdTe/CdS solar cells and diagnostic structures, it is helpful to recognize that alloy formation results in a lattice parameter distribution, detectable by XRD, that corresponds to a distribution in opto-electronic properties, which are detectable in films by variable angle spectroscopic ellipsometry (VASE) and in devices by quantum efficiency (QE). For compositionally graded alloys formed by diffusion from CdS into the CdTe film, we expect the maximum band gap variation in the materials to occur at the CdTe–CdS interface and possibly in grain boundary regions near the interface, due to enhanced diffusion in the grain boundaries. In devices, the long-wavelength quantum efficiency edge is generally found to correlate with compositionally broadened diffraction line profiles of prominent (hkl) reflections in alloyed films.

Formation of the $CdS_{1-y}Te_y$ alloy on the S-rich side of the junction reduces the band gap and increases absorption, which reduces photocurrent in the 500–600 nm range. This effect is suppressed by annealing the CdS film prior to CdTe deposition to reduce crystallographic defects in CdS. Formation of the $CdTe_{1-x}S_x$ alloy on the Te-rich side of the junction reduces the absorber layer bandgap, due to the relatively large optical bowing parameter of the CdTe–CdS alloy system. Overall, this has little effect on efficiency since the increase in long wavelength QE typically increases photocurrent by ~0.5 mA/cm^2, which is nearly offset by small reduction in $V_{oc} \sim 25$ mV.

Other significant effects of alloy formation include spatially non-uniform consumption of the CdS layer,

penetration of CdS into the CdTe film grain boundaries, and relaxation of lattice strain between CdTe and CdS. The rate of CdS consumption has been quantitatively determined in terms of bulk and grain boundary diffusion. For treatment at 420 °C in 10 mTorr $CdCl_2$ and 150 Torr O_2, similar diffusion coefficients for bulk (D_b) and grain boundary (D_{gb}) have been determined for CdS diffusion into CdTe deposited by electrodeposition, PVD, and CSS: $D_b = 1.25 \times 10^{-13}$ cm^2/s and $D_{gb} = 1.5 \times 10^{-8}$ cm^2/s (McCandless et al., 2001). For PVD films with ~1 μm diameter grains and 3–4 μm film thickness, the typical $CdCl_2$ treatment at 420 °C for 20 min consumes CdS at an equivalent thickness rate of ~0.05 nm/s. Spatially non-uniform consumption of CdS leads to parallel junctions between $CdTe_{1-x}S_x$/$CdS_{1-y}Te_y$ and $CdTe_{1-x}S_x$/ITO (or SnO_2); since the $CdTe_{1-x}S_x$/TCO junctions have higher J_o, the net result is an increase in total J_o, which reduces V_{oc}. For two predominant types of diode A and B and assuming comparable diode prefactors ($\beta = q/AkT$), the overall diode current can be described in terms of the usual diode equation and the fractional area of the two diode types:

$$f = \frac{\text{Area}(A)}{\text{Area}(A+B)} \tag{10}$$

$$J = \left[J_o^A(1-f) + J_o^B(f)\right]\exp(\beta V) - J_L \tag{11}$$

Solving for the open circuit voltage ($J = 0$) gives:

$$V_{oc} = \frac{1}{\beta}\ln\left[\frac{J_L}{J_o^A(1-f) + J_o^B(f)}\right] \tag{12}$$

Characterization of actual CdTe/CdS/ITO (A) and CdTe/ITO (B) cells shows comparable diode A-factors ~1.7 but diode currents of $J_o^A = 8 \times 10^{-8}$ mA/cm^2 and $J_o^B = 1 \times 10^{-4}$ mA/cm^2, respectively. For 1% fractional area of holes in the CdS film, the V_{oc} would thus be reduced by 300 mV. Modeling of thin-film device structures with a random distribution of different quality diodes in-parallel is more extensively covered in other recent work (Karpov et al., 2004). Penetration of S-rich species into the CdTe grain boundaries can produce a three-dimensional junction, which increases the actual junction area, also limiting V_{oc}. This grain boundary penetration of CdS in CdTe is accelerated by $CdCl_2$ and O_2 chemical activity during the post-deposition treatment and is extremely sensitive to the physical and chemical state of the CdTe film prior to the treatment (McCandless and Birkmire, 2000a,b).

The exposed (back) surface of the CdTe film is subjected to a wide range of ambient conditions during processing, which shift the surface state; shifts in equilibrium are expected to influence bulk properties if the processing is carried out at sufficient temperature to allow re-distribution of excess species. Thus it is also important to consider the CdTe–O_2–$CdCl_2$ chemical system. For CdTe–$CdCl_2$, the occurrence of a eutectic at ~490 °C suggests that enhanced surface mobility can be expected for $T > 450$ °C and high $CdCl_2$ concentration due to liquid Cd(TeCl). Note that the solubility limit for $CdCl_2$ in CdTe is <0.1 wt.% at 490 °C. At lower temperatures and low $CdCl_2$ concentration in the presence of O_2, chemical reaction at the surface and in grain boundary between $CdCl_2$, O_2, CdTe and CdS is expected. For treatments where solid $CdCl_2$ is in physical contact with CdTe in air ambient, the solid phase reaction is:

$$\begin{aligned}&CdCl_2(s) + O_2(g) + CdTe(s)\\ &\quad\leftrightarrow TeCl_2(g) + 2CdO(s), \Delta G_{rxn}\ (400\ ^\circ\text{C})\\ &\quad= -137.6\ \text{kJ/mol}.\end{aligned}$$

For vapor $CdCl_2$:O_2:Ar treatments, in which $CdCl_2$ condensation is prevented by maintaining the CdTe/CdS at a higher temperature than the $CdCl_2$ source, the reaction between gas phase $CdCl_2$ and O_2 and solid CdTe is:

$$\begin{aligned}&CdCl_2(g) + O_2(g) + CdTe(s)\\ &\quad\leftrightarrow TeCl_2(g) + 2CdO(s), \Delta G_{rxn}\ (400\ ^\circ\text{C})\\ &\quad= -206.2\ \text{kJ/mol}.\end{aligned}$$

Both cases are thermodynamically favored but the extent of reaction depends on the activity coefficient of the reactive species, and a large difference is expected between the solid–solid contact case ($CdCl_2$ activity coefficient = 1) and the solid–vapor case (activity coefficient ~10^{-8} atm). In fact, for vapor treatments, the $CdCl_2$ partial pressure can be varied over a wide range by controlling the source temperature. Analogous reactions exist for CdS–$CdCl_2$–O_2.

In these overall reactions, volatile VIB–VIIA species are generated and solid CdO phase is produced. We have verified this reaction scenario experimentally for treatments of both CdTe and CdS powders and films. The formation of volatile VIB–VIIA species provides a mechanism for enhanced atomic mobility within grain boundaries and may be the key to understanding enhanced diffusivity.

At the back surface of CdTe, the oxide is an undesired byproduct. CdO has halite (Fm3m) structure, is thermally stable up to 900 °C, has the highest ionicity value in the Cd-VIB system (0.78), is insulating, and therefore poses an obstacle for back contact formation.

For reaction in the presence of O_2 alone, CdTe forms a native oxide $CdTeO_3$, which lies on the TeO_2–CdO pseudobinary tie-line and is the equilibrium native oxide of CdTe, has cubic structure and is electrically insulating. We have verified this phase in films experimentally by GIXRD measurements of CdTe films treated at

450–600 °C in dry air (McCandless et al., 2003). For treatments in air containing a partial pressure of water, we have found that a different oxide, $CdTe_2O_5$ is consistently formed. The deviations from stoichiometry caused by oxide formation should have a profound effect on the near-surface Cd-vacancy concentration (Marfaing, 2001), impacting the ability to control both bulk and surface acceptor concentration.

5. Back contact formation

Due to the high work function of CdTe, ohmic contact formation is not possible with metal films. Pseudo-ohmic contacts are, therefore, produced by making the CdTe back surface more p-type (Durose et al., 1999). Thus, while increasing the barrier height for electron flow at the back contact interface, the resultant narrowing of the barrier allows electron tunneling. Formation of a pseudo-ohmic contact is usually obtained by the introduction of impurity metals at the back contact interface. Though a number of metals have been used to produce CdTe back contacts, including Au, Pb, Ni, Hg and Ag (Dobson et al., 2000), Cu is almost ubiquitously employed. CdTe itself is difficult to dope with impurity atoms, therefore, to produce a p+-surface, a Te-rich surface is nearly always produced during back contact processing to improve the efficiency and extent of the impurity doping or reaction at the back contact interface. However, this observation and the high Cu concentrations generally used, suggest that a chemical reaction takes place at the back contact to produce a bulk phase contact material (McCandless et al., 1998) as opposed to the concept of a 'doped' CdTe back surface.

A number of steps are required to form low resistance back contacts to CdTe/CdS devices; and nearly every research group applies their own contacting method, via different and varied empirically derived approaches. Often the steps employed have a historical basis, may not be necessary for successful back contact processing and may only complicate possible industrial scale up. The procedures employed for back contact processing of CdTe/CdS devices by most laboratories generally incorporate the following steps; (i) removal of residual surface oxides and other contaminants on the CdTe surface, (ii) formation of a Te-rich surface to improve CdTe reactivity for contacting, (iii) application of Cu or other impurity metals, (iv) formation of the back contact, generally via annealing, and (v) application of secondary contact and device completion. Many different contacting procedures have evolved empirically. Some may incorporate single treatments, which accomplish more than one of the above steps or some steps may not be required, for example (e.g. uninterrupted in vacuo CdTe processing is unlikely to require the removal of surface oxides), but the basic process sequence generally remains constant. Our approach is to begin to understand the fundamental materials chemistry of each of the common processing steps. With this, the goal is to develop a simple and universally applicable process that offers good quality and stable back contacts for CdTe/CdS for devices, irrespective of CdTe history and properties. In this section, each of the above processing points will be discussed, including briefly reviewing recent experiments at IEC and some of the recent literature.

5.1. Etching of CdTe

Prior to contacting, the CdTe back surface generally must be modified, as described above, to remove residual oxides and to form a Te-rich CdTe surface (Dobson et al., 2003). Most research groups generally employ a wet chemical etch step to achieve either or both of these modifications. At an industrial scale, due to the corrosive nature of most etchants, 'dry' techniques are being sought. However, wet chemical etching is used in a number of electronic technologies to achieve contaminant-free materials surfaces. For CdTe back contact processing, wet etches allow fast treatment times and are generally easy to use in the laboratory, requiring only small volumes and often no heating of the solution. CdTe etchant chemicals, however, tend to be toxic, corrosive and reactive. Common etchants include Br_2/methanol solutions (BM) and aqueous nitric acid/phosphoric acid mixtures (NP). Other CdTe etchants have included, H_2O_2, hydrazine, thiosulfate, acidified dichromate, citric acid, ammonia and alkali metal hydroxides. One treatment that has shown very good success at IEC, but also highlights the hazardous nature of these treatments, is the Br_2-Dichrol-Hydrazine (BDH) etch (McCandless et al., 1998). This treatment consists of three steps; a short etch in dilute BM to remove residual surface oxides, immediately followed by a dip in acidified dichromate (commercial dichrol solution) to produce a mixed Te/TeO_2 surface, and finally immersion in potentially explosive hydrazine at ~55 °C to reduce surface TeO_2 to Te. This treatment generates a good quality, 50 nm crystalline-Te (c-Te) surface layer on CdTe. At an industrial level, where the use corrosive chemicals may need to be avoided, pre-contact surface treatments may be ignored or less corrosive chemicals sought. For example, organic multi-dentate ligands, including diaminoethane and ethylendiaminetetreaacetic acid, EDTA, has had some success in an industrial process (Johnson et al., 2001). The action of such etches is thought to progress by solubilizing the Cd^{2+} ions from the CdTe surface by complexation, and leaving a Te-rich surface layer.

A number of factors regarding wet etching during contact processing are, however, of concern. These include; (i) the behavior of residual etchant within the

grain boundaries, which is not understood in relation to device chemistry and performance, (ii) the effects of the atmosphere on the freshly etched CdTe surface prior to application of Cu, (iii) effects of the significant changes to film and grain boundary morphology following etching on device performance, and (iv) the irreproducibility of wet etches, due to subtle differences in solution and substrate conditions, which may produce inconsistent surface products and morphological effects. Considering these points, and also the ease of industrial scale-up, considering the safety and disposal issues, of the contacting process, 'dry' or vacuum processes to form Te-rich CdTe surfaces have also been used (Hegedus et al., 2000).

Despite their widespread and historical use, the mechanism and dynamics of these etches on CdTe are not well understood. A knowledge of etchant behavior and the nature of the CdTe surface throughout the reaction, including its reactivity towards the atmosphere and back contact metals, will assist optimization of wet chemical treatments and contact processing to achieve the development of stable back contacts to CdTe/CdS devices. The development of a universal and safe wet etchant that can be easily applied to CdTe films, independent of thickness and history, would be advantageous for scale-up of the CdTe device processing.

As discussed in a previous section, $CdCl_2$ treatments of CdTe can, depending on treatment conditions, produce a range of Cd and Te surface oxides. The presence of significant oxide on the CdTe can produce an insulating and unreactive surface, and thus prevent the formation of a favorable back contact. If a wet chemical etch is used to produce the Te-rich surface for contacting, then the single treatment can suffice for both oxide removal and Te generation. However, for 'dry' depositions of Te for contacting or in order to carry out measurements or experiments directly on the CdTe surface, removal of the residual oxides is required. For this, short etches in weak BM solutions, $\approx$5 s in $\sim$0.01% BM, successfully removes the oxides without significant etching of the CdTe itself. Following etching, samples should be removed from the atmosphere, or immediately continued to the next processing step to minimize atmospheric oxidation of the surface.

The chemical treatments required for the formation of a Te-rich CdTe back surface for contacting, commonly involve an oxidation step, e.g. Br_2 and nitric acid, of BM and NP, respectively, are oxidizing agents. These treatments oxidize surface telluride ions, Te^{2-}, to elemental tellurium, Te^0, and dissolve Cd^{2+} ions, which are unable to remain in a tellurium environment, from the film. Reducing and complexing treatments have also been applied to CdTe devices. For successful back contacting, generally treatments of 5–20 s in 0.1–1% BM (Batzner et al., 2000) or a $\sim$60 s in aqueous $\sim$1% HNO_3: $\sim$70% H_3PO_4 mixture (NP) (Ibid; Sarlund et al., 1996; Li et al., 1999) are used. As NP etching progresses, the formation of bubbles on the Te surface is generally observed after $\sim$20 s immersion. These bubbles are due to the formation of gaseous NO or NO_2 products. The time for bubbles to appear can vary, dependent on temperature, solution concentration and the presence of surface oxides. The acidity of the NP etch is expected to remove any tellurium oxides formed during treatment (Sarlund et al., 1996). Following etching, the CdTe surface is silvery-gray and roughened, due to grain boundary etching, with a $\sim$50–100 nm surface Te layer (Ibid; Li et al., 1999; Dobson et al., 2003). Because of the aggressive nature of the NP etch, this treatment can generally only be used for etching thicker, $\gtrsim$ 5 μm, CdTe layers. BM etching produces a polished CdTe surface, generally consisting of $\sim$7–8 Å Te surface layer without significant grain boundary etching (Batzner et al., 2000; Dobson et al., 2003).

Understanding the nature of the CdTe surface prior to, during and following etching is of critical importance to the successful optimization and outcome of the back contacting process. We have recently reported the use of the surface sensitive techniques VASE and GIXRD to monitor effects of etching the CdTe surface, to clarify etch chemistry and the nature of the CdTe surface both during and following treatment (Dobson et al., 2003). Fig. 9 shows the 1.5–4.6 eV range of the ε_2 versus photon energy spectra, obtained from VASE, of 5 μm CdTe/ITO/7059 films prior to and following etching in NP and BM. ε_2 is the imaginary part of the complex dielectric constant and is proportional to the absorption coefficient of the material. Therefore, with knowledge of the electronic transitions of different materials, peaks in the ε_2 spectra can be directly related to materials present within the sample (Ibid). The ε_2 spectrum of unetched

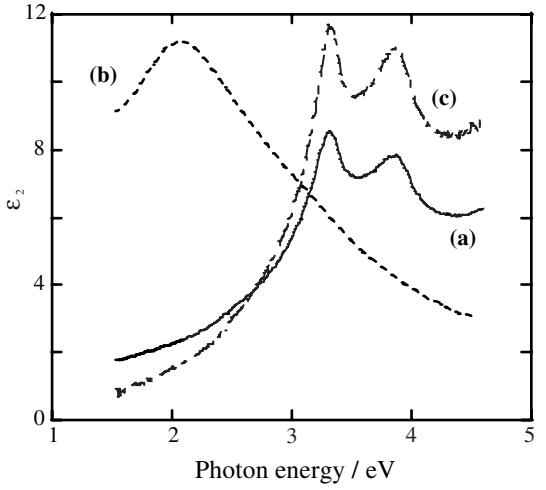

Fig. 9. VASE ε_2 spectra of (a) an unetched CdTe film and CdTe films following etching in (b) NP1 for 25 s and in (c) 0.1% BM for 10 s.

CdTe (curve *a*) contains two peaks at 3.3 and 3.9 eV. These peaks are due to the E_1 and $E_1 + \Delta_1$ transitions of CdTe, respectively. The CdTe peak intensity, with respect to the 3.3 eV transition, depends on the presence of native oxides, highlighting the use of the non-destructive VASE technique as a research and industrial processing diagnostic tool for fast analysis of the CdTe surface. Following 25 s NP etch, the ε_2 spectrum now contains a single broad peak at 2.1 eV, due to Te (curve *b*). The CdTe peaks are barely detectable, indicating a high degree of Te on the CdTe surface. Within a few minutes of etching, the Te peak was observed to grow and sharpen in subsequent VASE scans, before finally reaching a maximum intensity, due to crystallization of surface Te, which was confirmed with rapid GIXRD measurements. Fig. 10 shows the sequential GIXRD scans, ~3 min apart, of a CdTe sample immediately following a 25 s NP etch. The Te(1 0 1) reflection at 27.6° is observed to grow, completing crystallization after ~10 min following etching.

NP Etching for <35 s results in amorphous-Te (a-Te) films that spontaneously crystallizes following removal from solution. Crystallization time increases for shorter etches, e.g. less than 5 min for a 35 s etch to over 1 h for a 15 s etch. a-Te is known to be unstable at room temperature (Sarlund et al., 1996) and spontaneously crystallizes. The slower crystallization with shorter etches can be attributed to the lesser amounts of generated a-Te requiring a longer time to complete molecular rearrangements. It was found that for NP etches >40 s, crystallization occurs during etching and a crystalline Te film is observed.

In contrast to NP, curve *c* in Fig. 9 shows that, following BM etching, only an increase the CdTe VASE ε_2 intensity is observed. This is due to smoothing of the surface, which produces a greater surface sampling area and reduces scattering. Only very thin Te films are expected, and hence, no Te peak is observed with VASE or GIXRD. Modeling of the VASE data has indicated a 7–8 Å Te surface layer is formed, which is consistent with literature data (Aspnes and Arwin, 1984). From VASE measurements, BM etching has been found to be reproducible, giving very similar surfaces on CdTe films of differing microstructure and surface oxide amounts. This very important result allows confidence in the nature of the surface following BM etching.

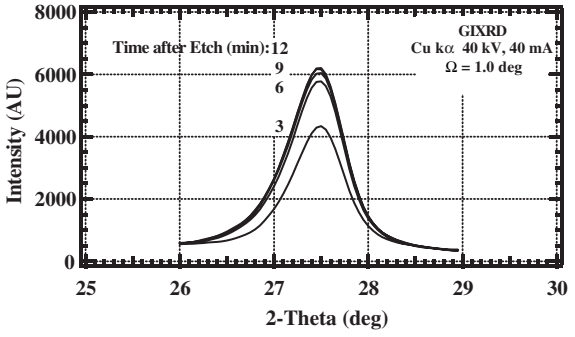

Fig. 10. Time-progressive GIXRD patterns taken at 2° incidence, of Te(1 0 1) reflection, for a CdTe film immediately following a 25 s NP1 etch. Each scan cycle was ~3 min apart.

IEC has also developed 'dry Te' or all-vapor processes for back contact processing (McCandless, 2001a,b; and Hegedus et al., 2000). A Te layer of only a few nm thickness can be deposited by vapor deposition or evaporation before application of a Cu layer and other back contact components. These dry processes completely avoid difficulties in handling corrosive chemicals and contamination of the device structure. Smooth crystalline Te films are deposited with good reproducibility and control of film thickness. Devices with 12% efficiency have been processed using dry Te contacting process (McCandless et al., 1996). However, preparation for dry and/or high vacuum techniques can take significant time, prevention of atmospheric oxidation of deposited layers is critical, and the scale up of such processes may involve far greater start-up costs and difficulties. We note, however, that a wet etch may still be required to remove residual oxides formed during optimized $CdCl_2$ treatment.

5.2. Atmospheric oxidation of Te on etched CdTe

Delays in contacting the devices following Te formation, and exposure to atmosphere allows the formation of oxides on the CdTe surface. These will affect reactivity of the Te layer and, hence, affect back contact formation, performance and reproducibility. VASE has been used to monitor the stability of freshly etched CdTe surfaces towards atmospheric oxidation (Dobson et al., 2003). Fig. 11 shows the amplitudes of the 2.1 and 3.3 eV photon energies obtained from ε_2 spectra of 25 s NP and 60 s 0.01% BM etched CdTe films, respectively, over the first 100 min following etching. These energies coincide with the Te peak and CdTe E_1 peaks for NP and BM etched pieces, respectively, of the Fig. 9 ε_2 spectra. As Te cannot be detected following BM etching, the CdTe E_1 peak is profiled as oxidation of the surface will result in a decrease in dielectric response and, hence, spectral intensity. A decrease in the CdTe E_1 peak is used as a signature for the formation of a surface layer, resulting in a loss of CdTe sampling depth, and therefore a loss in intensity.

Following NP, a rapid increase in intensity is observed due to Te crystallization. Following completion of crystallization, no changes are observed until ~60 min after etch, when the intensity begins to decrease as a result of atmospheric oxidation. This oxidation continues till around 7–8 h after etching. No oxidation was apparent on NP etched CdTe films that were stored in

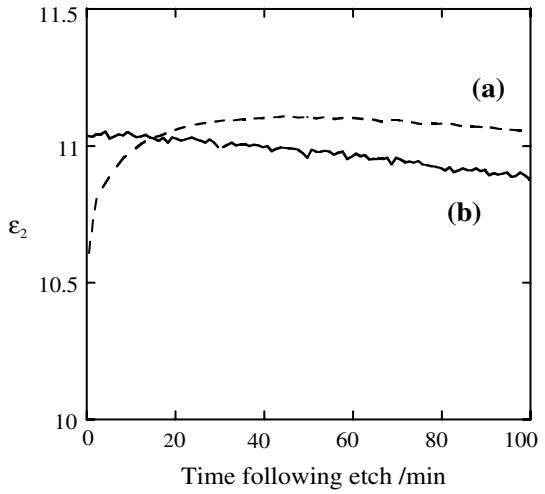

Fig. 11. Time profiles of ε_2 from (a) 25 s NP1 and (b) 60 s 0.1% BM etched CdTe films. ε_2 values were obtained at 2.1 and 3.3 eV, respectively.

vacuum or dry air immediately following etching, suggesting humidity plays a significant role in atmospheric oxidation of Te. Following BM etching, oxidation of the Te begins almost immediately and continues for 3–6 h. The fast oxidation of the BM etched surface can be attributed to the Te film being very thin and amorphous. These observations highlight the need for cells to be contacted immediately following Te formation to minimize oxidation of the surface.

5.3. Application of Cu

There are several methods to apply Cu to the CdTe back surface, including evaporation of thin Cu films onto the CdTe surface, application of graphite paste containing Cu powder, Cu salts or compounds or Cu-doped alloys, and dipping or spraying the surface with Cu salt solutions. An anneal step is generally required following contacting to force the chemical reaction between Cu and Te to completion, to form the desired copper telluride, $Cu_{2-x}Te$, phase (McCandless et al., 1998) and distribute Cu into the CdTe film. The application of a secondary contact, to provide for lateral current conduction, is also generally required to complete the back contact. The order of these steps is not always critical, being dependent on the nature of Cu deposition and simplification of the process. Sometimes following annealing and deposition of a metal film secondary contact, a short BM etch, which freely penetrates most metal films, is applied to remove excess Cu from the CdTe surface and grain boundaries (McCandless et al., 1998). The presence of excess Cu at the junction and/or in the CdS layer, distributed by grain boundary diffusion, has been suspected as a possible component of the instability exhibited by some CdTe/CdS devices (Dobson et al., 2000).

Vacuum evaporation of high purity Cu for back contact formation of CdTe devices offers good control of deposited metal layer thickness, which allows for careful tuning of the amount of applied Cu to give stoichiometric $Cu_{2-x}Te$ back contacts. The Te layer and metal secondary contact can also be sequentially deposited during the same vacuum process. Annealing of the back contact can also be carried out under vacuum immediately following contact deposition, thus avoiding any deleterious contact with the atmosphere. However, despite the control of deposited Cu, this method delivers an amount of Cu in excess of that required for successful contacting. High-vacuum techniques also require significant purging and pump down times and generally only a limited number of pieces may be processed at any given time in a laboratory setting.

The use of graphite pastes containing a Cu source allows fast and vacuum-free processing of back contacts, and has received much use at a research level. The paste, containing a suitable impurity additive, is merely applied or painted through a mask to a freshly etched CdTe surface and the device is annealed following drying. The graphite paste also acts as the current carrying secondary contact, but can also be coated with metal paste to improve conductivity. Acheson electrodag (#505-SS) is generally the graphite paste used, and often contains resins to improve adhesion and strength of the baked graphite layer. A number of Cu-source additives can be used, including elemental Cu powder, simple Cu salts and compounds, and Cu-doped alloys, e.g. Cu:HgTe and Cu:ZnTe. Care must be taken to ensure homogeneous mixing of the paste and additives. Methyl ethyl ketone or similar is commonly used as the paste solvent.

We have compared a range of Cu-based additives of elemental Cu powder, simple Cu(I) and Cu(II) salts, and Cu(II) complexes with simple chelate ligands. Table 5 lists the *JV* characteristics of CdTe/CdS devices contacted with graphite pastes containing these additives. An indicator for series resistance in *JV* behavior is the slope, dV/dJ at V_{oc}, which is represented as R_{oc}. For high performance devices, R_{oc} is typically less than 2 mS/cm^2, and devices having poor contact behavior or high contact resistance exhibit R_{oc} in excess of 10 mS/cm^2. In Table 5, we list R_{oc} and qualitative *JV* curve characteristics, including forward bias curvature (rollover), crossover between the light and dark curves (crossover), and forward–reverse *JV* retrace hysteresis. Rollover is a manifestation of a back-contact barrier as demonstrated in other work (McCandless et al., 1998). Crossover between light and dark curves, or loss of superposition, is commonly attributed to photoconductivty in the device. The occurrence of low-frequency (0.01–1 Hz) hysteresis can be due to either deep traps states in CdTe or additional capacitance from an insulating surface layer. GIXRD

measurements have shown residual oxide phases present at the back surface on devices that exhibit significant retrace hysteresis. In Table 5, pastes containing Cu powder, Cu(0), or Cu(I) salt additives produce the best devices with the lowest R_{oc} and the least amount of crossover or hysteresis. Simple dehydrated Cu(II) salts can produce reasonable back contacts, but tend to yield lower performance than Cu(I) salts. Cu(II) chelate complexes do not produce good contacts due to the stability of these molecules preventing reaction of Cu ions with Te.

While the concentration of Cu in the paste can be well controlled, an excess of Cu must be delivered to the device to ensure surface reaction and to dope the CdTe p-type, though only a limited amount of Cu will initially react with the Te-rich CdTe surface. Thermal treatment, such as experienced during contact annealing and accelerated life testing, of completed CdTe devices is likely to diffuse excess Cu from the paste into the CdTe (Dobson et al., 2000). Scale-up to industry may be difficult, though screen-printing, spin coating, spray or simple painting approaches have been demonstrated. A similar approach has been reported at an industrial scale, where a clay-based dielectric paste containing Cu salt additives (Johnson et al., 2001) is applied to the Te-rich CdTe surfaces for contacting. To complete devices, however, the paste had to be removed and conducting contacts applied.

Another method to deliver Cu species is via application of Cu salt solutions, by dipping or spraying onto the CdTe surface, or by evaporation (McCandless, 2001a,b). Dipping allows a small amount of Cu to become incorporated in the device, however, and similar to the solution $CdCl_2$ treatments, complete and uniform coverage of the surface cannot be guaranteed as the sample dries, resulting in a loss of control of the amount of Cu applied. Spray or evaporation methods allow more uniform delivery of precise quantities of Cu species to an area of substrate. Based on the work with Cu–Te metal contacts, devices with Cu_2Te, with Cu in the +1 valence state, Cu(I), yield the highest efficiency. This also seems to extend to the optimal valence state for Cu salts, as shown in Fig. 12. In the figure, devices were fabri-

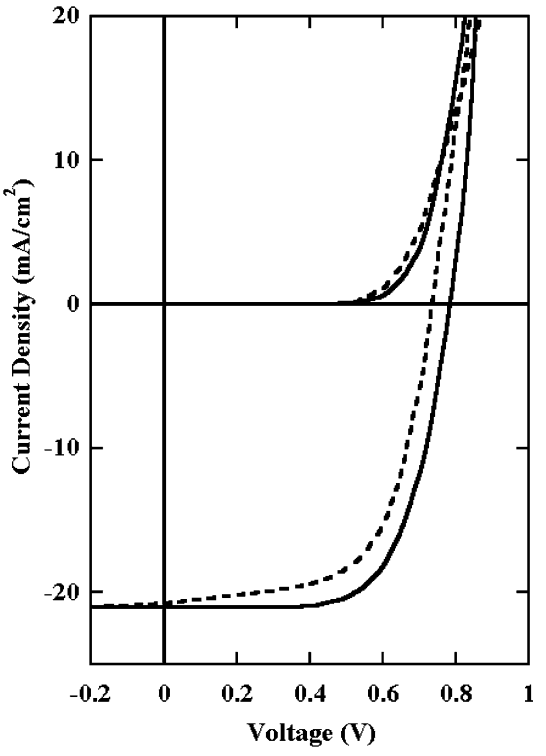

Fig. 12. Light and dark *JV* curves for CdTe/CdS devices processed with methanol solutions containing CuCl (solid) and $CuCl_2$ (dotted).

Table 5
J–V characteristics for CdTe/CdS devices contacted with graphite paste back contacts containing the listed Cu additives

Cu source		Cu state	R_{oc} (mS/cm^2)	Roll-over	Cross-over	Hysteresis
None		–	34.8	W	Y	W
Cu salts	Cu powder	0	13.6	N	Y	N
	CuCl	1	13.1	N	W	N
	CuI	1	11.2	N	W	N
	CuSCN	1	17.7	N	Y	N
	CuCN	1	30.1	Y	Y	W
	Cu(acetate)	2	24.1	N	Y	N
Cu complexes	Cu(oxalate)	2	21.4	N	Y	W
	Cu(maleate)	2	63.7	N	N	N
	Cu(succinate)	2	25.2	N	Y	N
	Cu(phthalate)	2	35.2	N	Y	N
	Cu(8-quinolinol)	2	34.8	N	Y	N
	Cu(EDTA)	2	85.8	N	Y	N

The strength of the effects are indicated by Y = yes, W = weak and N = no.

cated by spraying identical quantities of methanol solutions of CuCl and $CuCl_2$ onto dry etched CdTe, heating at 200 °C for 20 min, then applying graphite contacts. Devices prepared with Cu(I) salt exhibit 50 mV higher V_{oc} and higher FF than devices prepared with Cu(II) salt. Furthermore, no crossover was found between light and dark curves for devices prepared with Cu(I), indicating superposition of the dark diode characteristic. GIXRD analysis of the samples of Fig. 12 show Cu_2Te phase for the sample prepared with CuCl, Cu(I), and CuTe phase for the sample prepared with $CuCl_2$, Cu(II). Thus, solutions of Cu(I) salts seem preferrable, though solutions containing simple dehydrated Cu(II) salts can produce reasonable devices. For application of Cu(I) salts, dry non-aqueous solvents must be used as Cu(I) ions are generally unstable in aqueous conditions. After delivery of the Cu salt, the samples require annealing to promote reaction with Te, which can be carried out before or after application of the secondary contact.

5.4. Other back contacts

A number of other, "Cu-free", back contact materials, deposited by various methods, have been evaluated for CdTe devices e.g. including vacuum evaporated ZnTe and Sb_2Te_3, and solution deposited metals and $NiTe_2$ (Dobson et al., 2000). Generally, these contacts have not been superior to Cu-based contacts, or not as simple to process as some of the Cu-based options. The unexpected Cu contamination in some "Cu-free" cell processes may also have led to reported high device efficiencies (Durose et al., 2002). The success of Cu-based contacts, the simplicity of Cu application, and the difficulty in avoiding copper contamination in CdTe, CdS and back contacts, indicate that Cu containing contacts are yet a worthwhile R&D challenge for future successful device and module processing. However, this will require thorough understanding and control of the chemistry of Cu throughout the device structure, both during processing and post-fabrication, operational stresses.

5.5. Back contact anneal

Annealing of devices following Cu application is almost always required to produce the desired $Cu_{2-x}Te$ back contact (McCandless et al., 1998). Most back contact anneals are carried out at 150–250 °C for times of ~20–60 min. Annealing should always be carried out in a dry, inert atmosphere or under vacuum to avoid oxidation. Thin Cu films, Cu(I) ions and Te are susceptible to reaction with O_2 and water vapor, producing stable and insulating oxides.

The reaction between Cu metal and elemental Te is spontaneous, but heating is required to ensure this reaction goes to completion, or to force the reaction of Cu ions/salts with Te. Previously we showed the formation of $Cu_{2-x}Te$ on devices with back contacts formed by deposition and annealing of stoichiometric Cu and Te layers on CdTe (McCandless et al., 1998). Interestingly, the transformation of $Cu_{2-x}Te$ to CuTe with device stressing has been observed, linking chemical changes in the back contact with device degradation (Hegedus et al., 2000). Literature on the electrical properties of the Cu–Te compounds is sparse; and we speculate that the difference in electrical properties of CuTe and $Cu_{2-x}Te$ account for the increased R_{oc} and forward bias rollover observed for stressed devices. In comparative studies we have found that the CuTe phase dominates contacts formed by application of Cu powder/graphite pastes to NP and BM etched CdTe surfaces (Fig. 13). The difference in phases observed between the paste contact and stoichiometrically deposited metallic films is accounted for by excess surface Te and slow Cu delivery from the graphite paste. This observation highlights that CuTe may be a reasonable back contact, though likely poorer than $Cu_{2-x}Te$.

Significant diffusion of Cu throughout the cell structure occurs during the back contact anneal, which leads to an increase in accumulated Cu at the junction/CdS region of the device (Dobson et al., 2000). In addition, untreated CdTe/CdS structures, without purposefully added Cu, already contain significant Cu levels in the CdTe and CdS layers (Durose et al., 2002). With contacting and subsequent thermal stressing, the level of Cu increases in both CdTe and CdS layers (Asher et al., 2000), which reduces junction quality, manifested by a loss in V_{oc} and FF. We have carried out controlled experiments in which Cu was introduced to the device structure as a thin metal film between the CdS and CdTe and also between the CdS and the TCO. These devices exhibited markedly lower V_{oc} and FF than control

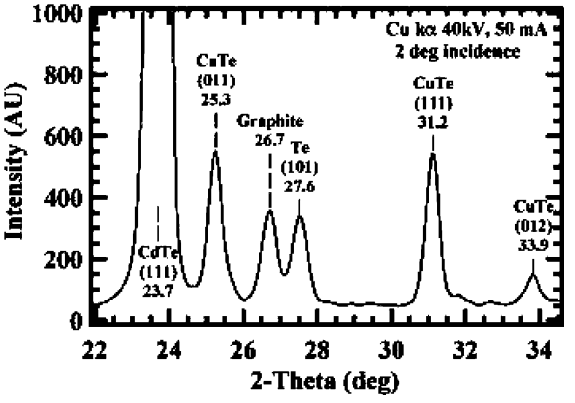

Fig. 13. GIXRD pattern taken at 2° incidence, of a 60 s NP etched CdTe film, following removal of a Cu powder/graphite paste contact.

devices, with the CdS exhibiting photoconductivity which was evident in short wavelength QE (Hegedus et al., 2003).

5.6. Secondary contacts and device completion

The secondary contact is the robust current-carrying contact. The most common secondary contacts are metal films or graphite paste. For back contacts produced from Cu-containing pastes, the graphite layer acts as both the Cu source and secondary contact. The secondary contact also protects the back contact from mechanical abrasion and from the atmosphere. Graphite paste, for example, will immediately seal the surface, preventing contact with the atmosphere, and should be applied immediately following etching or application of Cu. Following annealing, the dried graphite paste will be somewhat permeable to the atmosphere, however, both the thickness (~100 μm) and the gettering properties of the graphite may indeed provide some additional protection to the back contact from O_2 and water vapor over contacts made with thin metal films. The secondary contacts have been shown to influence device performance and stability (Hegedus et al., 2001).

Completion of devices requires isolation of the cells by scribing and metallization of the front contact. The secondary contacts should be isolated, by scribing, to prevent current collection outside the back contact area. The front contact is generally completed by application of In or other metal solders or metal pastes/paints to exposed CdS or TCO.

5.7. Contact stability

Thermal stressing in air of devices contacted with Cu-doped graphite has shown increased performance degradation compared to devices thermally stressed in dry inert atmospheres, though no difference in the rate of Cu diffusion through the devices was observed (Visoly-Fisher et al., 2003). This reinforces the concept that chemistry changes in the back contact region primarily dominate device stability and that it is critical to protect the back contact from the atmosphere during processing and stress. While modules in the field will be encapsulated from the atmosphere, effects of exposure to the atmosphere during processing or effects on device performance if encapsulation failure occurs, need to be understood.

We have recently shown Cu-based contacts that are less susceptible to atmospheric effects. A series of devices processed at IEC and other sources were stressed for an extensive period of time in the dark at 80 °C in atmospheres of varying humidity levels. Devices contacted with Cu/Au films deposited on a thick, ~100 nm, Te film, produced by a BDH etching followed by Te evaporation, showed significant chemistry occurring during stress, e.g. formation of TeO_2 at low humidity and hydroxides/hydrated oxide phases at high humidity. However, very little change in device performance was noted. Other devices, processed with very thin Te layers, while exhibiting good initial performance (>10%), showed significant degradation after 80 °C thermal stress. These results suggest that thick Te may make back contacts more robust towards chemical changes and atmospheric oxidation. Due to the chemical affinity of Te for Cu, a thick Te film is also expected to attenuate Cu diffusion through the device by gettering Cu at the back of the device and thus maintaining the favorable back contact for a longer period. This was also confirmed by stress testing of devices with varying back contact Te thicknesses, processed by NP etches of different times and completed with graphite paste containing 6% Cu powder (Dobson et al., 2003). Initial efficiencies of all devices were similar, however, after stressing for ~50 days at 80 °C in the dark, the devices with thinner Te, or shorter etch times, exhibited back contact degradation as evidenced increased R_{oc}, while the devices with thicker Te contacts showed almost no loss of performance. Thick Te-based contacts contribute to device robustness and may lengthen device lifetime.

6. Conclusions

Processing options which address a number of critical issues relating to processing of thin-film CdTe/CdS devices have been discussed. The window layer properties, including configuration, composition and thickness have been shown to have a significant effect on final device performance. Engineering and chemical aspects of the post-deposition $CdCl_2$ treatment of CdTe were presented. Annealing CdTe films in the presence of $CdCl_2$ and O_2 promotes CdS diffusion into CdTe and also shifts the chemical equilibrium of the film surface, which may influence the bulk electrical properties of the CdTe. Comparisons of wet and vapor $CdCl_2$ treatment were discussed including the development of a packed bed reactor for vapor $CdCl_2$ treatments. High device performance and good spatial uniformity were achieved with vapor $CdCl_2$ treatment. Careful control of the O_2 and humidity in the anneal atmosphere is required to avoid the formation of deleterious oxides, which will affect the Cd-vacancy concentration within the CdTe film, leading to poor device performance.

A number of steps are required for successful processing of back contacts to CdTe; the formation of a Te-rich surface, application of a Cu source, contact annealing and deposition of a secondary contact. A number of methods can be used for each of these steps. Consideration of different processes should include simplicity and ease of industrial scale up. The nature of each process may also be critical for contact and device

stability. A thorough knowledge of etching mechanics and surface chemistry will allow the development of alternate or modified etches that may be more efficient and faster, perhaps through the use of catalysts, and safer to use, all of which can only assist possible industrial scale-up of the technology. The results obtained from monitoring the etching processes have also highlighted the usefulness of VASE and GIXRD as diagnostic tools for monitoring the quality of material surfaces during processing.

The Te rich surface can be formed by wet chemical etching or by 'dry' deposition of Te, however, application of Cu should be carried out immediately, to prevent atmospheric oxidation of the Te-rich surface. A number of simple methods of Cu application are available. Contact annealing should be carried out in an inert atmosphere to avoid oxidizing the back contact. A full understanding of the role of Cu and other possible contact metals in the back contact chemistry and their behavior within the CdTe/CdS structure is required before optimization of device performance and stability can be obtained.

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