NVIDIA Jetson Nano

Product Design Guide

全是 Table 和 GPIO，似乎是为硬件的，为了把 Nano 作为 MCU 的，不用看

Document History

DG-09502-001_v2.4

Version	Date	Description of Change
1.0	June 7, 2019	Initial Release
2.0	March 2, 2020	• Added MPIO pad code and POR columns to the pin description tables through the design guide • Added chapter on modular connector (Chapter 3) • Updated power down figures (Figure 4-4 and Figure 4-5) • Updated Figure 5-1 to show details of FET used as level shifter for VBUS Detect to show it is inverted. • Corrected USB2 module pin numbers in Figure 5-1 • Corrected PCIE0_TX3/RX0 pin numbers in Figure 5-7 • Updated the notes to the PCIe signal routing requirements table (Table 5-9) • Updated Gigabit Ethernet controller in Section 5.3 • Updated Figure 7-1 to "4 Lanes…"
2.1	July 1, 2020	• Added Chapter 3 "Developer Kit Feature Considerations" • Updated notes for all pin description tables • Corrected module pin numbers in Figure 7-2 • Updated Table 9-1 include both 1.8V and 3.3V pins, since the pins are associated with a rail that may be set to one or the other voltage • Updated Figure 9-1 to change SDMMC_SD to connect to generic GPIO • Removed GPIO08 for SD Card Detect from Table 9-3 since figure shows generic GPIO • Updated Table 11-6 to mention buffer on module • The Jetson Nano pin description and design checklist are now attachments to this design guide
2.2	November 4, 2020	• Updated USB SS hub design with public part number • Added notes to Figure 6-7 related to AC cap requirements SoC RX lines and to clarify PCIe clock output and RX/TX signaling type • Added notes to Figure 9-1 requiring SD card supply to be controlled by GPIO and recommendation to have SD card supply be current limited • Updated the audio codec connection example figure and added notes (Figure 10-1) • Added Section 11.6 on USB recovery mode

Version	Date	Description of Change
2.3	February 23, 2022	General • Removed MPIO Code & Power-on Reset columns from Pin Desc. Power • Updated SHUTDOWN_REQ* Usage/Desc. in Power and System Pin Descriptions table. • Added note related to use eFUSE or current limiting devices • Updated power control signal descriptions for SHUTDOWN_REQ* and POWER_EN • Added warning note related to carrier board driving signals before SYS_RESET* goes high • Added delay requirement between VDD_IN and POWER_EN • Updated power sequence figures Other • Added USB SS and Wireless Coexistence section • Added test points for high-speed interfaces section
2.4	October 20, 2022	• Chapter 1 Intro: Added notes related to USB 3.2 and updated design guide to use USB 3.2 throughout • Chapter 1 Intro: Added note related to replacing "master" and "slatve" terminology and updated throughout design guide • Table 5-1 and Section 5.1.2: Corrected module name. • Section 5.1.1: Added additional description for SHUTDOWN_REQ* • Section 6.1: Updated text with details of USB host/device support. • Section 6.2: Added text related to PCIe polarity inversion support • Figure 10-2: Corrected I2C pull-up voltage in note 2 under figure. • Table 13-1: Removed SYS_RESET* • Sections 16.1, 16.2, 16.3, and 16.4: Updated text to use mm instead of in/mils and updated some signal related text.

Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

This design guide contains recommendations and guidelines for engineers to follow in creating a product that is optimized to achieve the best performance from the interfaces supported by the NVIDIA® Jetson Nano™ System-on-Module (SOM).

This design guide provides detailed information on the capabilities of the hardware module, which may differ from supported configurations by provided software. Refer to software release documentation for information on supported capabilities.

> **Note**:
>
> - Most of the interface usage noted in this design guide is based on the NVIDIA developer kit carrier board design.
> - All occurrences of USB 3.2 refer to USB 3.2 Gen 1x1: SuperSpeed USB 5 Gbps only.

> **IMPORTANT**: Throughout the design guide, references to "master" and "slave" configurations have been updated to "initiator" and "target" respectively.

1.1 References

Refer to the following list of documents or models for more information. Always use the latest revision of all documents.

- *Jetson Nano Module Data Sheet*
- *Tegra X1 (SoC) Technical Reference Manual*
- *Jetson Nano Developer Kit Carrier Board Specification*
- *Jetson Nano Module Pinmux*
- *Jetson Nano Thermal Design Guide*
- *Jetson Nano Developer Kit Carrier Board Design Files*
- *Jetson Nano Developer Kit Carrier Board BOM*
- *Jetson Nano SCL (Supported Component List)*

1.2 Abbreviations and Definitions

Table 1-1 lists abbreviations that may be used throughout this document and their definitions.

Table 1-1. Abbreviations and Definitions

Abbreviation	Definition
CEC	Consumer Electronic Control
CSI	Camera Serial Interface
Diff	Differential
DP	VESA® DisplayPort™ (output)
DSI	Display Serial Interface
eDP	Embedded DisplayPort
ESD	Electrostatic Discharge
eMMC	Embedded MMC
EMI	Electromagnetic Interference
FET	Field Effect Transistor
GPIO	General Purpose Input Output
HDCP	High-bandwidth Digital Content Protection
HDMI™	High Definition Multimedia Interface
I2C	Inter IC Interface
I2S	Inter IC Sound Interface
LCD	Liquid Crystal Display
LDO	Low Dropout (voltage regulator)
LPDDR4	Low Power Double Data Rate DRAM, Fourth generation
MDI	Medium-Dependent Interface
MIL	1/1000th of an inch
MIPI	Mobile Industry Processor Interface
mm	Millimeter
PCIe	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
PHY	Physical Interface (i.e. USB PHY)
ps	Pico-Seconds
PMU	Power Management Unit
RJ45	8P8C modular connector used in Ethernet and other data links
RTC	Real Time Clock

Abbreviation	Definition
SD Card	Secure Digital Card
SDIO	Secure Digital I/O Interface
SE	Single-Ended
SPI	Serial Peripheral Interface
TMDS	Transition-minimized differential signaling
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

Chapter 2. Jetson Nano

The Jetson Nano resides at the center of the embedded system solution and includes the following:

- Power (PMIC/Regulators, etc.)
- DRAM (LPDDR4)
- eMMC
- Gigabit Ethernet Controller
- Power Monitor

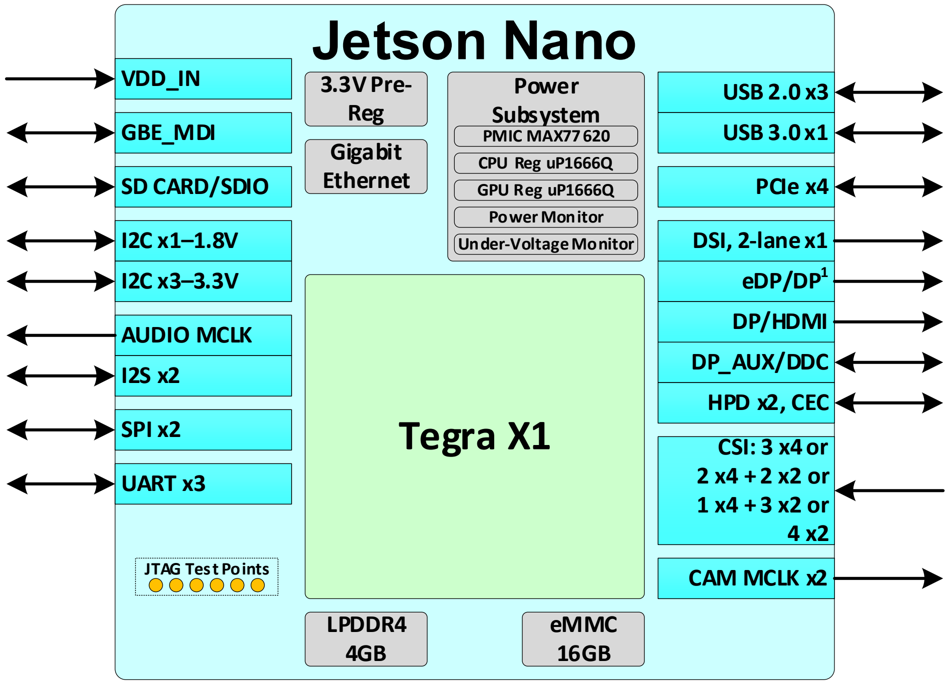
In addition, a wide range of interfaces are available at the main connector for use on the carrier board as shown Table 2-1 and Figure 2-1.

Table 2-1. Jetson Nano Interfaces

Category	Function	Category	Function
USB	USB 2.0 Interface (3x)	LAN	Gigabit Ethernet
	USB 3.2 (1x)	I2C	4x
PCIe	PCIe (x1/2/4)	UART	3x
Camera	CSI (3 x4 or 2 x4 + 2 x2 or 1 x4 + 3 x2), Control, Clock	SPI	2x
Display	eDP/DP (see Note 1)	Wi-Fi/BT/Modem	PCIe/UART/I2S, Control/handshake
	HDMI/DP Interface (w/CEC)	Fan	FAN PWM and Tach Input
	DSI (1, 2-lane), Display/Backlight Control	Debug	JTAG test points on module and UART
Audio	I2S Interface (2x) and Clock	System	Power Control, Reset, alerts
SD Card/SDIO	SD Card or SDIO Interface (1x)	Power	Main Input and battery back-up for RTC

Note: DP on eDP interface does not support HDCP or Audio

Figure 2-1. Jetson Nano Block Diagram



Note:

[1]DP on eDP interface does not support HDCP or Audio

Table 2-2 lists the 260-pin SO-DIM description for the Jetson Nano connector.

Table 2-2. Jetson Nano Connector Pinout Matrix

Module Signal Name	Pin #		Pin #	Module Signal Name
GND	1		2	GND
CSI1_D0_N	3		4	CSI0_D0_N
CSI1_D0_P	5		6	CSI0_D0_P
GND	7		8	GND
RSVD	9		10	CSI0_CLK_N
RSVD	11		12	CSI0_CLK_P
GND	13		14	GND
CSI1_D1_N	15		16	CSI0_D1_N
CSI1_D1_P	17		18	CSI0_D1_P
GND	19		20	GND
CSI3_D0_N	21		22	CSI2_D0_N
CSI3_D0_P	23		24	CSI2_D0_P
GND	25		26	GND
CSI3_CLK_N	27		28	CSI2_CLK_N
CSI3_CLK_P	29		30	CSI2_CLK_P
GND	31		32	GND

Module Signal Name	Pin #		Pin #	Module Signal Name
PCIE0_RX0_P	133		134	PCIE0_TX0_N
GND	135		136	PCIE0_TX0_P
PCIE0_RX1_N	137		138	GND
PCIE0_RX1_P	139		140	PCIE0_TX1_N
GND	141		142	PCIE0_TX1_P
RSVD	143		144	GND
KEY	KEY		KEY	KEY
RSVD	145		146	GND
GND	147		148	PCIE0_TX2_N
PCIE0_RX2_N	149		150	PCIE0_TX2_P
PCIE0_RX2_P	151		152	GND
GND	153		154	PCIE0_TX3_N
PCIE0_RX3_N	155		156	PCIE0_TX3_P
PCIE0_RX3_P	157		158	GND
GND	159		160	PCIE0_CLK_N
USBSS_RX_N	161		162	PCIE0_CLK_P

Module Signal Name	Pin #		Pin #	Module Signal Name
CSI3_D1_N	33		34	CSI2_D1_N
CSI3_D1_P	35		36	CSI2_D1_P
GND	37		38	GND
DP0_TXD0_N	39		40	CSI4_D2_N
DP0_TXD0_P	41		42	CSI4_D2_P
GND	43		44	GND
DP0_TXD1_N	45		46	CSI4_D0_N
DP0_TXD1_P	47		48	CSI4_D0_P
GND	49		50	GND
DP0_TXD2_N	51		52	CSI4_CLK_N
DP0_TXD2_P	53		54	CSI4_CLK_P
GND	55		56	GND
DP0_TXD3_N	57		58	CSI4_D1_N
DP0_TXD3_P	59		60	CSI4_D1_P
GND	61		62	GND
DP1_TXD0_N	63		64	CSI4_D3_N
DP1_TXD0_P	65		66	CSI4_D3_P
GND	67		68	GND
DP1_TXD1_N	69		70	DSI_D0_N
DP1_TXD1_P	71		72	DSI_D0_P
GND	73		74	GND
DP1_TXD2_N	75		76	DSI_CLK_N
DP1_TXD2_P	77		78	DSI_CLK_P
GND	79		80	GND
DP1_TXD3_N	81		82	DSI_D1_N
DP1_TXD3_P	83		84	DSI_D1_P
GND	85		86	GND
GPIO00	87		88	DP0_HPD
SPI0_MOSI	89		90	DP0_AUX_N
SPI0_SCK	91		92	DP0_AUX_P
SPI0_MISO	93		94	HDMI_CEC
SPI0_CS0*	95		96	DP1_HPD
SPI0_CS1*	97		98	DP1_AUX_N
UART0_TXD	99		100	DP1_AUX_P
UART0_RXD	101		102	GND
UART0_RTS*	103		104	SPI1_MOSI
UART0_CTS*	105		106	SPI1_SCK
GND	107		108	SPI1_MISO
USB0_D_N	109		110	SPI1_CS0*
USB0_D_P	111		112	SPI1_CS1*
GND	113		114	CAM0_PWDN
USB1_D_N	115		116	CAM0_MCLK
USB1_D_P	117		118	GPIO01
GND	119		120	CAM1_PWDN
USB2_D_N	121		122	CAM1_MCLK
USB2_D_P	123		124	GPIO02
GND	125		126	GPIO03
GPIO04	127		128	GPIO05
GND	129		130	GPIO06
PCIE0_RX0_N	131		132	GND

Module Signal Name	Pin #		Pin #	Module Signal Name
USBSS_RX_P	163		164	GND
GND	165		166	USBSS_TX_N
RSVD	167		168	USBSS_TX_P
RSVD	169		170	GND
GND	171		172	RSVD
RSVD	173		174	RSVD
RSVD	175		176	GND
GND	177		178	MOD_SLEEP*
PCIE_WAKE*	179		180	PCIE0_CLKREQ*
PCIE0_RST*	181		182	RSVD
RSVD	183		184	GBE_MDI0_N
I2C0_SCL	185		186	GBE_MDI0_P
I2C0_SDA	187		188	GBE_LED_LINK
I2C1_SCL	189		190	GBE_MDI1_N
I2C1_SDA	191		192	GBE_MDI1_P
I2S0_DOUT	193		194	GBE_LED_ACT
I2S0_DIN	195		196	GBE_MDI2_N
I2S0_FS	197		198	GBE_MDI2_P
I2S0_SCLK	199		200	GND
GND	201		202	GBE_MDI3_N
UART1_TXD	203		204	GBE_MDI3_P
UART1_RXD	205		206	GPIO07
UART1_RTS*	207		208	GPIO08
UART1_CTS*	209		210	CLK_32K_OUT
GPIO09	211		212	GPIO10
CAM_I2C_SCL	213		214	FORCE_RECOVERY*
CAM_I2C_SDA	215		216	GPIO11
GND	217		218	GPIO12
SDMMC_DAT0	219		220	I2S1_DOUT
SDMMC_DAT1	221		222	I2S1_DIN
SDMMC_DAT2	223		224	I2S1_FS
SDMMC_DAT3	225		226	I2S1_SCLK
SDMMC_CMD	227		228	GPIO13
SDMMC_CLK	229		230	GPIO14
GND	231		232	I2C2_SCL
SHUTDOWN_REQ*	233		234	I2C2_SDA
PMIC_BBAT	235		236	UART2_TXD
POWER_EN	237		238	UART2_RXD
SYS_RESET*	239		240	SLEEP/WAKE*
GND	241		242	GND
GND	243		244	GND
GND	245		246	GND
GND	247		248	GND
GND	249		250	GND
VDD_IN	251		252	VDD_IN
VDD_IN	253		254	VDD_IN
VDD_IN	255		256	VDD_IN
VDD_IN	257		258	VDD_IN
VDD_IN	259		260	VDD_IN

Legend	Ground	Power	Reserved - must be left unconnected

Chapter 3. Developer Kit Feature Considerations

The Jetson Nano Developer Kit Carrier Board design files are provided as a reference design. This chapter describes details necessary for designers to know to replicate certain features if desired. In addition, aspects of the design that are specific to the NVIDIA Developer Kit usage but not useful or supported on a custom carrier board are also identified.

Most of the features implemented on the Jetson Nano Developer Kit carrier board design can be duplicated by copying the connections from the P3449 carrier board reference design. The Some features have aspects that would require additional information as listed

- USB SuperSpeed Hub
- Power over Ethernet (PoE)
- TI TXB0108 level shifters
- ID EEPROM (Not to be copied from reference design)

3.1 USB SuperSpeed Hub

The USB 3.2 hub design uses a Realtek RTS5411-GRT device. The hub device has been customized using internal fuses with the Realtek tool. A design intending to duplicate the developer kit hub implementation should customize the hub as follows:

- Power enables (DPS1/2/3/4_PWR) set to be active high
- Charging feature disabled
- SSC valid

3.2 Power Over Ethernet (PoE)

The P3449 carrier board includes a 4-pin Power over Ethernet (PoE) header (J38) which brings out the VC power pins of the Ethernet connector. To use this alternate PoE power mechanism to power the carrier board, the design would require a power converter to take the high voltage PoE supply (38V-60V) and convert it to the correct voltage for the custom carrier board. This could be the 5V that the Jetson Nano Developer Kit uses, or a different voltage depending on the design of the custom carrier board.

3.3 TI TXB0108 Level Shifters

The P3449 carrier board uses these level shifters to shift many of the signals going to the 40-pin header from 1.8V to 3.3V. The design of these level shifters supports bidirectional signaling without the use of a direction signal but has some side effects that should be considered. See the *Jetson Nano Developer Kit 40-Pin Expansion Header GPIO Usage Considerations Applications Note* for details.

3.4 Features Not to be Implemented

The Jetson Nano Developer Kit carrier board features that should not be copied as they are not required or useful for a custom carrier board design. The ID EEPROM (P3449 - U11) is a feature that is used for NVIDIA internal purposes, but not useful on a custom design. A similar function may be desired for a custom design, but the NVIDIA software will not interact with these devices and the I2C address used by the developer kit carrier board ID EEPROM on the I2C2 interface (7'h57) should be avoided.

Chapter 4. Modular Connector

4.1 Module Connector Details

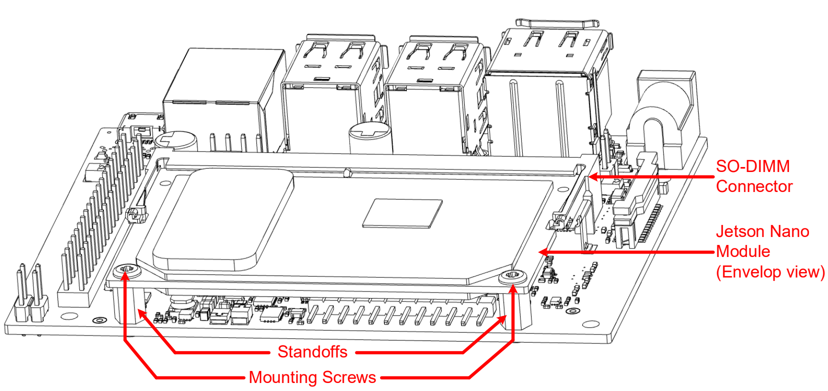
Jetson Nano modules connect to the carrier board using a 260-pin SO-DIMM connector. The mating connector used on the Developer Kit carrier board is listed in the Jetson Nano SCL (Supported Components List). This connector is a DDR4 SODIMM, 260-pin, right-angle, standard key type. The full height of the connector is 9.2 mm. Refer to the Connector specification for details. Other heights are available.

4.2 Module to Mounting Hardware

The Jetson Nano module is installed in the SODIMM connector which has latching mechanisms to hold the board in place. In addition, it is required that the module is mounted to the main carrier board PCB using metal standoffs and screws (or equivalent), both for mechanical integrity and to provide additional grounding points. The Developer Kit uses threaded standoffs that are hex, 4.5 mm widths (narrow diameter) x 6.57 ± 0.1 mm length. These have M.2.5 threads. The screws used are M2.5 x 3.7 mm, pad head.

Other SODIMM connector heights are available. If a different height connector is used, the standoff height will have to be adjusted accordingly to account for the difference in height from main PCB to module PCB.

Figure 4-1. Jetson Nano Module Installed in SODIMM Connector



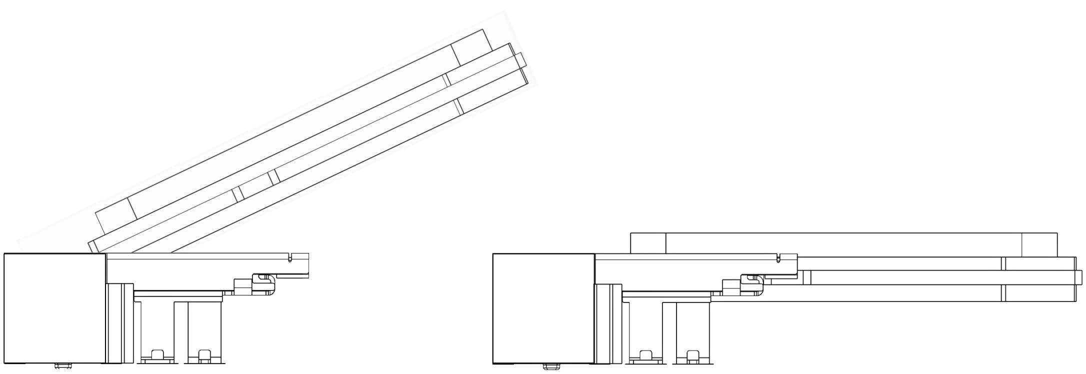
4.3 Module Installation and Removal

To install the Jetson Nano module correctly, follow the sequence and mounting hardware instructions:

Here are some suggested assembly guidelines.

1. Assemble any required thermal solution on the module.
2. Install the Jetson Nano module
   a) Baseboard with suitable standoff for as per SODIMM connector height defined
   b) Insert module fully at an angle of 25-35 degree into the SODIMM connector.
   c) Arc down the module board until the SODIMM connector latch engages.
   d) Secure the Jetson Nano module to the baseboard with screws into the standoff/spacer. The developer kit (shown in Figure 4-2) uses a standoff and screws to secure the module to the system/base- board.

Figure 4-2. Module to Connector Assembly Diagram



To remove the Jetson Nano module correctly, follow the reverse of the installation sequence.

Chapter 5. Power

Power for the module is supplied on the **VDD_IN** pins and is nominally 5.0V (see the *Jetson Nano Data Sheet* for supply tolerance and maximum current).

> **CAUTION:** Jetson Nano is not hot-pluggable. When installing the module, the main power supply should not be connected. Before removing the module, the main power supply (to **VDD_IN** pins) must be disconnected and allowed to discharge below 0.6V.

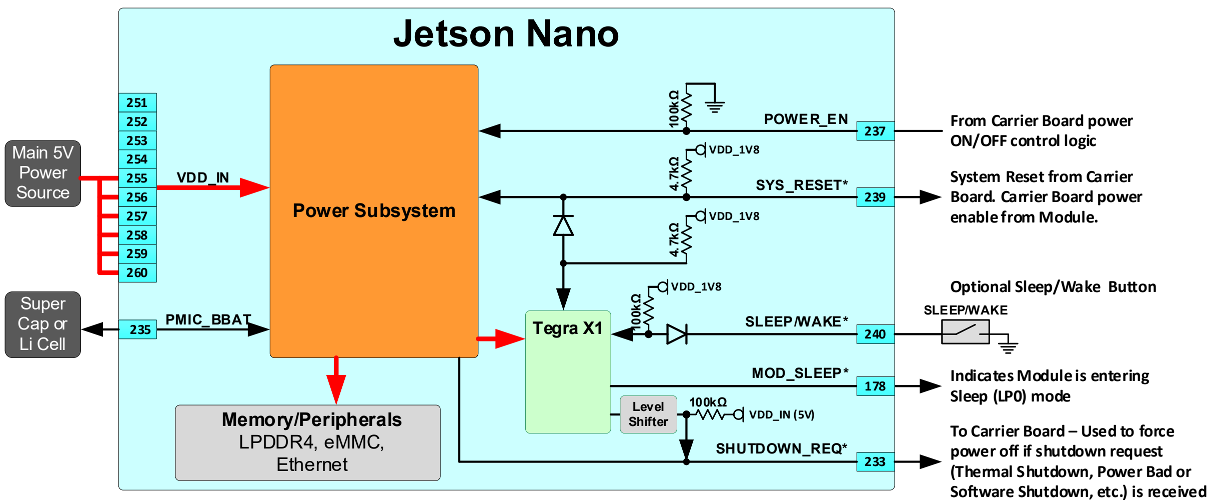
Table 5-1. Power and System Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
251 ↓ 260	VDD_IN	–	Main power – Supplies PMIC and other regulators	Main DC input	Input	5.0V
235	PMIC_BBAT	–	PMIC Battery Back-up. Optionally used to provide back-up power for the Real-Time-Clock (RTC). Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is source when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Battery Back-up using Super-capacitor	Bidir	1.65V-5.5V
214	FORCE_ RECOVERY*	BUTTON_VOL_UP	Force Recovery strap pin. Held low when SYS_RESET* goes high (i.e. during power-on) places system in USB recovery mode.	Automation header	Input	CMOS – 1.8V
240	SLEEP/WAKE*	BUTTON_PWR_ON	Sleep/Wake. Configured as GPIO for optional use to indicate the system should enter or exit sleep mode.	Automation header	Input	CMOS – 5.0V
233	SHUTDOWN_ REQ*	–	When driven/pulled low by the module, requests the carrier board to shut down. ~5kΩ pull-up to VDD_IN (5V) on the module.	System	Output	Open Drain, 5.0V
237	POWER_EN	(PMIC EN0 through converter logic)	Signal for module on/off: high level on, low level off. Connects to module PMIC EN0 through converter logic. POWER_EN is routed to a Schmitt trigger buffer on the module. A 100kΩ pulldown is also on the module.	System	Input	Analog 5.0V
239	SYS_RESET*	SYS_RESET_IN_N	Module Reset. Reset to the module when driven low by the carrier board. Used as carrier board supply enable when driven high by the module when module power sequence is complete. Used to ensure proper power on/off sequencing for between module and carrier board supplies. 4.7kΩ pull-up to 1.8V on the module.	Automation header	Bidir	Open Drain, 1.8V

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
178	MOD_SLEEP*	GPIO_PA6	Indicates the module sleep status. Low is in sleep mode, high is normal operation. This pin is controlled by system software and should not be modified.	HDMI termination pull-down FET control disable	Output	CMOS – 1.8V

Notes:
1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The directions for FORCE_RECOVERY* and SLEEP/WAKE* signals are true when used for those functions. Otherwise as GPIOs, the direction is bidirectional.

Figure 5-1. Jetson Nano Power and Control Block Diagram



5.1 Power Supply and Sequencing

This section details the power supply and sequencing for the Jetson Nano module.

5.1.1 Power Handshake Signals

The carrier board receives the main power source and uses this to generate the enable to Jetson Nano (**POWER_EN**) after the carrier board has ensured the main supply is stable and the associated decoupling capacitors have charged. The carrier board supplies are not enabled at this time. Once **POWER_EN** is driven active (high), the module begins to Power-ON. When the module Power-ON sequence has completed, the **SYS_RESET*** signal is released (pulled high on module) and this is used by the carrier board to enable its various supplies.

> **Note**: The carrier board cannot drive high or pull high any signals that are associated with the module when the module rails are off. If the designer cannot guarantee a signal will not be driven or pulled high, then either the power rail related to that signal should be left off, or the signals would need to be buffered to isolate them from the module pins. The buffers should only be enabled towards the module when SYS_RESET* goes high.

POWER_EN

- **POWER_EN** is a level active signal. When high, the system powers on or stays on. When low, the system powers down or stays off. A minimum delay of 400ms is required between VDD_IN valid to **POWER_EN** active.

SYS_RESET*

- **SYS_RESET*** is bidirectional. The signal is controlled by the PMIC during power-on and power-off. When the system is powered on, **SYS_RESET*** can be driven by the carrier board to reset the module. This results in a full system power cycle.
- The **SYS_RESET*** signal is asserted by the PMIC during power-on.
- **SYS_RESET*** is not asserted externally during the power-down sequence. When **POWER_EN** is de-asserted, the PMIC performs a power down sequence that includes asserting **SYS_RESET***.

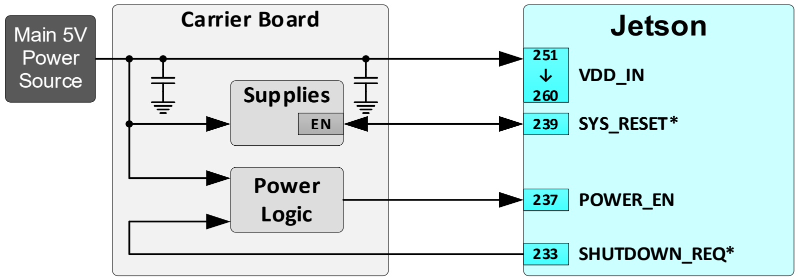
SHUTDOWN_REQ*

- **SHUTDOWN_REQ*** is driven active (low) by the module if the system must be shut down, due to a software shutdown request, over-temperature event, undervoltage event, or other faults. The power control logic on the carrier board must drive **POWER_EN** inactive (low) if **SHUTDOWN_REQ*** is asserted.
- **SHUTDOWN_REQ*** is not driven during power-on. It is pulled up to the 5V supply, so stays inactive. If the system is on and reset is driven low, the PMIC will initiate a full power cycle and start the power-on sequence. Again, **SHUTDOWN_REQ*** is not asserted. **SHUTDOWN_REQ*** will only go low when the system needs to shut down.
- **SHUTDOWN_REQ*** comes from a latch on module and is cleared when **POWER_EN** goes low.
- If **SHUTDOWN_REQ*** is asserted, the carrier board must de-assert **POWER_EN** as soon as possible. One reason for this is to give the system enough time to do a correct power down sequence in the case of a sudden power loss case. In this case, once the 5V supply drops to ~4.2V, the on-module **VIN_PWR_BAD_N** signal is asserted which results in **SHUTDOWN_REQ*** being asserted. The PMIC then starts the power down sequence, which takes ~4 to 5 ms. The sequence must finish before the input voltage drops below 3.0V to correctly power off the module.

Power Rail Discharge

- To satisfy the power down sequencing requirement and prevent unwanted back drive from the carrier board to the module, the following must be true:
- The carrier board 3.3V power supply that powers any module I/O must be off within 1.5 ms of **SYS_RESET*** assertion.
- The 1.8V power supply that powers any module I/O must be off within 4 ms.
- The power rails should be fully discharged before attempting to power back up.

Figure 5-2. System Power and Control Block Diagram



Note: Designs which implement an eFUSE or current limiting device on the input power rail of the module should select a part that DOES NOT limit reverse current.

5.1.2 Power Sequencing

The following figures show the power sequencing for the Jetson Nano module.

Figure 5-3. Power Up Sequence No Power Button – Auto Power-On

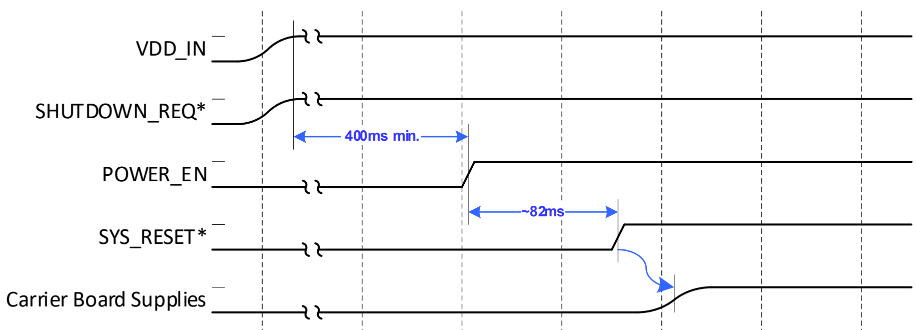


Figure 5-4. Power Up Sequence with Power Button

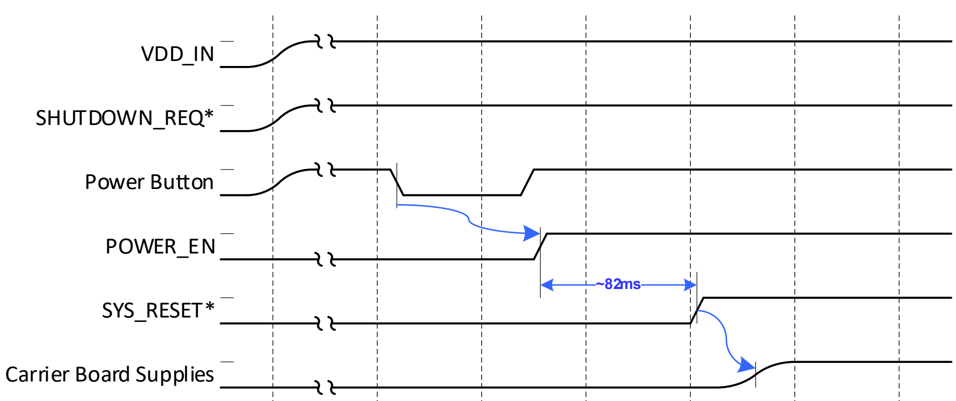


Figure 5-5. Power Down – Initiated by SHUTDOWN_REQ* Assertion

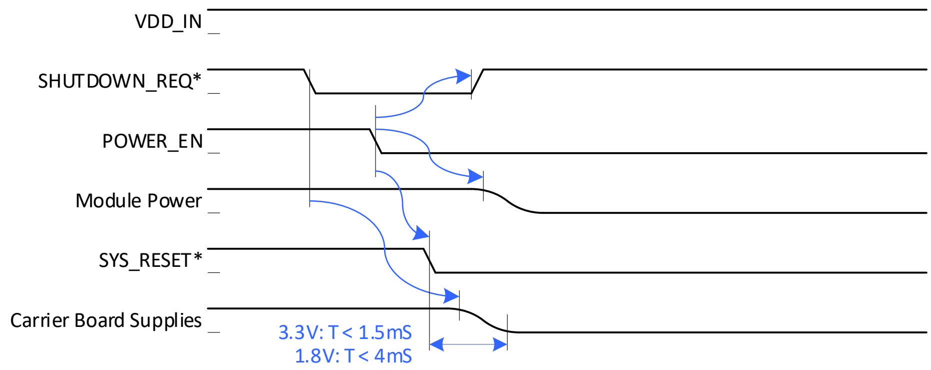
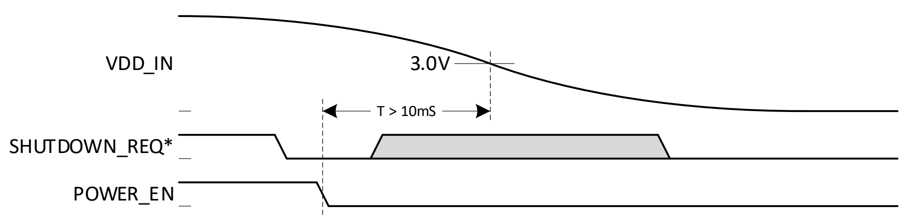


Figure 5-6. Power Down – Sudden Power Loss



Note: SHUTDOWN_REQ* must always be serviced by the carrier board to toggle POWER_EN from high to low, even in cases of sudden power loss.

Chapter 6. USB and PCI Express

Jetson Nano allows multiple USB 2.0, USB 3.2 and PCIe interfaces to be brought out of the module.

Table 6-1. USB 2.0 Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
87	GPIO00	USB_VBUS_EN0	GPIO #0 (USB 0 VBUS Detect)	USB 2.0 Micro B	Input	Open Drain, 1.8V
109	USB0_D_N	USB0_DN	USB 2.0 Port 0 Data	USB 2.0 Micro B	Bidir	USB PHY
111	USB0_D_P	USB0_DP				
115	USB1_D_N	USB1_DN	USB 2.0 Port 1 Data	USB Hub	Bidir	USB PHY
117	USB1_D_P	USB1_DP				
121	USB2_D_N	USB2_DN	USB 2.0, Port 2 Data	M.2 Key E	Bidir	USB PHY
123	USB2_D_P	USB2_DP				

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The direction of GPIO00 is true when used for this function. Otherwise as a GPIO, the direction is bidirectional.

Table 6-2. USB 3.2 and PCIe Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
131	PCIE0_RX0_N	PEX_RX4N	PCIe #0 Receive 0 (PCIe Ctrl #0 Lane 0)	M.2 Key E	Input	PCIe PHY
133	PCIE0_RX0_P	PEX_RX4P				
137	PCIE0_RX1_N	PEX_RX3N	PCIe #0 Receive 1 (PCIe Ctrl #0 Lane 1)	Not Assigned		
139	PCIE0_RX1_P	PEX_RX3P				
149	PCIE0_RX2_N	PEX_RX2N	PCIe #0 Receive 2 (PCIe Ctrl #0 Lane 2)			
151	PCIE0_RX2_P	PEX_RX2P				
155	PCIE0_RX3_N	PEX_RX1N	PCIe #0 Receive 3 (PCIe Ctrl #0 Lane 3)			
157	PCIE0_RX3_P	PEX_RX1P				

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
179	PCIE_WAKE*	PEX_WAKE_N	PCIe Wake. 100kΩ pull-up to 3.3V on the module.	M.2 Key E	Input	Open Drain 3.3V
181	PCIE0_RST*	PEX_L0_RST_N	PCIe #0 Reset (PCIe Ctrl #0). 4.7kΩ pull-up to 3.3V on the module.	Not Assigned	Output	Open Drain 3.3V
134	PCIE0_TX0_N	PEX_TX4N	PCIe #0 Transmit 0 (PCIe Ctrl #0 Lane 0)	M.2 Key E	Output	PCIe PHY
136	PCIE0_TX0_P	PEX_TX4P				
140	PCIE0_TX1_N	PEX_TX3N	PCIe #0 Transmit 1PCIe Ctrl #0 Lane 1)	Not Assigned		
142	PCIE0_TX1_P	PEX_TX3P				
148	PCIE0_TX2_N	PEX_TX2N	PCIe #0 Transmit 2 (PCIe Ctrl #0 Lane 2)			
150	PCIE0_TX2_P	PEX_TX2P				
154	PCIE0_TX3_N	PEX_TX1N	PCIe #0 Transmit 3 (PCIe Ctrl #0 Lane 3)			
156	PCIE0_TX3_P	PEX_TX1P				
160	PCIE0_CLK_N	PEX_CLK1N	PCIe #0 Reference Clock (PCIe Ctrl #0)	M.2 Key E	Output	PCIe PHY
162	PCIE0_CLK_P	PEX_CLK1P				
180	PCIE0_CLKREQ*	PEX_L0_ CLKREQ_N	PCIE #0 Clock Request (PCIe Ctrl #0). 47kΩ pull-up to 3.3V on the module.	Not Assigned	Bidir	Open Drain 3.3V
161	USBSS_RX_N	PEX_RX6N	USB 3.2 Receive (USB 3.2 Ctrl #0)	USB 3.2 Type A	Input	USB 3.2 PHY
163	USBSS_RX_P	PEX_RX6P				
166	USBSS_TX_N	PEX_TX6N	USB 3.2 Transmit (USB 3.2 Ctrl #0)		Output	USB 3.2 PHY
168	USBSS_TX_P	PEX_TX6P				

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The directions for PCIE_WAKE*, PCIE0_RST*, and PCIE0_CLKREQ are true when used for those functions. Otherwise as GPIOs, the direction is bidirectional.

Table 6-3 lists the mapping options for Jetson Nano.

Table 6-3. USB 3.2 and PCIe Lane Mapping Configurations

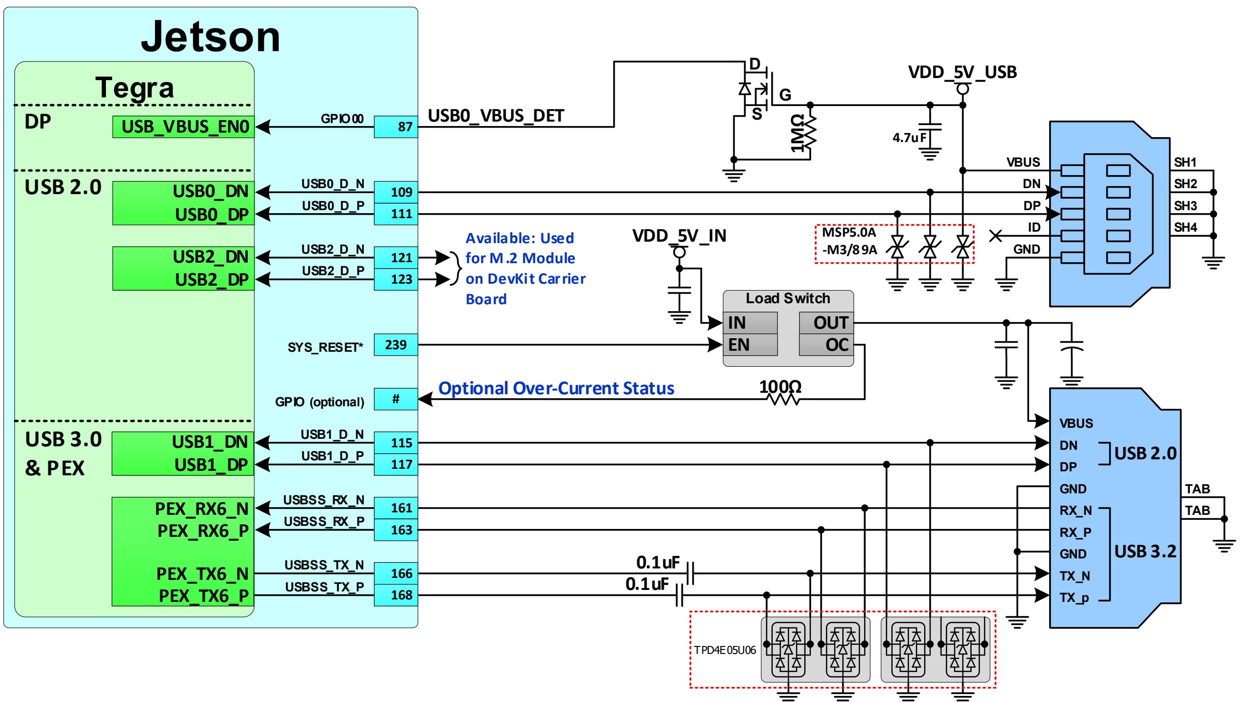
Module Pin Names		na	PCIe3	PCIe 2	PCIe 1	PCIe 0	USBSS
Tegra X1 Lanes		Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 6
USB 3.2	PCIe						
1	1x4	PCIe#1_0 - Used for Ethernet on Module	PCIe#0_3	PCIe#0_2	PCIe#0_1	PCIe#0_0	USB_SS#0
Usage on NVIDIA DevKit Carrier Board		N/A	Unused			M.2 Key E	USB Type A

6.1 USB

The USB 2.0 ports all support host mode. USB 2.0 Port 0 (USB0_D_N/P) also supports device mode (including USB Recovery Mode). The USB 3.2 port supports host mode only.

Figure 6-1 shows the USB connection example.

Figure 6-1. USB Connection Example



Notes:

1. AC capacitors should be located close to either the USB connector, or the Jetson Nano pins.
2. USB0 must be available to use as USB Device for USB Recovery Mode.
3. The load switch supplying VBUS should have over current protection. In Figure 6-1. this is supported by routing the over current (OC) pin of the load switch to the GPIO00 (USB_VBUS_EN0) which is bidirectional and can be used to detect an over current condition. Load switch can be enabled by SYS_RESET* or an available GPIO.
4. Connector used must be USB Implementers Forum certified if USB 3.2 implemented.

6.1.1 USB 2.0 Design Guidelines

These requirements apply to the USB 2.0 controller PHY interfaces: **USB[2:0]_D_N/P.**

Table 6-4. USB 2.0 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency (high speed) - Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Max loading - High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane	GND		
Trace impedance - Diff pair / SE	90 / 50	Ω	±15%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Max trace length/delay - Microstrip / Stripline	6 (960)	In (ps)	
Max intra-pair skew between USBx_D_P and USBx_D_N	7.5	ps	

Notes:
1. Up to four signal vias can share a single GND return via.
2. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

6.1.2 USB 3.2 Design Guidelines

The requirements following apply to the USB 3.2 port #0 PHY interface: **USBSS_TX_N/P, USBSS_RX_N/P**.

Table 6-5. USB 3.2 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data rate / UI period	5.0 / 200	Gbps / ps	
Max number of loads	1	load	
Termination	90 differential	Ω	On-die termination at TX and RX
Electrical Specification			
Insertion loss @ 2.5GHz Type-C Type A Resonance dip frequency	 <=2 <=7 >8	 dB dB GHz	Only PCB with add-on components (connector excluded) is considered
TDR dip	>= 75	Ω	Using TDR pulse with Tr (10%-90%) = 200ps
Near-end crosstalk (NEXT) @ DC to 5GHz	<=-45	dB	For each TX-RX NEXT
IL/NEXT plot	See Figure 6-2		
Impedance			

Parameter	Requirement	Units	Notes
Reference plane	GND		
Trace impedance - Diff pair / SE	85-90 / 45-55	Ω	±15%
Trace Spacing – for TX/RX non-interleaving			
TX-RX Xtalk is very critical in PCB trace routing. The ideal solution is to route TX and RX on different layers.			
If routing on the same layer, strongly recommend not interleaving TX and RX lanes			
If it is necessary to have interleaved routing in breakout, all the inter-pair spacing should follow the rule of inter-SNEXT			
The breakout trace width is suggested to be the minimum to increase inter-pair spacing			
Do not perform serpentine routing for intra-pair skew compensation in the breakout region			
See Figure 6-3			
Min inter-S_{NEXT} (between TX/RX) Breakout Main-route	 4.85x 3x	Dielectric height	This is the recommended dimension for meeting NEXT requirement Stripline structure in a GSSG structure is assumed; it holds in broadside-coupled stripline structure All values are in terms of minimum dielectric height
Min inter-S_{FEXT} (between TX/TX or RX/RX) Breakout Main-route	 1x 1x	Inter-pair spacing	
Max length Breakout Main-route	 11 Max trace length - LBRK	mm	
Trace Spacing			
Pair-Pair (inter-pair) - Microstrip / Stripline To plane and capacitor pad - Microstrip / Stripline To unrelated high-speed signals - Microstrip / Stripline	4x / 3x 4x / 3x 4x / 3x	dielectric height	
Trace Length/Skew			
Trace loss characteristic @ 2.5GHz	< 0.7	dB/in	The following max length is derived based on this characteristic. See Note 1.
Breakout region - Max trace delay	11	mm	Minimum width and spacing
Max trace length/delay	152.3 (1014)	mm (ps)	
Max PCB via distance/delay from pin	6.29 (41.9)	mm (ps)	
Max within pair (intra-pair) skew	0.15 (1)	mm (ps)	
Differential pair uncoupled length/delay	6.29 (41.9)	mm (ps)	
AC Cap			
Value	0.1	uF	Smallest size preferred (i.e. 0201). See note under USB Connection Diagrams for details on when AC capacitors are required
Location (max distance to adjacent discontinuities)	8 (53.22)	mm (ps)	The AC cap location should be located as close as possible to nearby discontinuities
Via			
via structure	Y-pattern is strongly recommended (keep symmetry)		Xtalk suppression is best when using Y-pattern. Can also reduce the limit of pair-pair distance. See Figure 6-4.
GND via	Place GND via as symmetrically as possible to the data pair vias.		GND via is used to maintain return path, while its Xtalk suppression is limited.

Parameter	Requirement	Units	Notes
	Up to 4 signal vias (2 diff pairs) can share a single **GND** return via"		
AC cap pad voiding	GND (or PWR) void under / above the cap is preferred		Voiding is required if cap size is 0603 or large.
Max via stub length	0.4	mm	long via stub requires review (IL and resonance dip check).
ESD			
Preferred device			Type: Texas Instruments TPD4I05U06. Optional. Place ESD component near connector
Max junction capacitance (IO to GND)	0.8	pF	
Location (max distance to connector)	8 (53)	mm (ps)	
Layout recommendations			See USB 3.2 Guideline Figure 6-5
Common-mode choke (not recommended – only used if absolutely required for EMI issues) See Chapter 16 for details on CMC if implemented.			
Component Order			
Component order			Chip — AC capacitor (TX only) — common mode choke — ESD — Connector: See Figure 6-6.
General: See Chapter 16 for guidelines related to serpentine routing, routing over voids and noise coupling			

Note:

1. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
2. Recommend trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion.
3. Place GND vias as symmetrically as possible to data pair vias.

The following figures show the USB 3.2 interface signal routing requirements.

Figure 6-2. IL/NEXT Plot

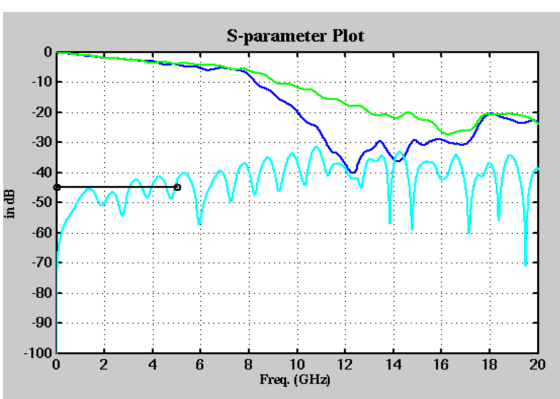


Figure 6-3. Trace Spacing for TX/RX Non-Interleaving

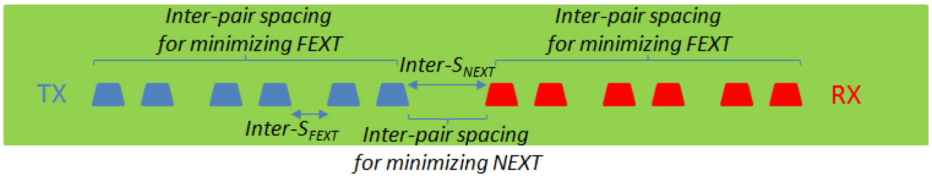


Figure 6-4. Via Structures

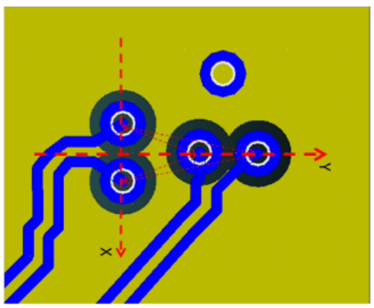


Figure 6-5. ESD Layout Recommendations

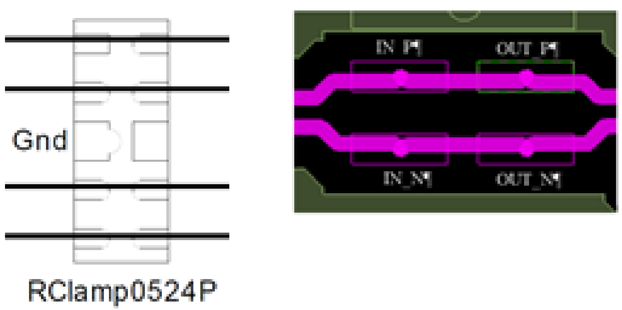
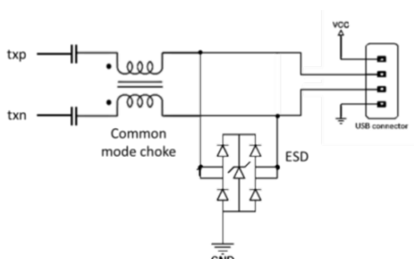


Figure 6-6. Component Order



6.1.3 Common USB Routing Guidelines

If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs and flexes must be used for the max trace and skew calculations.

Keep critical USB related traces away from other signal traces or unrelated power traces and areas or power supply components.

Table 6-6. USB 2.0 Signal Connections

Jetson Nano Ball Name	Type	Termination	Description
USB[2:0]_D_P USB[2:0]_D_N	DIFF I/O	90Ω common mode chokes close to connector. ESD Protection between choke and connector on each line to GND	USB Differential Data Pair: Connect to USB connector, Mini-Card socket, hub or another device on the PCB.

Table 6-7. Miscellaneous USB Signal Connections

Module Pin Name	Type	Termination	Description
GPIO00	A	5V to 1.8V level shifter	USB0 VBUS Enable: Connect to VBUS pin of USB connector receiving USB0_+/– interface through level shifter. Also connects to VBUS power supply if host mode supported.

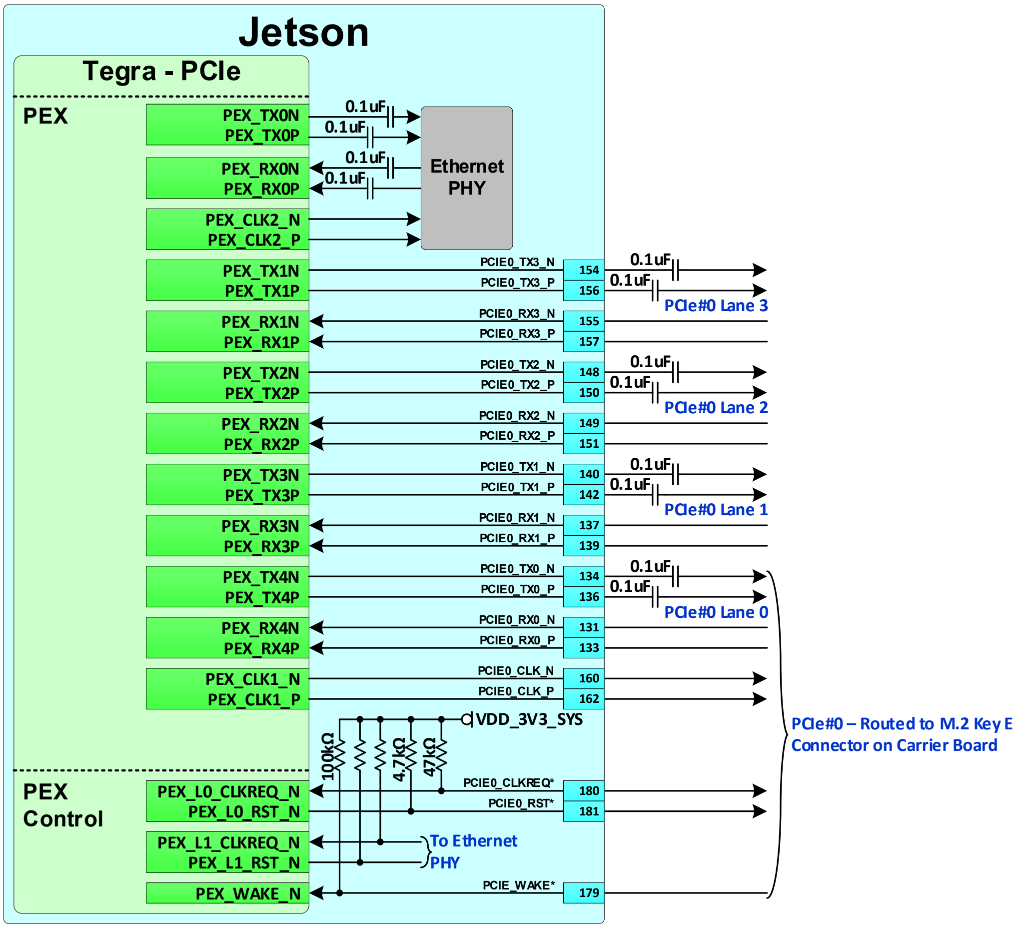
Table 6-8. USB 3.2 Signal Connections

Module Pin Name	Type	Termination	Description
USBSS_TX_N/P (USB 3.2 Port #0)	DIFF Out	Series 0.1uF caps. ESD Protection near connector if required.	USB 3.2 Differential Transmit Data Pairs: Connect to USB 3.2 connectors, hubs or other devices on the PCB.
USBSS_RX_N/P (USB 3.2 Port #0)	DIFF In	If routed directly to a peripheral on the board, AC caps are needed for the peripheral TX lines. ESD protection near connector if required.	USB 3.2 Differential Receive Data Pairs: Connect to USB 3.2 connectors, hubs or other devices on the PCB.

6.2 PCIe

NVIDIA® Tegra® contains a PCIe controller that brings one interface up to four lanes to the module pins for use on the carrier board. A second single-lane PCIe interface is used on-module for Ethernet. The Jetson Nano PCIe interface supports lane reversal and polarity inversion (P/N swapping).

Figure 6-7. Example PCIe Connections



Notes:

1. AC capacitors required on RX lines on carrier board if connected directly to device. They should not be on the carrier board if connected to PCIe connector, M.2 Key M, etc. In those cases, the AC caps are on the board connected to those connectors.
2. The PCIEx_CLK clock outputs comply to the PCIe CEM specification "REFCLK DC Specifications and AC Timing Requirements." The clocks and RX/TX signals are HCSL compatible.

6.2.1 PCIe Design Guidelines

Table 6-9 and Figure 6-8 provide the signal routing requirements for the PCIe interface.

Table 6-9. PCIe Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data rate / UI period	5.0 / 200	Gbps / ps	2.5GHz, half-rate architecture
Configuration / device organization	1	Load	
Topology	Point-point		Unidirectional, differential
Termination	50	Ω	To **GND** Single Ended for P and N
Impedance			
Trace Impedance - diff / SE	85 / 50	Ω	±15%. See Note 1
Reference plane	GND		
Spacing			
Trace Spacing (Stripline/Microstrip) pair – pair To plane and capacitor pad To unrelated high-speed signals	 3x / 4x 3x / 4x 3x / 4x	dielectric height	See Note 2
Length/Skew			
Trace loss characteristic @ 2.5 GHz	< 0.7	dB/in	The following max length is derived based on this characteristic. See Note 3
Breakout region (max length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length/delay	5.5 (880)	in (ps)	
Max PCB via distance from the BGA	41.9	ps	Max distance from BGA ball to first PCB via.
PCB within pair (intra-pair) skew	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of vias PTH vias Micro-vias	 2 for TX traces and 2 for RX trace No requirement		
Max via stub length	0.4	mm	Longer via stubs would require review
Routing signals over antipads	Not allowed		
AC Cap			
Value - Min/Max	0.075 / 0.2	uF	Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)	8	mm	Discontinuity such as edge finger, component pad

Parameter	Requirement	Units	Notes
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.		See Figure 6-7.
General: See Chapter 16 for guidelines related to serpentine routing, routing over voids and noise coupling			

Notes:

1. The PCIe specification has 40-60 Ω absolute min/max trace impedance, which can be used instead of the 50Ω, ± 15%.
2. If routing in the same layer is necessary, route group TX and RX separately without mixing RX/TX routes and keep distance between nearest TX/RX trace and RX to other signals 3x RX-RX separation.
3. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
4. Do length matching before via transitions to different layers or any discontinuity to minimize common mode conversion.

Figure 6-8. AC Cap Voiding

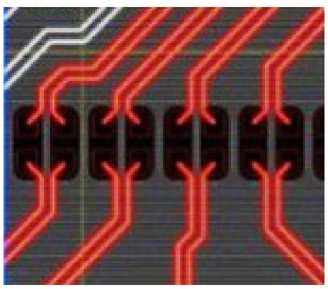


Table 6-10. PCIe Signal Connections

Module Pin Name	Type	Termination	Description
PCIe Interface #0 (x4)			
PCIE0_TX3_N/P (Lane 3) PCIE0_TX2_N/P (Lane 2) PCIE0_TX1_N/P (Lane 1) PCIE0_TX0_N/P (Lane 0)	DIFF OUT	Series 0.1uF Capacitor	Differential Transmit Data Pairs: Connect to TX_N/P pins of PCIe connector or **RX_N/P** pin of PCIe device through AC cap according to supported configuration.
PCIE0_RX3_N/P (Lane 3) PCIE0_RX2_N/P (Lane 2) PCIE0_RX1_N/P (Lane 1) PCIE0_RX0_N/P (Lane 0)	DIFF IN	Series 0.1uF capacitors near Jetson Nano pins or device if device on main PCB.	Differential Receive Data Pairs: Connect to RX_N/P pins of PCIe connector or **TX_N/P** pin of PCIe device through AC cap according to supported configuration.
PCIE0_CLK_N/P	DIFF OUT		**Differential Reference Clock Output: Connect to REFCLK_N/P pins** of PCIe device/connector
PCIE0_CLKREQ*	I/O	47kΩ pull-up to VDD_3V3_SYS on module	**PCIe Clock Request for PCIE0_CLK:** Connect to CLKREQ pins on device/connector(s)
PCIE0_RST*	O	4.7kΩ pull-up to VDD_3V3_SYS on module	**PCIe Reset:** Connect to PERST pins on device/connector(s)
PCIE_WAKE*	I	100kΩ pull-up to VDD_3V3_SYS on module	**PCIe Wake:** Connect to WAKE pins on device or connector

6.3 Gigabit Ethernet

Jetson Nano integrates a Realtek RTL8119I-CG Gigabit Ethernet controller. The magnetics and RJ45 connector would be implemented on the carrier board. Contact Realtek for carrier board placement and routing guidelines.

Table 6-11. Gigabit Ethernet Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
194	GBE_LED_ACT	–	Ethernet Activity LED (Yellow)	LAN	Output	–
188	GBE_LED_LINK	–	Ethernet Link LED (Green)		Output	–
184	GBE_MDI0_N	–	GbE Transformer Data 0		Bidir	MDI
186	GBE_MDI0_P	–				
190	GBE_MDI1_N	–	GbE Transformer Data 1			
192	GBE_MDI1_P	–				
196	GBE_MDI2_N	–	GbE Transformer Data 2			
198	GBE_MDI2_P	–				
202	GBE_MDI3_N	–	GbE Transformer Data 3			
204	GBE_MDI3_P	–				

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 6-9. Ethernet Connections

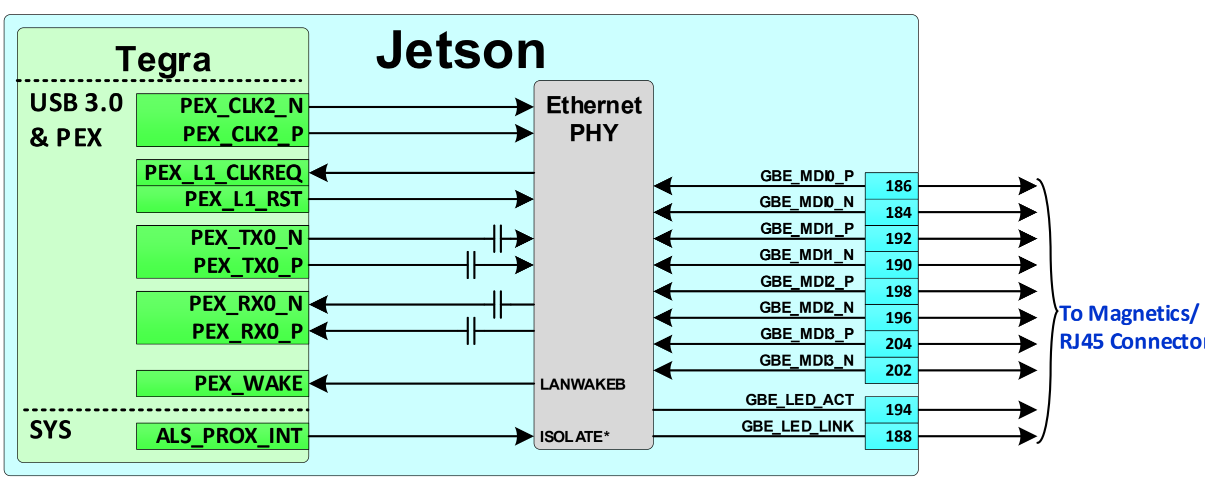


Figure 6-10. Gigabit Ethernet Magnetics and RJ45 Connections

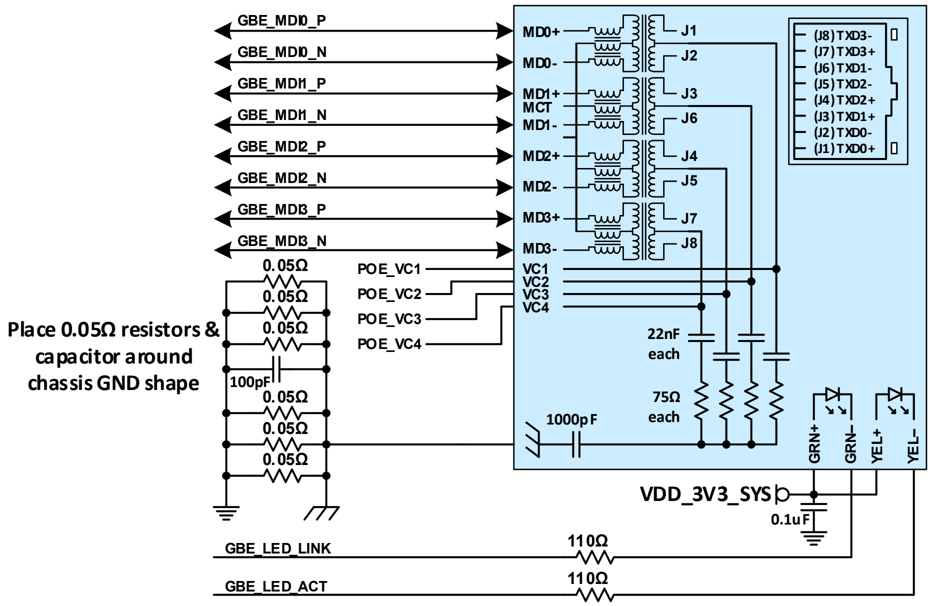


Table 6-12. Ethernet MDI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	GND		
Trace impedance - Diff pair / Single Ended	100 / 50	Ω	±15%. Differential impedance target is 100Ω. 90Ω can be used if 100Ω is not achievable
Min trace spacing (pair-pair)	0.763	mm	
Max trace length/delay	109 (690)	mm (ps)	
Max within pair (intra-pair) skew	0.15 (1)	mm (ps)	
Number of vias	minimum		Ideally there should be no vias, but if required for breakout to Ethernet controller or magnetics, keep very close to either device.

Table 6-13. Ethernet Signal Connections

Module Pin Name	Type	Termination	Description
GBE_MDI[3:0]_N/P	DIFF I/O		Gigabit Ethernet MDI IF Pairs: Connect to Magnetics -/+ pins
GBE_LED_LINK	O	110Ω series resistor	Gigabit Ethernet Link LED: Connect to green LED on RJ45 connector
GBE_LED_ACT	O	110Ω series resistor	Gigabit Ethernet Activity LED: Connect to yellow LED on RJ45 connector

Chapter 7. Display

Tegra X1 Embedded designs can select from several display options including MIPI DSI and eDP for embedded displays, and HDMI or DP for external displays. The maximum number of simultaneous displays supported by Jetson Nano is two.

Table 7-1. Display General Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
206	GPIO07	LCD_BL_PWM	GPIO or Pulse Width Modulation signal	Expansion header	Output	CMOS – 1.8V

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The direction of GPIO07 is true when used for this function. Otherwise as a GPIO, the direction is bidirectional.

7.1 MIPI DSI

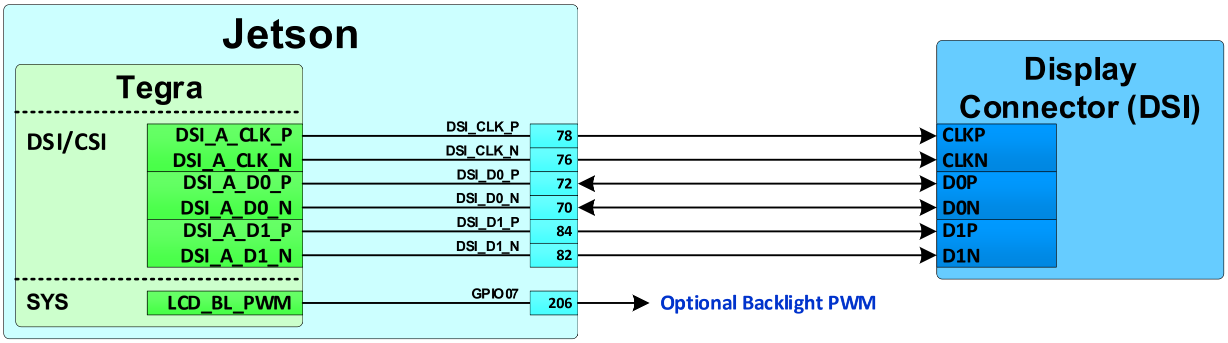
Tegra supports two total MIPI DSI data lanes and a single clock lane. Each data lane has a peak bandwidth up to 1.5Gbps.

Table 7-2. DSI Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
76	DSI_CLK_N	DSI_A_CLK_N	Display, DSI clock	Not assigned	Output	MIPI D-PHY
78	DSI_CLK_P	DSI_A_CLK_P				
70	DSI_D0_N	DSI_A_D0_N	Display, DSI data lane 0		Bidir	
72	DSI_D0_P	DSI_A_D0_P				
82	DSI_D1_N	DSI_A_D1_N	Display, DSI data lane 1		Output	
84	DSI_D1_P	DSI_A_D1_P				

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 7-1. DSI 1 x 2 Lane Connection Example



Note: If EMI/ESD devices are necessary, they must be tuned to minimize impact to signal quality, which must meet the DSI spec. requirements for the frequencies supported by the design.

7.1.1 MIPI DSI and CSI Design Guidelines

Table 7-3 details the MIPI DSI and CSI interface signal routing requirements.

Table 7-3. MIPI DSI and CSI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency/data rate (per data lane)	750 / 1500	MHz/Mbps	
Number of loads	1	load	
Reference plane	**GND**		
Trace impedance - Diff pair / SE	90-100 / 45-50	Ω	±10%
Via proximity (signal to reference)	< 0.65 (3.8)	mm (ps)	
Intra-pair trace spacing	0.15mm	mm	Can be adjusted to meet Differential Impedance. Loosely Coupled Diff. Pair recommended by Spec.
Inter-pair trace spacing - Microstrip / Stripline	4x / 3x	dielectric height	
Max PCB breakout length	5	mm	
Max trace delay 1 Gbps 1.5 Gbps	 1100 800	ps	
Max intra-pair skew	1	ps	
Max trace delay skew between **DQ** and **CLK**	5	ps	**DQ** includes all the data lines associated with a single clock. This may be 2 differential data lanes for a x2 interface, or 4 differential data lanes for a x4 interface.
Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components			

7.1.2 MIPI DSI and CSI Connection Guidelines

Table 7-4 details the MIPI DSI signal connections.

Table 7-4. MIPI DSI Signal Connections

Module Pin Name	Type	Termination	Description
DSI_CLK_N/P	DIFF OUT		DSI Differential Clock: Connect to CLKn and CLKp pins of the primary DSI display
DSI_D[1:0]_N/P	DIFF OUT		DSI Differential Data Lanes 1:0: Connect to corresponding data lanes of DSI display.
GPIO07	O		Optional LCD Backlight Pulse Width Modulation: Connect to LCD backlight solution PWM input if supported

7.2 eDP and DP

Table 7-5 details the MIPI DSI and CSI connection pin descriptions for the eDP and DP displays.

Table 7-5. eDP and DP Pin Description

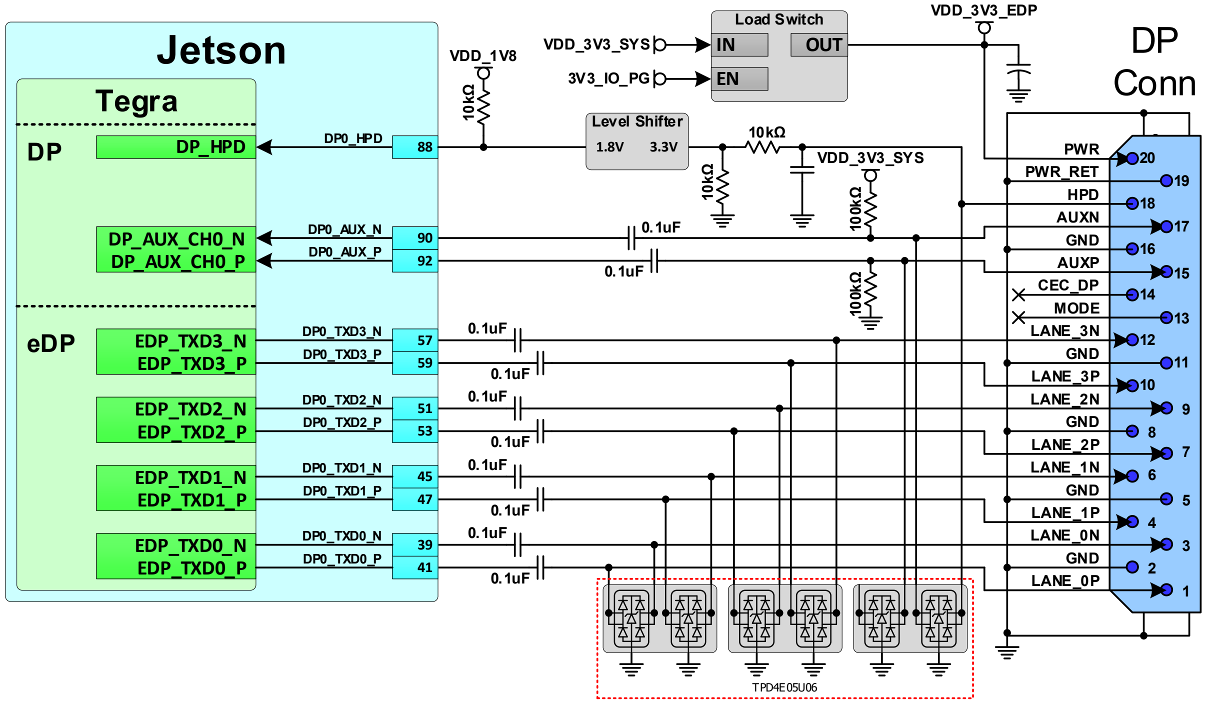
Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
90	DP0_AUX_N	DP_AUX_CH0_N	Display Port 0 auxiliary channel	DP connector	Bidir	eDP/DP
92	DP0_AUX_P	DP_AUX_CH0_P				
39	DP0_TXD0_N	EDP_TXDN0	Display port 0 data lane 0		Output	eDP/DP
41	DP0_TXD0_P	EDP_TXDP0				
45	DP0_TXD1_N	EDP_TXDN1	Display port 0 data lane 1			
47	DP0_TXD1_P	EDP_TXDP1				
51	DP0_TXD2_N	EDP_TXDN2	Display port 0 data lane 2			
53	DP0_TXD2_P	EDP_TXDP2				
57	DP0_TXD3_N	EDP_TXDN3	Display port 0 data lane 3			
59	DP0_TXD3_P	EDP_TXDP3				
88	DP0_HPD	DP_HPD0	Display port 0 hot-plug detect		Input	CMOS – 1.8V

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The direction for DP0_HPD is true when used for this function. Otherwise as a GPIO, the direction is bidirectional.

Tegra supports an eDP interface. The eDP interface can also be used for DP. DP support on these pins does not include HDCP or Audio.

Figure 7-2. DP/eDP Connection Example on DP0 Pins



Notes:

- Level shifter required on DP0_HPD to avoid the pin from being driven when Jetson Nano is off. The level shifter must be non-inverting (preserve the polarity of the HPD signal from the display).
- Load Switch enable is from powergood pin of main 3.3V supply.
- If eDP interface used for DP, note that HDCP is not supported.

7.2.1 eDP Routing Guidelines

Figure 7-3 shows the eDP topology, and Table gives the eDP and DP signal routing requirements.

Figure 7-3. eDP Differential Main Link Topology

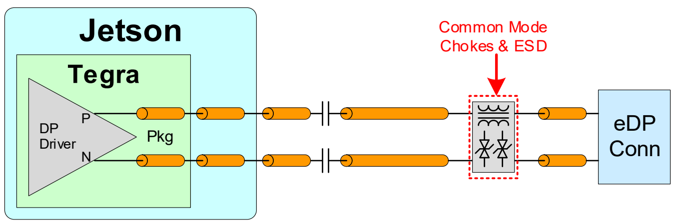


Table 7-6. eDP and DP Main Link Signal Routing Requirements Including DP_AUX

Parameter	Requirement	Units	Notes
Specification			
Max data rate / Min UI RBR HBR HBR2	 1.62 / 617 2.7 / 370 5.4 / 185	 Gbps / ps	Per data lane
Number of loads / topology	1	load	Point-Point, differential, unidirectional
Termination	100	Ω	On die at TX/RX
Electrical Spec			
IL RBR HBR HBR2	 0.7 1.2 2.4	 dB @ 0.81GHz dB @ 1.35GHz dB @ 2.7GHz	
Resonance dip frequency	>8	GHz	
TDR dip	>85	Ω	@ Tr-200ps (10%-90%)
FEXT	<= -40dB @ DC <= -30dB @ 2.7GHz	See Figure 7-4	
Impedance			
Trace impedance - Diff pair	90-100 85	Ω (±15%)	90Ω–100Ω is the spec. target. 85Ω is an implementation option (Zdiff does not account for trace coupling) 85Ω is preferable as it can provide better trace loss characteristic performance. See Note 1.
Reference plane	GND		
Trace Length, Spacing and Skew			

Parameter	Requirement	Units	Notes
Trace loss characteristic:	< 0.81	dB/in	@ 2.7GHz. The following max length is derived based on this characteristic. See Note 2.
Max PCB via dist. from connector RBR/HBR HBR2	 No requirement 7.63 (0.3)	mm (in)	
Max trace length/delay from Module TX to conn. RBR/HBR (Stripline / Microstrip) HBR2 (Stripline) HBR2 (Microstrip, 5x / 7x)	 215 (1138)/215 (975) 102 (700) 89 (525) / 102 (600)	mm (ps)	175ps/inch assumption for stripline, 150ps/inch for microstrip.
Trace spacing (pair-pair) Stripline Microstrip (HBR/RBR) Microstrip (HBR2)	 3x 4x 5x to 7x	dielectric height	
Trace spacing (Main link to AUX) - Stripline/Microstrip	3x / 5x	dielectric height	
Max intra-pair (within pair) skew	0.15 (1)	mm (ps)	See Note 2
Maxinter-pair (pair-pair) skew	150	ps	See Note 3
Via			
Max GND transition via distance	< 1x	diff pair pitch	For signals switching reference layers, add symmetrical GND stitching via near signal vias.
Via Structure			
Impedance dip Recommended via dimension Drill/Pad Antipad Via pitch	≥97 ≥92 200/400 >840 ≥880	Ω @ 200ps Ω @ 35ps um um um	The via dimension is required for HDMI-DP co-layout.
Topology	Y-pattern is recommended. Keep symmetry.		Y-pattern helps with Xtalk suppression. It can also reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. See Figure 7-5
	For in-line via, the distance from a via of one lane to the adjacent via from another lane >= 1.2 mm center-center.		See Figure 7-6
GND via	Place GND via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain a return path, while its Xtalk suppression is limited.
Max # of vias PTH vias Micro vias	 2 if all vias are PTH via Not limited if total channel loss meets IL spec		
Max via stub length	0.4	mm	
AC Cap			

Parameter	Requirement	Units	Notes
Value	0.1	uF	Discrete 0402
Max distance from AC cap to connector RBR/HBR HBR2	 No requirement 0.5	in	
Voiding RBR/HBR HBR2	 No requirement Voiding required		HBR2: Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.
Connector			
Voiding RBR/HBR HBR2	 No requirement Voiding required		HBR2: Standard DP connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7 mil larger than the connector pad.
General: See Chapter 16 for guidelines related to Serpentine routing, routing over voids and noise coupling			

Notes:

1. For eDP/DP, the spec puts a higher priority on the trace loss characteristic than on the impedance. However, before selecting 85Ω for impedance, it is important to make sure the selected stack-up, material and trace dimension can achieve the needed low loss characteristic.
2. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion.
4. The average of the differential signals is used for length matching.

The following figures show the eDP and DP interface signal routing requirements.

Figure 7-4. S-parameter

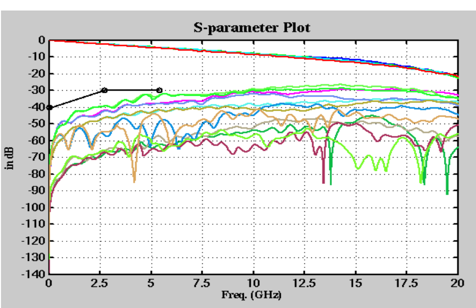


Figure 7-5. Via Topology #1

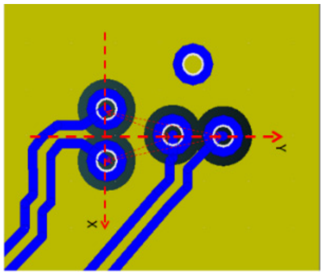


Figure 7-6. Via Topology #2

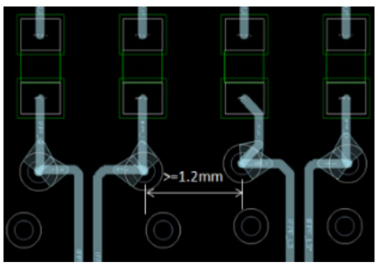


Table 7-7. eDP Signal Connections

Module Pin Name	Type	Termination	Description
DP0_TXD[3:0]_N/P	O	Series 0.1uF capacitors and ESD to GND on all.	eDP/DP Differential CLK/Data Lanes: Connect to matching pins on display connector.
DP0_AUX_N/P	I/OD	Series 0.1uF capacitors. 100kΩ pulldown on DP0_AUX_P and 100kΩ pull-up to VDD_3V3_SYS on DP0_AUX_N. ESD to GND on both.	**eDP/DP:** Auxiliary Channels: Connect to AUX_CH-/+ on display connector.
DP0_HPD	I	From module pin: 10kΩ pull-up to 1.8V, level shifter and 100kΩ pulldown on connector side of shifter and ESD to GND.	**eDP/DP: Hot Plug Detect**: Connect to HPD pin on display connector through level shifter.

7.3 HDMI and DP

A standard DP 1.2a or HDMI V2.0 interface is supported. These share the same set of interface pins, so either DisplayPort or HDMI can be supported natively.

Table 7-8. HDMI and DP Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
98	DP1_AUX_N	DP_AUX_CH1_N	DisplayPort 1 Aux– or HDMI DDC SDA	HDMI Conn.	Bidir	eDP/DP or Open-Drain, 1.8V (3.3V
100	DP1_AUX_P	DP_AUX_CH1_P	DisplayPort 1 Aux+ or HDMI DDC SCL			

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
						tolerant - DDC)
63	DP1_TXD0_N	HDMI_DP_TXDN0	DisplayPort 1 Lane 0 or HDMI Lane 2		Output	HDMI/DP
65	DP1_TXD0_P	HDMI_DP_TXDP0				
69	DP1_TXD1_N	HDMI_DP_TXDN1	DisplayPort or HDMI Lane 1			
71	DP1_TXD1_P	HDMI_DP_TXDP1				
75	DP1_TXD2_N	HDMI_DP_TXDN2	DisplayPort 1 Lane 2 or HDMI Lane 0			
77	DP1_TXD2_P	HDMI_DP_TXDP2				
81	DP1_TXD3_N	HDMI_DP_TXDN3	DisplayPort 1 Lane 3– or HDMI Clk Lane			
83	DP1_TXD3_P	HDMI_DP_TXDP3				
96	DP1_HPD	HDMI_INT_DP_HPD	HDMI or Display Port Hot Plug Detect		Input	CMOS – 1.8V
94	HDMI_CEC	HDMI_CEC	HDMI CEC		Bidir	Open Drain, 3.3V

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The directions for DP1_HPD and HDMI_CEC are true when used for these functions. Otherwise as GPIOs, the direction is bidirectional

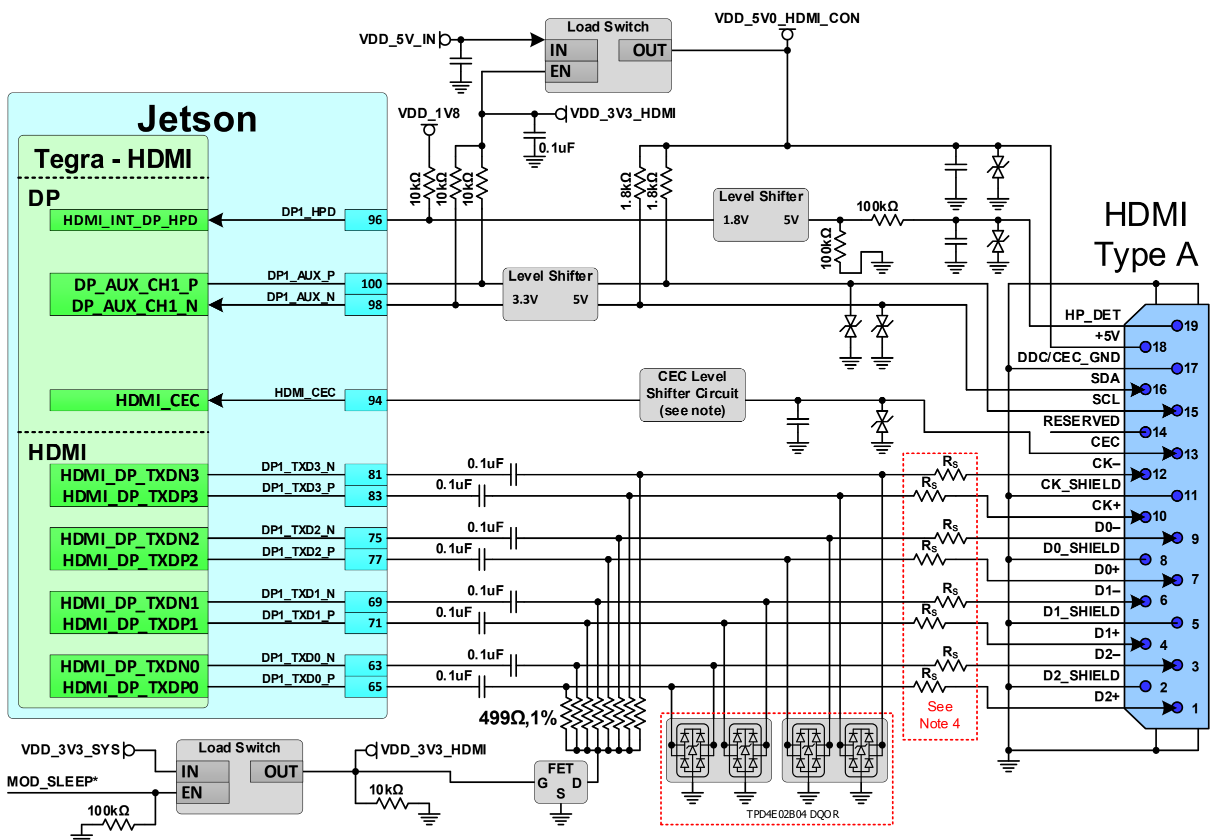
Table 7-9. DP and HDMI Pin Mapping

Module Pin Name	Module Pin #s	HDMI	DP
DP1_TXD3_P DP1_TXD3_N	83 81	TXC+ TXC –	TX3+ TX3–
DP1_TXD2_P DP1_TXD2_N	77 75	TX0+ TX0–	TX2+ TX2–
DP1_TXD1_P DP1_TXD1_N	71 69	TX1+ TX1–	TX1+ TX1–
DP1_TXD0_P DP1_TXD0_N	65 63	TX2+ TX2–	TX0+ TX0–

7.3.1 HDMI

This section shows the HDMI connection requirements, signal routing requirements, and topology.

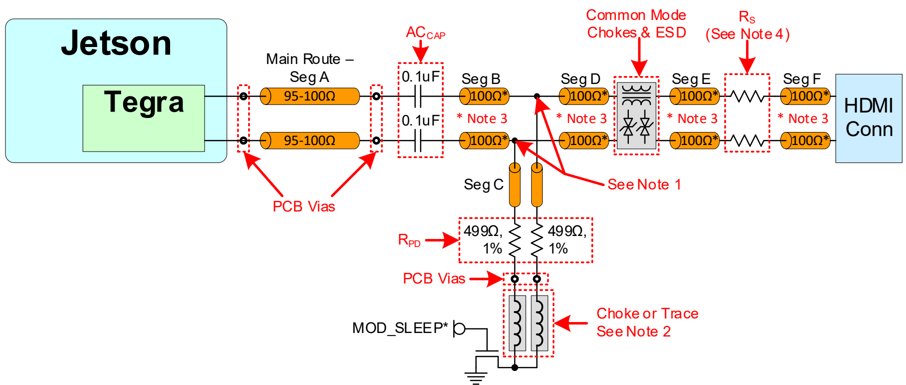
Figure 7-7. HDMI Connection Example



Notes:

1. Level shifters required on DDC/HPD. Tegra pads are not 5V tolerant and cannot directly meet HDMI VIL/VIH requirements. HPD level shifter can be non-inverting or inverting. HPD level shifter on the Jetson Nano Developer Kit is inverting.
2. If EMI/ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing and electrical requirements of the HDMI specification for the modes to be supported. See requirements and recommendations in the related sections of Table 7-10.
3. The DP1_TXx pads are native DP pads and require series AC capacitors (ACCAP) and pull-downs (RPD) to be HDMI compliant. The 499Ω, 1% pull-downs must be disabled when Jetson Nano is off or in sleep mode to meet the HDMI VOFF requirement. The enable to the FET, enables the pull-downs when the HDMI interface is to be used. Chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
4. Series resistors RS are required. See the RS section of Table 7-10 for details.
5. See reference design for CEC level shifting/blocking circuit.

Figure 7-8. HDMI Clk and Data Topology



Notes:

1. RPD pad must be on the main trace. RPD and ACCAP must be on same layer.
2. Chokes (600Ω @ 100 MHz) or narrow traces (1uH@DC-100 MHz) between pull-downs and FET are chokes between pull-downs and FET are optional improvements for HDMI 2.0 operation.
3. The trace after the main route via should be routed on the top or bottom layer of the PCB, and either with 100 ohm differential impedance, or as uncoupled 50 ohm SE traces.
4. RS series resistor is required. See the RS section of Table 7-10 for details.

Table 7-10. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max frequency / UI	5.94 / 168	Gbps / ps	Per lane – not total link bandwidth
Topology	Point to point		Unidirectional, differential
Termination At receiver On-board	 100 500	 Ω	Differential To 3.3V at receiver To GND near connector
Electrical Specification			
IL resonance dip frequency	<= 1.7 <= 2 <= 3 < 6 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85ohm that dip width should < 250ps
FEXT (PSFEXT)	<= -50 <= -40	dB at DC dB at 3GHz	PSNEXT is derived from an algebraic summation of the individual NEXT effects on each pair by the other pairs

Parameter	Requirement	Units	Notes
	<= -40	dB at 6GHz	
	IL/FEXT plot: See Figure 7-9		TDR plot: See Figure 7-10
Impedance			
Trace impedance - Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout and main route is an implementation option.
Reference plane	GND		
Trace spacing/Length/Skew			
Trace loss characteristic:	< 0.8 < 0.4	dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length is derived based on this characteristic. See Note 1.
Trace spacing (pair-pair) Stripline Microstrip: pre 1.4b Microstrip: 1.4b/2.0	 3x 4x 5x to 7x	dielectric height	For Stripline, this is 3x of the thinner of above and below.
Trace spacing (Main link to DDC) Stripline Microstrip	 3x 5x	dielectric height	For Stripline, this is 3x of the thinner of above and below.
Max total length/delay (1.4b/2.0 - up to 5.94Gbps) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	 63.5/2.5 (437) 50.8/2.0 (300) 63.5/2.5 (375)	mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max Total Length/Delay (Pre-1.4b - up to 165Mhz) Microstrip Stripline	254/10 (1500) 225/8.5 (1500)	mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max intra-pair (within pair) skew	0.15 (1)	mm (ps)	See notes 1, 2, and 3
Max inter-pair (pair to pair) skew	150	ps	See notes 1, 2, and 3
Max GND transition via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.
Via			
Topology	Y-pattern is recommended keep symmetry		Xtalk suppression is the best by Y-pattern. Also, it can reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. See Figure 7-11
Minimum impedance dip	97 92	Ω@200ps Ω@35ps	
Recommended via dimension drill/pad Antipad via pitch	 200/400 840 880	uM	
GND via	Place GND via as symmetrically as possible to data pair vias. Up to four signal vias (2 diff pairs) can share a single GND return via		GND via is used to maintain return path, while its Xtalk suppression is limited
Max # of vias PTH via u-via	 4 if all vias are PTH via Not limited if total channel loss meets IL spec.		

Parameter	Requirement	Units	Notes
Max via stub length	0.4	mm	long via stub requires review (IL and resonance dip check)
Topology			
The main route via dimensions should comply with the via structure rules (See via section)			See Figure 7-8
For the connector pin vias, follow the rules for the connector pin vias (See via section)			
The traces after main route via should be routed as 100Ω differential or as uncoupled 50ohm SE traces on PCB top or bottom.			
Max distance from R_{PD} to main trace (seg B)	1	mm	
Max distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Max distance between ESD and signal via	3	mm	
Add-on Components			
Example of a case where space is limited for placing components.	Top: See Figure 7-12		Bottom: See Figure 7-13
AC Cap			
Value	0.1	uF	
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.
Placement PTH design Micro-via design	 Place cap on bottom layer if main-route above core Place cap on top layer if main-route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		See Figure 7-14
Pull-down Resistor (R_{PD}), choke/FET			
Value	500	Ω	
Location.	Must be placed after AC cap		Placement: See Figure 7-15
Layer of placement	Same layer as AC cap. The FET and choke can be placed on the opposite layer thru a PTH via		
Choke between R_{PD} and FET choke Max trace Rdc Max trace length	 600 or 1 ≤20 4	 Ω @ 100 MHz uH@DC-100 MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	GND/PWR void under/above cap is preferred		
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues) See Appendix A for details on CMC if implemented.			
ESD (On-chip protection diode can withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance (IO to GND)	0.35	pF	e.g. Texas Instruments TPD4E02B04DQAR
Footprint	Pad right on the net instead of trace stub		See Figure 7-16

Parameter	Requirement	Units	Notes
Location	After pull-down resistor/CMC and before R_S		
Void	GND/PWR void under/above the cap is needed. Void size = 1mm x 2mm for 1 pair		See Figure 7-17
Series Resistor (R_S) – Series resistor on N/P path for HDMI 2.0 (mandatory)			
Value	≤ 6	Ω	± 10%. 0ohm is acceptable if the design passes the HDMI2.0 HF1-9 test. Otherwise, adjust the R_S value to ensure the HDMI2.0 tests pass: Eye diagram, Vlow test and HF1-9 TDR test
Location	After all components and before HDMI connector		
Void	GND/PWR void under/above the R_S device is needed. Void size = SMT area + 1x dielectric height keepout distance.		
Trace at Component Region			
Value	100	Ω	± 10%
Location	At component region (Microstrip)		
Trace entering the SMT pad	One 45°		See Figure 7-18
Trace between components	Uncoupled structure		See Figure 7-19
HDMI connector			
Connector voiding	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself		See Figure 7-20
General: See Chapter 16 for guidelines related to Serpentine routing, routing over voids and noise coupling			

Notes:

1. Longer trace lengths may be possible if the total trace loss is equal to or better than the target. If the loss is greater, the max trace lengths will need to be reduced.
2. The average of the differential signals is used for length matching.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion
4. If routing includes a flex or 2nd PCB, the max trace delay and skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.

The following figures show the HDMI interface signal routing requirements.

Figure 7-9. IL and FEXT Plot

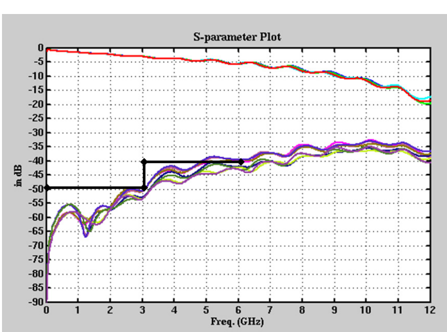


Figure 7-10. TDR Plot

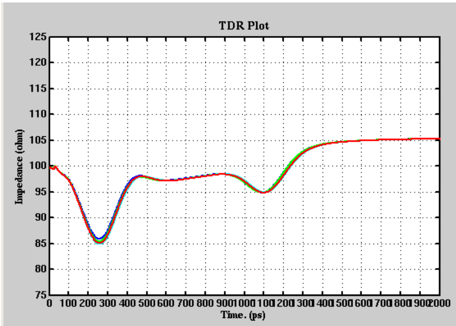


Figure 7-11. HDMI Via Topology

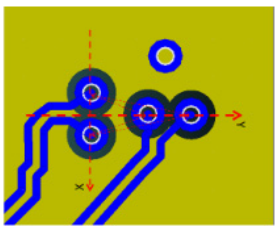


Figure 7-12. Add-on Components – Top

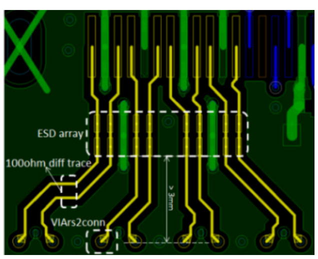


Figure 7-13. Add-on Components – Bottom

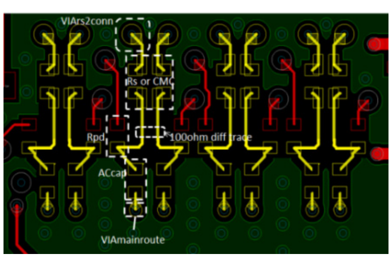


Figure 7-14. AC Cap Void

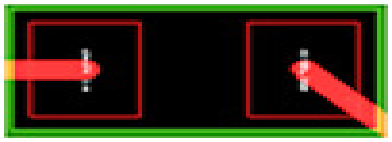


Figure 7-15. RPD, Choke, FET Placement

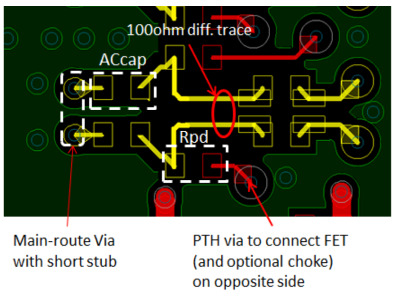


Figure 7-16. ESD Footprint

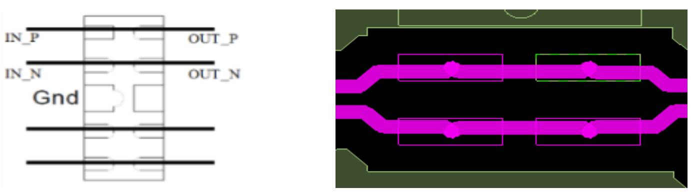


Figure 7-17. ESD Void

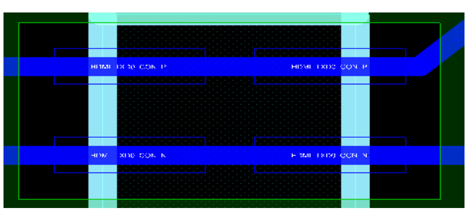


Figure 7-18. SMT Pad Trace Entering

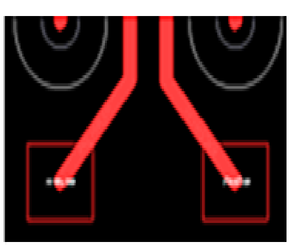


Figure 7-19. SMT Pad Trace Between

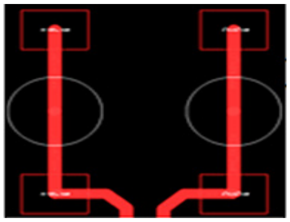


Figure 7-20. Connector Voiding

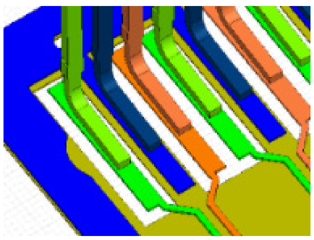


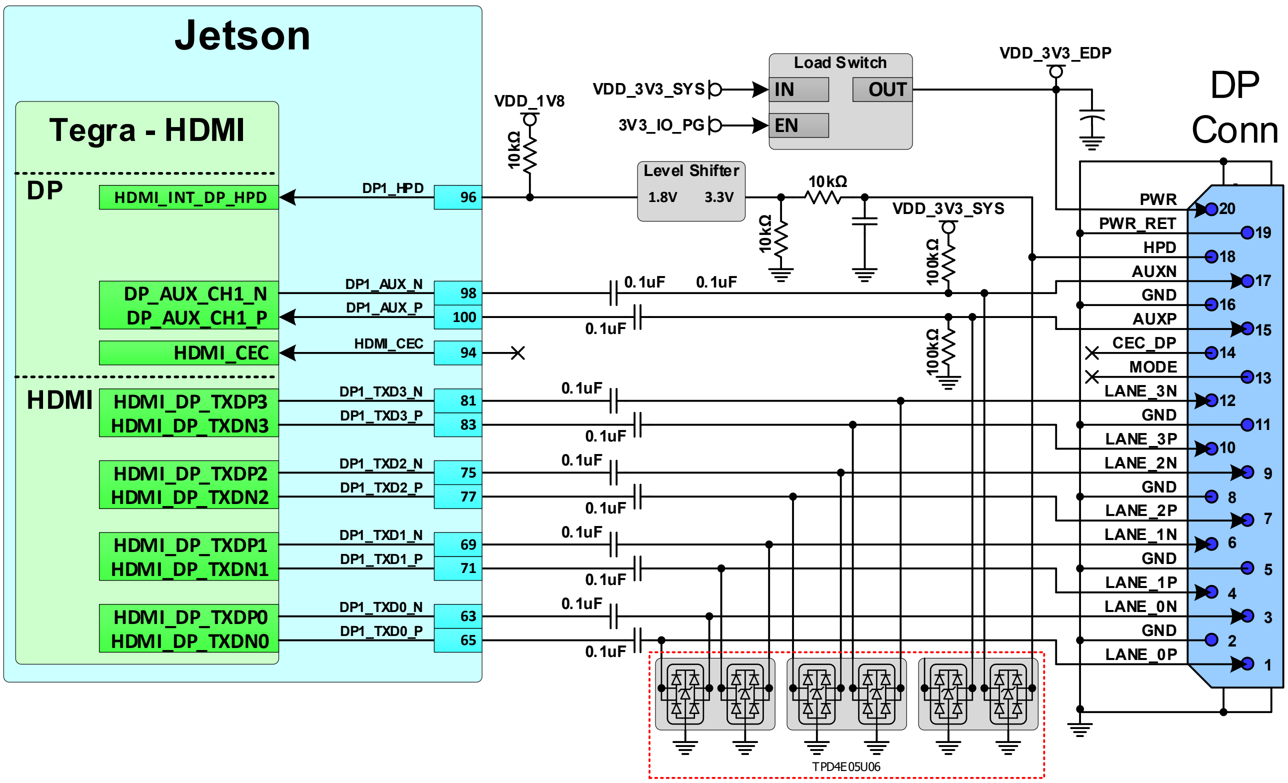
Table 7-11. HDMI Signal Connections

Module Pin Name	Type	Termination (see note on ESD)	Description
DP1_TXD3_N/P	DIFF OUT	0.1uF series AC_{CAP} → 500Ω R_{PD} (controlled by FET) → ESD to **GND** →.≤6Ω R_S (series resistor)	HDMI Differential Clock: Connect to **C–/C+** and pins on HDMI connector
DP1_TXD[2:0]_N/P	DIFF OUT		HDMI Differential Data: Connect to HDMI Data pins (See Table 7-9)
DP1_HPD	I	From module pin: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to **GND** on connector side → 100pF/12pF caps to **GND** → ESD to **GND**.	HDMI Hot Plug Detect: Connect to **HPD** pin on HDMI connector
HDMI_CEC	I/OD	Gating circuitry, See Figure 7-7 for details.	**HDMI Consumer Electronics Control:** Connect to CEC on HDMI connector through circuitry.
DP1_AUX_N/P	I/OD	From module pins: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → ESD to **GND**	**HDMI: DDC Interface – Clock and Data**: Connect **DP1_AUX_N** to **SDA** and **DP1_AUX_P** to **SCL** on HDMI connector
HDMI 5V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector and ESD to **GND**.	**HDMI 5V supply to connector: Connect to +5V on HDMI connector.**
Note: Any ESD and /or EMI solutions must support targeted modes (frequencies).			

7.3.2 DP on DP1 Pins

Figure 7-21 shows the DisplayPort connection.

Figure 7-21. DP Connection Example



Notes:

1. Level shifter required on DP1_HPD to avoid the pin from being driven when Jetson Nano is off. The level shifter must be non-inverting (preserve the polarity of the HPD signal from the display).
2. Any EMI/ESD included on the HDMI_DP pins must be suitable for the highest frequency modes supported (<1pf capacitive load recommended).

7.3.2.1 DP Interface Signal Routing Requirements

See eDP and DP signal routing requirements.

Table 7-12. DP Signal Connections

Module Pin Name	Type	Termination (see note on ESD)	Description
DP1_TXD3_N/P DP1_TXD[2:0]_N/P	O	Series 0.1uF capacitors → ESD on all.	DP Differential Lanes: Connect to D[3:0] –/+. See DP/HDMI pin mapping table for correct connections of data pins.
DP1_HPD	I	From Module pin: 10kΩ pull-up to 1.8V → level shifter and 100kΩ pulldown on connector side of shifter → ESD to GND.	DP Interrupt (Hot Plug Detect): Connect to HPD pin on DP connector w/termination described.
DP1_AUX_N/P	I/OD	From module pins: series 0.1uF caps → then 100KΩ PD on AUX_P and 100KΩ PU to 3.3V on AUX_N → ESD.	DP: Auxiliary Channels: Connect to AUX_CH–/+ on DP connector
DP 3.3V Supply	P	Adequate decoupling (0.1uF and 10uF recommended) on supply near connector.	DP supply to connector: Connect 3.3V supply pin on DP connector to VDD_3V3_SYS.
Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).			

Chapter 8. MIPI CSI Video Input

Jetson Nano brings twelve MIPI CSI lanes to the connector. Three quad-lane camera streams or two quad-lane plus two dual-lane camera streams or one quad-lane plus three dual-lane camera streams are supported. Each data lane has a peak bandwidth of up to 1.5 Gbps.

> **Note**: In Table 8-1 and Table 8-2 the Direction column, the Output is from Jetson Nano and the Input is to Jetson Nano. Bidir is for bidirectional signals.

Table 8-1. CSI Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
10	CSI0_CLK_N	CSI_A_CLK_N	Camera, CSI 0 Clock	Camera Connector #1	Input	MIPI D-PHY
12	CSI0_CLK_P	CSI_A_CLK_P				
4	CSI0_D0_N	CSI_A_D0_N	Camera, CSI 0 Data 0			
6	CSI0_D0_P	CSI_A_D0_P				
16	CSI0_D1_N	CSI_A_D1_N	Camera, CSI 0 Data 1			
18	CSI0_D1_P	CSI_A_D1_P				
3	CSI1_D0_N	CSI_B_D0_N	Camera, CSI 1 Data 0	Not Assigned		
5	CSI1_D0_P	CSI_B_D0_P				
15	CSI1_D1_N	CSI_B_D1_N	Camera, CSI 1 Data 1			
17	CSI1_D1_P	CSI_B_D1_P				
28	CSI2_CLK_N	CSI_E_CLK_N	Camera, CSI 2 Clock	Camera Connector #2		
30	CSI2_CLK_P	CSI_E_CLK_P				
22	CSI2_D0_N	CSI_E_D0_N	Camera, CSI 2 Data 0			
24	CSI2_D0_P	CSI_E_D0_P				
34	CSI2_D1_N	CSI_E_D1_N	Camera, CSI 2 Data 1			
36	CSI2_D1_P	CSI_E_D1_P				
27	CSI3_CLK_N	CSI_F_CLK_N	Camera, CSI 3 Clock	Not Assigned		
29	CSI3_CLK_P	CSI_F_CLK_P				
21	CSI3_D0_N	CSI_F_D0_N	Camera, CSI 3 Data 0			
23	CSI3_D0_P	CSI_F_D0_P				

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
33	CSI3_D1_N	CSI_F_D1_N	Camera, CSI 3 Data 1			
35	CSI3_D1_P	CSI_F_D1_P				
52	CSI4_CLK_N	CSI_C_CLK_N	Camera, CSI 4 Clock			
54	CSI4_CLK_P	CSI_C_CLK_P				
46	CSI4_D0_N	CSI_C_D0_N	Camera, CSI 4 Data 0			
48	CSI4_D0_P	CSI_C_D0_P				
58	CSI4_D1_N	CSI_C_D1_N	Camera, CSI 4 Data 1			
60	CSI4_D1_P	CSI_C_D1_P				
40	CSI4_D2_N	CSI_D_D0_N	Camera, CSI 4 Data 2			
42	CSI4_D2_P	CSI_D_D0_P				
64	CSI4_D3_N	CSI_D_D1_N	Camera, CSI 4 Data 3			
66	CSI4_D3_P	CSI_D_D1_P				

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Table 8-2. Miscellaneous Camera Pin Descriptions

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
213	CAM_I2C_SCL	CAM_I2C_SCL	Camera I2C Clock. 2.2kΩ pull-up to 3.3V on the module.	CSI Mux	Bidir	Open Drain – 3.3V
215	CAM_I2C_SDA	CAM_I2C_SDA	Camera I2C Data. 2.2kΩ pull-up to 3.3V on the module.			
114	CAM0_PWDN	CAM1_PWDN	Camera 0 Powerdown or GPIO	Camera Connector #1	Output	CMOS – 1.8V
116	CAM0_MCLK	CAM1_MCLK	Camera 0 Reference Clock			
120	CAM1_PWDN	CAM2_PWDN	Camera 1 Powerdown or GPIO	Camera Connector #2		
122	CAM1_MCLK	CAM2_MCLK	Camera 1 Reference Clock			

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The directions for CAM[1:0]_PWDN and CAM[1:0]_MCLK are true when used for these functions. Otherwise as GPIOs, the directions are bidirectional.

Figure 8-1. 4 Lane CSI Camera Connection Example

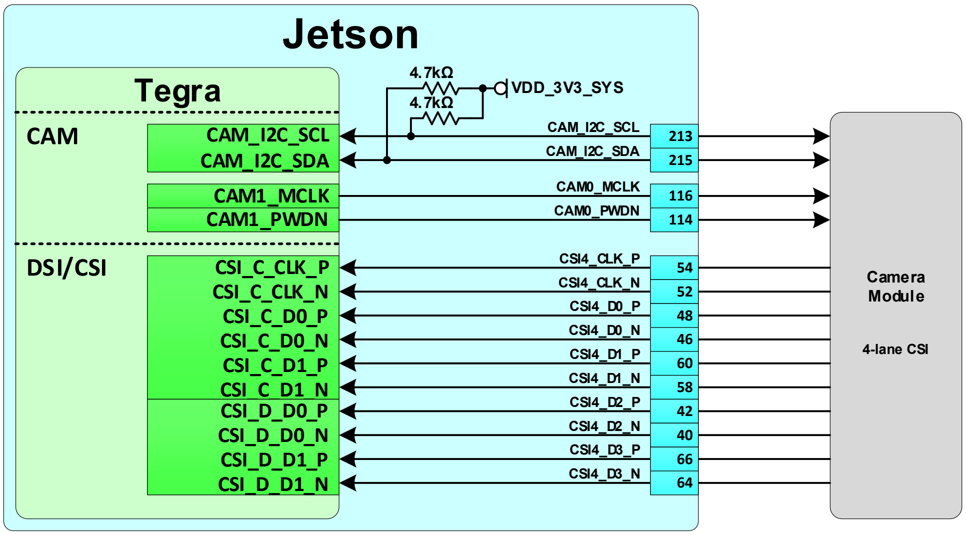


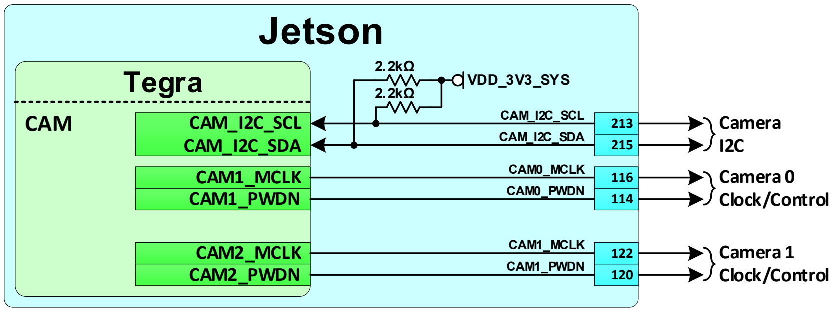
Table 8-3. CSI Configuration

Cameras	CSI_0 CLK/Data[1:0]	CSI_1 Data[1:0]	CSI_2 CLK/Data[1:0]	CSI_3 CLK	CSI_3 Data[1:0]	CSI_4 CLK/Data[1:0]
2-Lanes Each						
1 of 4 cameras	√					
2 of 4 cameras			√			
3 of 4 cameras				√	√	
4 of 4 cameras						√
4-Lanes Each						
1 of 3 cameras	√	√				
2 of 3 cameras			√		√	
3 of 3 cameras						√

Notes:

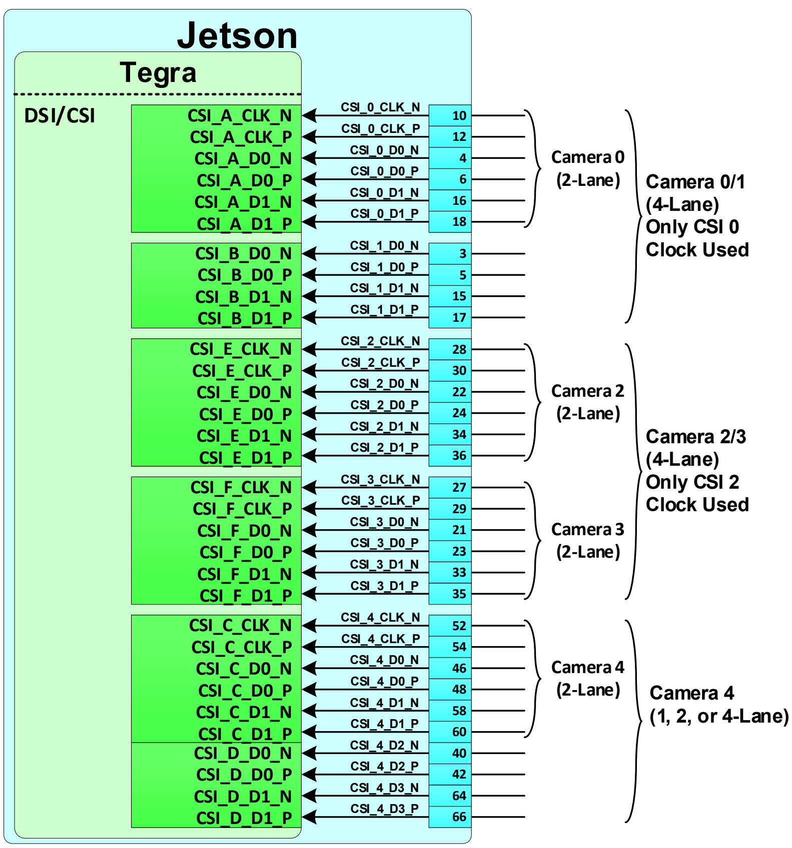
1. CSI 4 can be used as as a x1, x2, or x4 CSI interface.
2. If CSI 0/1 and CSI 4 are used for 4-lane interfaces each, CSI 2 and CSI 2 can be used for two 1 or 2-lane interfaces.
3. Each 2-lane options shown above can also be used for one single lane camera.

Figure 8-2. Available Cameral Control Pins



> **Note**: The CAM_I2C interface is connected to the power monitor device on the module which uses I2C address 7'h40.

Figure 8-3. CSI Connection Options



> **Note**: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing and Vil/Vih requirements at the receiver and maintain signal quality and meet requirements for the frequencies supported by the design.

8.1 CSI Design Guidelines

CSI and DSI use the MIPI D-PHY for the physical interface. The routing and connection requirements are found in the DSI section (Section 7.1),

Table 8-4. MIPI CSI Signal Connections

Module Pin Name	Type	Termination	Description
CSI[4:2,0]_CLK_N/P	I	See Note	CSI Differential Clocks. Connect to clock pins of camera. See Table 8-3 for details
CSI[3:0]_D[1:0]_N/P CSI4_D[3:0]_N/P	I/O	See Note	CSI Differential Data Lanes: Connect to data pins of camera. See Table 8-3 for details
Note: Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. In addition, EMI control may be needed. Both are shown in Figure 8-1. Any EMI/ESD solution must be compatible with the frequency required by the design.			

Table 8-5. Miscellaneous Camera Connections

Module Pin Name	Type	Termination	Description
CAM_I2C_CLK CAM_I2C_DAT	O I/O	2.2kΩ pull-ups **VDD_3V3_SYS** (on Jetson Nano). See note related to EMI/ESD in Table 8-4.	Camera I2C Interface: Connect to I2C SCL and SDA pins of imager. The CAM_I2C interface is connected to the power monitor device on the module which uses I2C address 7'h40.
CAM[1:0]_MCLK	O	120Ω bead in series (on Jetson Nano) See note related to EMI/ESD under MIPI CSI Signal Connections table.	Camera Master Clocks: Connect to camera reference clock inputs.
CAM[1:0]_PWDN	O		Camera Power Control signals (or GPIOs [1:0]): Connect to power down pins on camera(s).

Chapter 9. SD Card and SDIO

Jetson Nano uses one SDMMC interface for on-module eMMC (SDMMC4 on Tegra) and brings one to the connector pins for SD Card or SDIO use.

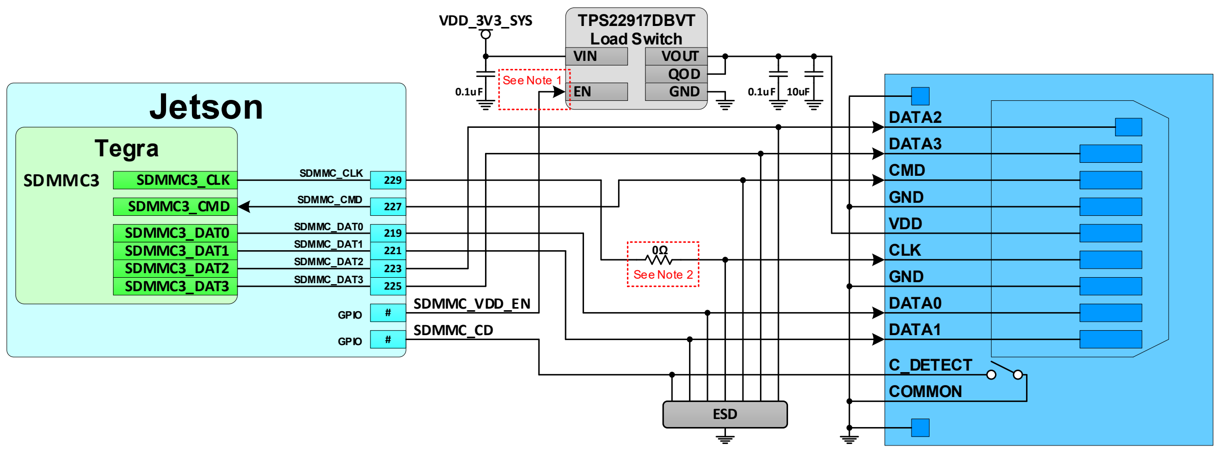
Table 9-1. SDIO Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
229	SDMMC_CLK	SDMMC3_CLK	SD Card or SDIO Clock	Not Assigned	Output	CMOS – 1.8V/3.3V
227	SDMMC_CMD	SDMMC3_CMD	SD Card or SDIO Command		Bidir	
219	SDMMC_DAT0	SDMMC3_DAT0	SD Card or SDIO Data 0			
221	SDMMC_DAT1	SDMMC3_DAT1	SD Card or SDIO Data 1			
223	SDMMC_DAT2	SDMMC3_DAT2	SD Card or SDIO Data 2			
225	SDMMC_DAT3	SDMMC3_DAT3	SD Card or SDIO Data 3			

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The directions for SDMMC_x and GPIO08 are true when used for these functions. Otherwise as GPIOs, the directions are bidirectional.

Figure 9-1. SD Card Connection Example



Notes:

1. The SD card supply must be enabled with a GPIO to prevent back-driving the Tegra SDMMC interface during power-on sequencing. The GPIO should have power-on reset (POR) that will ensure the supply is not enabled by default.
2. Having 0Ω, 0402 resistor is recommended in case of issues with EMI where it can be replaced with an appropriate device.
3. It is recommended that the SD card supply is current limited in case the supply is shorted to GND.

Table 9-2. SD Card and SDIO Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency			See Note 1
3.3V Signaling			
DS	25 (12.5)	MHz (MB/s)	
HS	50 (25)		
1.8V Signaling			
SDR12	25 (12.5)		
SDR25	50 (25)		
SDR50	100 (50)		
SDR104	208 (104)		
DDR50	50 (50)		
Topology	Point to point		
Reference plane	GND or PWR		See Note 2
Trace impedance	50	Ω	±15%. 45Ω optional depending on stack-up
Max via count			Independent of stack-up layers.
PTH	4		Depends on stack-up layers.
HDI	10		

Parameter	Requirement	Units	Notes
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	Up to four signal vias can share 1 GND return via
Trace spacing Microstrip / Stripline	4x / 3x	dielectric height	
Trace length SDR50 / SDR25 / SDR12 / HS / DS Min Max SDR104 / DDR50 Min Max	 16 (100) 139 (876) 16 (100) 83 (521)	mm (ps)	
Max trace length/delay skew in/between CLK and CMD/DAT SDR50 / SDR25 / SDR12 / HS / DS SDR104 / DDR50	 14 (87.5) 2 (12.5)	mm (ps)	See Note 3
Keep CLK, CMD and DATA traces away from other signal traces or unrelated power traces/areas or power supply components			

Notes:

1. Actual frequencies may be lower due to clock source/divider limitations.
2. If PWR, 0.01uF decoupling cap required for return current.

Table 9-3. SD Card and SDIO Signal Connections

Function Signal Name	Type	Termination	Description
SDMMC_CLK	O		SD Card / SDIO Clock: Connect to CLK pin of device.
SDMMC_CMD	I/O		SD Card / SDIO Command: Connect to CMD pin of device
SDMMC_D[3:0]	I/O		SD Card / SDIO Data: Connect to Data pins of device

Chapter 10. Audio

Tegra supports multiple PCM/I2S audio interfaces and includes a flexible audio-port switching architecture.

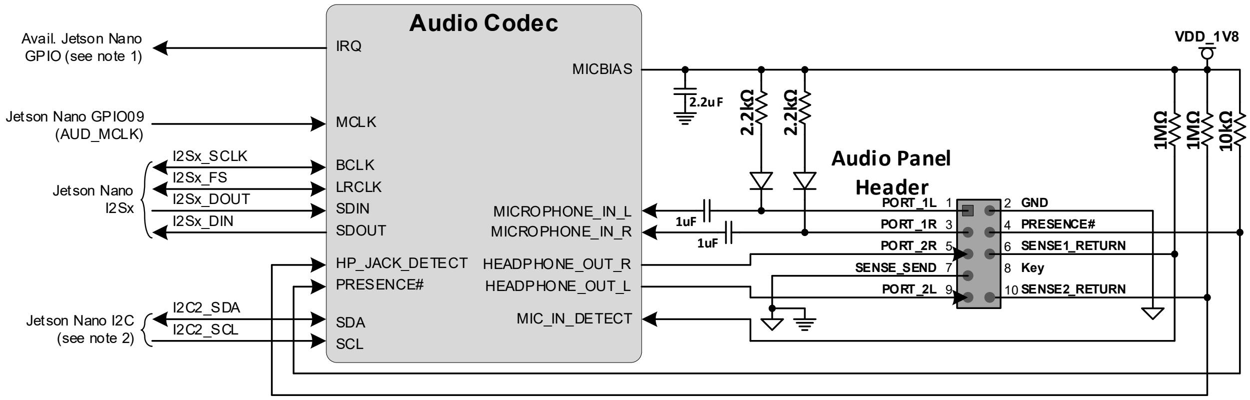
Table 10-1. Audio Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
193	I2S0_DOUT	DAP4_DOUT	I2S Audio Port 0 Data Out	Expansion Header	Output	CMOS – 1.8V
195	I2S0_DIN	DAP4_DIN	I2S Audio Port 0 Data In		Input	CMOS – 1.8V
197	I2S0_FS	DAP4_FS	I2S Audio Port 0 Left/Right Clock		Bidir	CMOS – 1.8V
199	I2S0_SCLK	DAP4_SCLK	I2S Audio Port 0 Clock		Bidir	CMOS – 1.8V
220	I2S1_DOUT	DMIC2_CLK	I2S Audio Port 1 Data Out	M.2 Key E	Bidir	CMOS – 1.8V
222	I2S1_DIN	DMIC1_DAT	I2S Audio Port 1 Data In		Input	CMOS – 1.8V
224	I2S1_FS	DMIC1_CLK	I2S Audio Port 1 Left/Right Clock		Bidir	CMOS – 1.8V
226	I2S1_SCLK	DMIC2_DAT	I2S Audio Port 1 Clock		Bidir	CMOS – 1.8V
211	GPIO09	AUD_MCLK	GPIO #9 or Audio Codec Master Clock	Expansion Header	Output	CMOS – 1.8V

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The directions for I2S[1:0]x and GPIO09 are true when used for those functions. Otherwise as GPIOs, the directions are bidirectional.

Figure 10-1. Audio Codec Connection Example



> **Notes:**
> 1. The Interrupt pin from the audio codec can connect to any available Jetson Nano GPIO. If the pin must be wake-capable, choose one of the GPIOs that supports this function.
> 2. I2C2 supports 1.8V operation since the interface is pulled to 1.8V through 2.2kΩ resistors on the module. If another I2C interface on Jetson Nano is used, a level shifter will be required as all the others are 3.3V.
> 3. Refer to the Intel High Definition Audio/AC'97 website for the latest information: https://www.intel.com/content/www/us/en/support/articles/000005512/boards-and-kits/desktop-boards.html.

Table 10-2. Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration / device organization	1	load	
Max loading	8	pF	
Reference plane	GND		
Breakout region impedance	Min width/spacing		
Trace impedance	50	Ω	±20%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See note
Trace spacing - Microstrip or Stripline	2x	dielectric height	
Max trace length/delay	~22 (3600)	In (ps)	
Max trace length/delay skew between **SCLK** and SDATA_**OUT/IN**	~1.6 (250)	In (ps)	
Note: Up to four signal vias can share a single **GND** return via.			

Table 10-3. Audio Signal Connections

Module Pin Name	Type	Termination	Description
I2S[1:0]_SCLK	I/O		I2S Serial Clock: Connect to I2S/PCM CLK pin of audio device.
I2S[1:0]_FS	I/O		I2S Frame Select (Left/Right Clock): Connect to corresponding pin of audio device.
I2S[1:0]_DOUT	I/O		I2S Data Output: Connect to data input pin of audio device.
I2S[1:0]_DIN	I		I2S Data Input: Connect to data output pin of audio device.
GPIO09	O		Audio Codec Master Clock: Connect to clock pin of audio codec.

Chapter 11. Miscellaneous Interfaces

11.1 I2C

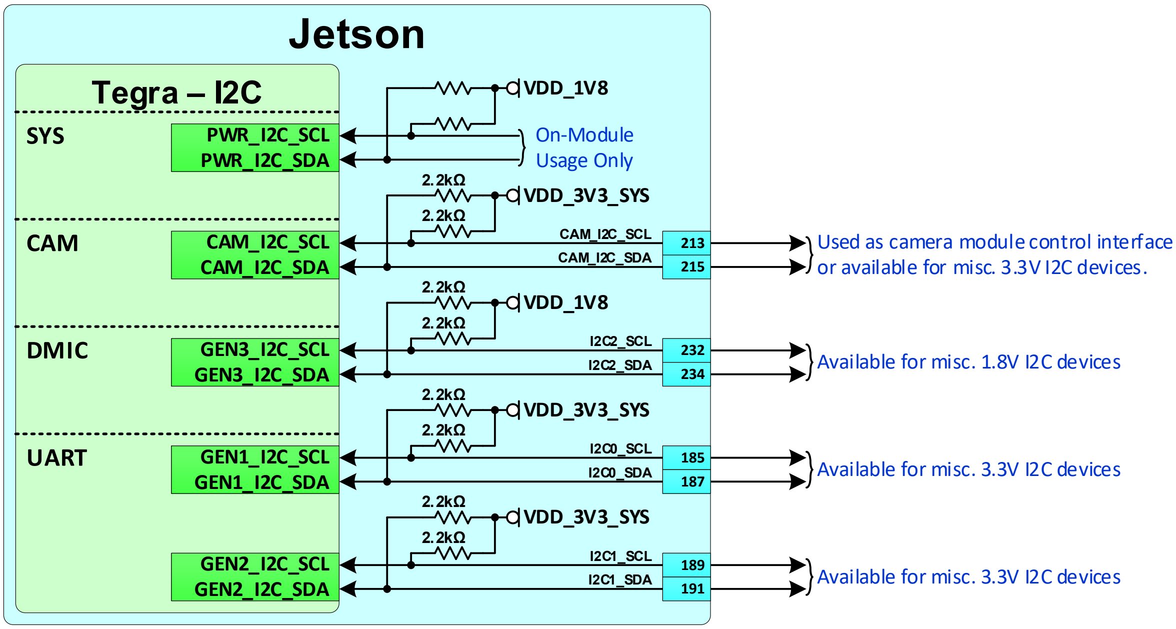
Jetson Nano brings four I2C interfaces to the connector pins. CAM_I2C is included in Table 8-2. The assignments in the I2C interface mapping table should be used where applicable for the I2C interfaces.

Table 11-1. I2C Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
185	I2C0_SCL	GEN1_I2C_SCL	General I2C 0 Clock. 2.2kΩ pull-up to 3.3V on module.	I2C (general)	Bidir	Open Drain – 3.3V
187	I2C0_SDA	GEN1_I2C_SDA	General I2C 0 Data. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
189	I2C1_SCL	GEN2_I2C_SCL	General I2C 1 Clock. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
191	I2C1_SDA	GEN2_I2C_SDA	General I2C 1 Data. 2.2kΩ pull-up to 3.3V on the module.			Open Drain – 3.3V
232	I2C2_SCL	GEN3_I2C_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.			Open Drain – 1.8V
234	I2C2_SDA	GEN3_I2C_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.			Open Drain – 1.8V

Notes: In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.

Figure 11-1. I2C Connections



Note: If an I2C interface is routed to an M.2 Key E or M.2 Key M socket, it is recommended that 0Ω series resistors be included on the lines. If the design will be used with WiFi modules that require I2C then the 0Ω series resistors would be installed. However, the WiFi modules must be fully spec compliant and not hold the I2C lines low during boot, which could interfere with communications with other devices on this I2C bus and possibly prevent the system from booting.

11.1.1 I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to Jetson Nano do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the read/write bit removed or 8-bit including the read/write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format). The I2C2 interface is connected to an EEPROM on the module which uses I2C address 7'h50. The CAM_I2C interface is connected to the power monitor device on the module which uses I2C address 7'h40.

Notes:

- The Jetson Nano I2C interfaces have 2.2kΩ pull-ups on the module. Pads for additional pull-ups are recommended in case a stronger pull-up is required due to additional loading on the interfaces.
- The I2C pad LPMD bit is set by default for the I2C[2:0] pins, but not for the CAM_I2C pins. These settings can be changed if necessary, to improve signal integrity.

Table 11-2. I2C Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency - Standard-mode / Fm / Fm+	100 / 400 / 1000	kHz	See Note 1
Topology	Single ended, bi-directional, multiple initiators and targets		
Max loading - Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane	GND or PWR		
Trace impedance	50 – 60	Ω	±15%
Trace spacing	1x	dielectric height	
Max trace length/delay Standard Mode Fm, Fm+ Modes	 3400 (~20) 1700 (~10)	ps (in)	

Notes:
1. Fm = Fast-mode, Fm+ = Fast-mode Plus.
2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
3. No requirement for decoupling caps for PWR reference.

Table 11-3. I2C Signal Connections

Module Pin Name	Type	Termination	Description
I2C0_SCL/SDA	I/OD	2.2kΩ pull-ups to VDD_3V3_SYS on Jetson Nano	I2C #0 Clock and Data. Connect to CLK and Data pins of any 3.3V devices
I2C1_SCL/SDA	I/OD	2.2kΩ pull-ups to VDD_3V3_SYS on Jetson Nano	I2C #1 Clock and Data. Connect to CLK and Data pins of 3.3V devices.
I2C2_SCL/SDA	I/OD	2.2kΩ pull-ups to VDD_1V8 on Jetson Nano	I2C #2 Clock and Data. Connect to CLK and Data pins of any 1.8V devices
CAM_I2C_SCL/SDA	I/OD	2.2kΩ pull-ups to VDD_3V3_SYS on Jetson Nano	Camera I2C Clock and Data. Connect to CLK and Data pins of any 3.3V devices

Notes:
1. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
2. For I2C interfaces that are pulled up to 1.8V, disable the E_IO_HV option for these pads. For I2C interfaces that are pulled up to 3.3V, enable the E_IO_HV option. The E_IO_HV option is selected in the Pinmux registers.

11.2 SPI

The Jetson Nano brings out two of the Tegra SPI interfaces. See Figure 11-2.

Table 11-4. SPI Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
89	SPI0_MOSI	SPI1_MOSI	SPI 0 Initiator Out and Target In	Expansion header	Bidir	CMOS – 1.8V
91	SPI0_SCK	SPI1_SCK	SPI 0 Clock			

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
93	SPI0_MISO	SPI1_MISO	SPI 0 Initiator In and Master Out			
95	SPI0_CS0*	SPI1_CS0	SPI 0 Chip Select 0			
97	SPI0_CS1*	SPI1_CS1	SPI 0 Chip Select 1			
104	SPI1_MOSI	SPI2_MOSI	SPI 1 Initiator Out and Target In			
106	SPI1_SCK	SPI2_SCK	SPI 1 Clock			
108	SPI1_MISO	SPI2_MISO	SPI 1 Initiator In and Target Out			
110	SPI1_CS0*	SPI2_CS0	SPI 1 Chip Select 0			
112	SPI1_CS1*	SPI2_CS1	SPI 1 Chip Select 1			

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The directions for SPI[1:0]x are true when used for those functions. Otherwise as GPIOs, the directions are bidirectional.

Figure 11-2. SPI Connections

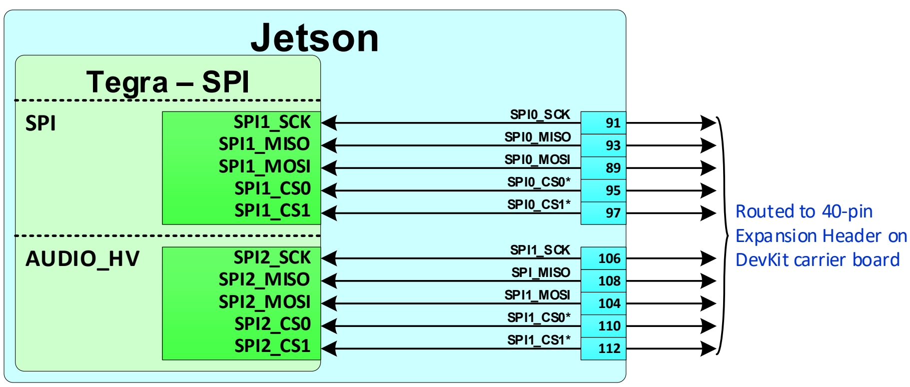
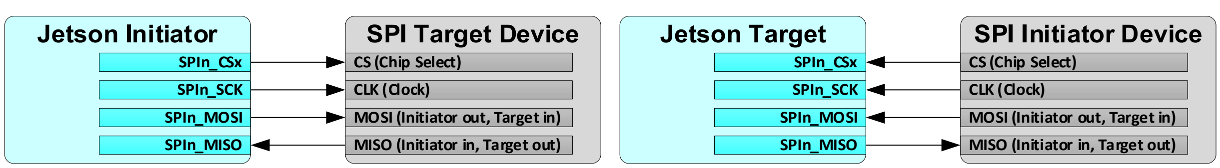


Figure 11-3 shows the basic connections used.

Figure 11-3. Basic SPI Initiator and Target Connections



11.2.1 SPI Design Guidelines

Figure 11-4 shows the SPI topologies and Table gives the SPI interface signal routing requirements.

Figure 11-4. SPI Topologies

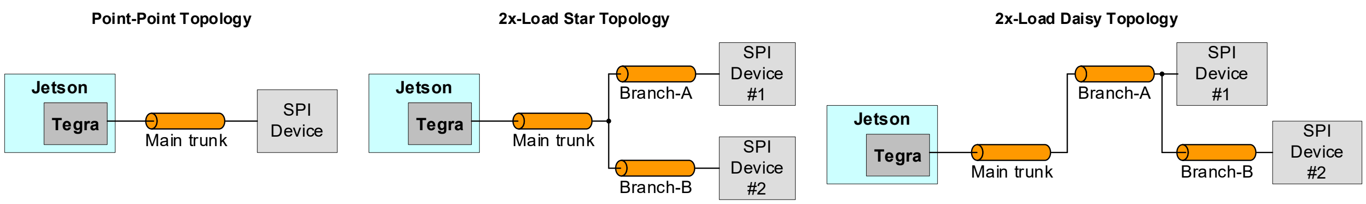


Table 11-5. SPI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max frequency	65	MHz	
Configuration / device organization	4	load	
Max loading (total of all loads)	15	pF	
Reference plane	GND		
Breakout region impedance	Minimum width and spacing		
Max PCB breakout delay	75	ps	
Trace impedance	50 – 60	Ω	±15%
Via proximity (signal to reference)	< 3.8 (24)	mm (ps)	See note
Trace spacing - Microstrip / Stripline	4x / 3x	dielectric height	
Max trace length/delay (PCB main trunk - For MOSI, MISO, SCK & CS) Point-point 2x-load star/daisy	 195 (1228) 120 (756)	mm (ps)	
Max trace length/delay (Branch-A) for MOSI, MISO, SCK and CS 2x-load star/daisy	75 (472)	mm (ps)	
Max trace length/delay skew from MOSI, MISO and CS to SCK	16 (100)	mm (ps)	At any point
Note: Up to four signal vias can share a single GND return via.			

11.3 UART

The Jetson Nano brings three UARTs out to the main connector. See Figure 11-5 for typical assignments of the three available UARTs.

Table 11-6. UART Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
99	UART0_TXD	UART3_TXD	UART #0 Transmit. Buffered on module to keep connected devices from affecting state of the pin during power-on as it is one of the SoC strap pins.	M.2 Key E	Output	CMOS – 1.8V
101	UART0_RXD	UART3_RXD	UART #0 Receive	M.2 Key E	Input	
103	UART0_RTS*	UART3_RTS	UART #0 Request to Send	M.2 Key E	Output	
105	UART0_CTS*	UART3_CTS	UART #0 Clear to Send	M.2 Key E	Input	
203	UART1_TXD	UART2_TXD	UART #1 Transmit	Expansion Header	Output	
205	UART1_RXD	UART2_RXD	UART #1 Receive	Expansion Header	Input	
207	UART1_RTS*	UART2_RTS	UART #1 Request to Send	Expansion Header	Output	
209	UART1_CTS*	UART2_CTS	UART #1 Clear to Send	Expansion Header	Input	
236	UART2_TXD	UART1_TXD	UART #2 Transmit. Buffered on module to keep connected devices from affecting state of the pin during power-on as it is one of the SoC strap pins.	Automation Header	Output	
238	UART2_RXD	UART1_RXD	UART #2 Receive	Automation Header	Input	

Notes:
1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The directions for UART[2:0]x are true when used for those functions. Otherwise as GPIOs, the direction is bidirectional.

Figure 11-5. Jetson Nano UART Connections

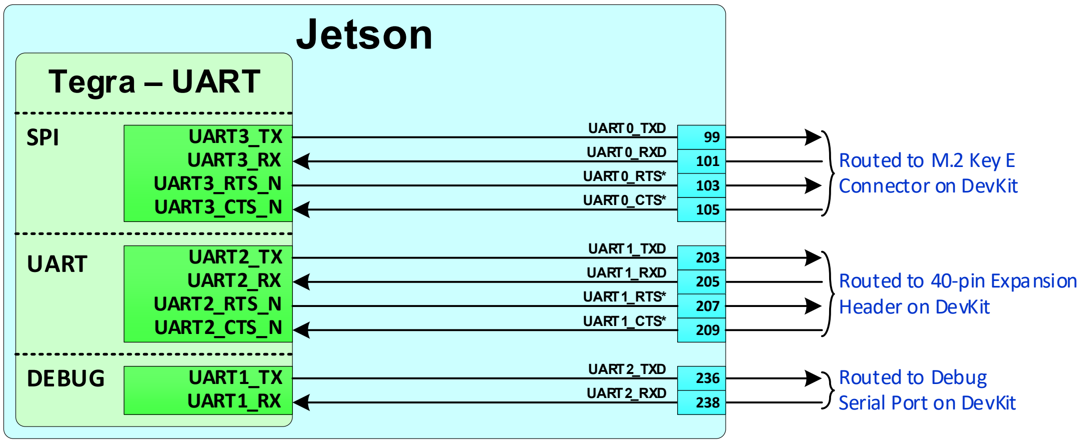


Table 11-7. UART Signal Connections

Ball Name	Type	Termination	Description
UART[2:0]_TXD	O		UART Transmit: Connect to peripheral RXD pin of device
UART[2:0]_RXD	I		UART Receive: Connect to peripheral TXD pin of device
UART[1:0]_CTS*	I		UART Clear to Send: Connect to peripheral RTS pin of device
UART[1:0]_RTS*	O		UART Request to Send: Connect to peripheral CTS pin of device

11.4 Fan

Jetson Nano provides PWM and Tachometer functionality for controlling a fan as part of the thermal solution. Information on the PWM and Tachometer pins/functions can be found in the following locations:

- **Jetson Nano Module Pin Mux:**
  - This is used to configure GPIO14 (PWM) for FAN_PWM and GPIO08 (SDMMC_CD) for FAN_TACH. The pin used for FAN_PWM is configured as PM3_PWM3. The pin used for FAN_TACH is configured as a GPIO.
- **Tegra X1 (SoC) Technical Reference Manual (TRM):**
  - Functional descriptions and related registers can be found in the TRM for the FAN_PWM (PWM chapter).

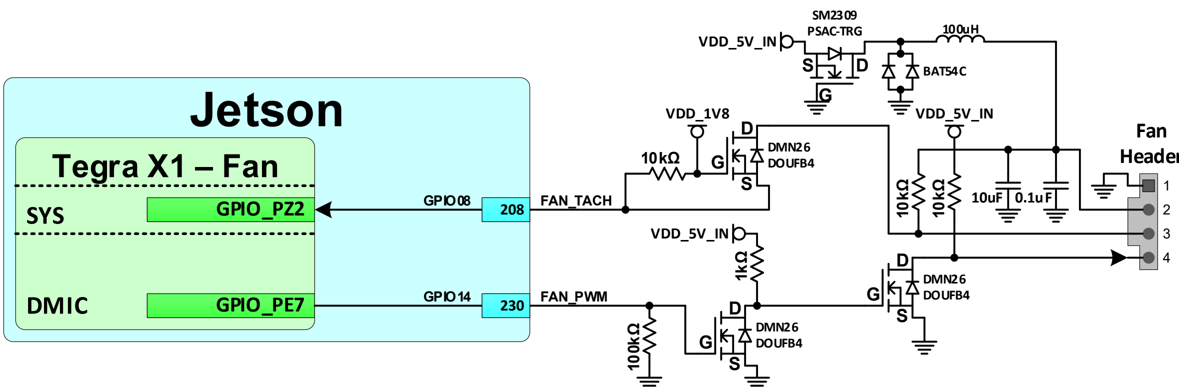
Table 11-8. Fan Pin Description

Pin #	Module Pin Name	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
230	GPIO14	GPIO_PE7	Fan PWM	Fan	Output	CMOS – 1.8V
208	GPIO08	GPIO_PX2	Fan tachometer	Fan	Input	CMOS – 1.8V

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The directions for GPIO14 and GPIO08 are true when used for those functions. Otherwise as GPIOs, the directions are bidirectional.

Figure 11-6. Jetson Nano Fan Connections



11.5 Debug

Jetson Nano supports a UART and JTAG for debugging purposes. The UART intended for debug is UART2 with is routed to a level shifter then to a 12-pin automation header on the developer kit carrier board. JTAG is not brought to the module pins, however, but to test points on the module.

Table 11-9. JTAG and Debug UART Description

Pin #	Module Pin Name (See Note)	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
	JTAG_GP0	JTAG_TRST_N	JTAG test reset	None – JTAG not brought to the module pins on Jetson Nano	Input	CMOS – 1.8V
	JTAG_RTCK	JTAG_RTCK	JTAG return clock		Input	CMOS – 1.8V
	JTAG_TCK	JTAG_TCK	JTAG test clock		Input	CMOS – 1.8V
	JTAG_TDI	JTAG_TDI	JTAG test data In		Input	CMOS – 1.8V

Pin #	Module Pin Name (See Note)	Tegra X1 Signal	Usage/Description	Usage on NVIDIA DevKit Carrier Board	Direction	Pin Type
	JTAG_TDO	JTAG_TDO	JTAG test data Out		Output	CMOS – 1.8V
	JTAG_TMS	JTAG_TMS	JTAG test mode select		Input	CMOS – 1.8V
238	UART2_RXD	UART1_RX	UART 2 receive	Automation Header	Input	CMOS – 1.8V
236	UART2_TXD	UART1_TX	UART 2 transmit		Output	

Notes:

1. In the Type/Dir column, Output is from Jetson Nano. Input is to Jetson Nano. Bidir is for Bidirectional signals.
2. The direction for UART2_RXD is true when used for this function. Otherwise as a GPIO, the direction is bidirectional.
3. JTAG is brought to on-module test points only.

11.5.1 Debug UART

The UART2 interface is intended to be used for debug purposes.

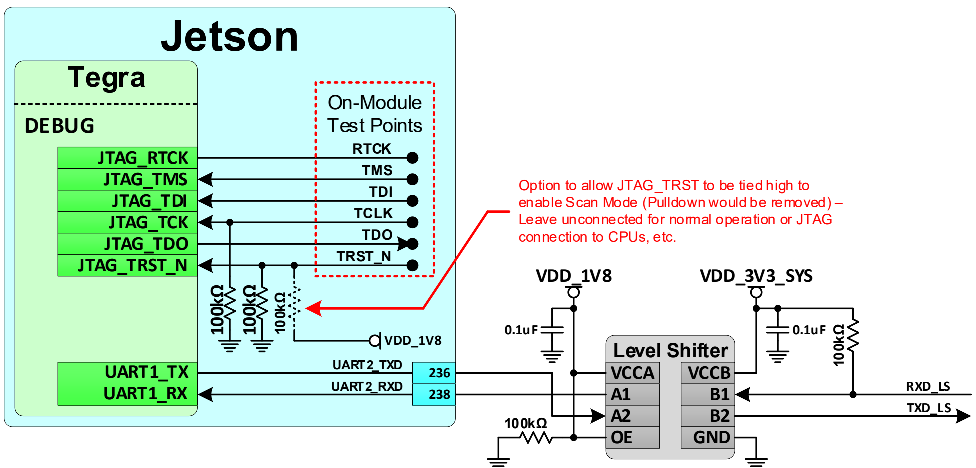
Table 11-10. Debug UART Connections

Module Pin Name	Type	Termination	Description
UART2_TXD	O		UART #2 Transmit: Connect to RX pin of serial device
UART2_RXD	I	If level shifter implemented, 100kΩ to supply on the non-Jetson Nano side of the device.	UART #2 Receive: Connect to TX pin of serial device

11.5.2 JTAG

Jetson Nano provides access to JTAG via test points on the module. Figure 11-7 shows the JTAG and debug UART connections based on the Jetson Nano Developer Kit design.

Figure 11-7. JTAG and Debug UART Connections



> **Notes**:
>
> 1. Pull-ups or Pull-downs are present on the UART TX and RTS lines for RAM Code strapping.
> 2. If level shifter is implemented, pull-up is required on the RXD line on the non-Jetson Nano side of the level shifter. This is required to keep the input from floating and toggling when no device is connected to the debug UART.

Figure 11-8. JTAG Test Point Detail

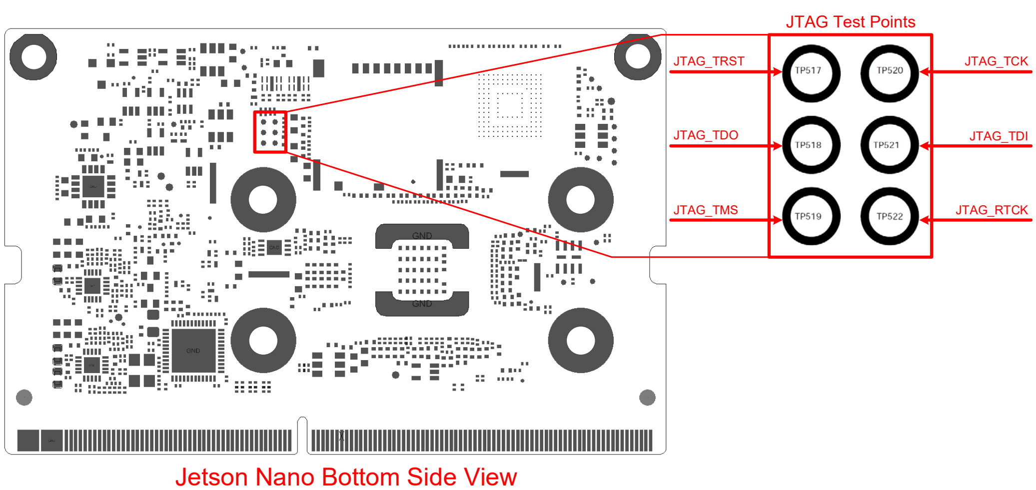


Table 11-11. JTAG Connections

Jetson Nano Test Point Signal Name	Type	Termination	Description
JTAG_TMS	I		JTAG Mode Select: Connect to TMS pin of connector
JTAG_TCK	I	100kΩ to **GND (on module)**	JTAG Clock: Connect to TCK pin of connector
JTAG_TDO	O		JTAG Data Out: Connect to TDO pin of connector
JTAG_TDI	I		JTAG Data In: Connect to TDI pin of connector
JTAG_RTCLK	I		JTAG Return Clock: Connect to RTCK pin of connector
JTAG_TRST_N	I	100kΩ to **GND (on module)**	JTAG Test Reset: This signal is used to select normal operation or scan test mode operation. • Normal operation: Leave pulldown resistor on module installed. • Boundary Scan test mode: Connect **JTAG_TRST_N** to **VDD_1V8** install 100kΩ resistor to VDD_1V8 and remove 100kΩ resistor to GND. Or install strong enough resistor connected to VDD_1V8 to overcome weak 100kΩ pulldown (1ΩΩ to 4.7kΩ).

11.6 USB Recovery Mode

- USB Recovery mode provides an alternate boot device (USB). In this mode, the system is connected to a host system and boots over USB. This is used when a new image needs to be flashed. To enter USB recovery mode, the **FORCE_RECOVERY*** pin is held low when **SYS_RESET*** goes high which can be when the system is powered on or **SYS_RESET*** is asserted after the system is powered on. **FORCE_RECOVERY*** is the SoC RCM0 strap.
- Only **USB0_D_N/P** supports USB Recovery Mode.

No other signals are required or supported for entering Force Recovery mode. Neither VBUS or ID detection is needed. As long as the force recovery strap is held low coming out of reset, Jetson Nano will configure USB0 as a device and enter recovery mode.

See the USB section (Section 6.1) for an example figure that shows USB0 connected to a USB Micro B connector.

Chapter 12. PADS

Jetson Nano signals that come from Tegra X1 may glitch when the associated power rail is enabled. This may affect pins that are used as GPIO outputs. Designers should take this into account. GPIO outputs that must maintain a low state even while the power rail is being ramped up may require special handling.

12.1 Internal Pull-ups for Dual-Voltage Block Pins Powered at 1.8V

Several of the MPIO pads are on blocks designed to be powered at either 1.8V or 3.3V. These blocks are powered at 1.8V on Jetson Nano, and the internal pull-up at initial Power-ON is not effective. The signal may only be pulled up a fraction of the 1.8V rail. Once the system boots, software can configure the pins for 1.8V operation and the internal pull-ups will work correctly. If these signals need the pull-ups during Power-ON, external pull-up resistors should be added. The following list is the affected pins list. These are the Jetson Nano pins on the dual-voltage blocks powered at 1.8V with Power-ON reset default of Internal pull-up enabled.

- SDMMC_DAT0
- SDMMC_DAT1
- SDMMC_DAT2
- SDMMC_DAT3
- SDMMC_CMD
- SPI1_CS0*
- SPI1_CS1*

12.2 Schmitt Trigger Usage

The MPIO pins have an option to enable or disable Schmitt-trigger mode on a per-pin basis. This mode is recommended for pins used for edge-sensitive functions such as input clocks, or other functions where each edge detected will affect the operation of a device. Schmitt-trigger mode provides better noise immunity and can help avoid extra edges from being "seen" by the Tegra inputs. Input clocks include the I2S and SPI clocks (I2Sx_SCLK and SPIx_SCK) when

Tegra is in target mode. The FAN_TACH pin [GPIO8] is another input that could be affected by noise on the signal edges. The SDMMC_CLK pin, while used to output the clock, also sample the clock at the input to help with read timing. Therefore, the SDMMC_CLK pin may benefit from enabling Schmitt-trigger mode. Care should be taken if the Schmitt-trigger mode setting is changed from the default initialization mode as this can influence interface timing.

12.3 Pins Pulled and Driven High During Power-ON

The Jetson Nano is powered up before the carrier board (See Section 5.1). Table 12-1 lists the pins on Jetson Nano that default to being pulled or driven high. Care must be taken on the carrier board design to ensure that any of these pins that connect to devices on the carrier board (or devices connected to the carrier board) do not cause damage or excessive leakage to those devices. Some of the ways to avoid issues with sensitive devices are:

- External pull-downs on the carrier board that are strong enough to keep the signals low are one solution, given that this does not affect the function of the pin.
- Buffers or level shifters can be used to separate the signals from devices that may be affected. The buffer and shifter should be disabled until the device power is enabled.

Table 12-1. Pins Pulled and Driven High by Tegra Prior to SYS_RESET* Inactive

Jetson Nano Pin	Power-ON reset Default	Pull-up Strength (kΩ)		Jetson Nano Pin	Power-ON reset Default	Pull-up Strength (kΩ)
SLEEP/WAKE*	Internal pull-up	~100		SPI0_CS0*	Internal pull-up	~15
FORCE_RECOVERY*	Internal pull-up	~100		SPI0_CS1*	Internal pull-up	~15
UART1_RXD	Internal pull-up	~100		SPI1_CS0*	Internal pull-up	~18
				SPI1_CS1*	Internal pull-up	~18

Table 12-2. Pins Pulled High on Module with External Resistors Prior to SYS_RESET_IN* Inactive

Jetson Nano Pin	Pull-up Supply Voltage (V)	External Pull-up (kΩ)		Jetson Nano Pin	Pull-up Supply Voltage (V)	External Pull-up (kΩ)
I2C0_SCL/SDA	3.3	2.2		SPI1_CS0*	1.8	100
I2C1_SCL/SDA	3.3	2.2		SPI1_CS1*	1.8	100
I2C2_SCL/SDA	1.8	2.2		PCIE0_CLKREQ*	3.3	47
CAM_I2C_SCL/SDA	3.3	2.2		PCIE0_RST*	3.3	4.7
				PCIE_WAKE*	3.3	100

Chapter 13. Unused Interface Terminations

13.1 Unused Multi-purpose Standard CMPS Pad Interfaces

The following Jetson Nano pins (and groups of pins) are Tegra MPIO pins that support either special function IOs (SFIO) and/or GPIO capabilities. Any unused pins or portions of pin groups listed in Table 13-1 that are not used can be left unconnected.

Table 13-1. Unused MPIO Pins and Pin Groups

Jetson Nano Pins and Pin Groups		Jetson Nano Pins and Pin Groups
FORCE_RECOVERY*		SDMMC
GPIO00		I2S
PCIE0_CLK/RST/CLKREQ/WAKE		UART
GPIO07, GPIO13, GPIO14		I2C
DP0_HPD, DP1_HPD, HDMI_CEC		SPI
CAM Control, Clock		

Chapter 14. USB 3.2 and Wireless Coexistence

USB 3.2 supports a 5 Gbps (or multiple) signaling rate. The USB 3.2 specification requires USB 3.2 data to be scrambled and spread spectrum is required. The noise from the USB 3.2 data spectrum has been found from around DC to 4 GHz and beyond. This noise can desensitize nearby receivers operating in the cellular and WiFi 2.4 GHz band. This includes, for example, WiFi 802.11b/g/n or Bluetooth® including Bluetooth mouse devices, Bluetooth keyboards, and so on. This noise causes:

- WiFi sensitivity degradation
- Wireless link throughput drop
- Wireless operation range degradation

This chapter is focusing on USB 3.2. However, other high-speed interfaces such as HDMI, DP, and so on, can also cause issues with wireless subsystems. The issues and recommended mitigation techniques would be similar.

14.1 Mitigation Techniques

Each design is different due to unique construction and relative location of USB 3.2 circuits and connectors and receiving antenna. Depending on the level of noise generated, emitted, radiated, and coupled to receiver antenna, some or all the recommendations might need to be implemented to limit unwanted noise from radiating from the circuit.

The following mitigation techniques described will help minimize the USB 3.2 de-sense.

INCREASE THE USB 3.2 TO ANTENNA SEPARATION

During the placement phase of the design, care must be taken to identify the noise source and try to physically increase the separation between the noise source and antenna. One of the major noise sources is the USB 3.2 connector itself. If possible, the antenna or USB 3.2 location can be changed to increase physical isolation. In general, doubling the distance between antenna and noise source, reduces the coupling by around 6 dB.

USB 3.2 CONNECTOR PART SELECTION: CHOOSE A BETTER USB 3.2 PART

A USB 3.2 connector has many metal fingers that are perfect in length for radiating in and around the 2.4 GHz band and beyond. A USB 3.2 connector should be selected to minimize radiation from the USB 3.2 part itself. Some recommendations are:

- Connector fully enclosed by metal
- No slots in the connector walls, or if there are slots, the size is very small. Also, the number of slots should be minimal.
- Connector has as many grounding legs as possible. More legs provide better grounding from the USB 3.2 exterior to the PCB and the structure is less likely to radiate. Choose four legged connectors over two legged connectors and so on.

The quality of the external USB 3.2 device used in the USB 3.2 port will have impact on the overall experience. If the external USB 3.2 device used in the USB 3.2 port is of poor quality, the part itself will radiate and issues will continue. A plastic base USB 3.2 device works inferior compared to fully metalized USB 3.2 devices.

GROUND THE USB 3.2 PART SOLIDLY

The USB 3.2 connector is grounded through "the grounding legs" previously mentioned. Care must be taken to ensure the leg area is a very good RF ground. One way to do this is to increase the number of ground vias placed in the "grounding leg" area.

IMPROVE THE ROUTING AND GROUNDING AROUND THE USB 3.2 PART AREA

The routing and grounding around the USB 3.2 connector part area must be handled carefully. Since this area is very "hot," any traces running on the surface layer below the physical connector part can pick up noise and transfer it to other areas or radiate the noise. These traces need to be moved to an inner layer, and this area needs to be made a very good ground.

BURY THE USB 3.2 LINES IN INNER LAYERS

The USB 3.2 lines should be routed as impedance controlled differential pairs, with ground on either side and on the layers above and below.

SHIELD THE USB 3.2 CONNECTOR PART

The radiation from the USB 3.2 connector part is very strong. Need to make a "shield" and put on top of the USB 3.2 connectors. The shield must touch the USB 3.2 body in multiple points. The shield track must have number of grounding vias so that any emitted noise from the USB 3.2 connector is swiftly grounded.

Chapter 15. Jetson Nano Pin Descriptions and Design Checklist

The Jetson Nano pin description and design checklist are attached to this design guide.

To access the attached files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the documents. Excel files with the .nvxlsx extension will need to be renamed to .xlsx to open.

Chapter 16. General Routing Guidelines

16.1 Signal Name Conventions

The following conventions are used in describing the signals for Tegra:

- Signal names use a mnemonic to represent the function of the signal. For example, Secure Digital Interface #3 Command signal is represented as **SDMMC_CMD**, and in a different font to distinguish it from other text. All active-low single-ended signals are identified by an asterisk (*) after the signal name. For example, **SYS_RESET*** indicates an active-low signal. Active-high signals do not have the asterisk after the signal name. For example, **SDMMC_CMD** indicates an active-high signal. Differential signals are identified as a pair with the same names that end with _P and _N (for positive and negative, respectively). For example, **CSI_0_D0_P** and **CSI_0_D0_N** indicate a differential signal pair.
- The signal I/O type is represented as a code to indicate the operational characteristics of the signal. The following table lists the I/O codes used in the signal description tables.

Table 16-1. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

16.2 Routing Guideline Format

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from BGA ball either to a point beyond the ball array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 12.5 mm unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow max and min trace delays where specified. Trace delays are typically shown in "mm" (millimeter) in terms of signal delay in "ps" (pico-seconds) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing.
  - Spacing to other signals/pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) and inner (stripline) layers of a PCB.

16.3 Signal Routing Conventions

Throughout this design guide, the following signal routing conventions are used:

- SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing
  - SE impedance of trace (along with diff impedance for diff pairs) is achieved by spacing requirement. Spacing is multiple of dielectric height. Dielectric height is typically different for microstrip and stripline.

Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

16.4 General Routing Guidelines

Pay close attention when routing high speed interfaces, such as HDMI/DP, USB 3.2, PCIe or DSI/CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay/flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this design guide.

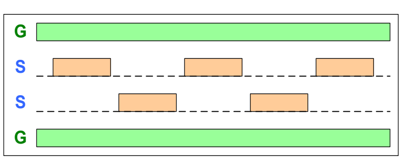
- **Controlled Impedance**
  Each interface has different trace impedance requirements and spacing to other traces. It is up to designer to calculate trace width and spacing required to achieve specified SE and Diff impedances. Unless otherwise noted, trace impedance values are ±15%.

- **Max Trace Lengths/Delays**
  Trace lengths/delays should include the carrier board PCB routing (where the Jetson Nano mating connector resides) and any additional routing on a Flex/ secondary PCB segment connected to main PCB. The max length/delay should be from Jetson Nano to the actual connector (i.e. USB, HDMI, etc.) or device (i.e. onboard USB device, Display driver IC, camera imager IC, etc.)
- **Trace Delay/Flight Time Matching**
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths within specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - For six layers or more, it is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 5.9 ps/mm and inner-layer 6.9 ps/mm. If one signal is routed 250 mm on the outer layer and second signal is routed 250 mm in the inner layer, the difference in flight time between two signals will be 250 ps! That is a big difference if required matching is 15 ps (trace delay matching). To fix this, inner trace needs to be 36 mm shorter or outer trace needs to be 42 mm longer.
  - In this design guide, terms such as intra-pair and inter-pair are used when describing differential pair delays. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pair average delays.

16.5 General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (see Figure 6-1).

Figure 16-1. GSSG Stack-Up



Do not route other signals or power traces/areas directly under or over critical high-speed interface signals.

Note: The requirements detailed in the interface signal routing requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.

16.6 Common High-Speed Interface Requirements

Table 16-2 provides the common high-speed interface requirements.

Table 16-2. Common High-Speed Interface Requirements

Parameter	**Requirement**	**Units**	**Notes**
Common-mode Choke (Not recommended – only used if absolutely required for EMI issues)			
Preferred device			Type: TDK ACM2012D-900-2P. Only if needed. Place near connector. See Figure 16-2
Location - Max distance from to adjacent discontinuities – ex, connector, AC cap)	8 (53)	mm (ps)	TDK ACM2012D-900-2P See Figure 16-2
Common-mode impedance @ 100MHz Min/Max	65/90	Ω	
Max Rdc	0.3	Ω	
Differential TDR impedance	90	Ω	@T_R-200ps (10%-90%)
Min Sdd21 @ 2.5GHz	2.22	dB	
Max Scc21 @ 2.5GHz	19.2	dB	
Serpentine			
Min bend angle	135	deg (α)	S1 must be taken care in order to consider Xtalk to adjacent pair. See Figure 16-3
Dimension Min A Spacing Min B, C Length Min Jog Width	4x 1.5x 3x	Trace width	
General			
Routing over Voids	Routing over voids not allowed except void around device ball/pin the signal is routed to.		
Noise Coupling	Keep critical high-speed traces away from other signal traces or unrelated power traces/areas or power supply components		

The following figures are the common high-speed interface signal routing requirements figures.

Figure 16-2. Common Mode Choke

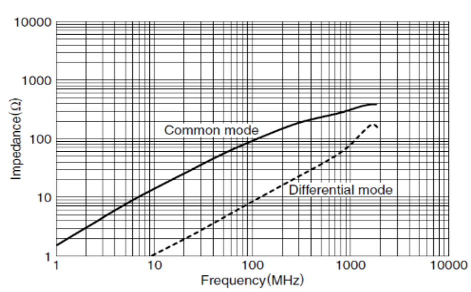
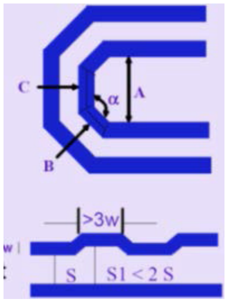


Figure 16-3. Serpentine



16.7 Test Points for High-Speed Interfaces

Ideally, test points are not preferred on very high-speed interface traces as they can degrade signal integrity. However, to be able to do compliance testing, or interface tuning where applicable, it may be necessary to include test points at least for early revisions of a design. The test points are generally required near the receiver. If a connector or some other device (capacitor, resistor, and so on) exists near the receiver, the pins can be used as test points without creating additional signal degradation. Where connector or discrete device pins are not accessible near the receiver end of an interface, it may be necessary to include test points. When test points are needed for very high-speed interface signals, follow these recommendations:

- Test points should be very small (less than 0.5 mm).
- Test points should be located on the existing trace (no stub).

If the test points are placed on differential signals, they should be symmetric for each P and N signal.

NVIDIA Corporation | 2788 San Tomas Expressway, Santa Clara, CA 95051

http://www.nvidia.com