# One-Sided Schmitt-Trigger-Based 9T SRAM Cell for Near-Threshold Operation

Keonhee Cho, Juhyun Park, Tae Woo Oh, and Seong-Ook Jung, *Senior Member, IEEE*

***Abstract*— This paper presents a one-sided Schmitt-trigger-based 9T static random access memory cell with low energy consumption and high read stability, write ability, and hold stability yields in a bit-interleaving structure without write-back scheme. The proposed Schmitt-trigger-based 9T static random access memory cell obtains a high read stability yield by using a one-sided Schmitt-trigger inverter with a single bit-line structure. In addition, the write ability yield is improved by applying selective power gating and a Schmitt-trigger inverter write assist technique that controls the trip voltage of the Schmitt-trigger inverter. The proposed Schmitt-trigger-based 9T static random access memory cell has 0.79, 0.77, and 0.79 times the area, and consumes 0.31, 0.68, and 0.90 times the energy of Chang's 10T, the Schmitt-trigger-based 10T, and MH's 9T static random access memory cells, respectively, based on 22-nm FinFET technology.**

***Index Terms*— Bit interleaving, low energy, near-threshold, Schmitt-trigger, static random access memory (SRAM).**

## I. Introduction

LOW energy consumption has become important in the design of system-on-chips (SoCs), such as bio implants, mobile devices, self-powered wireless sensors, and energy harvesting devices, because they operate with limited energy from a battery or harvesting. Because static random access memory (SRAM) occupies a significant area on the SoC [1], reducing the energy consumption of SRAM is a critical way to reduce the energy consumption of the SoC. The most effective way to reduce energy consumption is to reduce power by scaling down the supply voltage ($V_{DD}$). As the $V_{DD}$ scales down, the power decreases quadratically [2]. However, as $V_{DD}$ scales down, the delay and soft error rates (SERs) increase, and operational yields degrade.

In the sub-threshold voltage ($V_{th}$) region where $V_{DD}$ is lower than $V_{th}$, the delay increases exponentially. Thus, the energy consumption is increased because of the significantly increased static energy consumption, even though very low power is achieved. Operation in the near-$V_{th}$ region where $V_{DD}$ is slightly higher than $V_{th}$ can achieve a large power reduction compared with super-$V_{th}$ operation, and a very large improvement in delay compared with sub-$V_{th}$ operation. As a result, energy consumption can be minimized by optimization between power and delay in the near-$V_{th}$ region [3].

The soft error induced by $\alpha$-particles becomes a problem in near-$V_{th}$ operation [4], [5]. This is because the SER is increased by the shrunken critical charge in near-$V_{th}$ operation [6]. In the non-bit-interleaving structure, in which the bits of a word are stored consecutively, a multi-bit error can occur in one word. This is because when a soft error occurs, bit errors occur simultaneously in cells that are spatially close to each other. Multi-bit error correction requires the structure of the error correction code (ECC) circuit to have a very large area and energy consumption. However, in bit-interleaving structure, single bit errors occur in each word because the bits of a word are spatially interleaved. Single-bit errors can be corrected by using a simple ECC circuit [7]. Therefore, in the near-$V_{th}$ region, the bit-interleaving structure has been applied to resolve the increased SER.

In the near-$V_{th}$ region, the transistor current is highly susceptible to $V_{th}$ variation. In particular, SRAM cells are vulnerable to $V_{th}$ variation because they should be designed with small size transistors for high density in a limited area. In addition, because in the conventional 6T SRAM cell there is a trade-off between read stability and write ability, it is difficult to obtain sufficient read stability and write ability simultaneously. Various SRAM cells have been proposed to achieve sufficient read stability and write ability in the near-$V_{th}$ region [5], [7]–[11]. However, these SRAM cells have some drawbacks, such as requirement of write-back scheme for bit-interleaving structure, large SRAM cell size, or high energy consumption. In this paper, we propose an Schmitt-trigger-based 9T (ST 9T) SRAM cell that uses a bit-interleaving structure without write-back scheme, and has a lower energy consumption than other SRAM cells within a smaller SRAM cell area while ensuring sufficient read stability and write ability in the near-$V_{th}$ region by using the following features: (1) improvement in read stability by using the cross-coupled structure of standard and Schmitt-trigger (ST) inverters, (2) reduction in energy consumption and area by using a single bit-line (BL) structure, and (3) write ability improvement by using a selective power gating technique with the ST inverter write assist technique.

This paper is organized as follows. The design and problems of previous SRAM cells are described in Section II. In Section III, the proposed 9T SRAM cell is introduced.

Manuscript received August 22, 2019; revised December 11, 2019, January 3, 2020, and January 5, 2020; accepted January 5, 2020. Date of publication February 26, 2020; date of current version May 1, 2020. This work was supported by the IT Research and Development Program of MOTIE/KEIT under Grant 10052716 and in part by the Design Technology Development of Ultra-Low Voltage Operating Circuit and IP for Smart Sensor SoC. This article was recommended by Associate Editor M. Mozaffari Kermani. *(Corresponding author: Seong-Ook Jung.)*

The authors are with the School of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, South Korea (e-mail: sjung@yonsei.ac.kr).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2020.2964903

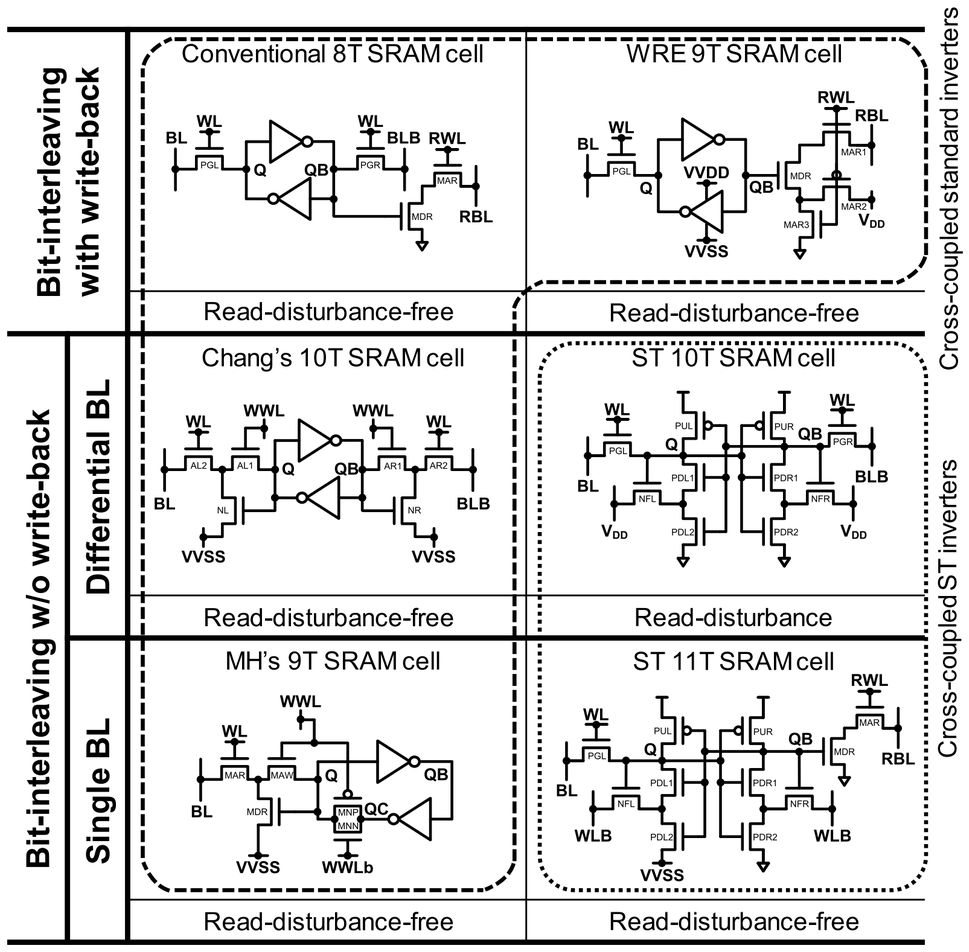


Fig. 1. Schematics of the previous SRAM cells.

Section IV compares simulated results for the previous and proposed cells that operate in the near-$V_{th}$ region, based on 22-nm FinFET technology. Finally, the conclusion is drawn in Section V.

## II. Previous SRAM Cell Design

Various SRAM cells (MH's 9T [5], Chang's 10T [7], conventional 8T [8], write- and read-enhanced (WRE) 9T [9], ST 10T [10], ST 11T [11]) have been proposed for near-$V_{th}$ operation as shown in Fig. 1. The conventional 6T and 8T, WRE 9T, Chang's 10T, and MH's 9T SRAM cells have cross-coupled standard inverters, while ST 10T and ST 11T SRAM cells have cross-coupled ST inverters. In addition, the SRAM cells will be classified into read-disturbance and read-disturbance-free cells, depending on whether the storage node suffers from read disturbance.

The conventional 6T SRAM cell can be classified into read-disturbance cell because the read disturbance from BL or BLB can flip the stored data. The conventional 8T SRAM cell adds a read buffer to resolve a read disturbance problem. Because the read buffer decouples the storage node from read BL, the conventional 8T SRAM cell has the same read stability as hold stability. Thus, the conventional 8T SRAM cell ensures sufficient read stability. The WRE 9T SRAM cell improves leakage current of the read buffer as well as write ability by using power gating. During the write operation, however, the conventional 8T and WRE 9T SRAM cells experience read disturbance from BL or BLB. Thus, the bit-interleaving structure can be applied only by using write-back scheme that increases the delay, energy consumption, and area.

To apply a bit-interleaving structure without write-back scheme, Chang's 10T, ST 10T, MH's 9T, and ST 11T SRAM cells have been proposed. Chang's 10T SRAM cell has read buffers and additional transistors that are connected in series to the pass gate (PG). These transistors are controlled by a column-based write word-line (WWL) signal. The row half-selected cells in the un-selected column are decoupled from BL by turning off the additional transistor in the write operation, so a half-selected cell problem does not occur. The ST 10T SRAM cell is classified into read-disturbance cell. Although the ST 10T SRAM cell experiences read disturbance, the stored data is not flipped because the ST inverters improve read stability. However, Chang's 10T and ST 10T SRAM cells have area and energy consumption overheads due to the number of transistors and differential BL structure.

The read energy consumption is significant in SRAM energy consumption, because SRAM performs the write operation only when a cache miss occurs and performs the read operation most of the time [12]. During the read operation of SRAM that uses a differential BL structure, either BL or BLB should be discharged to almost 0 V in all columns in the near-$V_{th}$ region. This is because the cell current in the near-$V_{th}$ region has large variation, and the cell with the smallest current requires a long time to achieve a sufficient voltage difference for the differential sense amplifier (SA) [13]. Thus, the read energy consumption of a single BL structure is stochastically one half that of the differential BL structure because the BL may or may not discharge depending on the read data [13].

MH's 9T and ST 11T SRAM cell use a single BL structure for read operation. MH's 9T SRAM cell has a read buffer and a transmission gate between the cross-coupled standard inverters. Thus, it achieves a high read stability by using the read buffer and improves its write ability by cutting off the positive feedback in the cross-coupled standard inverters by turning off the transmission gate. However, MH's 9T SRAM cell has area overhead owing to the many control signals, and it cannot sufficiently improve write-1 ability due to the weak write-1 drivability of nMOS PG. In addition, the delay can be degraded due to the row-based VVSS structure in the worst case read operation, where all cells in the selected row store data Q = "1". This is because the current bottleneck is caused in the cell located farthest from the VVSS driver due to the limited discharging current by the size of the VVSS driver and wire resistance and capacitance.

The ST 11T SRAM cell uses cross-coupled ST inverters with a read buffer. Hold stability is improved by the cross-coupled ST inverters, and read stability is improved by the read buffer. The row-based floating VVSS scheme improves write-1 ability by weakening the pull-down transistor. However, the ST 11T SRAM cell has a large area owing to the large number of transistors. In addition, in the case that only one cell performs the write-1 operation, and all other cells perform the write-0 operation, VVSS is driven by the write-0 cells. As a result, the improvement in write-1 ability is not significant.

## III. Proposed ST 9T SRAM Cell

Figs. 2(a) and (b) show the schematic and operational timing diagram of the proposed ST 9T SRAM cell having a single BL structure. The proposed ST 9T SRAM cell consists of a cross-coupled structure of a standard inverter with stacked transistors (PUL1, PUL2, PDL1, PDL2), an ST inverter

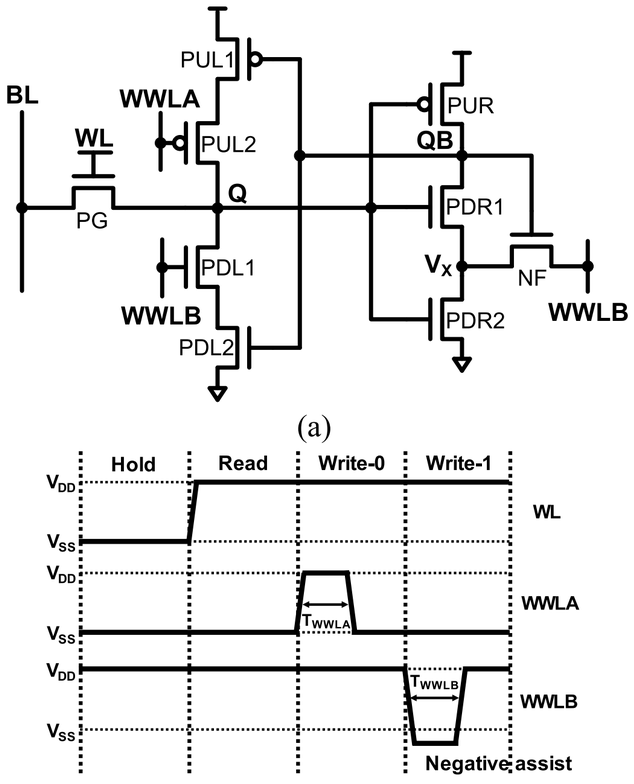


Fig. 2. (a) Schematic, (b) operation timing diagram of the proposed ST 9T SRAM cell.

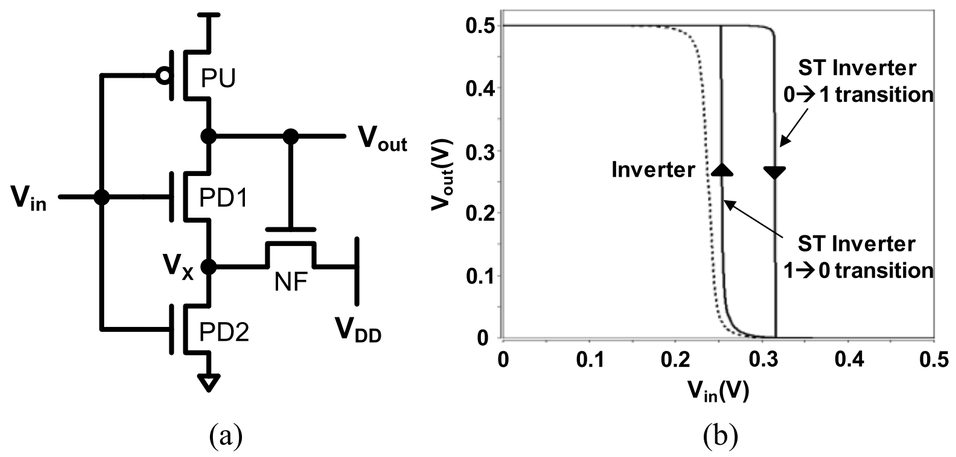


Fig. 3. (a) Schematic of the ST inverter, (b) characteristics of standard inverter and ST inverter at $V_{DD} = 0.5$ V.

(PUR, PDR1, PDR2, NF), and one nMOS PG. Word-line (WL) is a row-based signal; write word-line A (WWLA) and write word-line B (WWLB) are column-based signals. WL and WWLA are connected to the gates of PG and PUL2, respectively. WWLB is connected to both the gate of PDL1 and the source of NF.

### *A. Read Operation*

In the read operation, WWLA and WWLB are "0" and "1," and thus PUL2 and PDL1 are turned on, respectively. The storage node Q is driven by the standard inverter. At the same time, WL is enabled, and PG is turned ON. Then, the BL is discharged or not, depending on the stored data at node Q. Read failure is commonly caused by a read disturbance from BL. When the storage node is bumped by a read disturbance and the voltage of the storage node exceeds the trip voltage of the inverter, the stored data can be flipped. The proposed ST 9T SRAM cell solves this read failure problem by using a cross-coupled structure of standard and ST inverters.

Figs. 3(a) and (b) show the schematic and DC characteristics of the ST inverter, respectively. When the input voltage ($V_{in}$) transits from "0" to "1," the ST inverter has a higher trip voltage than the standard inverter. This is because the strength of PD1 is weakened by the $V_X$ increased through the feedback transistor NF. Thus, when the storage node is bumped by a read disturbance, the ST inverter is more robust to the read disturbance than the standard inverter.

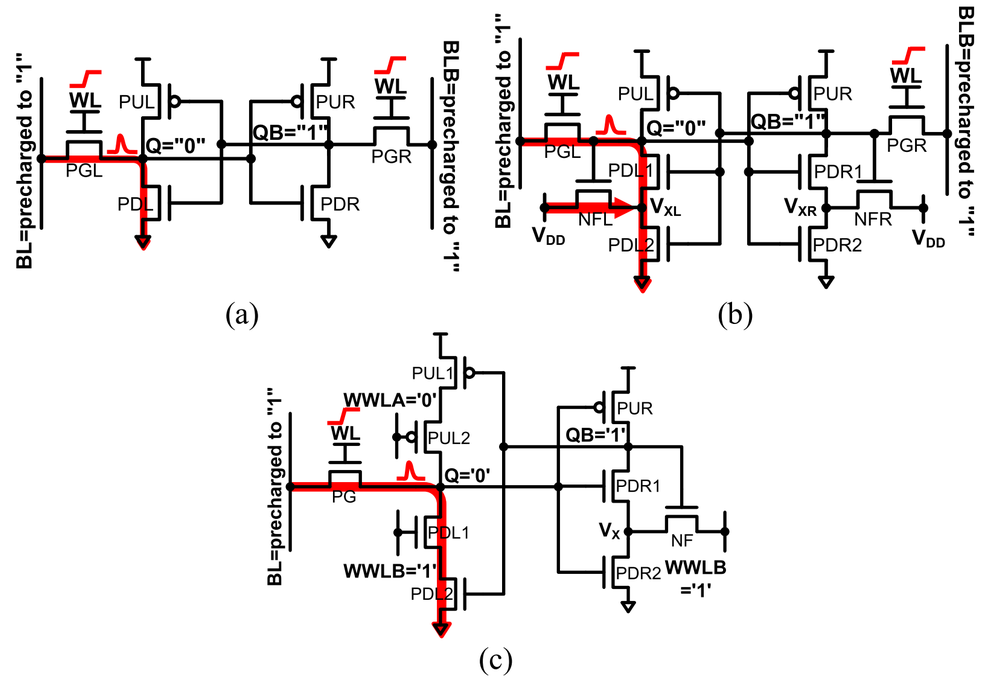


Fig. 4. Read operation (a) in conventional 6T, (b) ST 10T, and (c) the proposed ST 9T SRAM cells.

Fig. 4(a), (b), and (c) shows the bumped storage node in the read-disturbance cells. The ST 10T and proposed ST 9T SRAM cells improve the read stability through the benefit of ST inverter. Furthermore, the proposed ST 9T SRAM cell has a larger read stability than ST 10T SRAM cell where the ST inverters are cross-coupled. The reason is as follows. When the node Q storing the data "0" in the ST 10T SRAM cell is bumped by the read disturbance, NFL is slightly turned ON and the strength of PDL1 is weakened by the increase in $V_{XL}$ through NFL. As a result, the magnitude of the read disturbance increases. On the other hand, the proposed ST 9T SRAM cell avoids this problem by using a cross-coupled structure of standard and ST inverters. This is possible because the read disturbance only occurs when storage node Q is "0" in the single BL structure.

This concept was verified using the butterfly curves of the read-disturbance cells. Fig. 5 shows the magnitude of the read static noise margin (RSNM) when Q is "0" and QB is "1" in the conventional 6T, ST 10T, and the proposed ST 9T SRAM cells. The length of the square indicates the RSNM. The RSNM of the proposed ST 9T SRAM cell is larger when Q stores "1" than when it stored "0" due to asymmetrical structure. For the fair comparison with the other SRAM cells, the worst case RSNM was considered in the proposed ST 9T SRAM cell. The RSNM of the ST 10T SRAM cell is larger than that of the conventional 6T SRAM cell because of the increased trip voltage of the ST inverter. Moreover, the proposed ST 9T SRAM cell achieves the largest RSNM by avoiding the bad effects caused by the magnitude of the read disturbance in the ST 10T SRAM cell.

### *B. Write Operation*

The write operation differs depending on the written data. Fig. 6(a) shows a write-0 operation. During the write-0

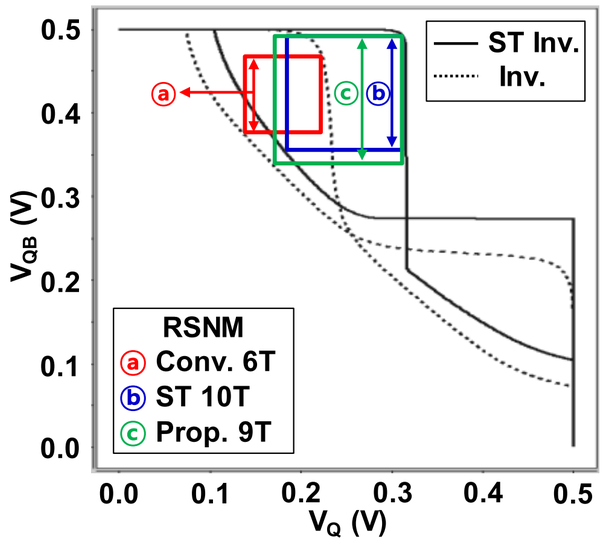


Fig. 5. Comparison of the butterfly curve in the read-disturbance cells.

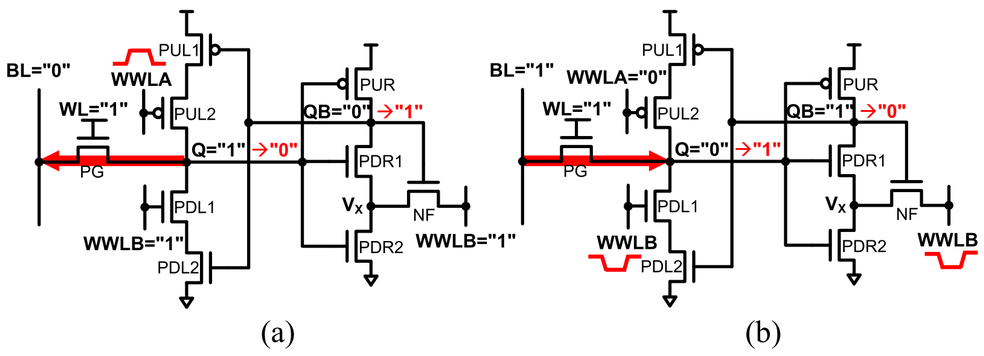


Fig. 6. (a) Write-0, and (b) write-1 operations in the proposed ST 9T SRAM cell.

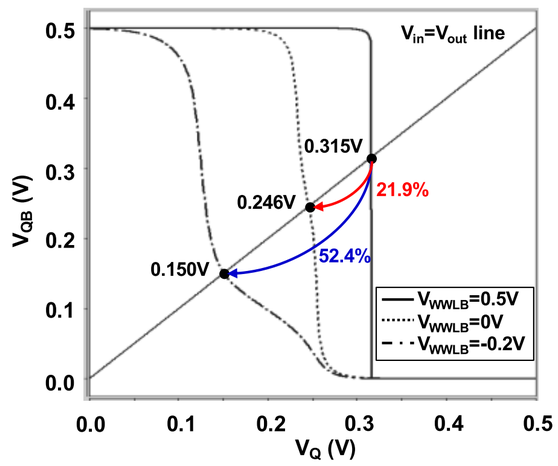


Fig. 7. DC characteristics and trip voltage of the ST inverter when negative $V_{WWLB}$ is applied at $V_{DD}$ = 0.5 V.

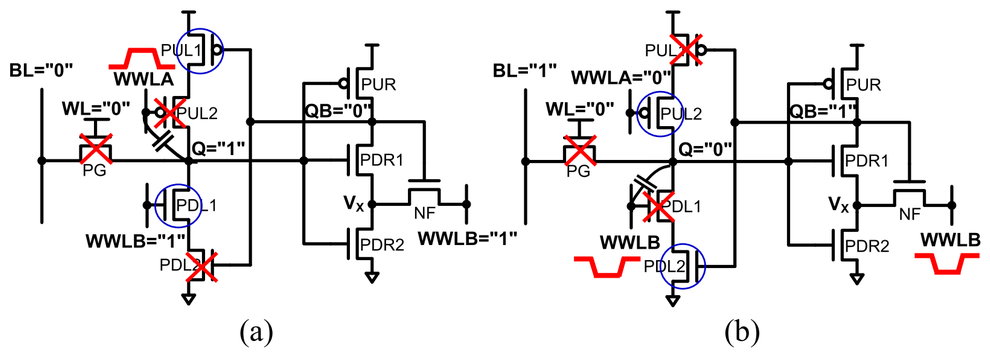


Fig. 8. The column half-selected cells during (a) write-0, and (b) write-1 operations.

operation, the column-based WWLB remains "1", the write driver drives BL to "0", and the WL is enabled. As the column-based WWLA is changed to "1" to disconnect the path from the $V_{DD}$ power source by turning off PUL2, node Q storing data "1" is power-gated. The power-gated Q node is driven to "0" through the turned-on PG, and the ST inverter is flipped. The column-based WWLA is reset to "0" after the stored data of node QB is flipped. The pulse width of WWLA ($T_{WWLA}$) is determined considering the column half-selected cell, which will be discussed in detail in the following section. The proposed ST 9T SRAM cell adopts a single PG instead of the series PGs used in Chang's 10T or MH's 9T SRAM cells, and disconnects the path from the $V_{DD}$ power source by turning off PUL2 in the write-0 operation. As a result, the proposed ST 9T SRAM cell achieves sufficient write-0 ability.

Fig. 6(b) shows a write-1 operation. During the write-1 operation, the column-based WWLA remains "0", the write driver drives BL to "1", and the WL is enabled. As the column-based WWLB is changed to "0" to disconnect the path from the $V_{SS}$ power source by turning off PDL1, the node Q storing data "0" is power-gated. In addition, the trip voltage of the ST inverter becomes similar to that of a standard inverter because the feedback mechanism of the ST inverter is removed. The power-gated Q node is driven to "1" through the turned-on PG, and the ST inverter is flipped. The column-based WWLB is reset to "1" after the data stored in node QB is flipped. The pulse width of WWLB ($T_{WWLB}$) is determined considering the column half-selected cell. Similar to the write-0 operation, the write-1 operation is supported by disconnecting the path from the $V_{SS}$ power source. However, because nMOS PG has a weak write-1 drivability, the write-1 ability cannot be sufficiently ensured.

The novel negative $V_{WWLB}$ assist technique is applied to improve write-1 ability in the proposed ST 9T SRAM cell. When WWLB is driven to a negative voltage, the Vx node is instantaneously driven to a negative voltage through the turned-on NF. The decrease in Vx means that the strength of PDR1 increases, which significantly reduces the trip voltage of the ST inverter. This makes the write-1 operation easy. Fig. 7 shows how much the trip voltage changes. When WWLB is forced to be "0" in the write-1 operation, the trip voltage of the ST inverter is reduced by 21.9% as the feedback mechanism of the ST inverter is eliminated, and it becomes similar to that of the inverter. When WWLB is driven to the negative voltage of -0.2 V, the trip voltage is reduced by 52.4%. Therefore, the negative $V_{WWLB}$ assist technique can significantly improve the write-1 ability by decreasing the trip voltage.

### *C. Half-Selected Cell Issue*

During the read and write operations, the data at the half-selected cells should remain stable, and thus the hold stabilities at these cells should be considered in SRAM design. To apply a bit-interleaving structure, the hold stability in the row half-selected cell in all operations should be sufficiently ensured. During read and write operations, the row half-selected cells experience a disturbance from BL as the selected cell in the read operation. Because the read stability in the selected cell is sufficiently ensured, there are no stability problems in the row half-selected cells.

Fig. 8 shows the column half-selected cells during write-0 and write-1 operations. As the column-based WWLA

TABLE I

TECHNOLOGY PARAMETERS FOR $V_{DD} = 0.8$ V

| Parameter | NMOS | PMOS |
|---|---|---|
| Gate length | 34 nm | 34 nm |
| Equivalent oxide thickness | 0.9 nm | 0.9 nm |
| Fin thickness | 8 nm | 8 nm |
| Fin height | 34 nm | 34 nm |
| On-current | 880 μA/μm | 780 μA/μm |
| Off-current | 1 nA/μm | 1 nA/μm |
| Sub-threshold swing | 69 mV/dec | 72 mV/dec |
| DIBL | 46 mV/V | 50 mV/V |
| Threshold voltage ($V_{th}$)[(a)] | 230 mV (Sat.)<br>264 mV (Lin.) | 245 mV (Sat.)<br>283 mV (Lin.) |
| $C_{gg}$ | 1.47 fF/μm | |
| $C_d$ | 0.33 fF/μm | |

[(a)] Vth in the saturation and linear model are measured as $V_{GS}$ when the drain current per effective width is $10^{-5}$ A/μm with $|V_{DS}| = V_{DD}$ and $|V_{DS}| = 0.05$V.

and WWLB turn off PUL2 and PDL1, respectively, the storage node Q in the column half-selected cell can be floating for a moment, but the hold stability of the column half-selected cell is sufficiently ensured. The reason is as follows. The column half-selected cell becomes more stable by the coupling effect between the storage node Q and WWLA (or WWLB), because the floated node Q storing "1" (or "0") becomes higher than $V_{DD}$ (or lower than GND) by the rise in WWLA (or the fall in WWLB). In addition, the sufficiently short floating time of storage node Q can be achieved by controlling $T_{WWLA}$ and $T_{WWLB}$, because the data flip time is very short [14]. As a result, in the proposed ST 9T SRAM cell, the hold stability in the half-selected cell can be sufficiently ensured.

## IV. SIMULATION RESULT AND COMPARISON

The proposed ST 9T and previous SRAM cells are compared in 22-nm FinFET technology. HSPICE Monte Carlo simulations are performed with a BSIM-CMG model [15]. The characteristics of this model are fitted to those of a commercial low-power device model based on the experiment results with 22-nm FinFET technology [16]. Table I shows detailed parameter. The distribution of $V_{th}$ is modeled as a Gaussian distribution where the standard deviation ($\sigma_{Vth}$) is expressed as:

$$\sigma_{Vth} = \frac{A_{Vt}}{\sqrt{Length \times Width}} \quad (1)$$

where the Pelgrom coefficient ($A_{vt}$) was set to 1.8 mV·$\mu$m [17].

The static and dynamic metrics such as static noise margin [1], word line write trip voltage [18], dynamic read noise margin, or dynamic write noise margin [19] are commonly used to estimate a hold stability, read stability, or write ability yield. The distribution of these metrics are fitted to the Gaussian distribution and the yields are determined by the mean and standard deviation of the fitted distribution. However, this method may not be accurate because the distribution of these metrics do not follow a Gaussian distribution [20]. Instead of theses metrics, importance sampling can be a good alternative for estimating operational yields with high reliability in this study [21]. In importance sampling, the operational yields are calculated by summing weight values calculated by the mean-shifted magnitude of each transistor $V_{th}$ in the fail samples. The fail samples in each operation are obtained from 10,000 Monte Carlo samples. It is assumed that the SRAM cell array has 256 rows and 128 columns with 4:1 bit-interleaving structure. The wire parasitic resistance and capacitance are considered using a $\pi$-model with 21 Ω/$\mu$m and 0.16 fF/$\mu$m, respectively, according to [22]. The target yield is $5\sigma$ to guarantee a fail rate of less than 1 per million [23].

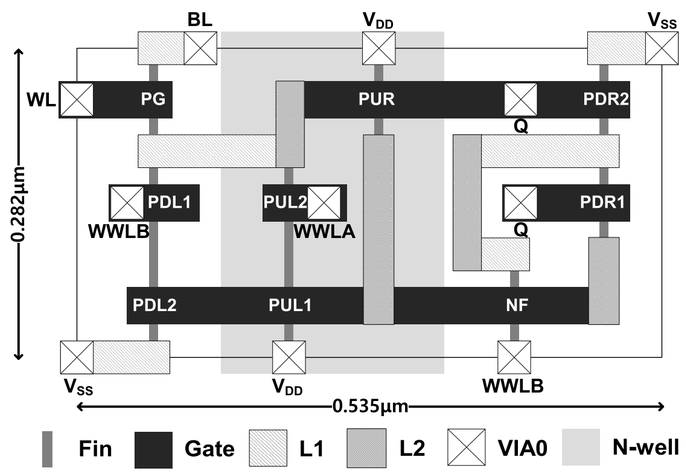


Fig. 9. Layout of proposed ST 9T SRAM cell based on 22-nm FinFET technology.

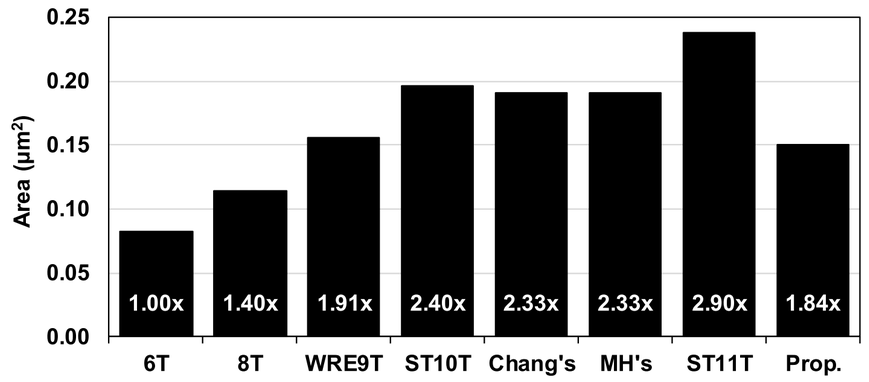


Fig. 10. Cell area comparison of proposed ST 9T with previous SRAM cells.

### A. Cell Area

Fig. 9 shows the layout of the proposed ST 9T SRAM cell with the 22-nm FinFET design rule reported in [24], [25]. A constant gate pitch is used for regularity of the layout [26]. The number of metal layers is reduced by applying local wires (L1, L2) in the middle of the layer [27]. $V_{DD}$ and $V_{SS}$ are routed by metal 1, BL and WWLA are routed by metal 2, WL is routed by metal 3, and $V_{SS}$ and WWLB are routed by metal 4.

Fig. 10 shows the comparison result of the cell area. All transistors in the previous and proposed SRAM cells are designed with a single fin to minimize the cell area. The proposed ST 9T SRAM cell has a smaller area than Chang's 10T, the ST 10T, and ST 11T SRAM cells because it has a fewer number of transistors. In addition, the proposed ST 9T SRAM cell has a smaller area than WRE 9T and MH's 9T SRAM cells thanks to a smaller number of control signals. As a result, the proposed ST 9T SRAM cell has an approximately 24% larger area than conventional 8T SRAM cell, but 4%, 21%, 23%, 21%, and 37% smaller area than WRE 9T, Chang's 10T, ST 10T, MH's 9T, and ST 11T SRAM cells, respectively.

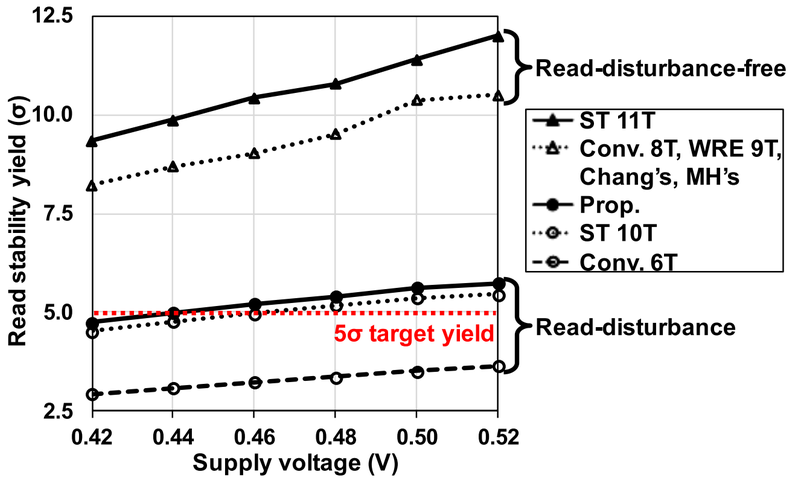


Fig. 11. Read stability yield of previous and proposed ST 9T SRAM cells.

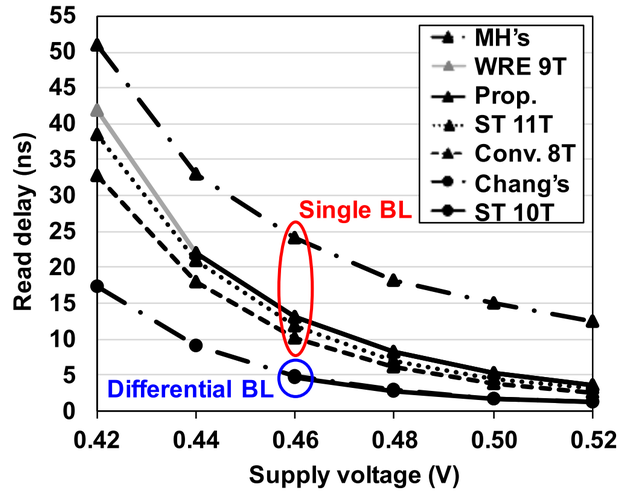


Fig. 12. Read delay in the proposed, and previous SRAM cells.

### *B. Read Stability*

Read failure is measured when the previously stored data in the selected cell is flipped during read operations. Fig. 11 shows the comparison result of the read stability yield. The SRAM cells are divided into read-disturbance and read-disturbance-free cells. As there is no disturbance to the storage node from the read BL, the read-disturbance-free cells sufficiently ensure a $5\sigma$ read stability yield in the near-$V_{th}$ region. The ST 11T SRAM cell has the largest read stability yield because the cross-coupled ST inverters have a larger hold stability yield than the cross-coupled standard inverters [10].

The conventional 6T and ST 10T, and the proposed ST 9T SRAM cells are read disturbance cells. In the near-$V_{th}$ region, the conventional 6T with its cross-coupled standard inverters does not ensure a $5\sigma$ read stability yield, as mentioned in Section I. Comparatively, the ST 10T SRAM cell can ensure a $5\sigma$ read stability yield until $V_{DD}$ falls to 460 mV, thanks to the cross-coupled ST inverters. The proposed ST 9T SRAM cell enhances the read stability by reducing the read disturbance such that a $5\sigma$ read stability yield is ensured until $V_{DD}$ falls to 440 mV, as described in section III-A. Among the read disturbance cells, the proposed ST 9T SRAM cell can operate at the lowest $V_{DD}$ and has the highest read stability yield at the same $V_{DD}$.

### *C. Read Delay*

In [28], the read delay is defined as the time from when WL is asserted to when 50 mV voltage difference between BL and BLB in the differential BL structure occurs. The voltage swing of 50 mV is also used for the single BL structure. On the other hand, in this paper, the different read delay definition is used to consider the sensing method difference between the differential and single BL structures.

The differential BL structure reads data by sensing the voltage difference between BL and BLB. The voltage latch SA (VLSA), which requires the small voltage swing for read data sensing, is applied to the differential BL structure. On the other hand, the single BL structure reads data by sensing the discharged BL voltage. The small voltage swing for the single BL structure with reference voltage ($V_{ref}$) can be considered by using VLSA. However, the benefit of the small voltage swing in the differential sensing using VLSA for the single BL structure with $V_{ref}$ can be canceled out because the variation in $V_{ref}$ necessitates timing margin [29]. In addition, the circuitry to generate $V_{ref}$ increases the area and energy consumption. Thus, in general, the inverter SA is used for the single BL structure [30]. In this paper, it is assumed that the differential BL structure uses VLSA and the single BL structure uses inverter SA as in [31].

The mean of the offset voltage ($\mu_{VOS}$) of VLSA is assumed to be zero considering its symmetrical design. The standard deviation of the offset voltage ($\sigma_{VOS}$) of VLSA is designed to be 20 mV because the industry design target of $3\sigma_{VOS}$ is typically 50-70 mV [32]. The inverter SA is designed to be high-skewed within the area of the VLSA to speed up the read "0" operation, taking into account the sensing yield in the read "1" operation.

The sensing failure is measured when the voltage difference between the BL pair does not reach $5\sigma_{VOS}$ in the differential BL structure, while it is measured when the BL voltage does not reach the $5\sigma$ worst trip voltage of the inverter SA in the single BL structure. The read delay is defined as time from when WL is activated to $V_{DD}/2$ to when the $5\sigma$ sensing yield is ensured.

Fig. 12 shows the read delay of the previous and proposed SRAM cells at $V_{DD}$, ensuring a $5\sigma$ read stability yield. The read delay of MH's 9T SRAM cell is the largest because of the current bottleneck described in Section II. A differential BL structure, such as in Chang's 10T and the ST 10T SRAM cell, has a smaller read delay than the single BL structure. This is because VLSA requires a relatively small BL voltage swing compared with the inverter SA.

### *D. Write Assist Technique*

In the near-$V_{th}$ region, previous and proposed SRAM cells cannot ensure a $5\sigma$ write ability yield. Thus, write assist techniques such as the suppressed cell $V_{DD}$ [33], raised cell $V_{SS}$ [34], boosted $V_{WL}$ [35], negative $V_{BL}$ [36], and the proposed negative $V_{WWLB}$ techniques should be applied. However, the write assist technique can degrade the hold stability yield in a half-selected cell depending on the assist method, and it can increase energy consumption. Thus, write assist techniques with a low energy consumption should be adopted while ensuring a $5\sigma$ hold stability yield in the half-selected cell. Table II shows the write assist technique applied to each SRAM. In this table, the conventional 8T, WRE 9T,

TABLE II
WRITE ASSIST TECHNIQUE FOR LOW ENERGY CONSUMPTION

| SRAM | Write assist technique |
|---|---|
| Chang's 10T | 1) Negative $V_{BL}$(column) or<br>2) Boosted $V_{WL}$(row) + Boosted $V_{WWL}$(column)[(a)] |
| ST 10T | Boosted $V_{WL}$(row) + Negative $V_{BL}$(column) |
| MH's 9T | Boosted $V_{WL}$(row) + Boosted $V_{WWL}$(column) |
| Proposed ST 9T | Boosted $V_{WL}$(row) + Negative $V_{WWLB}$(column) |

[(a)] Boosted $V_{WL}$ and $V_{WWL}$ can be applied at $V_{DD}$ where negative $V_{BL}$ is restricted.

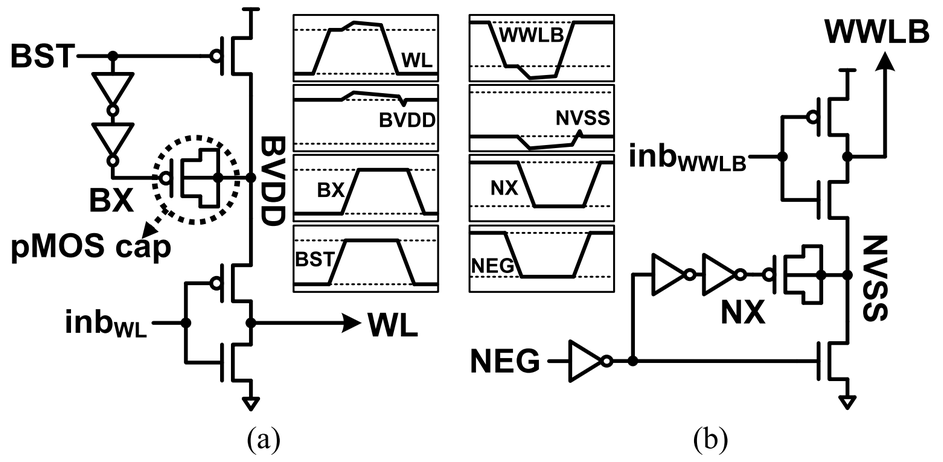


Fig. 13. (a) Boosted $V_{WL}$ and (b) negative $V_{WWLB}$ write assist circuits.

and ST 11T SRAMs are excluded. This is because the row half-selected cells in the conventional 8T and WRE 9T SRAMs do not achieve $5\sigma$ hold stability yield without the write-back scheme, and the ST 11T SRAM does not achieve $5\sigma$ write ability and hold stability yields at the same time in the near-$V_{th}$ region due to the condition mentioned in Section II.

In the Chang's 10T SRAM, the negative $V_{BL}$ and boosted $V_{WL}$ and $V_{WWL}$ are the most suitable write assist techniques. Although the boosted $V_{WL}$ and $V_{WWL}$ consume more energy than the negative $V_{BL}$ due to the higher capacitance of WWL signal, it is more suitable at the lower $V_{DD}$ because the negative $V_{BL}$ degrades the hold stability of the column half-selected cells. On the other hand, the suppressed cell $V_{DD}$ and raised cell $V_{SS}$ are inappropriate because they increase dynamic energy due to the charge and discharge of the high storage node capacitance of the column half-selected cells [37]. In the same way, the negative $V_{BL}$ and boosted $V_{WL}$ are the most suitable for the ST 10T SRAM. In addition, they can be used simultaneously to effectively improve the write ability.

In the single BL structure such as the MH's 9T and proposed ST 9T SRAMs, the write-1 assist technique should be applied due to the weak write-1 drivability of nMOS PG. In these SRAMs, the suppressed cell $V_{DD}$ and raised cell $V_{SS}$ are not effective due to the power-gated storage node. In addition, the negative $V_{BL}$ is not appropriate because it cannot improve write-1 ability in the single BL structure. Instead, the MH's 9T SRAM can adopt the boosted $V_{WL}$ and $V_{WWL}$ for write-1 ability improvement. In the proposed ST 9T SRAM, the boosted $V_{WL}$ and proposed negative $V_{WWLB}$ can be applied as described in Section III-B. In addition, they can be used simultaneously to effectively improve the write ability. Figs. 13(a) and (b) show the boosted $V_{WL}$ and negative $V_{WWLB}$ write assist circuits for the proposed ST 9T SRAM.

### *E. Write Ability and Half-Selected Cell Stability*

As the row-based assist technique controls only a single selected row, it consumes less energy than the column-based assist technique which controls all selected columns. Thus, for low energy consumption, the boosted WL voltage in the row-based boosted $V_{WL}$ is maximally selected under the condition that the half-selected cell ensures a $5\sigma$ hold stability yield. Fig. 14 shows the maximum boosted WL voltage according to $V_{DD}$. The maximum boosted WL voltage of the proposed

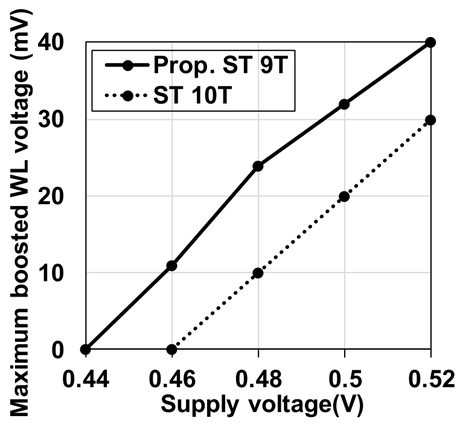


Fig. 14. Maximum boosted WL voltage for $5\sigma$ hold stability yield in the row half-selected cells in proposed ST 9T and ST 10T SRAMs.

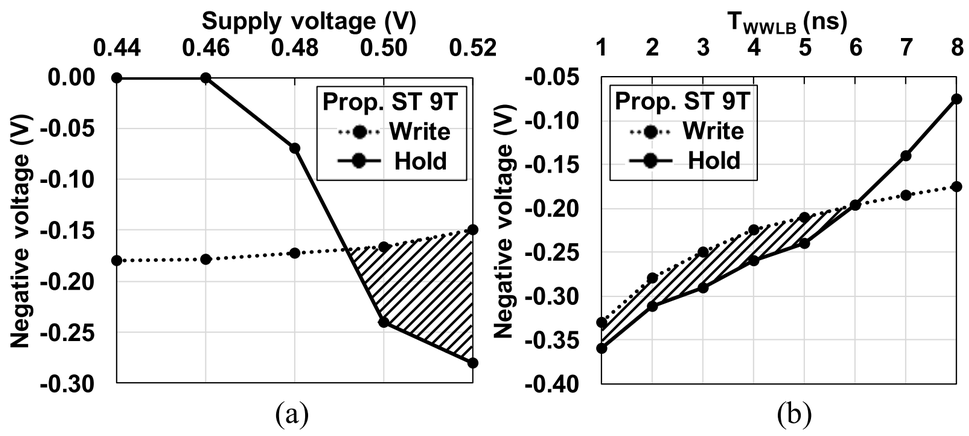


Fig. 15. The minimum and maximum negative $V_{WWLB}$ for $5\sigma$ write ability and hold stability yields, respectively, (a) according to $V_{DD}$, and (b) according to $T_{WWLB}$ at $V_{DD} = 0.48$ V in the proposed ST 9T SRAM.

ST 9T SRAM is larger than that of the ST 10T SRAM, because the hold stability yield in the row half-selected cell is higher in the proposed ST 9T SRAM.

Fig. 15(a) shows the minimum negative $V_{WWLB}$ for $5\sigma$ write ability yield (dotted line) and the maximum negative $V_{WWLB}$ that ensures $5\sigma$ hold stability yield in the column half-selected cell (solid line) when the maximum boosted $V_{WL}$ is applied to the proposed ST 9T SRAM. Thus, the proposed ST 9T SRAM can achieve both $5\sigma$ write ability and hold stability yields at the negative WWLB voltage of the hatched area.

In addition, the proposed ST 9T SRAM has the minimum $V_{DD}$ of 0.48 V for the write operation while ensuring both the $5\sigma$ write ability and hold stability yields by controlling $T_{WWLB}$. Fig. 15(b) shows the minimum and maximum negative $V_{WWLB}$ for $5\sigma$ write ability and hold stability yields according to $T_{WWLB}$ at $V_{DD} = 0.48$ V, respectively. As $T_{WWLB}$ increases, the minimum negative $V_{WWLB}$ increases less sensitively, because the effective write data flip time is

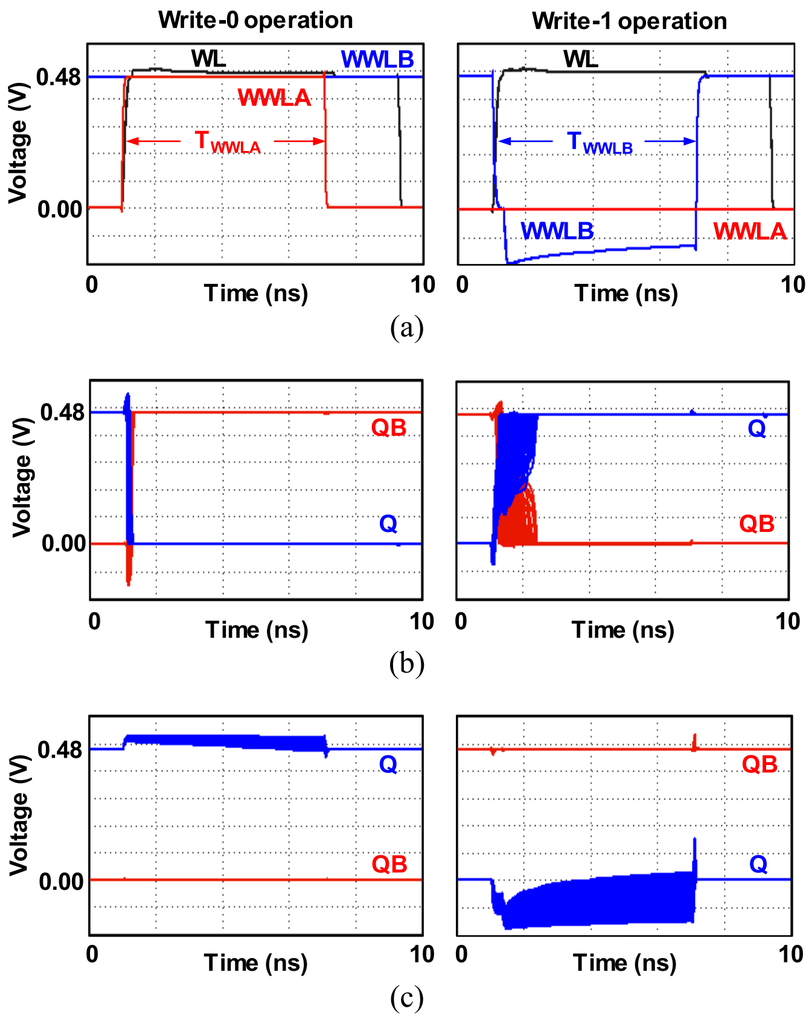


Fig. 16. Waveforms in (a) the control signals, (b) storage nodes of selected cells, and (c) storage nodes of column half-selected cells during write-0 and write-1 operations.

sufficiently short. As $T_{WWLB}$ decreases, the floating time of node Q storing data "0" decreases in the column half-selected cell, so the maximum negative $V_{WWLB}$ is lowered. Thus, the proposed ST 9T SRAM can achieve both $5\sigma$ write ability and hold stability yields at the negative WWLB voltage of the hatched area. To reduce energy consumption, the $T_{WWLB}$ is set to 6 ns, because the write assist voltage is minimized. Fig. 16 shows the waveforms of the storage node and control signals during write-0 and write-1 operations, respectively, at $V_{DD}$ = 0.48 V and $T_{WWLA} = T_{WWLB}$ = 6 ns, obtained from the 10,000 Monte Carlo samples. $T_{WWLA}$ is simply set equal to $T_{WWLB}$ because the write ability and hold stability yields are sufficiently ensured during the write-0 operation.

In the proposed ST 9T SRAM, WWLA driver controls only gate of PUL2 in the column half-selected cells, whereas WWLB driver controls the gate of PDL1, diffusion of NF, and $V_X$ (when Q=0) nodes in column half-selected cells. Thus, asymmetric driver needs to be carefully designed by considering the capacitance of WWLA and WWLB nodes.

Fig. 17 shows the minimum and maximum negative $V_{BL}$ that ensure a $5\sigma$ write ability yield in the selected cell, and a $5\sigma$ hold stability yield in the column half-selected cell, respectively, in Chang's 10T and ST 10T SRAMs. Chang's 10T and ST 10T SRAMs can achieve both $5\sigma$ write ability and hold stability yields at the negative BL voltage of the hatched area. Thus, the negative $V_{BL}$ can be applied to Chang's 10T and ST 10T SRAMs when $V_{DD}$ is above 0.48 V and 0.42 V, respectively.

In addition, Chang's 10T SRAM can operate under a $V_{DD}$ of 0.48 V while ensuring both $5\sigma$ write ability and hold stability yields with a boosted $V_{WL}$ and $V_{WWL}$, which have

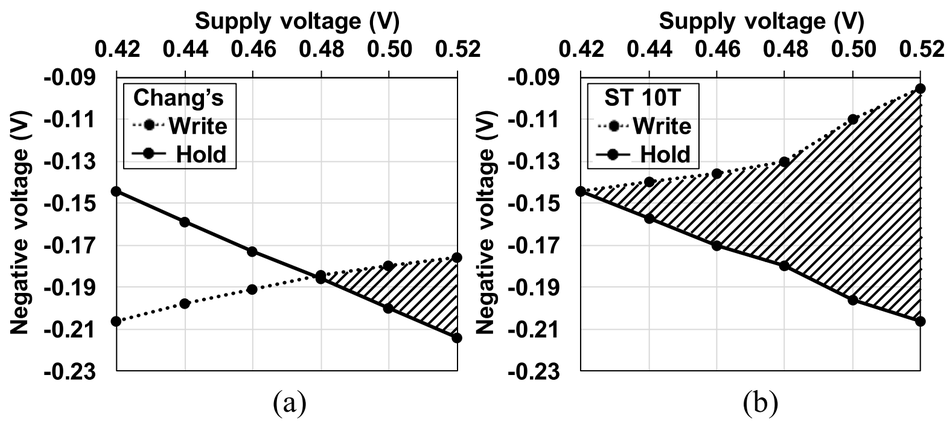


Fig. 17. The minimum and maximum negative $V_{BL}$ for $5\sigma$ write ability and hold stability yields, respectively, (a) in Chang 10T, and (b) ST 10T SRAM.

a negligible effect on the hold stability yield in the half-selected cell. Like Chang's 10T SRAM, MH's 9T SRAM can also operate at any supply voltage in the near-$V_{th}$ region by using the boosted $V_{WL}$ and $V_{WWL}$. Although the boosted $V_{WL}$ and $V_{WWL}$ can be applied at all supply voltages in the near-$V_{th}$ region, the energy consumption does not decrease efficiently because as $V_{DD}$ scales down, the delay increases exponentially. These details will be discussed in following section.

### *F. Energy Consumption*

The average energy consumption is measured to include the energy consumption of SRAM cell macro and peripheral circuits. It is assumed that the read (or write) "0" and "1" operations occur at the same rate during read and write operations. Figs. 18(a) and (b) show the read and write energy consumptions at a $V_{DD}$ that ensures the target yields. As $V_{DD}$ scales down, the read and write energy consumptions decrease. However, when $V_{DD}$ drops below a specific value, the read and write energy consumption instead increases because the delay increases exponentially, as shown in Fig. 12, and the required write assist voltage increases.

The read energy consumption is dominant in the total energy consumption because SRAM performs read operations most of the time, as mentioned in Section II. The read:write operation ratio is assumed to be 7:1 [12]. Fig. 18(c) shows the comparison of energy consumption at the supply voltage having the minimum total energy consumption ($V_{min\_energy}$) while ensuring the target yields. The $V_{min\_energy}$ is 0.40 V, 0.46 V, 0.46 V, and 0.48 V in Chang's 10T, ST 10T, MH's 9T, and the proposed ST 9T SRAMs, respectively.

Chang's 10T and ST 10T SRAMs with differential BL structures have a higher read energy consumption than the other SRAMs with single BL structures. This is because the differential BL structure discharges either BL or BLB regardless of the stored data, but the single BL structure discharges BL only in a read-1 operation, as mentioned in Section II. In particular, Chang's 10T SRAM consumes more read energy than the ST 10T SRAM as it toggles a large VVSS capacitance because of the shared column-based VVSS signal. With the single BL structure, the proposed ST 9T SRAM has the lowest read energy consumption because of a lower static energy consumption by a smaller delay than MH's 9T SRAM cell. The read energy consumption in the proposed

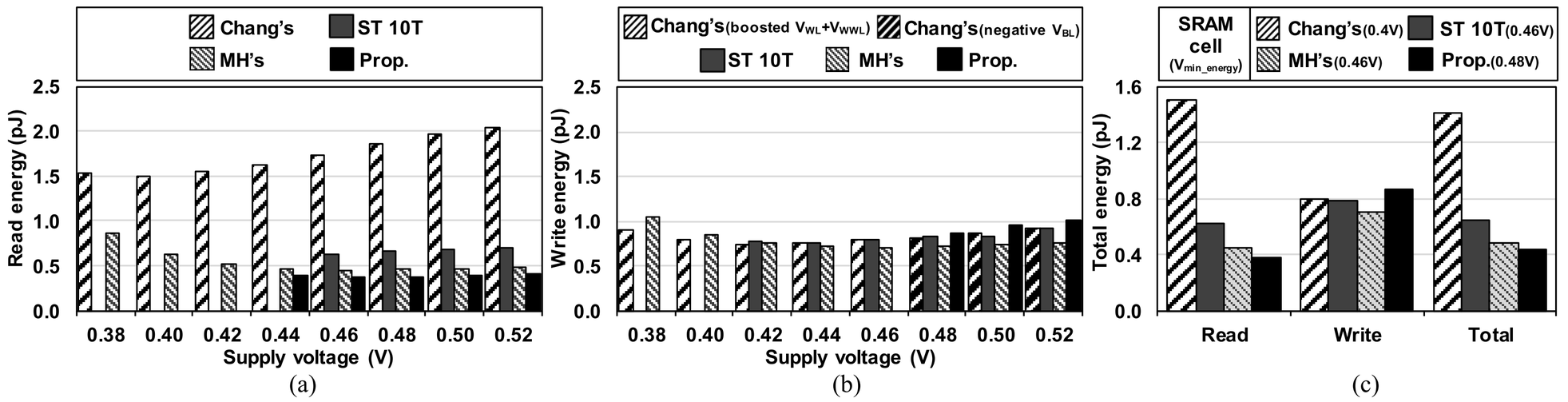


Fig. 18. Energy consumption in (a) read and (b) write operations, and (c) total energy consumption at $V_{min\_energy}$.

ST 9T SRAM is lower by 75%, 40%, and 17% than in Chang's 10T, ST 10T, and MH's 9T SRAMs, respectively.

During the write operation in Chang's 10T and MH's 9T SRAMs, BL discharging does not occur in unselected columns owing to VVSS = $V_{DD}$. Comparatively, BL discharging occurs in the unselected columns of the ST 10T and proposed ST 9T SRAMs. Thus, the ST 10T and proposed ST 9T SRAMs consume additional write energy in unselected columns. MH's 9T SRAM has the lowest write energy consumption. This is because SRAM with the single BL structure only discharges BL to "0" during the write-0 operation, and not during the write-1 operation. Thus, the BL control energy consumption is half that of the differential BL structure. Chang's 10T SRAM has a write energy consumption similar to that of the ST 10T SRAM, because the ST 10T SRAM cell has no additional column-based control signal. The proposed ST 9T SRAM has the highest write energy consumption owing to the additional energy consumption in the unselected columns. The write energy consumption in Chang's 10T, the ST 10T, and MH's 9T SRAMs are 8%, 10%, and 18% lower than that of the proposed ST 9T SRAM. However, the total energy consumption in the proposed ST 9T SRAM is 69 %, 32 %, and 10 % lower than in Chang's 10T, the ST 10T, and MH's 9T SRAMs, respectively.

### *G. Data Retention Voltage and Leakage Power*

Leakage power is measured at the minimum data retention voltage (DRV) that ensures a $5\sigma$ hold stability yield. The hold stability yield of the proposed ST 9T SRAM cell differs depending on the stored data because of the asymmetric cell structure. When the storage node Q is "0," the ST inverter has a higher trip voltage than a standard inverter. On the other hand, when the storage node Q is "1," the ST inverter has a trip voltage similar to that of the inverter. Thus, the hold stability yield when the storage node Q is "0" is much higher than when the storage node Q is "1". As a result, the DRV of the proposed ST 9T SRAM cell is determined by the hold stability yield when the storage node Q is "1."

Table III shows the DRV and leakage power of previous and proposed SRAM cells. SRAM cells using cross-coupled ST inverters have larger hold stability yields than SRAM cells using cross-coupled standard inverters, because the ST inverter has a higher trip voltage than a standard inverter. Thus, the DRV of the ST 10T SRAM cell is lower than those of other SRAM cells. However, the leakage power of the ST 10T SRAM cell is the highest, because the ST inverter has an additional subthreshold leakage path through the feedback transistor NF. Chang's 10T and MH's 9T SRAM cells have the same DRV because they use the same cross-coupled standard inverters. However, the leakage power of MH's 9T SRAM cell is lower than that of Chang's 10T SRAM cell owing to the single BL structure. The DRV of the proposed ST 9T SRAM cell is lower than that of SRAM cells with cross-coupled standard inverters. This is because the variation in the stacked nMOS in the ST inverter is smaller than that of a single nMOS. The leakage power of the proposed ST 9T SRAM cell is 7% and 18% higher than that of Chang's 10T and MH's 9T SRAM cells owing to the additional subthreshold leakage path in the ST inverter. However, the leakage power of the proposed ST 9T SRAM cell is 22% lower than that of ST 10T SRAM cell with the ST inverters, because only one ST inverter is used in the proposed ST 9T SRAM cell.

TABLE III
DATA RETENTION VOLTAGE AND LEAKAGE POWER

| SRAM cell | Chang's | ST 10T | MH's | Proposed |
|---|---|---|---|---|
| DRV | 0.275 V | 0.256 V | 0.275 V | 0.265 V |
| Leakage Power | 0.859 μW | 1.173 μW | 0.781 μW | 0.919 μW |

### *H. Comparison in Near-$V_{th}$ Region*

Table 4 summarizes the comparison of the previous and proposed ST 9T SRAMs at each $V_{min\_energy}$. A figure of merit (FOM) is often introduced to compare digital circuits that perform the same function using different designs. To consider both energy and performance, an energy-delay product (EDP) is usually used. An EDP with the same weight for delay and energy do not reflect the importance of delay and energy according to the $V_{DD}$. Thus, the weights of delay and energy should be considered according to the $V_{DD}$. In the near-$V_{th}$ region, the EDP is calculated by following equation according to [38]:

$$\text{Near-V}_{\text{th}}\text{EDP} = \text{Energy} \times \text{Delay}^{0.2} \tag{2}$$

TABLE IV
COMPARISON IN 22-nm FINFET TECHNOLOGY

| SRAM cell | Chang's | ST 10T | MH's | Proposed |
|---|---|---|---|---|
| $V_{min\_energy}$ | 0.40 V | 0.46 V | 0.46 V | 0.48 V |
| Cell area | 0.191 μm$^2$ | 0.197 μm$^2$ | 0.191 μm$^2$ | 0.151 μm$^2$ |
| Read stability yield | 8.1σ | 5.0σ | 9.0σ | 5.4σ |
| Read delay | 34.7 ns | 4.6 ns | 24.0 ns | 8.2 ns |
| Write ability yield | 5.0σ | 5.0σ | 5.0σ | 5.0σ |
| Write assist voltage (row) | 0.11 V | 0.00 V | 0.09 V | 0.02 V |
| Write assist voltage (column)[(a)] | 0.11 V | 0.14 V | 0.09 V | 0.10 V |
| Read energy | 1.50 pJ | 0.63 pJ | 0.45 pJ | 0.38 pJ |
| Write energy | 0.79 pJ | 0.78 pJ | 0.71 pJ | 0.87 pJ |
| Total energy | 1.41 pJ | 0.65 pJ | 0.49 pJ | 0.44 pJ |
| Normalized near-$V_{th}$ EDP | 4.30 | 1.31 | 1.37 | 1.00 |

[(a)] Applied write assist voltage per column.

The proposed ST 9T SRAM has a 77%, 24%, and 27% smaller near-$V_{th}$ EDP than Chang's 10T, the ST 10T, and MH's 9T SRAMs at $V_{min\_energy}$. The proposed ST 9T SRAM cell has smaller cell area, lower energy consumption, and smaller near-$V_{th}$ EDP than other SRAM cells at the cost of delay. Thus, the proposed ST 9T SRAM cell is the most efficient SRAM cell design for low energy application such as bio implants and mobile devices, rather than high speed applications.

## V. CONCLUSION

Low energy consumption has become important for bio implants and mobile devices because they need to operate with limited energy. For minimization of the energy consumption, it is important to operate the SRAM in near-$V_{th}$ region. This paper proposed a one-sided ST 9T SRAM cell with low energy consumption, and high read stability, write ability, and hold stability yields in the near-$V_{th}$ region. The read stability yield was improved in the proposed ST 9T SRAM cell by using a cross-coupled structure of standard and ST inverters. In addition, the proposed ST 9T SRAM cell ensured a $5\sigma$ target write ability yield by using selective power gating and a novel negative $V_{WWLB}$ assist technique that controlled the trip voltage of the ST inverter. The proposed ST 9T SRAM cell has a smaller area than Chang's 10T, the ST 10T, and MH's 9T SRAM cells. The proposed ST 9T SRAM consumes much less energy than Chang's 10T, the ST 10T, and MH's 9T SRAMs at each $V_{min\_energy}$, although it has a larger read delay owing to the single BL structure. As a result, the proposed ST 9T SRAM cell has the best near-$V_{th}$ EDP.

## REFERENCES


[1] B. Calhoun and A. Chandrakasan, "Static noise margin variation for sub-threshold SRAM in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1673–1679, Jul. 2006.

[2] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits," *Proc. IEEE*, vol. 98, no. 2, pp. 253–266, Feb. 2010.

[3] B. H. Calhoun, J. F. Ryan, S. Khanna, M. Putic, and J. Lach, "Flexible circuits and architectures for ultralow power," *Proc. IEEE*, vol. 98, no. 2, pp. 267–282, Feb. 2010.

[4] R. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 305–316, Sep. 2005.

[5] M.-H. Chang, Y.-T. Chiu, and W. Hwang, "Design and iso-area $V_{min}$ analysis of 9T subthreshold SRAM with bit-interleaving scheme in 65-nm CMOS," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 59, no. 7, pp. 429–433, Jul. 2012.

[6] P. Hazucha *et al.*, "Neutron soft error rate measurements in a 90-nm CMOS process and scaling trends in SRAM from 0.25-mm to 90-nm generation," in *IEDM Tech. Dig.*, Dec. 2003, pp. 21.5.1–21.5.4.

[7] I. J. Chang, J.-J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T subthreshold SRAM cell array with bit-interleaving and differential read scheme in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 650–658, Feb. 2009.

[8] L. Chang *et al.*, "An 8T-SRAM for variability tolerance and low-voltage operation in high-performance caches," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 956–963, Apr. 2008.

[9] G. Pasandi and S. M. Fakhraie, "A 256-kb 9T near-threshold SRAM with 1k cells per bitline and enhanced write and read operations," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 11, pp. 2438–2446, Nov. 2015.

[10] J. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based sub-threshold SRAM cell," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.

[11] S. Ahmad, M. K. Gupta, N. Alam, and M. Hasan, "Single-ended Schmitt-trigger-based robust low-power SRAM cell," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 8, pp. 2634–2642, Aug. 2016.

[12] Y. Xie, *Emerging Memory Technologies: Design, Architecture, and Applications*. Springer, Oct. 2013, p. 187.

[13] M.-H. Tu *et al.*, "A single-ended disturb-free 9t subthreshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1469–1482, Jun. 2012.

[14] T. W. Oh, H. Jeong, K. Kang, J. Park, Y. Yang, and S.-O. Jung, "Power-gated 9T SRAM cell for low-energy operation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 3, pp. 1183–1187, Mar. 2017.

[15] *BSIM-CMG 107.0.0 Multi-Gate MOSFET Compact Model*. Accessed: Jul. 2013. [Online]. Available: http://wwwdevice.eecs.berkeley.edu/bsim/?page= BSIMCMG_LR

[16] C. Auth *et al.*, "A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *Proc. Symp. VLSI Technol.*, Jun. 2012, pp. 131–132.

[17] C.-H. Lin *et al.*, "Channel doping impact on FinFETs for 22 nm and beyond," in *Proc. Symp. VLSI Technol.*, Jun. 2012, pp. 15–16.

[18] Z. Guo, A. Carlson, L.-T. Pang, K. T. Duong, T.-J.-K. Liu, and B. Nikolic, "Large-scale SRAM variability characterization in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3174–3192, Nov. 2009.

[19] J. Wang, S. Nalam, and B. H. Calhoun, "Analyzing static and dynamic write margin for nanometer SRAMs," in *Proc. 13th Int. Symp. Low Power Electron. Design (ISLPED)*, 2008, pp. 129–134.

[20] T. S. Doorn, E. J. W. T. Maten, J. A. Croon, A. Di Bucchianico, and O. Wittich, "Importance sampling Monte Carlo simulations for accurate estimation of SRAM yield," in *IEEE 34th ESSCIRC Dig. Tech. Papers*, Sep. 2008, pp. 230–233.

[21] T. Date, S. Hagiwara, K. Masu, and T. Sato, "Robust importance sampling for efficient SRAM cell yield analysis," in *Proc. 11th Int. Symp. Quality Electron. Design (ISQED)*, Mar. 2010, pp. 15–21.

[22] D. Ingerly *et al.*, "Low-k wire stack with metal-insulator-metal capacitors for 22 nm high volume manufacturing," in *Proc. Intrcnt. Tech. Conf. (IITC)*, 2012, pp. 1–3.

[23] R. V. Joshi, R. Kanj, and V. Ramadurai, "A novel column-decoupled 8T cell for low-power differential and domino-based SRAM design," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*, vol. 19, no. 5, pp. 869–882, May 2011.

[24] H. Kawasaki *et al.*, "Demonstration of highly scaled FinFET SRAM cells with high-*k*/metal gate and investigation of characteristic variability for the 32 nm node and beyond," in *IEDM Tech. Dig.*, Dec. 2008, pp. 237–240,.

[25] C.-H. Jan *et al.*, "A 22 nm SoC platform technology featuring 3-D tri-gate and high-*k*/metal gate optimized for ultra low power high performance and high density SoC applications," in *IEDM Tech. Dig.*, Dec. 2012, pp. 3.1.1–3.1.4.
[26] H. Sunagawa, H. Terada, A. Tsuchiya, K. Kobayashi, and H. Onodera, "Effect of regularity-enhanced layout on printability and circuit performance of standard cells," in *Proc. 10th Int. Symp. Qual. Electron. Design (ISQED)*, Mar. 2009, pp. 195–200.
[27] K. Ronse *et al.*, "Opportunities and challenges in device scaling by the introduction of EUV lithography," in *IEDM Tech. Dig.*, Dec. 2012, pp. 435–438.
[28] G. Pasandi and S. M. Fakhraie, "An 8T low-voltage and low-leakage half-selection disturb-free SRAM using bulk-CMOS and FinFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 7, pp. 2357–2363, Jul. 2014.
[29] H. Jeong, T. Kim, T. Song, G. Kim, and S.-O. Jung, "Trip-point bitline precharge sensing scheme for single-ended SRAM," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 7, pp. 1370–1374, Jul. 2015.
[30] H. Noguchi *et al.*, "Which is the best dual-port SRAM in 45-nm process technology?—8T, 10T single end, and 10T differential," in *Proc. IEEE Int. Conf. Integr. Circuit Design Technol.*, Jun. 2008, pp. 55–58.
[31] B. Zimmer *et al.*, "SRAM assist techniques for operation in a wide voltage range in 28-nm CMOS," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 59, no. 12, pp. 853–857, Dec. 2012.
[32] T. Na, S.-H. Woo, J. Kim, H. Jeong, and S.-O. Jung, "Comparative study of various latch-type sense amplifiers," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst*, vol. 22, no. 2, pp. 425–429, Feb. 2014.
[33] M. E. Sinangil *et al.*, "A 28 nm 2 Mbit 6 T SRAM with highly configurable low-voltage write-ability assist implementation and capacitor-based sense-amplifier input offset compensation," *IEEE J. Solid-State Circuits*, vol. 51, no. 2, pp. 557–567, Feb. 2016.
[34] M. H. Tu *et al.*, "Single-ended subthreshold SRAM cell with asymmetrical write/read-assist," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3039–3047, Dec. 2010.
[35] M. E. Sinangil, H. Mair, and A. P. Chandrakasan, "A 28 nm high-density 6T SRAM with optimized peripheral-assist circuits for operation down to 0.6 V," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2011, pp. 260–261.
[36] Y. Fujimura *et al.*, "A configurable SRAM with constant-negative-level write buffer for low-voltage operation with 0.149 $\mu m^2$ cell in 32 nm high-*k* metal-gate CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 348–349.
[37] K. Kang, H. Jeong, Y. Yang, J. Park, K. Kim, and S.-O. Jung, "Full-swing local bitline SRAM architecture based on the 22-nm FinFET technology for low-voltage operation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 4, pp. 1342–1350, Apr. 2016.
[38] H. Jeong, Y. Yang, S. Chul Song, J. Wang, G. Yeap, and S.-O. Jung, "Variation-aware figure of merit for integrated circuit in near-threshold region," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1754–1759, Jun. 2015.

**Keonhee Cho** was born in Seoul, South Korea, in 1994. He received the B.S. degree in electronic and electrical engineering from Yonsei University, Seoul, in 2018, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering. His research interest is focused on FinFET-based near-$V_{th}$ and sub-$V_{th}$ SRAM cell design.

**Juhyun Park** was born in Incheon, South Korea, in 1988. He received the B.S. degree in electronic and electrical engineering from Hongik University, Seoul, South Korea, in 2012. He is currently purusing the Ph.D. degree in electrical and electronic engineering with Yonsei University, Seoul, South Korea. His research interest is focused on FinFET-based near-$V_{th}$ and sub-$V_{th}$ SRAM cell design.

**Tae Woo Oh** was born in Seoul, South Korea, in 1992. He received the B.S. degree in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2015, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering. His research interest is focused on FinFET-based low-power and high-performance SRAM cell.

**Seong-Ook Jung** (Senior Member, IEEE) received the B.S. and M.S. degrees in electronic engineering from Yonsei University, Seoul, South Korea, in 1987 and 1989, respectively, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana–Champaign, Urbana, in 2002.

From 1989 to 1998, he was with Samsung Electronics, where he worked on specialty memory types, such as video RAM, graphic RAM, window RAM, and merged memory logic. From 2001 to 2003, he was with T-RAM Inc., where he led the thyristor-based memory design team. From 2003 to 2006, he was with Qualcomm Inc., San Diego, CA, USA, where he worked on high-performance low-power embedded memory, process variation-tolerant circuit design, and low-power circuit techniques. Since 2006, he has been a Professor with Yonsei University. His research interests include process variation-tolerant circuit design, low-power circuit design, mixed-mode circuit design, and future-generation memory.